

Room-temperature operation of an exclusive-OR circuit using a highly doped Si single-electron transistor

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We fabricated highly doped Si single-electron transistors (SETs) with a series of geometrically defined multiple islands. Highly doped SETs have the advantage of being easy to fabricate. Moreover, SETs with multiple islands provide a larger peak-to-valley current ratio (PVCr) than SETs with a single island. A PVCr for the Coulomb oscillation of up to 77 was observed at room temperature. This large PVCr is advantageous for circuit operations. We applied the Coulomb oscillation and multiple-gate input characteristics of only one SET to obtain an exclusive-OR operation at room temperature. © 2005 American Institute of Physics. [DOI: 10.1063/1.1894594]

Single-electron devices utilizing the Coulomb blockade effect are promising for use as the basic elements of future low-power, high-density integrated circuits.¹⁻⁴ To develop these devices into commercial products, room-temperature operation capability and Si-based fabrication are necessary.

Single-electron transistors (SETs) applied in logic circuits require more advanced functionality than conventional complementary metal-oxide-semiconductor (CMOS) circuits. Takahashi *et al.*⁵ reported an exclusive-OR (XOR) circuit operation using a Si SET fabricated by pattern-dependent oxidation at 40 K. They utilized the Coulomb oscillation and the ability of a SET to contain several gate electrodes. Saitoh *et al.*⁶ reported an XOR circuit operation using a point-contact channel single-hole transistor with a single island at room temperature. They utilized the Coulomb oscillation and negative differential conductance to achieve XOR operation. In both of these circuits, the number of transistors necessary for XOR circuit operation could be greatly reduced as compared with a CMOS logic circuit. So far, however, only few SET circuits have been developed with such advanced functionality.

On the other hand, the above two SETs are inversion-carrier-type field-effect SETs, in which the inversion layers are used as source/drain electrodes. Recently, we have fabricated a highly doped Si SET with a series of multiple geometrically defined islands and multiple side gates.⁷⁻⁹ In highly doped SETs, carriers are generated from dopants. Highly doped SETs have the advantage of being easy to fabricate, because they require only one electron beam (EB) mask to form both the Coulomb islands and multiple side gates. Moreover, SETs with multiple serially connected Coulomb islands have the advantages of offering high-temperature operation⁸ and suppressing cotunneling. We previously reported an exclusive-not-OR circuit operation at 77 K with this SET.⁹

In the current work, we observed a large peak-to-valley current ratio (PVCr) for the Coulomb oscillation even at room temperature in a SET with multiple Coulomb islands. Therefore, based on these characteristics, we report an XOR operation at room temperature. The reduced number of required transistors, the room-temperature operation, and easy

circuit fabrication should open up the development of SET logic circuits.

We fabricated a regular one-dimensional array of nanoscale islands in a silicon-on-insulator layer by using EB lithography. SETs with one island were also fabricated for comparative purposes. Figures 1(a) and 1(b) respectively show a schematic diagram and a scanning electron microscopy (SEM) image of the SET with one-dimensional array structure. Multiple gates (indicated as Gate 1 and Gate 2) were formed on both sides of the channel wire. The top Si layer was doped by POCl₃ annealing. The doping level was $2 \times 10^{19} - 1 \times 10^{20} \text{ cm}^{-3}$. After dry etching with an electron cyclotron resonance etcher with the resist pattern as a mask, subsequent isotropic wet etching in an NH₄OH/H₂O₂/H₂O solution was conducted to reduce the device dimensions.¹⁰ The final thickness of the top Si layer was about 10 nm. After the wet etching [Fig. 1(b)], the width of an island and that of the region between adjacent islands were about 20 and 10 nm, respectively. The distance between the centers of adjacent islands was 250 nm, and the length of the narrow channel-wire region, which had a width of about 10 nm between adjacent islands, was 50–100 nm. The separation between the channel wire and the side gates was 240 nm.

Figures 2(a) and 2(b) respectively show the Coulomb oscillations at room temperature for SETs with a single island and 22 islands. The maximum observed PVCrs were 3.5 for the SET with a single island and 77 for the one with 22 islands. Figure 3 shows PVCr versus island number of the measured devices in which Coulomb oscillations are observed at room temperature. There are several SETs having much larger PVCr values for multiple islands than those for a single island. One possible reason for the large values is the reduction of effective junction capacitance of the SETs with multiple islands due to the multiple junctions. Nevertheless, the effect of overall size reduction and the increased probability of encountering small islands due to the increased number of serially connected islands cannot be ruled out as the reason. Further study is necessary to clarify the reason.

A large PVCr is advantageous for circuit operations without errors. Though a multiple-island structure has an ability to make a PVCr larger, it requires a larger area. There is a tradeoff between the area and the reduction of effective junction capacitance due to the serial connection of multiple junctions. Therefore, we have to find an optimal island num-

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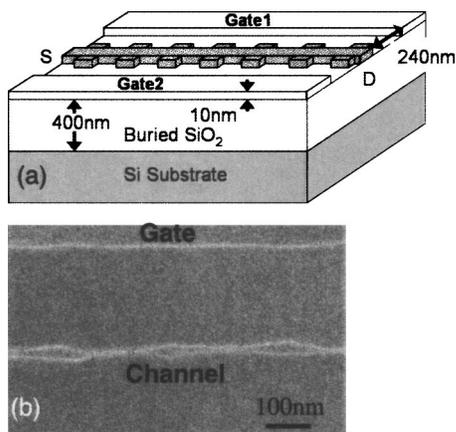


FIG. 1. (a) Schematic diagram and (b) SEM image of a SET with double side gates and a highly doped narrow channel with an array of nanoscale islands.

ber for practical use. On the other hand, for high voltage gain, we have to enlarge the gate-island capacitance C_g compared with the junction capacitance C_j . In the side-gate structure, C_g is usually small due to the large gate-island distance. Therefore, we have to make an effort to reduce the distance. This, in turn, loses the advantage of reduction of the effective junction capacitance by a multiple junction system. For practical use, we also have to find out an optimal distance, otherwise we have to use an additional amplifier.

A SET with multiple gates can operate as an XOR circuit by utilizing its oscillatory drain current (I_d) characteristics (i.e., Coulomb oscillation). Figure 4(a) shows the equivalent circuit of our SET with multiple (double) gates, while Fig. 4(b) illustrates the operation principle of the SET with multiple gates. Since the I_d value is determined by the sum of the products of each gate capacitance (C_{gi}) and gate voltage (V_{gi}), I_d is simply a function of the sum of the V_{gi} when C_{g1} is equal to C_{g2} . We can choose V_{gi} as a low input voltage (L) or a high input voltage (H) so as to satisfy the following conditions: A I_d peak appears when V_{g1} (V_{g2}) values is H and V_{g2} (V_{g1}) is L . Simultaneously, a I_d valley appears when the values of V_{g1} and V_{g2} are both H or both L . Thus, the output current I_d is low (L) when the input voltages are in the HH state (both V_{g1} and V_{g2} H) or the LL state (both V_{g1} and V_{g2} L). Likewise, the output current I_d is high (H) when the input voltages are in the HL or LH state [V_{g1} (V_{g2}) is H and V_{g2} (V_{g1}) is L]. This corresponds to the operation of an XOR circuit.

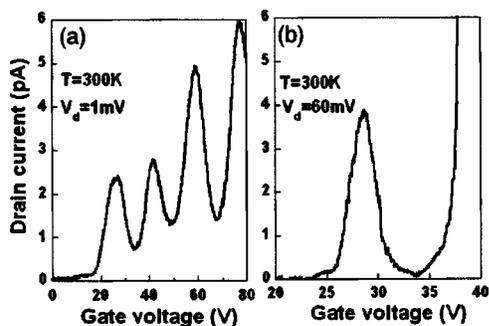


FIG. 2. Drain current vs gate voltage characteristics at room temperature for SETs with (a) a single island and (b) 22 islands. The observed maximum PVCRCs were (a) 3.5 and (b) 77.

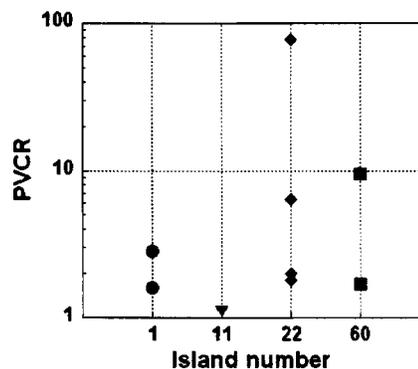


FIG. 3. PVCRC vs island number of all the devices in which Coulomb oscillations are observed at room temperature. Closed circle, inverted triangle, diamond, and square represent the observed PVCRCs for 1, 11, 22, and 60 islands, respectively.

Figure 5(a) shows the room-temperature I_d characteristics of our SET with 22 islands as a function of V_{g1} or V_{g2} . Here, the voltage of only one of the side gates was swept, while that of the other side gate was kept at 0 V. The noisy characteristics for V_{g1} sweep are probably due to the existence of traps between the array and Gate 1. As seen in the figure, the characteristics for V_{g1} are nearly equal to those for V_{g2} . This indicates that C_{g1} almost equals C_{g2} , which enables easy application of our SET to an XOR logic circuit. The I_d peak appears when V_{g2} is about 34.3 V, while the I_d valley appears when V_{g1} is about 38.6 V. Also, I_d is nearly zero when V_{g1} or V_{g2} is around 30 V. Taking the nearly equal I_d characteristics for V_{g1} and V_{g2} into account, if we choose the low (L) and high (H) input voltages for one side gate as 15 and 19.3 V, respectively, the sum of the voltages of the two side gates becomes 30 and 38.6 V for the LL and HH input states, respectively, where the I_d valleys appear. Also, for the LH and HL input states, the sum becomes 34.3 V, where the I_d peak appears.

Figure 5(b) shows the I_d switching in response to switching the two input gate voltages between 15 V (L) and 19.3 V (H) at room temperature. When the input voltages are in the LL or HH state, the output I_d is L (less than 0.3 pA). When the input voltages are in the LH or HL state, the output I_d is H (more than 0.6 pA). These results demonstrate XOR operation with our SET. It should be noted that the H (and L) output states of I_d will become higher (and lower) if the I_d peak and valley each appear at completely the same values of V_{g1} and V_{g2} in Fig. 5(a).

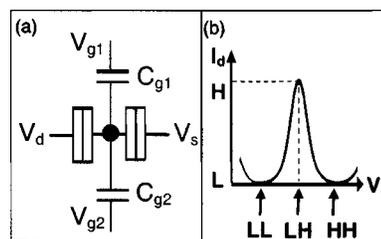


FIG. 4. (a) Equivalent circuit for our SET with double gates. C_{gi} and V_{gi} stand for the gate capacitance and voltage, respectively. V_d and V_s are the respective drain and source voltages. V_s is grounded. (b) Operation principle of a SET with multiple gates. When the sum of the two input voltages becomes a voltage corresponding to a peak, the drain current (I_d) increases [the high (H) output state]. On the other hand, when the sum becomes a voltage corresponding to a valley, I_d decreases [the low (L) output state].

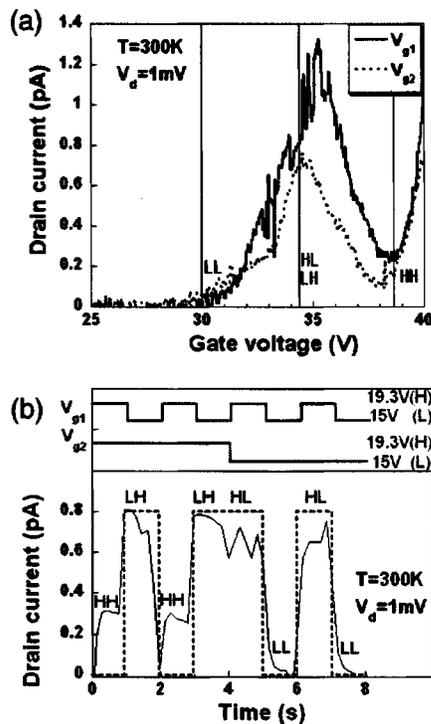


FIG. 5. (a) Drain current (I_d) vs gate voltage characteristics at room temperature for a SET with 22 islands. The solid and broken lines are the characteristics shown as a function of V_{g1} and V_{g2} , respectively. Here, the voltage of only one of the side gates was swept, while that of the other side gate was kept at 0 V. (b) Measured I_d switching characteristics when the input gate voltages (V_{g1} and V_{g2}) were switched between 15 and 19.3 V at room temperature. The dotted line shows the ideal output current for an XOR circuit. These characteristics are for a different device from the one measured in Fig. 2(b).

In summary, we have fabricated a highly-doped Si SET with multiple islands and multiple side gates. The SET exhibited Coulomb oscillation with a large PVCR at room temperature. We applied the Coulomb oscillation and multiple-gate input characteristics to XOR circuit operation and achieved I_d switching at room temperature. Using a SET with multiple gates requires fewer transistors in a logic circuit as compared with a circuit composed of conventional CMOS transistors. In addition to its advanced functionality, the easy fabrication and room-temperature operation of our proposed circuit demonstrate the feasibility of practical SET logic circuits.

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