Coulomb blockade effects and conduction mechanism in extremely thin polycrystalline-silicon wires

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Narrow ($\geqslant$95 nm) and extremely thin ($\sim$7 nm) heavily phosphorous-doped polycrystalline-silicon (poly-Si) wires were fabricated by low-pressure chemical vapor deposition. The electrical conduction mechanism has been investigated at low temperatures (down to $\sim$5 K), and observation by transmission electron microscopy (TEM) was carried out. Single-electron effects such as Coulomb oscillations have been observed at temperatures up to 80 K. The size of the island in the poly-Si wires was estimated from the electrical properties, and it was in the same order as the grain size of the poly-Si measured by TEM. A maximum tunnel barrier height of $\sim$26 meV of the poly-Si grain boundary is obtained from the temperature dependence of the conductance of the sample. A model for the electronic conduction through multiple islands was proposed from the width dependence of their electrical properties. © *2002 American Institute of Physics.*
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I. INTRODUCTION

Polycrystalline-silicon (poly-Si) is widely used as a key material in ultralarge-scale integrated circuits (ULSIs). With a reduction in the size of electronic devices, the thickness and width of the poly-Si wires decrease and may ultimately approach a limit where the presence of a single-electron effect determines the ''on'' and ''off'' states of the devices.[1–4] The thickness of thin film transistors and the width of the gate in the metal–oxide–semiconductor field-effect transistor are typical examples of reduction.

When the size of the poly-Si wire enters the nanoscale regime, single-electron charging effects appear at around room temperature and significantly influence electron transport in the devices. Therefore, it is necessary to clarify the influence of these single-electron charging effects in order to utilize ultrasmall poly-Si wires in the near future.

The structural characteristics of the poly-Si wires strongly depend on the deposition method and conditions, and directly influence the electrical properties. Ng *et al.*[5] examined the effect of wire length on the single-electron effect in ultrathin ($\sim$7 nm) wires of nanocrystalline silicon fabricated by electron-beam annealing of recrystallized hydrogenated amorphous silicon (*a*-Si) deposited by plasma-enhanced chemical vapor deposition (PECVD). In their work long wires of micron-scale length and 50 nm width were likely to exhibit the Coulomb blockade effect at a high temperature of 70 K. Furthermore, Tan *et al.*[6] also showed the single-electron effect at 15 K in 14-nm-thick poly-Si wires (30–90 nm widths) fabricated by annealing *a*-Si deposited by PECVD. Yano *et al.*[1] have demonstrated room-temperature operation of a single-electron memory in ultrathin (4 nm) undoped poly-Si film formed by solid-phase crystallization of *a*-Si deposited by low-pressure chemical vapor deposition (LPCVD). However, only a few studies have been reported on the single-electron effect in heavily doped poly-Si wires fabricated by LPCVD, which are most commonly used in ULSI processes.

In this article, we report detailed electrical and structural characteristics of heavily doped narrow and extremely thin poly-Si wires fabricated by LPCVD. We discuss the conduction mechanism, paying particular attention to the dependence on the wire width. We show that multiple islands in series connection contribute to the low-temperature electron conduction in the poly-Si wires, and that the Coulomb gap increases with decreasing wire width. We propose a model for the conduction mechanism in poly-Si wires of various widths, based on the experimental results.

II. EXPERIMENT

Thermal SiO_2 150-nm-thick was grown on *p*-type Si substrate with $\langle 100 \rangle$ crystal orientation and a resistivity of 8–12 $\Omega \cdot$cm, by wet oxidation at 1000 °C. Then, *a*-Si was deposited on the SiO_2 film at 520 °C by LPCVD using SiH_4 and polycrystallized by annealing at 650 °C for 10 min in N_2 ambient. This two-step process is effective for obtaining a smooth surface. The average sample thicknesses were $\sim$7, $\sim$10, and $\sim$82 nm. Doping of these samples was carried out by $POCl_3$ diffusion at 900 °C for 150 s ($\sim$7 nm), 60 s ($\sim$10 nm), and 300 s ($\sim$82 nm). We estimated the doping level of the poly-Si film by secondary ion mass spectroscopy (SIMS) analysis. The thickness of poly-Si film used for the SIMS measurement was $\sim$10 nm, and doping was carried out by $POCl_3$ diffusion at 900 °C for 150 s. The obtained doping level was about 3×10^{20} cm^{-3}. Since the temperature and the time of $POCl_3$ diffusion were the same as those for the thinner sample of $\sim$7 nm poly-Si, the doping level for the sample of $\sim$7 nm thickness was considered to be around or above 3×10^{20} cm^{-3}. The doped poly-Si wires were formed

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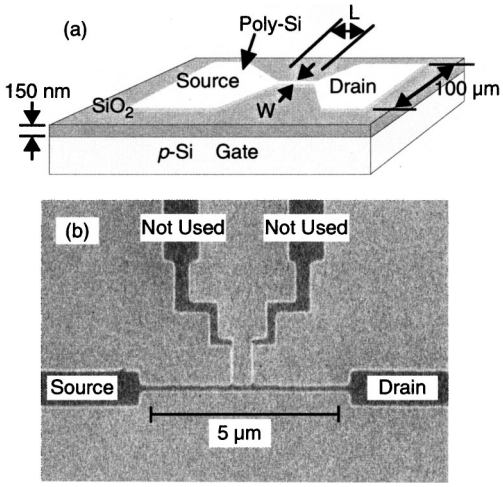

FIG. 1. (a) Schematic diagram of fabricated transistor structure with a narrow, extremely thin poly-Si wire. The average sample thicknesses are ~7, ~10, and ~82 nm. The nominal wire length L and the width W of the fabricated pattern are 4, 5, and 7 μm and 95–2000 nm, respectively. (b) Plan-view SEM of the fabricated poly-Si wire. The wire length and the width are 5 μm and 175 nm, respectively.

by electron-beam lithography and dry etching using the electron cyclotron resonance etcher. Figure 1(a) shows a schematic drawing of the fabricated narrow, extremely thin poly-Si wire. The transistor operation was achieved using the substrate as a gate. Figure 1(b) shows a plan-view scanning electron micrograph of the fabricated poly-Si wire; the wire length and the width were 5 μm and 175 nm, respectively. The passivation SiO_2 film was deposited by atmospheric-pressure chemical vapor deposition at 400 °C using $SiH_4 + O_2$. The contact holes were formed by wet etching, and an Al electrode was formed by sputter deposition and wet etching. Finally, the sample was annealed at 400 °C for 30 min in a $H_2 + N_2$ mixture to reduce the contact resistance. The nominal wire length and the width of the fabricated patterns were 4, 5, 7 μm and 95–2000 nm, respectively.

We studied the microstructure of the fabricated poly-Si wires via transmission electron microscopy (TEM) with a Hitachi HF-2100 operated at 200 kV. We prepared the cross sectional TEM samples using focused ion beam etching with Ga ions. Current–voltage ($I-V$) measurements were performed with a HP 4156A semiconductor parameter analyzer. Low-temperature measurements were carried out with a cryogenic manipulated probe system (HYTT-01) in the temperature range from 4.2 to 300 K.

III. RESULTS AND DISCUSSION

A. Thickness dependence

We investigated the thickness dependence of the Coulomb gap. Figure 2 shows drain current (I_d) versus drain voltage (V_d) characteristics for three samples with different average thicknesses. The measurement temperature was 10 K. The nominal length and width of the three samples were almost the same. The Coulomb gap is defined as the voltage region in the central area of the I_d-V_d curve where the absolute value of the current is lower than 30 fA, because the minimum measurable current with our experimental setup is

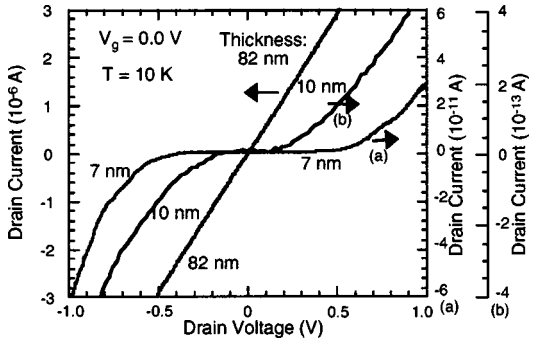

FIG. 2. Drain current (I_d) vs drain voltage (V_d) characteristics for three samples with different poly-Si thicknesses. Gate voltage V_g is 0.0 V. The measurement temperature is 10 K. The nominal length (5 μm) and width (100 nm) of the three samples are almost constant. The average thicknesses of the three samples are ~7 nm (from 4 to 9 nm), ~10 nm (from 8 to 12 nm), and ~82 nm (from 80 to 86 nm).

30 fA. It is observed in Fig. 2 that the Coulomb gap becomes small with increasing thickness. With the thickness of ~82 nm, the Coulomb gap could not be observed.

Cross sectional microstructures of the three kinds of poly-Si wires with different thicknesses are shown in Fig. 3. The average poly-Si film thicknesses measured by TEM were (a) ~7 nm (from 4 to 9 nm), (b) ~10 nm (from 8 to 12 nm), and (c) ~82 nm (from 80 to 86 nm). The grain sizes in the three samples measured by TEM varied: (a) from 14 to 60 nm, (b) from 20 to 80 nm, and (c) from 35 to 80 nm. The grain boundaries between the grains can be seen as regions without the crystal orientation, by TEM. The grain boundary as seen by TEM is considered to consist of amorphous material or a layer of highly disordered atoms. Figure 3 shows that the height of the poly-Si grains is nearly equal to the film thickness and that the lateral size of the grains increases with increasing thickness of the poly-Si film. One possible reason for this thickness dependence of the Coulomb gap in Fig. 2 is that poly-Si grains are the islands responsible for the

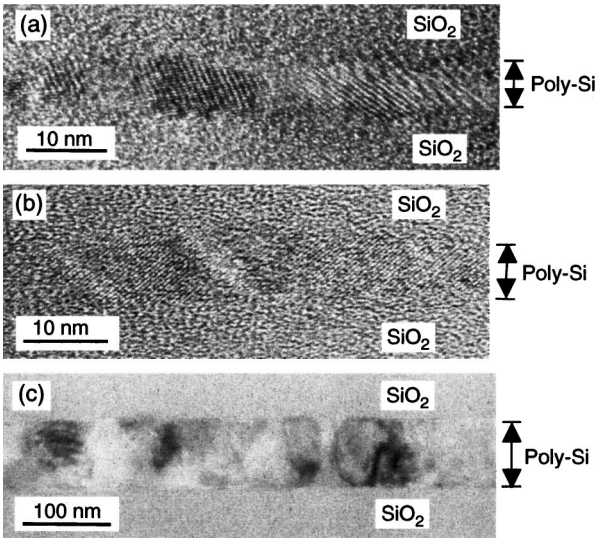

FIG. 3. Cross sectional TEM micrographs of the fabricated poly-Si wires. The average thicknesses of the poly-Si wires are (a) ~7 nm, (b) ~10 nm, and (c) ~82 nm.

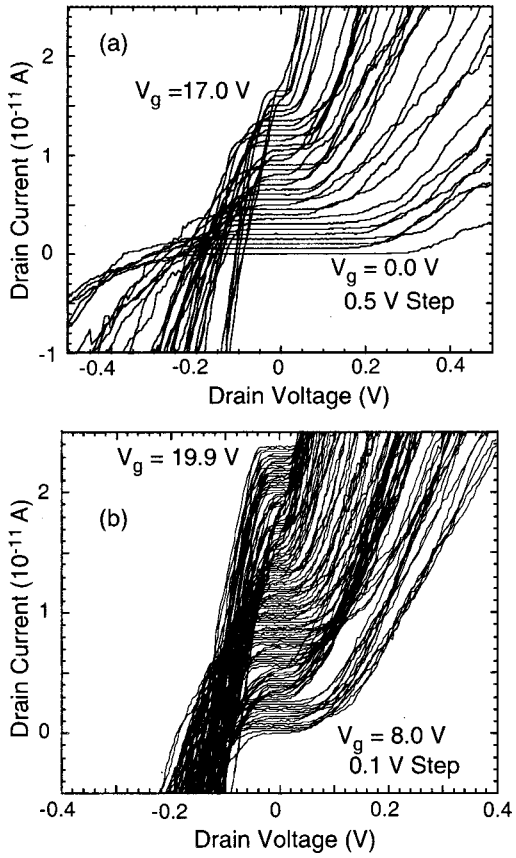

FIG. 4. I_d vs V_d characteristics as a function of substrate voltage (V_g) at 6 K(a) V_g from 0.0 to 17.0 V in V_g steps of 0.5 V. Each curve is offset by 0.5 pA of I_d for clarity. (b) V_g from 8.0 to 19.9 V in V_g steps of 0.1 V. Each curve is offset by 0.2 pA. The nominal wire length and width are 5 μm and 170 nm, respectively. The average thickness of the poly-Si wire is ~7 nm.

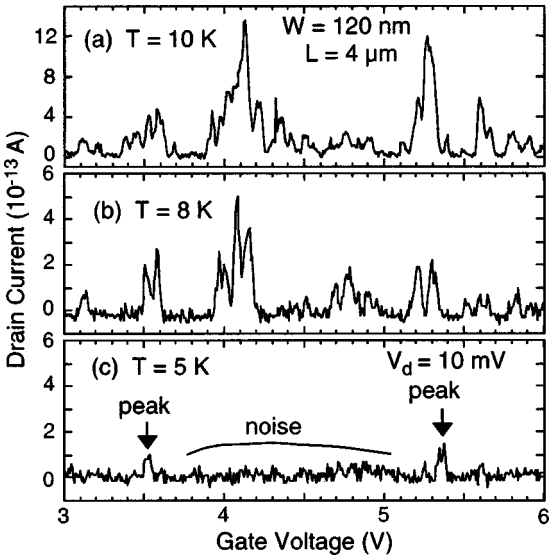

FIG. 5. I_d vs V_g characteristics at three different temperatures: (a) $T=10$ K, (b) $T=8$ K, (c) $T=5$ K. V_d is 10 mV. The nominal wire length and width are 4 μm and 120 nm, respectively. The average thickness of the poly-Si wire is ~7 nm.

gap. Since the island becomes larger with increasing sample thickness, the total capacitance of islands becomes high with increasing sample thickness. This leads to the low charging energy of the islands and the small Coulomb gap.

B. Coulomb blockade and oscillation characteristics

Figure 4 shows the I_d versus V_d characteristics as a function of substrate voltage (V_g) at 6 K. The average thickness of the poly-Si wire is ~7 nm. Figure 4(a) shows I_d-V_d curves for V_g from 0.0 to 17.0 V in V_g steps of 0.5 V. Each curve is offset by 0.5 pA of I_d for clarity. Figure 4(b) shows I_d-V_d curves for V_g from 8.0 to 19.9 V in V_g steps of 0.1 V. Each curve is offset by 0.2 pA of I_d. A zero-current Coulomb gap region and the modulation of the Coulomb gap by V_g are clearly observed. When the electron conduction occurs through a single-Coulomb island, a regular diamond-like pattern of characteristics of the same size should appear periodically with the gate voltage. Since the sizes of the patterns in Fig. 4 are not constant, the electron conduction is thought to be through multiple Coulomb islands of various sizes, giving rise to fluctuation in the Coulomb gap. It is noted that in Fig. 4, the Coulomb gap is extremely large in the V_g region near $V_g=0$ V. The reason for this may be the change in effective island size due to the change in the Fermi level with gate bias voltage.[1,6] Also, there is a possibility that the potential fluctuation in a poly-Si grain due to the impurity fluctuation has an influence on the size of the island and the Coulomb gap. However, the dopants are thought to be preferentially in the poly-Si grain boundary region forming the potential barriers as described later (Sec. III C). Thus, the potential fluctuation in a grain is thought to be small compared to the barrier height at grain boundary. Therefore, we think the effect of the impurity fluctuation in a grain on the island size is small.

Figure 5 shows the temperature dependence of I_d versus V_g characteristics. The nominal wire length and width were 4 μm and 120 nm, respectively. The average thickness of the poly-Si wire was ~7 nm. Complex, but reproducible Coulomb oscillations are seen in Fig. 5. Since a single island would produce a simple periodic current oscillation, the observed complex Coulomb oscillations can not be explained by a single-island system. The number of observed peaks originating from the Coulomb oscillations gradually increases with rising temperature. A few irregular peaks are expected in the Coulomb oscillation for multiple islands in series according to Ruzin *et al.*,[7] because the coincidence in electrochemical potential among multiple islands in series connection does not occur simultaneously at low temperatures and low drain voltage. Ruzin *et al.*[7] demonstrated theoretically that the number of peaks of Coulomb oscillation increases with increasing temperature due to the thermal broadening of the energy levels in two islands connected in series. Moreover, Kemerink and Molenkamp[8] experimentally observed the increase in the number of peaks with increasing temperature for a double-island system connected in series in the (Al,Ga)As heterostructure. Here, we have also observed, for the poly-Si wire, that the number of peaks of Coulomb oscillation increased with increasing temperature for the multiple-island system. For a single-Coulomb island, neglecting quantum confinement effects,[9,10] the condition required for observing a conductance peak is given by[11]

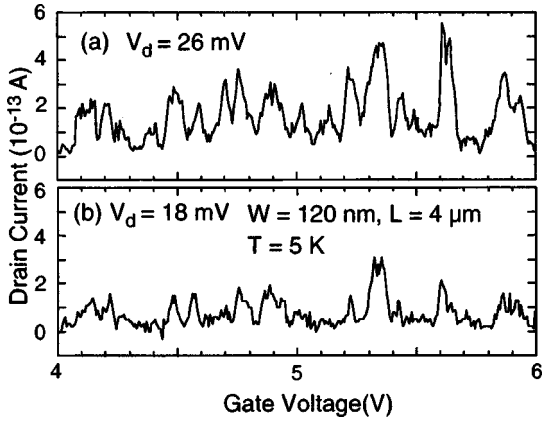

FIG. 6. I_d vs V_g characteristics at two different drain voltages: (a) $V_d=26$ mV and (b) $V_d=18$ mV. The graph for $V_d=10$ mV is the same as that shown in Fig. 5(c). The measurement temperature was 5 K. The nominal wire length and width are 4 μm and 120 nm, respectively. The average thickness of the poly-Si wire is ~7 nm.

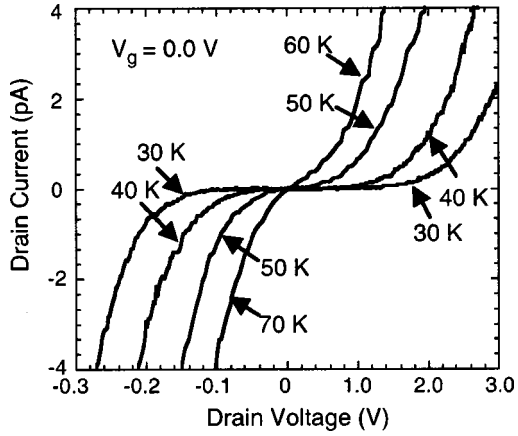

FIG. 7. I_d vs V_d characteristics at four different temperatures. V_g is 0.0 V. The nominal wire length and width are 7 μm and 120 nm, respectively. The average thickness of the poly-Si wire is ~7 nm.

$$V_g=\frac{e}{C_g}\left(n+\frac{1}{2}\right),\quad n=0,\pm1,\pm2,\ldots, \tag{1}$$

where C_g is the island-to-gate capacitance and e is the electron charge. For electrical conduction to occur in multiple islands connected in series, electrochemical potentials of each island must be in the same level within the limits imposed by thermal smearing. At low but finite temperatures, this implies

$$\left|eV_g-\left(n_m+\frac{1}{2}\right)\Delta_m\right|\leqslant k_BT,\quad n=1,2,\ldots, \tag{2}$$

where k_BT is the thermal energy, n_m is the number of electrons on the mth island, and $\Delta_m=e^2/C_{gm}$ (C_{gm} is C_g of the mth Coulomb island). Therefore, condition (2) will rarely be fulfilled simultaneously at low temperatures ($k_BT \ll \Delta_1/2, \Delta_2/2,\ldots$). This leads to fewer conductance peaks. Since k_BT determines the allowable mismatch among the electrochemical potentials of all of the islands, the number of V_g values of which condition (2) is fulfilled increases with increasing temperature.[8]

Figure 6 shows I_d versus V_g characteristics with a parameter of V_d (18 and 26 mV) at 5 K. The plot for $V_d=10$ mV is the same as that in Fig. 5(c). As V_d increases (from 10 to 18 and 26 mV), new peaks due to the Coulomb oscillation appear, and finally the peaks of Coulomb oscillation become periodic (at $V_d=26$ mV). This period corresponds to the C_g for the largest island in the wire, as follows. The period (ΔV_g) of Coulomb oscillation is about 0.1 V, as shown in Fig. 6(a). From $C_g=e/\Delta V_g$, C_g is estimated to be 1.6 aF. Assuming that C_g is a simple parallel-plate capacitor where the plate separation is equal to the SiO_2 thickness (150 nm), the island size is estimated to be 90 nm. This is close to the large grain size (60 nm) observed in the cross sectional TEM micrograph shown in Fig. 3(a). An amplitude modulation of the Coulomb oscillations is also seen as V_d is increased to 26 mV. This modulation is considered to be due to the different periods of Coulomb oscillations for the other smaller islands. These results of the drain voltage dependence of Coulomb oscillations indicate that the tunneling process occurs in the nonresonant inelastic tunneling mode in our experiment.[12] In nonresonant inelastic tunneling, an electron can tunnel through the multiple barriers between two adjacent islands nonresonantly by emitting acoustic phonons.[12] Wang and Tarucha[12] observed that irregular Coulomb oscillation peaks were observed at low drain voltages and the number of the peaks increases with increasing drain voltage for an asymmetric double-island system connected in series in a pseudomorphic AlGaAs/InGaAs/GaAs modulation-doped heterostructure. Furthermore, they reported that the irregular Coulomb oscillations change into periodic oscillations with increasing drain voltage.[12] They interpreted their results in terms of the stochastic Coulomb blockade model and nonresonant inelastic tunneling. We have also observed that the Coulomb oscillations become periodic with increasing drain voltage in our multiple-island Si system (see Fig. 6).

Figure 7 shows the temperature dependence of I_d versus V_d characteristics. Here, V_g is 0.0 V. As the temperature increases, the voltage range corresponding to the zero current region in the central area of the I–V curve decreases. A nonlinearity in the I_d versus V_d curves is observed up to about 80 K (not shown in Fig. 7). However, the Coulomb gap where the current level is the noise level remains up to about 40 K in this sample. Cordan *et al.*[13] reported that the Coulomb gap disappears at a much lower temperature than that where the nonlinearity disappears in the two-dimensional (2D) array of disordered islands. They insisted that the decrease in the critical temperature of the disappearance of the Coulomb gap is related to the change in conduction path with temperature in the 2D disordered array. In addition, the conduction path can also be changed with V_g. Therefore, it is complex and difficult to estimate the charging energy of the islands from this temperature dependence of the Coulomb gap.

Tan *et al.*[6] estimated the charging energy of the minimum island and its size from the temperature at which a Coulomb oscillation disappears in the multiple-island system. Thus, we also obtained the critical temperature (T_C) for the estimation of charging energy and the island size. Figure

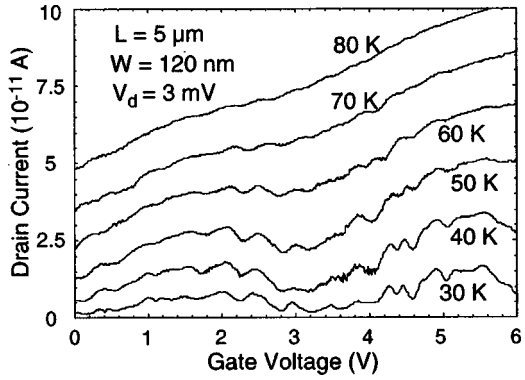

FIG. 8. I_d vs V_g characteristics of poly-Si wire at $V_d=3$ mV for various temperatures from 30 to 80 K. The conductance oscillations are observed up to about 80 K. The nominal wire length and width are 5 μm and 120 nm, respectively. The average thickness of the poly-Si wire is ~7 nm.

8 shows I_d versus V_g characteristics of poly-Si wire at $V_d=3$ mV for various temperatures from 30 to 80 K. In Fig. 8, the Coulomb oscillation can be seen up to about 80 K. On the basis of the orthodox Coulomb blockade theory,[11,14] Coulomb oscillations are visible up to T_C which is related to the charging energy (E_c) of the associated island by $E_c=e^2/(2C_\Sigma)\approx 2-3k_BT_C$. Here, C_Σ is the total capacitance corresponding to the smallest island in the poly-Si wire. Using this temperature (80 K), the value of E_c is estimated to be ~14–21 meV, which leads to C_Σ of ~4–6 aF. To estimate the island size from the C_Σ experimentally obtained, we calculated C_Σ based on the rough approximation as follows. We assume that the shape of the island in the poly-Si wires is cylindrical, and the surrounding islands are uniformly and densely distributed around this island. Since the capacitance between the island and gate is much smaller than that between the islands due to the thick gate SiO_2. Then, the capacitance between the island and the surrounding islands is approximated by the coaxial cylindrical model $[2\pi\epsilon l/\log(b/a)]$. Here, ϵ is the dielectric constant of Si, l is the height of the cylinder (~7 nm), a the radius of the cylinder, and b the sum of the grain boundary width and a. Assuming that the width of the grain boundary $(b-a)$ is equal to the tunnel barrier width ~3 nm (theoretically estimated from grain boundary width in Refs. 15 and 16). The island size a is obtained as ~4 nm. This is comparable to the smallest grain size (14 nm) obtained from the cross sectional TEM micrograph shown in Fig. 3(a). Even if this rough estimate can not be applied to our experimental situation, we nevertheless obtain the appropriate order of magnitude for the size of the islands present in our disordered multiple-island system.

C. Temperature dependence of conductance

The electronic transport properties of poly-Si films are influenced by the grain boundaries.[17] The grain boundary has a complex structure usually consisting of a few atomic layers of disordered atoms. The atoms in the grain boundary represent a transitional region between the different orientations of neighboring crystallites. There are two distinct models for the effects of the grain boundary on the electrical properties

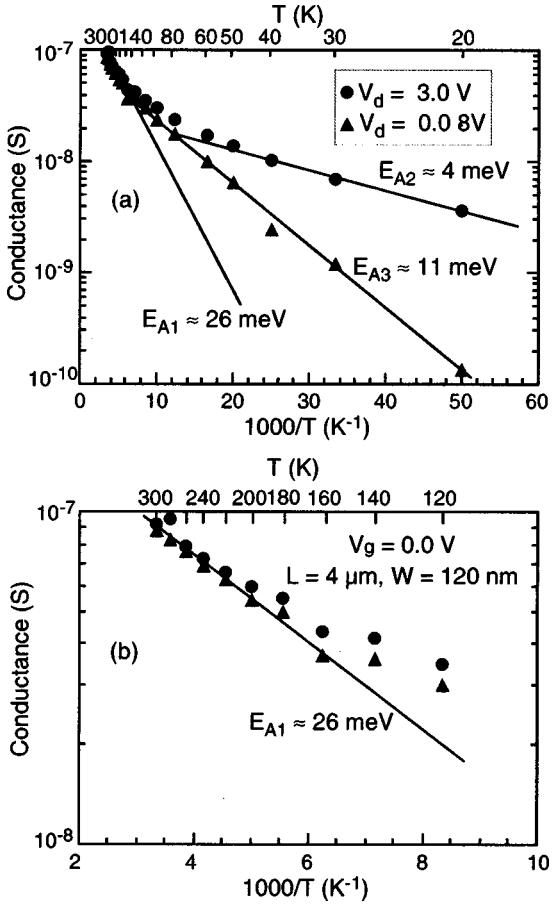

FIG. 9. (a) Arrhenius plot of the conductance at $V_d=3.0$ V (circles) and $V_d=0.08$ V (triangles). $V_g=0.0$ V. The nominal wire length and width are 4 μm and 120 nm, respectively. The average thickness of the poly-Si wire is ~7 nm. E_{A1} is the activation energy obtained at high temperatures (above 160 K). E_{A2} is the activation energy obtained at low temperatures (below 60 K) at $V_d=3.0$ V. E_{A3} is the activation energy obtained at low temperatures (below 160 K) at $V_d=0.08$ V. (b) Expanded figure for the temperature region from 120 to 300 K.

of doped poly-Si.[18] One is the segregated theory,[19] according to which impurity atoms tend to segregate at the grain boundary where they are electrically inactive. The other one is the grain boundary trapping theory[17] in which the presence of a large number of trapping states at the grain boundary is able to capture and therefore immobilize free carriers. These charged states at the grain boundary create potential barriers. These effects are likely to occur in poly-Si wires.[18]

We investigated the electron transport characteristics across the grain boundary from the temperature dependence of the conductance of the poly-Si wire. Figure 9 shows an Arrhenius plot of the conductance of the poly-Si wire as a function of inverse temperature: the temperature region (a) from 20 to 300 K and (b) from 120 to 300 K. The conductance was measured at $V_d=3.0$ V (circles) and 0.08 V (triangles). At $V_d=3.0$ V, the device operates outside the Coulomb gap. It is seen that the conductance is due to a thermally activated process, which has two different activation energies [E_{A1} at high temperatures (above 160 K) and E_{A2} at low temperatures (below 60 K)]. From the slopes of the fitted lines, $E_{A1}\sim 26$ meV and $E_{A2}\sim 4$ meV are obtained. Since at low temperatures the electron conduction is domi-

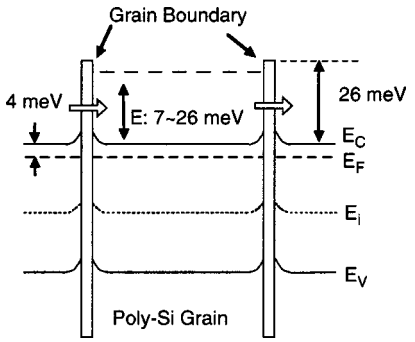

FIG. 10. Proposed energy-band diagram for the smallest island in the poly-Si wire. E is the energy level when one electron is added to the island.

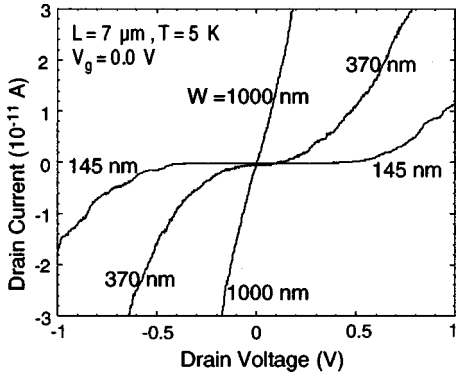

FIG. 11. Wire width dependence of I_d vs V_d characteristics at 5 K. V_g is 0.0 V. The length of the measured wires is constant (7 μm). The average thickness of the poly-Si wires is constant (~7 nm).

nated by a thermally assisted tunneling process through the barriers at the grain boundary,[16] E_{A2} (~4 meV) should be related to the change in the electron density and is considered to correspond to the difference between the Fermi level and conduction band edge of the poly-Si grains. On the other hand, at high temperatures above 160 K, the electron conduction is dominated by thermally activated hopping over the barriers at the grain boundaries. Therefore, E_{A1} (~26 meV) is considered to be the maximum barrier height at the grain boundary[17,18] (see Fig. 10).

On the other hand, for the measurement at $V_d = 0.08$ V, the device operates inside the Coulomb gap. In this case, we can obtain the two distinct activation energies [activation energy (~26 meV) at high temperatures (above 160 K) and E_{A3} (~11 meV) at low temperatures (below 160 K)]. At high temperatures above 160 K, the activation energy is the same as that (E_{A1}) at $V_d = 3.0$ V. This indicates that the Coulomb gap in this device disappears in the high-temperature region (above 160 K) and that the conduction mechanism for $V_d = 0.08$ V becomes similar to that for $V_d = 3.0$ V. When free electrons are the dominant charge carrier, the electron transport is attributed to a thermally assisted single-electron tunneling process through the barriers[16] at the grain boundaries at low temperatures. In this case, the activation energy ($E_{A3} \sim 11$ meV) is considered to be due to the sum of the charging energy of the island and the energy difference between the Fermi level and the conduction band edge in the poly-Si grains ($E_{A2} \sim 4$ meV). Therefore, the charging energy of the island in this device is obtained as ~7 meV (11−4 meV). However, this sample should be regarded as a 2 D array with disordered poly-Si grains since the width of this sample (120 nm) is larger than its grain size (from 14 to 60 nm). In such a 2D array, charge solitons may play a dominant role.[13,20,21] Following Tighe *et al.*,[20] the activation of the conductance in a Coulomb gap at low temperatures for a 2D array can be seen as the thermal generation of a population of free solitons and antisolitons able to move under an applied voltage. Tighe *et al.*[20] also showed that $4E_a = E_c$ for lithographically defined 2D regular arrays, where E_a is the activation energy observed in the Arrhenius plot of the conductance and E_c the charging energy of metal island. Following this relation, E_c in this sample becomes about 44 meV using $E_{A3} \sim 11$ meV. This value is inconsistent since it is larger than the previously obtained maximum barrier height, 26 meV. The existence of random offset charges may lead to the relation $E_c < 4E_a$ since they might play a role in screening the interaction between the soliton and antisoliton. The screening will lower E_c. Taking the ambiguity into account, the value of E_c is thought to be between 7 and 26 meV for this sample. This value is consistent with that obtained from the temperature at which the Coulomb oscillation disappears as previously obtained (14−21 meV) in Sec. III B. Figure 10 summarizes the proposed energy-band diagram for the poly-Si wires.

D. Wire width dependence and conduction mechanism

Figure 11 shows the wire width dependence of I_d as a function of V_d at 5 K. The nominal length and thickness of the measured wires were 7 μm and ~7 nm, respectively. The Coulomb gap for the wire width of 145 nm is ~550 mV, which is too large for the Coulomb gap of a single island. As previously described, the total capacitance of an island estimated at the temperature (80 K) where the Coulomb oscillation disappears, is ~4−6 aF, which corresponds to the Coulomb gap of ~40 mV. This estimated Coulomb gap is too small compared with the observed Coulomb gap (~550 mV) for the wire of 145 nm width in Fig. 11.

For the case of a single tunnel junction (TJ), the Coulomb gap corresponds to the voltage offset $V_{\text{off}} = e/C_t$ (C_t is the capacitance of a single TJ). Here, the voltage offset (V_{off}) means the width of the zero-current region due to the Coulomb blockade effect. However, for a system with multiple TJs connected in series, $V_{\text{off}} = Ne/C_t$, where N is the total number of TJs.[5] Therefore, the observed large Coulomb gap (~550 mV) suggests that the conduction is through multiple islands. Assuming the same island size, the number of islands is estimated to be about 13 (~550÷40). This is a simple estimation when the islands are all in series. Because the wire width used in the estimation is 145 nm, the sample is a 2D array of disordered islands rather than a one-dimensional array. It is reported that the Coulomb gap decreases with increasing width of the 2D array of islands.[13,22] Therefore, the number of islands connected in series can be considered to be greater than the above simply estimated number (13).

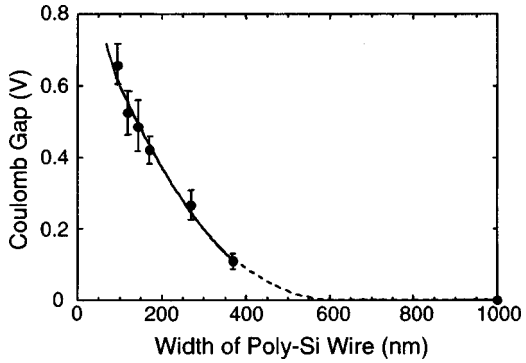

FIG. 12. Wire width dependence of Coulomb gap at 5 K. The length of the measured wires is constant (7 μm). The average thickness of the poly-Si wires is constant (~7 nm).

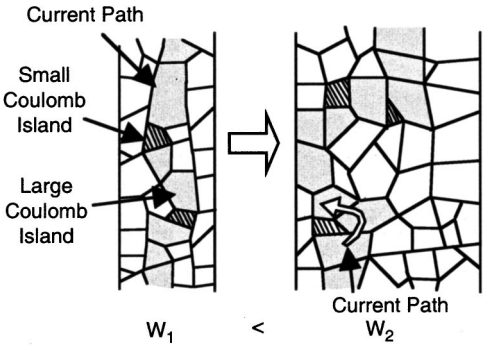

FIG. 13. Schematic representation of the wire dependence of the conduction mechanism.

It is also observed in Fig. 11 that the Coulomb gap becomes small with increasing wire width. For the width of 1000 nm, no Coulomb gap was observed. In addition, for narrower wires, step-like I_d-V_d characteristics are noticeable in the higher voltage region ($|V_d|>0.5$ V), which indicates the presence of the Coulomb staircase.

The width dependence of the Coulomb gap is examined in detail and summarized in Fig. 12. With increasing wire width, the Coulomb gap decreases and finally disappears at around 600 nm. It is speculated that there are two possible reasons for the decrease in the Coulomb gap. One is that islands become larger as the wire width increases. The other is that the number of islands which contribute the Coulomb gap in the current path becomes smaller with increasing wire width. The grain size of the poly-Si wire is determined by the conditions of the thermal processes. Since we annealed the *a*-Si films to achieve polycrystallization and doping before the poly-Si wires were patterned, the grain size is not changed on varying the wire width. Therefore, the size of the island in our sample does not vary. Because grains of various sizes exist in the poly-Si wire as seen in the cross sectional TEM micrographs [Fig. 3(a)], small poly-Si grains are regarded as the islands which contribute to the Coulomb gap. Therefore, it is considered that the number of islands which contribute to the electronic conduction becomes small with increasing wire width.

The reduction of the Coulomb gap with increasing width of the 2D array of islands in metallic dots has been reported by Cordan *et al.*[13] They have interpreted the reduction of the Coulomb gap as being due to the increasing probability for the conductive electrons to take a lower resistance path when the width becomes high. In their model, the size of the metallic dot is assumed to be almost constant and the fluctuation of the distance between the dots is considered to dominate the electronic conduction.

To explain the observed width dependence of the Coulomb gap, we propose a current path model in the poly-Si wire, as shown in Fig. 13. In our model, the grain-boundary thickness is assumed to be almost constant, and the grain size and poly-Si film thickness fluctuations, which are observed by TEM, mainly determine the electronic properties of the poly-Si wire. A similar model was also proposed by Yano *et al.*[1] Since a larger grain has a lower charging energy, the current tends to flow preferentially through the larger grains. When the wire becomes narrow, the probability for the electron to pass through the small grains becomes high. This leads to the observation of the large Coulomb gap for the narrow wires. When the wire becomes wide, the probability of the electron to meet the large grains becomes high, leading to the small Coulomb gap.

IV. CONCLUSIONS

The conduction mechanism of narrow and extremely thin poly-Si wires has been investigated by TEM and electrical measurements. We have observed the variation in size of diamond-like pattern of I_d-V_d characteristics and the complex reproducible Coulomb oscillations in the poly-Si wires. The temperature and V_d dependence of the number of peaks due to the Coulomb oscillation indicate that multiple islands connected in series contribute to the electron conduction in the wire. The size of the islands estimated from the electrical properties was in the same order as the grain size of the poly-Si measured by TEM. We have observed single-electron effects up to a temperature of 80 K. The maximum tunnel barrier height of 26 meV at the grain boundary was obtained from the temperature dependence of conductance. From the wire width dependence of the Coulomb gap, it was found that the Coulomb gap decreases with increasing wire width and finally disappears. The conduction mechanism of multiple islands connected in series was proposed to explain the wire width dependence and the observed magnitude of the Coulomb gap. The results of this study strongly suggest that the single-electron effects will become significant with down scaling of the device size of future ULSIs.

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[1] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, Appl. Phys. Lett. **67**, 828 (1995).
[2] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, Tech. Dig. Int. Electron Devices Meet. **1994**, 938 (1994).
[3] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, Appl. Phys. Lett. **70**, 1742 (1997).
[4] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, Appl. Phys. Lett. **71**, 353 (1997).
[5] V. Ng, H. Ahmed, and T. Shimada, J. Appl. Phys. **86**, 6931 (1999).
[6] Y. T. Tan, Z. A. K. Durrani, and H. Ahmed, J. Appl. Phys. **89**, 1262 (2001).
[7] I. M. Ruzin, V. Chandrasekhar, E. I. Levin, and L. I. Glazman, Phys. Rev. B **45**, 13469 (1992).
[8] M. Kemerink and L. W. Molenkamp, Appl. Phys. Lett. **65**, 1012 (1994).
[9] T. Suemoto, K. Tanaka, and A. Nakajima, Phys. Rev. B **49**, 11005 (1994).
[10] T. Suemoto, K. Tanaka, A. Nakajima, and T. Itakura, Phys. Rev. Lett. **70**, 3659 (1993).
[11] H. v. Houten, C. W. J. Beenakker, and A. A. M. Staring, *Single Charge Tunneling-Coulomb Blockade Phenomena in Nanostructures*, NATO ASI Series B, Physics, Vol. 294 edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992).
[12] T. H. Wang and S. Tarucha, Appl. Phys. Lett. **71**, 2499 (1997).
[13] A. S. Cordan, Y. Leroy, A. Goltzené, A. Pépin, C. Vieu, M. Mejias, and H. Launois, J. Appl. Phys. **87**, 345 (2000).
[14] G. Timp, *Nanotechnology* (Springer, New York, 1999).
[15] A. C. Irvine, Z. A. K. Durrani, and H. Ahmed, Appl. Phys. Lett. **73**, 1113 (1998).
[16] Y. L. He, G. Y. Hu, M. Liu, J. L. Wang, and G. Y. Xu, Phys. Rev. B **59**, 15352 (1999).
[17] J. Y. W. Seto, J. Appl. Phys. **46**, 5247 (1975).
[18] G. Baccarani, B. Ricco, and G. Spadini, J. Appl. Phys. **49**, 5565 (1978).
[19] A. L. Fripp, J. Appl. Phys. **46**, 1240 (1975).
[20] T. S. Tighe, M. T. Tuominen, J. M. Hergenrother, and M. Tinkham, Phys. Rev. B **47**, 1145 (1993).
[21] J. E. Mooij, B. J. van Wees, L. J. Geerling, M. Peters, R. Fazio, and G. Schon, Phys. Rev. Lett. **65**, 645 (1990).
[22] C. Vieu, A. Pepin, J. Gierak, C. David, Y. Jin, F. Carcencac, and H. Launois, J. Vac. Sci. Technol. B **16**, 3789 (1998).