Fabrication of Si single-electron transistors having double SiO_2 barriers

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(Received 7 February 2002; accepted for publication 22 April 2002)

We fabricated Si single-electron transistors (SETs) having double SiO_2 barriers and a polycrystalline Si (poly-Si) dot. The fabrication method of this device is completely compatible with the complementary metal–oxide–semiconductor technology, and the position of the poly-Si dot is self-aligned between the source and drain regions. The device exhibits drain current (I_d) oscillation against gate voltage. From the dot size dependence of the electrical characteristics, the I_d oscillation is considered to be due to the Coulomb blockade effect caused by poly-Si grains in the poly-Si dot. The self-alignment of the poly-Si dot in the fabrication process also means that the SET is promising for practical use. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1485306]

The single-electron device using the Coulomb blockade effect[1–17] is a promising candidate for future electron devices which can realize low power consumption and high integration. Research into the Si-based single-electron transistor (SET) has been carried out by many groups.[8–17] For the practical use of these SETs, room temperature operation of the device and the compatibility of the fabrication process with the complementary metal–oxide–semiconductor (CMOS) technology are extremely important.

In this study, we fabricated Si-based SETs having double SiO_2 barriers with a polycrystalline Si (poly-Si) dot and report their electrical characteristics from the viewpoint of their practical application. The fabrication method of this device is completely compatible with CMOS technology. This device has tunnel barriers with high potential, which will lead to high-temperature device operation, since a SiO_2 film is used for the tunnel barrier. To date, only a few SETs using the SiO_2 barrier have been reported.[14] Also in our device, the position of the poly-Si dot is precisely self-aligned between the source and drain, which will enable the easy fabrication of a single Coulomb island. Several self-aligned methods for Coulomb islands have been reported to date, where Si nanocrystals were deposited on the interelectrode region between the source and drain.[15–17] However, due to the random distribution of the position of the deposited Si nanocrystals, these methods are insufficient for forming a single Coulomb island in SETs. The method proposed here has the potential to realize the single Coulomb island system as described later. Previously, we developed a fabrication technology of the SET and evaluated plasma-induced damage at the sidewall of the Si trench in which a poly-Si dot is embedded.[18] In this study, we fabricate the SET using the developed technologies.

Figure 1 shows the schematic diagram of the fabricated SET. This is the same structure as we proposed previously.[18] The poly-Si dot is embedded in the trench. The thin (oxide thickness $T_{ox}=1.7$ nm) SiO_2 tunnel barrier surrounds the poly-Si dot, forming double tunnel barriers. A top poly-Si gate is used to invert the surface of the poly-Si dot. To produce a trench with a small width, we first deposited silicon dioxide by low-pressure chemical vapor deposition (LPCVD) using SiH_4 and N_2O at 750 °C on the Si substrate, and the oxide mask was patterned by using electron beam (EB) lithography and reactive ion etching (RIE). Several widths (50, 62.5, 87.5, and 100 nm) of the EB mask pattern (resist uncovered region) for the trench were used. The width of the oxide mask for the trench was reduced by etching back the successively deposited LPCVD SiO_2 film using RIE. The

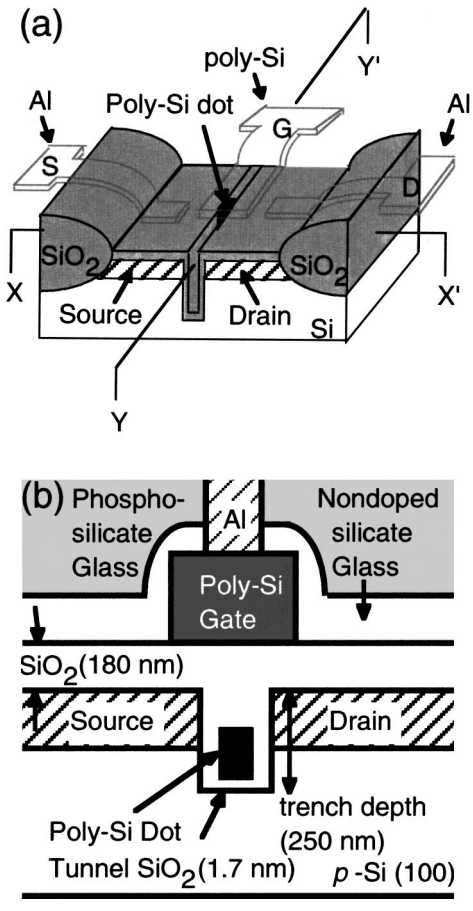

FIG. 1. (a) Schematic diagram of the Si single-electron transistor having double SiO_2 barriers with a poly-Si dot and (b) cross-sectional view along the $X-X'$ line.

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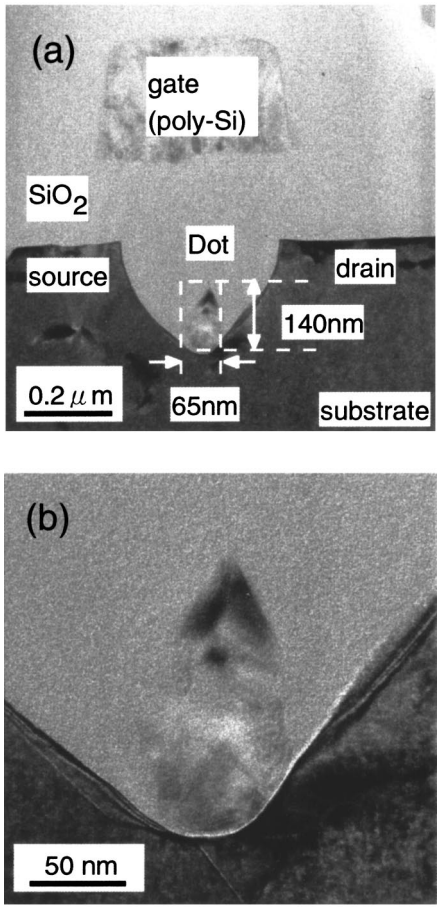

FIG. 2. (a) TEM micrograph of cross-sectional view along the $X-X'$ line in Fig. 1 and (b) high-resolution micrograph.

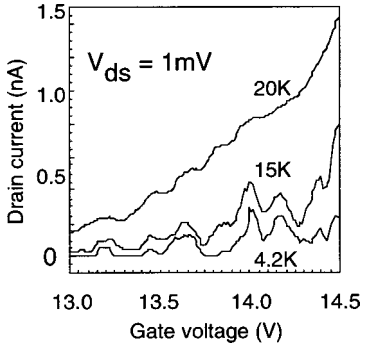

FIG. 3. Drain current (I_d) vs gate voltage (V_g) characteristics of the device (a) at 4.2, (b) at 15, and (c) at 20 K. Drain voltage (V_{ds}) is 1 mV. The mask width of the trench [along the $X-X'$ line in Fig. 1(a)] is 62.5 nm. The mask size along the $Y-Y'$ line is 100 nm.

sacrificial oxidation of 20 nm was carried out to eliminate the plasma-induced damaged layer due to the electron cyclotron resonance (ECR) etching of the Si substrate during the trench formation, which increases the leakage current.[18] After the sacrificial oxide was removed, a tunnel barrier was formed by the dry oxidation. Afterwards, the poly-Si was deposited and etched back to leave only the poly-Si in the trench. Then, a narrow line shape oxide mask pattern was formed using EB lithography perpendicularly across the trench. Using the mask, ECR etching was carried out. After these processes, the poly-Si dot was formed in the trench. We reduced the size of the poly-Si dot by wet oxidation at 1000 °C. After the gate insulator deposition (SiO_2, 113 nm) by the LPCVD using SiH_4 and N_2O at 750 °C and the top poly-Si gate formation, the gate and source/drain regions were heavily As^+ implanted. We measured the size, shape, and position of the fabricated poly-Si dot using transmission electron microscopy (TEM) with a Hitachi HF-2100 operating at 200 kV.

Figure 2(a) shows a cross-sectional TEM micrograph along the $X-X'$ line of the fabricated SET shown in Fig. 1. This micrograph indicates that the poly-Si dot has indeed been formed inside the trench. It should be noted that it is rather difficult to find the poly-Si dot position and we prepared the TEM sample using focused ion beam (FIB) etching with Ga ions in order to find the dot. It is seen that the width of the trench surface is about 250 nm although the width of the mask pattern for the trench was 62.5 nm. The reason for the size difference is considered to be the effects of the resolution of the lithography, side etching in dry etching, sacrificial oxidation, and the oxidation for reducing the poly-Si dot. The lateral size and height of the poly-Si dot were observed to be about 65 and 140 nm, respectively. Also, we were able to find the poly-Si grain in the poly-Si dot [Fig. 2(b)] with the size of 10–50 nm.

Figure 3 shows the temperature dependence of drain current (I_d) versus gate voltage (V_g) characteristics for the SET with the same width of mask pattern for the trench (62.5 nm) as that shown in Fig. 2. The periodic Coulomb oscillation is observed up to 20 K. This periodic oscillation suggests that the Coulomb oscillation occurred from a single Coulomb island, as explained later. The observed period ΔV is about 180 mV. From this value, the gate capacitance C_{gi} between the top gate and the island is evaluated to be 0.90 aF using the formula $\Delta V = e/C_{\mathrm{gi}}$. On the other hand, the gate capacitance of the poly-Si grain with the size of 50 nm is calculated to be 0.94 aF from the self-capacitance, considering the ratio of the solid angle for the dot toward the top poly-Si gate. Here, we used the oxide thickness of 300 nm from the TEM micrograph [Fig. 2(a)]. Since this gate capacitance value is close to the experimentally obtained C_{gi}, we believe that such a poly-Si grain is the Coulomb island. Taking the electron tunnel probability into account, the current path is considered to be close to the bottom of the trench because thin SiO_2 barrier exist only near the bottom as can be seen in Fig. 2(b). An electron probably tunnels from the Si-substrate region (source side) close to the bottom of the trench into the poly-Si dot due to the gate electric field and tunnels out to the Si-substrate region (drain side) near the bottom due to the drain voltage. It is noted that the background current increases with increasing V_g. Since the junction depth of the source and drain is simulated to be around 50–110 nm,[18] which is shallower than the trench depth, the current increase is considered to be due to the inversion current which flows along the bottom surface of the trench.

Figure 4 shows I_d vs V_g characteristics of the SET with different EB mask widths for the trench. The EB mask widths (along the $X-X'$ line) are 50 and 100 nm for the devices in Figs. 4(a) and 4(b), respectively. The EB mask pattern size along the $Y-Y'$ line is the same (100 nm) for both devices. Since the dot formation has been carried out under the same conditions for dry etching and thermal oxi-

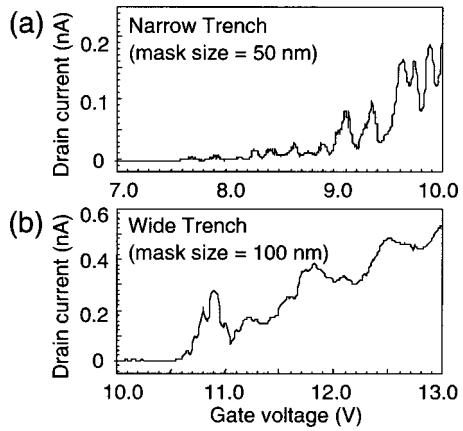

FIG. 4. Drain current (I_d) vs gate voltage (V_g) characteristics of the single-electron transistor having different trench widths at 4.2 K. Drain voltage (V_{ds}) is 1 mV. The mask size along the $Y-Y'$ line in Fig. 1(a) is 100 nm. The width of the trench surface is estimated to be about 240 nm [(a), mask size of 50 nm] and 290 nm [(b), mask size of 100 nm] along the $X-X'$ line.

dation for all EB trench mask widths, the difference in mask width is almost equal to the difference in the actual width of the poly-Si dot. Thus, the device with a small EB trench mask width is considered to have a poly-Si dot with small width. In Fig. 4(a), we observe a periodic I_d oscillation with a period of about 200 mV. This period is slightly larger than that (180 mV) in Fig. 3, suggesting that the Coulomb island of the sample shown in Fig. 4(a) is slightly smaller than that of the sample shown in Fig. 3. On the other hand, complex and irregular but reproducible Coulomb oscillations are seen in Fig. 4(b). Since a single Coulomb island would produce a periodic simple Coulomb oscillation, the observed complex Coulomb oscillations cannot be explained by a single Coulomb island system.[5,11,16,17] It is noted that the periodic oscillations become difficult to be observed with increasing trench width. Since the size of the grain is almost the same on average in spite of the change in the trench width, the number of grains in the poly-Si dot is considered to increase with the trench width. This leads to the increase in the number of SETs having more than two Coulomb islands connected in series, if we assume that the poly-Si grain is the Coulomb island. Such SETs with multiple Coulomb islands show a complex and irregular Coulomb oscillation. Therefore, we consider the SET in Fig. 4(b) to have multiple Coulomb islands. It is to be noted that the heavy oxidation carried out in this study for the size reduction of the poly-Si dot may lead to oxidation in the grain boundary region in the dot, causing the tunnel barriers to have high potentials.

In our SET, the self-aligned poly-Si dot has been formed in the trench region. If the width of the trench is made smaller than about 50 nm by optimizing the lithography and etching conditions, we can fabricate a poly-Si dot consisting of only one grain since the grain size is about 10–50 nm as described earlier, which leads to a single Coulomb island. To reduce the width of the poly-Si dot along the $Y-Y'$ line, a combination of wet etching[19] in $NH_4OH/H_2O_2/H_2O$ with thermal oxidation is another promising way.

In summary, we developed a self-aligned method for fabricating a poly-Si dot between the source and drain regions for the Coulomb island in SETs. Utilizing this technique, we fabricated SETs with SiO_2 double tunnel barriers and the poly-Si dot, and reported their I_d-V_g characteristics. We observed the shape and the microstructure of the dot using TEM with the FIB method. On the basis of the C_{gi} value calculated geometrically, which is close to that obtained experimentally, and the trench width dependence of the Coulomb oscillation, we regarded the poly-Si grain in the dot as the Coulomb island. We found that when the trench is very narrow ($\leqq$ mask size of 62.5 nm), there are SETs with only one Coulomb island along the current path. By optimizing the fabrication process for the poly-Si dot to reduce its size, the SET will be able to operate at higher temperatures due to the SiO_2 high potential barriers.

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