Soft-breakdown-suppressed ultrathin atomic-layer-deposited silicon–nitride/SiO_2 stack gate dielectrics for advanced complementary metal–oxide–semiconductor technology

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We report a high-quality, ultrathin atomic-layer-deposited silicon–nitride/SiO_2 stack gate dielectric. p^+-polycrystalline silicon gate metal–oxide–semiconductor (MOS) capacitors with the proposed dielectrics showed enhanced reliability with respect to conventional SiO_2. An exciting feature of suppressed soft-breakdown (SBD) events is observed in ramped voltage stressing which has been reconfirmed during time-dependent-dielectric breakdown measurements under constant field stressing. Introducing the idea of injected-carrier-induced localized physical damages resulting in the formation of conductive filaments near both Si/SiO_2 and poly-Si/SiO_2 interfaces, a model has been proposed to explain the SBD phenomena observed in the conventional SiO_2 dielectrics. It is then consistently extended to explain the suppressed SBD in the proposed dielectrics. The reported dielectric can be a good choice to meet the urgent need for highly reliable ultrathin gate dielectrics in nanoscale complementary-MOS technology. © *2001 American Institute of Physics.*
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Aggressive scaling of gate oxide thickness for nanoscale complementary metal–oxide–semiconductor (CMOS) technology has raised reliability concerns under normal as well as anomalous operating conditions. The major problems associated with the decreased oxide thickness are a significant increase of gate leakage current and boron penetration in surface-channel *p*-MOS devices with p^+-polycrystalline silicon (poly-Si) gates.[1] It is reported that these ultrathin oxides exhibit a new stable failure mode referred to as soft-breakdown (SBD) in addition to the well-known stress-induced leakage current (SILC) and hard-breakdown (HBD) phenomena.[2] The SBD phenomena in ultrathin gate oxides has been described as a severe problem in the progress of the scaling trend of device dimensions towards nanoscale generation and it has been a loud roar in the research community in recent years.[2–9] One efficient way to reduce these unwanted events is to go for an alternate gate dielectric better than SiO_2. Stack dielectrics of silicon–nitride/SiO_2 have been suggested as promising gate dielectrics due to their thinner equivalent oxide thickness and more effective suppression of boron penetration compared to thermally grown oxides or oxynitrides of identical thicknesses.[10,11] However, reports of SBD free ultrathin dielectrics are still missing in the literature. The SBD event causes unpredicted and premature failure of device operations. Therefore, gate dielectrics free from the SBD phenomena are highly desired to meet the scaling requirements for advanced CMOS technology. In this work, we report a high-quality, ultrathin, atomic-layer-deposited (ALD) silicon–nitride/SiO_2 stack gate dielectric with excellent properties against stress-induced leakage and importantly free from the curse of the SBD phenomena.

p^+-poly-Si gate MOS capacitors with both ALD silicon–nitride/SiO_2 stack gate dielectrics and conventional SiO_2 dielectrics are fabricated using *n*-type Si(001) wafers (10 Ω cm). An extremely thin layer (~0.4 nm) of silicon nitride is deposited on thermally grown ultrathin (2.0 nm) SiO_2 using an alternate technique[11] for N-atom-profile engineering by employing self-limiting atomic-layer-deposition of silicon nitride. After the silicon–nitride deposition, a 200 nm thick poly-Si gate is formed by 20 keV BF_2^+-ion implantation at a dose of $5\times10^{15}\,cm^{-2}$ followed by an activation annealing at 1000 °C for 40 s in a N_2 ambient. The capacitors thus fabricated are subjected to various standard electrical stressing to measure stress-induced leakage, subsequent breakdown, and time-dependent dielectric breakdown (TDDB) characteristics and has been compared with those of capacitors with conventional SiO_2 dielectrics. Note that the gate voltages in all electrical stressing measurements are determined so as to induce the same oxide electric fields in either dielectrics.

Figure 1 shows the current versus oxide-field characteristics representing stress-induced leakage and breakdown of ALD silicon–nitride/SiO_2 stack gate dielectrics, while the corresponding characteristics for the conventional SiO_2 di-

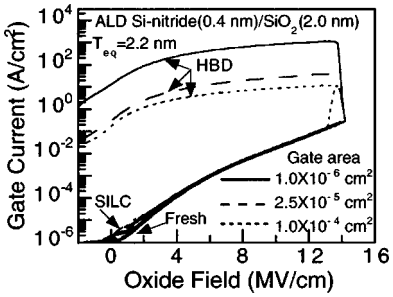

FIG. 1. Ramped voltage induced gate current density as a function of oxide field for MOS devices with ALD silicon–nitride/SiO_2 stack gate dielectrics.

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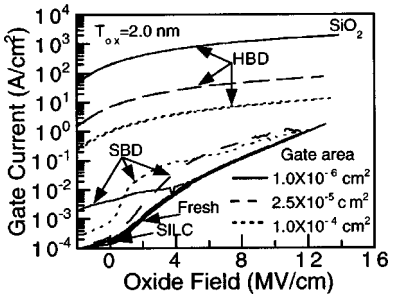

FIG. 2. Ramped voltage induced gate current density as a function of oxide field for MOS devices with conventional SiO_2 dielectrics. Only the onset of SBD events are presented. Several such SBD events are observed before the HBD in each device.

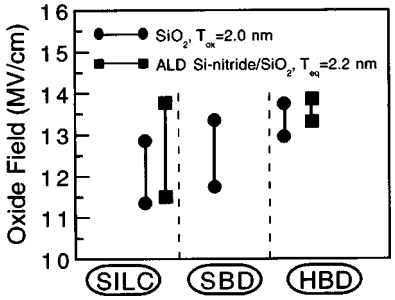

FIG. 3. Oxide field bands of electrical stress induced phenomena for MOS devices with both ALD silicon–nitride/SiO_2 and conventional SiO_2 gate dielectrics.

electrics are presented in Fig. 2. The dielectric quality (leakage and breakdown characteristics shown in Figs. 1 and 2) is investigated by ramped voltage electrical breakdown measurements wherein the maximum gate voltage is slightly increased in successive measurement cycles. From the onset of SILC, the increment of the maximum gate voltage in successive cycles is restricted to 0.02 V for precise determination of each breakdown mode and the respective transitions. It is obvious in Fig. 1 that the ALD silicon–nitride/SiO_2 dielectrics show excellent stability against high voltage stressing and a small amount of SILC flows through the gate before a sharp and sudden breakdown at very high oxide fields. An exciting feature to be noticed is the disappearance of the so-discussed SBD phenomenon. On the other hand, as can be seen in Fig. 2, all known stress induced features (SILC, SBD, and HBD) are present in the conventional SiO_2 MOS capacitors. It is worth mentioning that the results presented in Figs. 1 and 2 are reconfirmed in as many as 25 test devices of each type. Note that only the onset of SBD events are presented in Fig. 2, while several such events are observed before the HBD in each test devices with SiO_2 dielectrics. This is consistent with reported experimental results[9] and demonstrates that the change from SBD to HBD is continuous, which indicates the possibility that a common statistical origin is being shared by these breakdown phenomena.

Now, the observed SBD phenomena in the conventional SiO_2 dielectrics and suppressed SBD in the ALD silicon–nitride/SiO_2 dielectrics can be explained using the concept of injected-carrier-induced localized physical damages resulting in the formation of conductive filaments near the Si/SiO_2 interface.[3,12] We propose the formation of localized conductive filaments near both the Si/SiO_2 and the poly-Si/SiO_2 interfaces caused by the injected carriers during high voltage stressing. In our measurements with the substrate in accumulation, electrons are injected from the *n*-type substrate while a small number of holes are injected from the poly-Si gate. The formation of conductive filaments near the poly-Si/SiO_2 interface is likely due to poor interfacial inhomogeneities.[13,14] These conductive filaments from both the interfaces trigger the SBD through a reduction of effective oxide thickness leading to the eventual HBD. This model can be extended to explain the suppressed-SBD phenomena observed in the devices with the ALD silicon–nitride/SiO_2 stack gate dielectrics as well. Note that an extremely thin and very uniform silicon nitride layer on a thermally grown oxide substantially improves the interface quality of the ALD Si–nitride/SiO_2 interface. Likewise, formation of the conductive filaments at the poly-Si/ALD Si–nitride interface is suppressed due to a strengthened structure of Si–N bonds.[15] As a consequence, unlike the poly-Si/SiO_2 interface, the formation of conductive filaments are suppressed near the poly-Si/ALD Si–nitride/SiO_2 interfaces during electrical stressing. Localized physical damages, however, occur at the Si/SiO_2 interface and bulk SiO_2 causing SILC, but the effective thickness reduction is inadequate to trigger the SBD before the eventual HBD. The HBD occurs due to the formation of a conductive path between the gate and substrate by the activation of sufficient number of distorted $Si–O_4$ tetrahedron with strained Si–O bonds and other H-related trap precursors.[16,17]

Figure 3 presents the oxide field bands for SILC, SBD, and HBD as observed in all test devices of each dielectric type. The lower end of each band indicates the onset of the respective degradation mode as mentioned along the horizontal axis. It exhibits that SILC and HBD degradation modes occur at lower fields in SiO_2 devices than in ALD silicon–nitride/SiO_2 devices. It also reveals that the ALD silicon–nitride/SiO_2 has no SBD events which indicates excellent dielectric properties against high voltage stressing.

Superior quality of the proposed dielectric is further verified by measuring TDDB characteristics under constant oxide field stressing. A representative plot of current versus time during the constant field (12 MV/cm) stressing is shown in Fig. 4, while the Weibull plot of the TDDB characteristics is presented in Fig. 5. The data presented in Figs. 4 and 5 are measured under the same oxide field for all the devices regardless of dielectric types. These results demonstrate substantially improved dielectric reliability in favor of the proposed stack dielectric. A region with an unstable current is observed in ultrathin SiO_2 dielectrics as can be seen in Fig. 4,

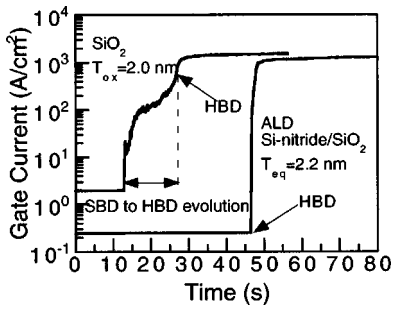

FIG. 4. A representative TDDB characteristics under constant field (12 MV/cm) stressing.

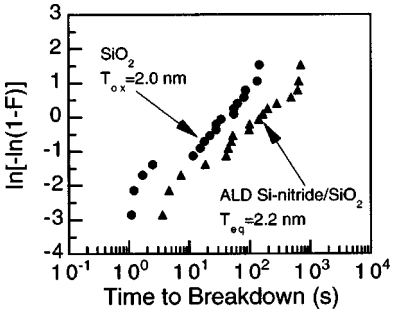

FIG. 5. Weibull plot of constant field (12 MV/cm) stressed TDDB characteristics for MOS devices with different gate dielectrics as mentioned.

which is caused by the SBD events and Fig. 4 clearly indicates an evolution from SBD to HBD. This result is identical to the observations[4,6,7] under constant current stressing of thin gate oxides. To the contrary, a significant enhancement of reliability is observed for the devices with ultrathin ALD silicon–nitride/SiO_2 stack gate dielectrics. The deposition of an extremely thin silicon nitride layer on the SiO_2 has brought about remarkable improvements in the breakdown characteristics. A very stable current with a sharp transition into HBD proclaims a significant suppression of the SBD or any such degradation events before the HBD. It eliminates any possibility of reliability overestimation for disregarding the SBD phenomenon.[4]

In conclusion, we fabricated p^+-poly-Si gate MOS capacitors with ALD silicon–nitride/SiO_2 stack gate dielectrics. The quality of the dielectric is evaluated by measuring various reliability characteristics and comparing with those of conventional SiO_2 dielectrics of identical thickness. The proposed stack gate dielectric exhibited much better results in all standard reliability tests. An interesting feature of SBD suppression is observed only in the devices with the proposed gate dielectrics. Possible breakdown mechanisms are discussed and a model, based on the concept of localized physical damages resulting in the formation of conductive filaments near both the interfaces, has been proposed to explain the observed stress induced phenomena. It is worth mentioning that the absence of the undesired SBD phenomenon in the proposed stack gate dielectric can be considered as positive feedback and encouragement for sustaining the scaling trend of device dimensions towards next generation integrated circuit technology.

[1] H. H. Tseng, P. G. Y. Tsui, P. J. Tobin, J. Mogab, M. Khare, X. W. Wang, T. P. Ma, R. Hegde, C. Hobbs, J. Veteran, M. Hartig, G. Kenig, V. Wang, R. Blumenthal, R. Cotton, V. Kaushik, T. Tamagawa, B. L. Halpern, G. J. Cui, and J. J. Schmitt, Tech. Dig. - Int. Electron Devices Meet., 647 (1997).
[2] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, and X. Aymerich, IEEE Electron Device Lett. **20**, 265 (1999).
[3] S. H. Lee, B. J. Cho, J. C. Kim, and S. H. Choi, Tech. Dig. - Int. Electron Devices Meet., 605 (1994).
[4] M. Depas, T. Nigam, and M. M. Heyns, IEEE Trans. Electron Devices **43**, 1499 (1996).
[5] K. Okada and K. Taniguchi, Appl. Phys. Lett. **70**, 351 (1997).
[6] M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, Appl. Phys. Lett. **73**, 514 (1998).
[7] T. Sakura, H. Utsunomiya, Y. Kamakura, and K. Taniguchi, Tech. Dig. - Int. Electron Devices Meet., 183 (1998).
[8] M. A. Alam, B. Weir, J. Bude, P. Silverman, and D. Monroe, Tech. Dig. - Int. Electron Devices Meet., 449 (1999).
[9] J. Sune and E. Miranda, Tech. Dig. - Int. Electron Devices Meet., 441 (2000).
[10] B. Y. Kim, H. F. Luan, and D. L. Kwong, Tech. Dig. - Int. Electron Devices Meet., 463 (1997).
[11] A. Nakajima, T. Yoshimoto, T. Kidera, K. Obata, S. Yokoyama, H. Sunami, and M. Hirose, Appl. Phys. Lett. **77**, 2855 (2000).
[12] M. Hirose, Mater. Sci. Eng., B **41**, 35 (1996).
[13] K. F. Schuegraf and C. Hu, IEEE Trans. Electron Devices **41**, 761 (1994).
[14] Y. Hokari, IEEE Trans. Electron Devices **35**, 1299 (1988).
[15] D. Wristers, L. K. Han, T. Chen, H. H. Wang, D. L. Kwong, M. Allen, and J. Fulford, Appl. Phys. Lett. **68**, 2094 (1996).
[16] L. K. Han, M. Bhat, D. Wristers, J. Fulford, and D. L. Kwong, Tech. Dig. - Int. Electron Devices Meet., 617 (1994).
[17] Q. D. M. Khosru, N. Yasuda, K. Taniguchi, and C. Hamaguchi, J. Appl. Phys. **77**, 4494 (1995).