博 士 論 文
（Doctoral Thesis）

Compact Modeling of Dual-Gate-Control Mechanism in Thin-Layer-MOSFETs for Advanced Circuit Applications

（高性能回路設計に向けた薄膜MOSFET におけるデュアルゲート制御機構のコンパクトモデル開発）

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Chapter 1

Introduction

1.1 Background

On December 23, 1947, the first transistor (trans resistor) was successfully demonstrated at Bell Laboratories in Murray Hill, New Jersey by American scientists W. H. Brattain and J. Bardeen. They were awarded the Noble prize for this innovation in 1956. Almost all the advanced transistors are based on same concept as that with the first transistor invented. Later, Mohamed Atalla and Dawon Kahng of Bell Labs invented the MOSFET (metal-oxide-semiconductor field-effect transistor) in 1959. MOSFETs use even less power, which has led to the mass production of MOS transistors for a variety of applications. Since then, the MOSFET has become the most widely produced device in the history of semiconductor physics.

The famous paper by Gordon Moore tracing the development of integrated circuit transistor density was published in 1965. The transistor count on a chip would quadruple every three years, according to his prediction [1]. For the past 40 years, the semiconductor industry has impressively adhered to this prediction, which was later dubbed Moore's law. Since the early 1990s, academic institutions and semiconductor companies have collaborated to make more accurate industry predictions. The International Technology Roadmap for Semiconductors (ITRS) [2] organization was founded as a result of this initiative. The ITRS publishes a report each year that acts as a standard for the semiconductor sector. These reports outline the types of technology, equipment, and metrology tools that must be created in order to keep up with Moore's law's prediction of the exponential growth of semiconductor devices. Figure 1.1 depicts the development of the predicted number of transistors per chip for high-performance microprocessors from the ITRS 2009.

Silicon Complementary Metal Oxide Semiconductor (CMOS), developed by C. T. Sah and Frank Wanlass of the Fairchild R & D Laboratory in the year 1963 [3], becomes the mainstream technology for semiconductor industry because of its obvious advantage for low power consumption. Combining p-channel and n-channel MOS

transistors in a complementary symmetry circuit configuration drew close to zero power in standby mode. This invention revolutionizes digital semiconductor industry. The first high volume production started with battery operated consumer products such as digital watch (Hamilton pulsar) in 1974. To keep up with Moore's law's rapid pace, transistor linear dimensions are reduced by half every three years. The sub-micron dimension barrier was crossed in the early 1980s, and by 2013, semiconductor manufacturers start to transistors with feature size of 20nm. Since the first integrated circuit transistors were manufactured on "bulk" silicon wafers, however, by the end of the 1990s, it became clear that considerable performance improvements could be obtained by moving to a new type of substrate known as SOI (Silicon-On-Insulator) [4-6], in which transistors are built in a thin silicon layer lying on top of a SiO_2 layer. It has been demonstrated that SOI technology improves both circuit speed and power consumption. In the early 2000s, major semiconductor companies such as IBM and AMD began manufacturing microprocessors (32-bit, 64-bit PowerPC 750 microprocessors [7] on 0.22um CMOS SOI process node, AMD Hammer microprocessor on 0.13um CMOS SOI process node) on an industrial scale using SOI substrates. SOI devices have lower parasitic capacitances and higher current drive. This enables SOI devices to operate at high frequency with low operating voltage. However, the advantage of SOI technology is not limited to higher operating frequency and lower power consumption, they also have high radiation hardness, can withstand high temperatures, and can handle high voltages. Furthermore, because an insulator separates devices from the substrate, it enables flexible device design; for example, the properties of the substrate can be modified independently of those of the device layer.

Network operators are pushed to improve performance by the need for additional bandwidth to send ever-increasing volumes of data (video, photographs, and data files) between a network and mobile phones. 3G was the first major milestone in 2001, followed by the adoption of 4G LTE (Long Term Evolution) and ultimately 5G. Mobile devices must support more bands, higher frequency bands, emission on adjacent bands, and downlink and uplink carrier aggregation in order to comply with these network standards.

The front-end module is getting more and more complicated in order to accommodate a wide variety of network settings. Advanced RF design methods, meticulously refined manufacturing process and specific substrates suitable with RF performance criteria are needed for integrated devices for front-end modules. Today, RF-SOI is used to construct the vast majority of RF switches instead of GaAs substrates in those applications. Additionally, antenna tuners and power amplifiers use RF-SOI. SOI technology enables the use of very-high-resistivity substrates to reduce crosstalk between

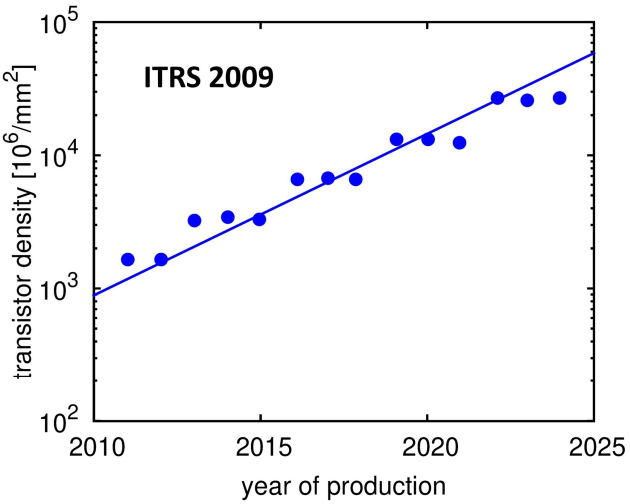

Figure 1.1: Evolution of transistor count per chip for high performance microprocessor for last five decades. (ITRS 2009)

different sub-circuits on common substrate. This capability, combined with SOI n-FETs with very high gain-bandwidth cut-off frequency f_T, opens exciting possibilities for low-power RF circuits. Soitec, a pioneer in SOI technology, has created two types of RF-SOI products, Soitec High-Resistance (HR) SOI and Soitec RF Enhanced Signal Integrity (RFeSI™) SOI [8], both of which are compatible with common CMOS processes. These products address the various communication standards and functions used in front-end modules. Soitec RFeSI™ SOI can fulfill substantially greater linearity and isolation parameters than normal HR-SOI, which enables designers to meet some of the most demanding LTE requirements. Standard HR-SOI is capable of meeting 2G or 3G requirements. This opens the door for adding additional features to a device while

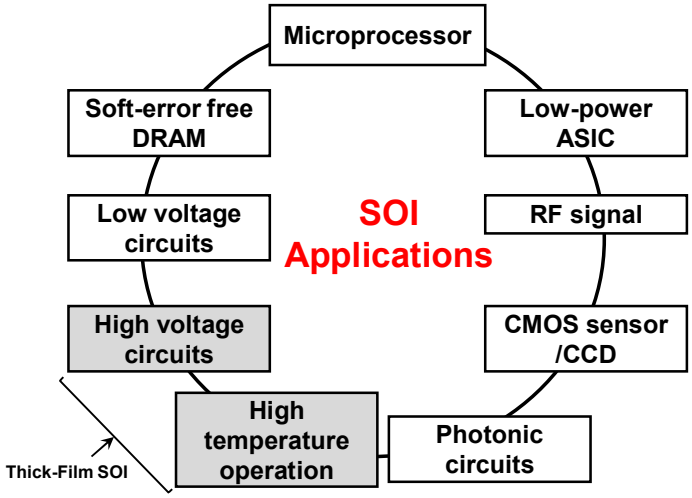

Figure 1.2: Various applications for SOI technology.

maintaining competitive pricing and greater RF performance. Thus, SOI technology has wide range of applicability including from low-power to high-frequency application (summarized in Figure 1.2).

1.2 Motivation

Using small amounts of energy harvesting such as light and vibration without using batteries to supply power at all, it is necessary to develop MOS structures that can be operated as desired in circuits. Such devices will create new opportunities where battery maintenance is not required in a wide range of application fields such as wearable devices, fitness wear and shoes, from consumer to healthcare. Bulk MOSFET technology is essentially inadequate to match that kind of power scaling due to its structural constraints. At lower operating voltage bulk MOSFET suffers from various short-channel-effects due to poor gate control in the channel. So, bulk MOSFET tends to be operated at higher voltage than what voltage scaling rule allows it to do to achieve desired speed performance, which is undesirable for low voltage applications.

Silicon on Insulator (SOI) MOSFET technology (see Figure 1.3) emerged as the best candidate for such low voltage application, which enables better device performance at lower operating voltage (that essentially leads to reduce power loss) due to reduced junction capacitances and improved electrostatic controllability. Structural modification also allows SOI MOSFET to be more immune to various short-channel-effects (SCE). To enable further improvement in low power operation, SOI technology is shifting focus from single-gate structure to multi-gate (two or more gates) structures. One of such devices belonging to SOI category is Silicon on Thin BOX (SOTB) MOSFET [9] (also referred as Dual-Gate (DG) MOSFET), where two independently controlled gates (front- and back-) influence the electrostatic behavior of the channels inside SOI layer. Although SOTB-generation MOSFET has been successfully investigated for 0.4V circuit operations [10], there remains ample of scope to research on complicated control mechanism of front- and back-gate that leads to achieve low power circuit operations. Different charge distribution for wide range of back-gate biasing within SOI layer and substrate are yet to be investigated in detail. This motivates me to do my research on this topic so that more refined dual-gate control mechanisms can be learned. Not only it will be limited to dual-gate structure, but this understanding will also help to explore Multi-Gate (MG) MOSFET generation as well.

SOI technology is not limited to low voltage operation. It is also suitable for RF/mm-Wave applications where linearity of the device is highly regarded to avoid

crosstalk through common substrate. Today, the most advanced CMOS nodes, and in particular silicon-on-insulator (SOI) flavors, are boasting impressive RF figures of merit (FoMs), proposing an attractive path for cost-effective mass market productions of RF and mm-wave applications and smart sensors [Internet of Things (IoT)] and radars. HR-SOI substrate was adequate enough to avoid crosstalk for 2G, 3G communication protocol. But for 4G LTE and 5G, linearity requirement is substantially high (see Table 1.1). To meet that requirement structural modification has been incorporated by introducing polysilicon layer in SOI substrate. Although this structure has been successfully demonstrated by SOITEC, there are several areas to investigate thoroughly to understand the whole mechanism of trapping, de-trapping and trap stability. My research objective is to develop a model for this mechanism which captures detailed physics behind trap, de-trap mechanism. This understanding will also be applicable to MG-MOSFET structure.

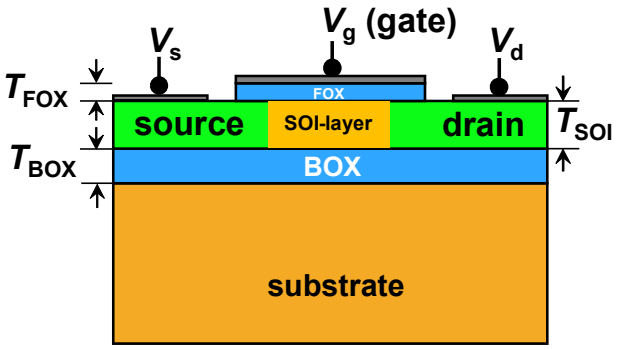

Figure 1.3: Structural description of SOI MOSFET with thick buried oxide (BOX).

Table 1.1: Linearity standard required for different network
(Source: Intel Mobile Corporation, "Challenges for Radios due to Carrier Aggregation Requirements", Nov 6, 2012)

Network	Linearity (IIP3 in dBm)
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90

1.3 Objective

The key areas where most of my work is concentrated are as follows.

1. To develop an analytical threshold voltage (V_{th}) model for dual-gate

MOSFET structures which can be extended for multi-gate MOSFETs generation (FinFET, GAA). This model derives a relation of V_{th} as a function of back-gate biasing for wider range of operation. The uniqueness of this developed model is that it is based on GMLE (Gm Gradient Maximum Linear-Extrapolation) V_{th} extraction method, which is characterized by carrier-density increase, rather than CMLE (Current Gradient Maximum Linear-Extrapolation) method, which incorporates carrier-mobility reduction. The newly developed V_{th} equation includes only device parameters, and accurately predicts the V_{th} value for any back-gate-bias conditions. Based on this V_{th} model, a further analytical equation is derived for the situation, where the back-gate charge becomes comparable and starts to exceed the front-gate charge. The independent gate control induces two V_{th} values, if the back-gate control becomes strong enough in comparison to that of the front gate. It is further shown, that the developed model can be applied for device-performance optimization to meet circuitry requirements. [Chapter 4]

2. To realize adaptive threshold-voltage controlling of thin-film multi-gate (MG) MOSFETs, using independent back-gate biasing, for latency and power optimization. Additionally, figuring out structural optimization to improve those key areas. [Chapter 5]
3. To investigate the effect of impact ionization in SOI structure and its influence in circuit operation. [Chapter 6]
4. High frequency analysis of RFSOI structures (crosstalk). [Chapter 7]

Chapter 2

SOI-Technology Development History

For ULSI (Ultra Large-Scale Integration) technology, reduction of power consumption is the most challenging issue as transistor density is increasing exponentially to meet different types of compute demand (scalar, vector and matrix compute). Bulk MOSFETs are on the verge of fundamental limit of device physics due to reduction of carrier mobility [2]. These make conventional scaling less viable for advanced transistor nodes. Operating voltage is set at higher than that of required by scaling rule to achieve desired speed performance. SOI technology provides the best solution to mitigate this challenge. Not only it provides high speed operation at lower operating voltage due to lower capacitance, but it also inculcates other advantages such as immune to cosmic radiation, withstanding higher operating temperate and voltage.

2.1 Progression of SOI MOSFET Development

Before SOI technology came into commercialization, numerous research efforts were put ranging from material of SOI wafers to device and circuit levels. The idea of SOI evolved first back in the year 1960 through growing MOSFET on the top of an insulator and experimentally implemented in thin-film-transistor (TFT) [11]. Subsequently, it translated on the top of single-crystal sapphire (Al_2O_3), also known as silicon-on-sapphire (SOS) structure. In 1964, C.W. Miller and P.H. Robinson proposed the idea of deposition of single crystal layers of silicon on sapphire surfaces by the hydrogen reduction of silicon tetrachloride [12]. SOS devices are expected to provide high switching performance due to low junction capacitance, but it failed gradually due to extreme dislocation density developing from the lattice mismatch at the Si/sapphire interface. Aluminum present in the sapphire substrate tended to migrate into the epitaxial film, obscuring the fabrication process. The large difference in coefficient of thermal expansion between Si and sapphire used to degrade carrier mobility. All these key demerits together obscure the SOS

technology.

Later in 1966, Watanabe and Tooi [13] started working on oxygen ions implantation methods in Si using RF gas discharge method and discovered that breakdown voltage, infrared absorption peak and dielectric constant of implanted film is equal to thermally grown SiO_2. In 1978, Izumi, et al. [14] produced a continuous SiO_2 layer with superior electrical characteristics by oxygen implantation with accelerated voltage of 150 KV followed by annealing at 1150°C. This process is known as SIMOX. Later in 1983, Fujitsu research team [15], under S. Kawamura, fabricated ICs with SOI CMOS technology. In 1989, at IBM Watson Research Center, a research team led by Ghavam G. Shahidi contributed to material research for SOI technology which ensued development of first commercially viable devices. He was the key person to make SOI technology suitable for mass production with high yield. In 1994, IBM fabricated the first sub-100 nanometer SOI CMOS devices [16]. Later in 2001, low-power RFSOI CMOS technology was developed by Shahidi's team at IBM [17], which was suitable for high frequency application.

2.2 Advantage of SOI Technology

The most significant structural modification for SOI technology compared to bulk MOSFET is additional silicon dioxide (SiO_2) which is also referred to as buried oxide (BOX) and is fabricated by oxidation of silicon substrate. BOX layer in SOI MOSFET provides several advantages over conventional bulk MOSFET structure, which are described as follows. All the advantages mentioned below are valid for both PD (Partially Depleted)- and FD (Fully Depleted)-SOI MOSFETs.

1. Reduced junction capacitance

In SOI technology, junction-capacitance is significantly smaller compared to bulk counterpart. As seen in Figure 1, drain (or source) side junction-capacitance is formed in conjugation with buried oxide (BOX). Thicker oxide layer (BOX) along with lower permittivity (for SiO_2, ε_r=3.9, for Si, ε_r=11.7) make negligible junction-capacitance at Si-SiO_2 interface. Therefore, SOI MOSFET is suitable for high-frequency-switching applications.

2. More immune to short-channel-effects (SCE)

Buried oxide layer isolates body region (also termed as SOI layer) from substrate. Therefore, gate control over thin body remains profound. This leads to stronger vertical

electric field compared to lateral. Therefore, most of the subthreshold charges flow through the channel, not through middle of SOI layer, which reduces short-channel-effects. Additionally, for multi-gate configuration (SOTB structure), positive back-gate biasing increases strength of vertical electric field component, leading to minimize short-channel-effects.

3. Advantage of back-gate biasing

Low power circuits are required to be operated within constraint supply-voltage limits, which is a source of inferior electrostatic control for the bulk MOSFET. Additional back-gate contact can be utilized as an additional control gate, which leads to improve electrostatic control in the channel along with extended design flexibility due to adjustability of V_{th}.

4. Better soft-error immunity

SOI structure exhibit radiation harness to ionized-charged-particles (mostly alpha-particle) [18]. For bulk structure, in high-radiation-environment, ICs tend to be affected by soft-error (also known as single-event-upset), which can alter bit-cell value in memory circuits. High energy alpha particles create ion track along its loci in Si-substrate. Generated ions can affect body potential which, in turn, changes V_{th} of the device. But in SOI devices, thick BOX layer isolates body from substrate. So, ions generated at substrate don't influence body potential, thus more immune to soft-error.

5. Immune to latch-up formation

For bulk CMOS configuration, parasitic n-p-n-p (or p-n-p-n) configuration gives rise to latch up formation, which essentially sets upper limit of maximum operating voltage. In SOI MOSFETs, presence of BOX oxide prevents any latch-up.

2.3 Partially Depleted and Fully Depleted SOI

Through the early development phase of SOI MOSFET technology, among fully depleted and partially depleted structure, the later leads in mainstream CMOS technology development due to its scalability advantage. Figure 2.1a depicts PDSOI structure where SOI layer thickness is greater than maximum depletion extension in SOI layer. Usually,

in this case SOI layer thickness exceeds 50nm. Therefore, PDSOI device is easier to fabricate as thickness variation sensitivity will be less impactful for thicker SOI layer. This leads to simplified process step requirements. Additionally, PDSOI technology is also more compatible with existing bulk CMOS technology compared to FDSOI. For applications which require high frequency clocking, PDSOI device is more ideal. PDSOI MOSFETs were initially utilized in specialized applications such as radiation-hardened or high-temperature electronics. As time progressed, leading semiconductor manufacturers began to adopt PDSOI technology to create high-performance microprocessors. Since then, the attention has shifted to 0.18um, 0.13um CMOS SOI technology [19], with a much larger client base. But the charge neutral body region in PDSOI introduces circuit instability due to floating body effect. This causes unwanted glitches along with inconsistent rise- and fall-time in memory circuits, resulting in altering bit-cell values. This phenomenon becomes more obvious with shorter-channel-length devices due to reduced noise margin.

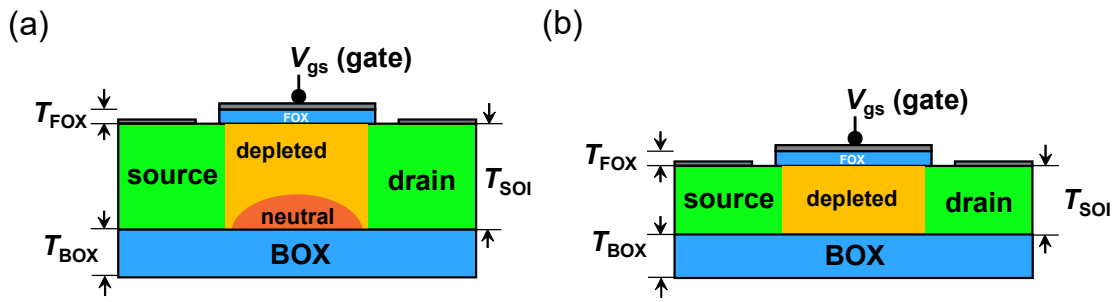

Figure 2.1: (a) Partially depleted (PD)-SOI MOSFET with charge neutral region inside SOI layer. (b) Fully depleted (FD)-SOI MOSFET with thin SOI layer.

The floating body effects affects both DC (kink and hump in drain current I_{ds} for output and transfer characteristics respectively) and transient (inconsistent rise and fall time during switching event) characteristics of the transistor. Although many research work has been accomplished to investigate the reason of Floating Body (FB) effect, the phenomenon is not fully understood, specially at transient. The effect is also known as History effect. To capture complex FB effect in transient, it is essential to capture body-charge discharging and charging phenomenon through source side in PDSOI. Detailed analysis of FB effect in transient is investigated in chapter 6.

Although body-tied PDSOI MOSFET eradicates the challenges of floating-body-effect, it affects MOSFET performance at low voltage due to weak gate-overdrive. Fully depleted structure remains unaffected by FB effect due to non-existence of charge

neutral region in SOI layer. SOI layer thickness remains thinner (usually below 50nm) than maximum depletion width, indicating depletion region extends throughout SOI layer. As depletion region exists throughout inside SOI layer, impact ionization generated carriers can easily drift out through source-side due high lateral electric field strength, which mitigates FB effect. Therefore, drain current depicts no hump in transfer characteristics. Additionally, thinner SOI layer makes gate control stronger along device depth direction perpendicular to the channel. This reduces punch-through current deep inside SOI layer. These phenomena improve subthreshold slope. Consequently, leakage power reduces, making it suitable for very low power application. However, threshold voltage variation can affect FDSOI MOSFET, as thickness variation sensitivity is intense for thin SOI layer.

2.4 Evolution of Multi-Gate MOSFET

Although SOI structure mitigates the key challenges of bulk MOSFET, further development for novel structure was necessary for sub 28nm technology to improve power density footprint. More than one gate was essential to improve electrostatic control with high-current-density to mitigate the effect of SCEs and mobility degradation.

2.4.1 Double-Gate SOI MOSFET

Early prototype of this idea started with double gate structure realized on SOI technology during late 80s [12]. Presence of both front- and back-gate improves electrostatic control over the channel. SOI layer is sandwiched between two gates, resulting in the formation of two different channels at opposite sides of the silicon layer. T. Sekigawa and Y.

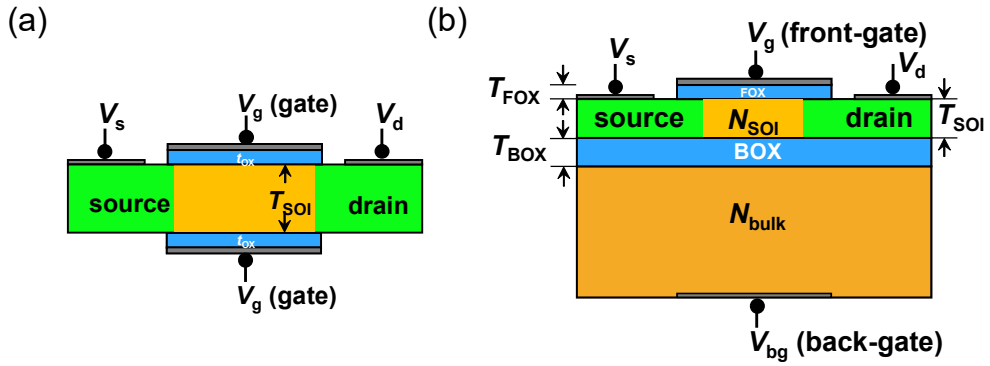

Figure 2.2: (a) Schematic of double-gate MOSFET with symmetric gate control in SOI layer. (b) SOTB MOSFET (also known as dual-gate MOSFET) with asymmetric and independent gate control.

Hayashi released the first article on the double-gate MOSFET transistor in 1984 [20]. This research demonstrates that sandwiching a totally depleted SOI device between two gate electrodes coupled together can significantly reduce short-channel effects. The device was given the name XMOS because its cross section resembles the Greek letter Ξ (Xi). This arrangement results in a better control MOSFET, since the influence of the drain electric field on the channel is reduced, reducing short-channel. Frank, Laux, and Fischetti released a more extensive modeling that included Monte-Carlo simulations in a work that explored the ultimate scaling of the silicon MOSFET in 1992 [21]. When front- and back-gate-oxide thickness is identical and both gates are controlled through a common voltage source, this structure is referred to as Double-Gate MOSFET as shown in Figure 2.2a. Electrostatic behavior of such structure is symmetric inside SOI layer. From modeling perspective, describing the physics of this MOSFET structure is relatively easier compared to asymmetric structure. Gradually, structural modification was done to configure double-gate structure with independently controlled voltage source on the top of thin buried oxide as depicted in Figure 2.2b. This structure is referred to as SOTB (or Dual-Gate) MOSFET. It improves transistor density compared to single-channel SOI MOSFET by reducing back-gate oxide thickness. Presence of additional substrate region beneath the BOX layer improves the scope for back-gate controllability. Electrostatic behavior inside SOI layer of such structure remains asymmetric which makes modeling more complicated compared to double-gate structure.

2.4.2 Multi-Gate SOI MOSFET

The concept of DG structure is extended to multi-gate structure, such as tri-gate FinFET and Gate All Around (GAA) MOSFET [12]. The influence of Drain Induced Barrier Lowering (DIBL) is reduced through multi-gate control, which obviously helps to reduce short-channel-effect. FinFET structure consists of three-gate with identical length but Contribution of the third insulator gate is smaller than other two due to the shorter length. Therefore, the third gate can hardly contribute electrostatically. Excellent gate-controllability and mobility improvement is attained by the realization of volume inversion for MOS structure with more degree of freedom in terms of gate wrapping and smaller area of cross-section along device depth direction. By wrapping a gate electrode around a vertical silicon pillar, the first surrounding-gate MOSFETs were created. The CYNTHIA device (circular-section device) [22] and the pillar surrounding-gate MOSFET (square-section device) [25] are examples of such devices. Planar surrounding-gate devices with square or circular cross sections have recently been reported [24].

Surrounding-gate SOI MOSFETs with gate lengths as short as 5 nm and diameters as small as 3 nm have been reported to be fully functional [25]. Multiple surrounding-gate channels can be stacked on top of one another to increase current drive per unit area while sharing a common gate, source, and drain. Example of such device is Multi-Bridge Channel MOSFET (MBCFET) [26], Twin-Silicon-Nanowire MOSFET (TSNWFET) [27].

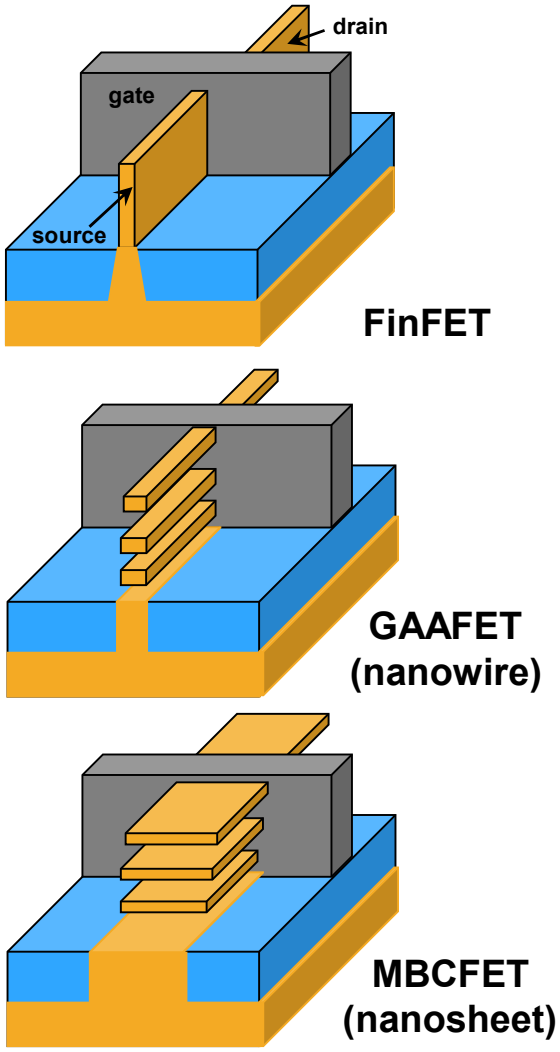

Figure 2.3: Schematic of different MG-MOSFET structures.

Chapter 3

Compact Models for MOSFETs

Important feature of modern circuit simulation tools is that it doesn't require to write down set of algebraic and differential equations to describe circuit characteristics. Rather circuit designers only require to describe circuit configuration with set of parameter values. The circuit simulators automatically solve the equations numerically with the parameter values to produce circuit response. This chapter describes different types of MOSFET compact models which are popular throughout the history of compact model development. The necessity of compact modelling originated for simulating MOSFET characteristics with accuracy and speed. 2D-device-simulation is good for understanding relationship between device structure and device characteristics but not suitable for simulating influences among many transistors, as it solves algorithms in every node of the mesh in the device structure two dimensionally. Compact models come into play to mitigate this issue. Current generation integrated circuits consist of billions of transistors.

For designing an integrated circuits with billions of transistors require circuit simulator which can accurately predict circuit behavior within constraint time limit. To achieve the requirement, device models are essential to describe characteristics of non-linear circuit elements (such as typical semiconductor devices like MOS transistors, diode etc.) with accuracy. These models must explain the device physics using not only physically accurate but also computationally effective basic analytical equations in order to obtain sufficient simulation speed for actual commercial application and steady convergence. They are hence typically referred to as "compact models" [28]. The link between technology, circuit simulations, and design is provided by compact models. At the design verification stage, precise compact models aid in ensuring functionality and high yield of items. A working group called the Compact Model Coalition (CMC) [29] was established in the Electronic Design Automation (EDA) sector to choose, uphold, and encourage the usage of common compact models. The specified compact models on the CMC are displayed in Table 3.1. As may be observed, different device models have so far undergone standardization.

Table 3.1: Standardized compact models on the Compact Model Coalition (CMC)

	Bulk MOSFET	LD_MOS/ HV_MOS	SOI MOSFET	Bipolar	Varactor & Diode
UC Berkeley	BSIM3 BSIM6		BSIM-CMG BSIM-IMG		
Hiroshima Univ.	HiSIM2	HiSIM_HV	HiSIM-SOI HiSIM-SOTB		
Philips and Arizona State Univ.	PSP				
UC San Diego				HICUM L2	
Auburn Univ.				MEXTRAM	

3.1 Basic Device Equations: bulk MOSFET

Figure 3.1 depicts the cross section of an n-channel MOSFET (metal-oxide-semiconductor field effect transistor). The device is composed of a p-type substrate that forms the drain and source of two n+ diffusion zones. The metal-oxide-semiconductor (MOS) structure is the core component of the MOSFET. The distance between the source

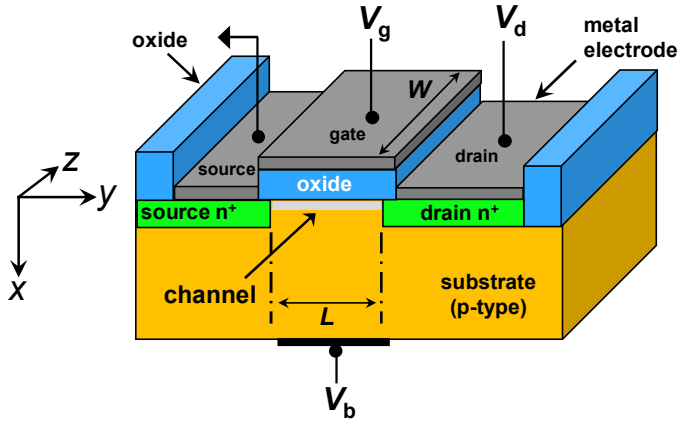

Figure 3.1: Description of two-dimensional Bulk n-MOSFET.

and drain is considered as the effective channel length L, and the channel width W is the lateral extent of the MOSFET called “width”. The oxide layer that covers the active channel region is having thickness t_{ox}. Under the gate oxide, a channel made up of moving carriers during MOSFET operation. The applied gate voltage affects the carriers, which enter through the source and exit through the drain. The electric field produced by the gate voltage regulates the carrier flow between the source and drain, which is referred to as the drain current. The ground potential is typically used to define the source voltage.

The voltages for the drain, gate, and substrate are V_{ds}, V_{gs}, and V_{bs}, respectively.
It is necessary to simultaneously solve the following fundamental device equations in order to analytically explain the MOSFET properties, which is valid for devices controlled by field induced within the devices and adopted by 2D numerical simulator.

- Poisson's equation

$$\nabla^2\phi = -\frac{q}{\varepsilon_{si}}\left(N_d - N_a + p - n\right) \tag{3.1}$$

$$n = n_i \exp\frac{q\left(\phi - \phi_{fn}\right)}{kT}$$

$$p = n_i \exp\frac{q\left(\phi_{fp} - \phi\right)}{kT}$$

- Current density equation

$$j_n = q\mu_n n\frac{\partial\phi}{\partial y} + qD_n\nabla n \tag{3.2}$$

$$j_p = q\mu_p p\frac{\partial\phi}{\partial y} - qD_p\nabla p$$

- Continuity equation

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla . j_n \tag{3.3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla . j_p$$

where ϕ, q, ε_{si}, N_a, N_d, p, n, k, T, μ, D represent potential, electronic charge, Si permittivity, acceptor impurity concentration, donor impurity concentration, hole concentration, electron concentration, Boltzmann constant, temperature in k, carrier mobility and diffusion constant respectively. The relation between potential and carrier concentration is described by the Poisson equation. Current flow mechanism in MOSFET channel is described by current density equation, which was first proposed by Pao and Sah [34]. In subthreshold condition, diffusion term dominates whereas beyond inversion, drift term dominates. Sum of these two components give total current density in MOSFET. Time dependent current continuity equation is required for solving transient characteristics.

In order to simplify analytical solutions for circuit simulation, some of the key assumptions are considered which are not rigorously true but simplify the equations.

Assumption 1: Variation of electric field along *y*-direction (along channel direction) is much less as compared to variation along *x*-direction. This assumption is referred as the Gradual-Channel Approximation (GCA). This indicates potential increases gradually along *y*-direction. The validity of the GCA for the most part along the channel can be confirmed using 2-D numerical analysis of long-channel cases. Even for long channel devices, however, it does fail close to the drain area, when the field induced along the channel becomes comparable to the field induced by the gate control. To compensate the shortcoming, channel-length modulation is introduced, where the field induced by gate voltage determines the device characteristics. The GCA is applied because it simplifies the system to a 1-D current flow problem and the field induced by the drain voltage is considered as the high-field originating undesired problems in advanced devices, called short-channel effect.

Assumption 2: Hole current contribution can be neglected in normal mode of low V_{ds} operation in n-channel transistors. It should be noted that for high V_{ds} operation , where impact ionization can produce electron and hole pairs, and causes hole current flow, which is measured as the substrate current.

Assumption 3: Carrier generation and recombination can be neglected if only static characteristics are considered for MOSFET operation. In that case current continuity equation reduces to

$$\nabla . j_n = 0$$

Thus, compact model considers two basic equations and the third equation is solved by circuit simulation.

Assumption 4: Current flows only along the y-direction (channel- direction). Neglecting the current flow along *x*-direction (device depth direction perpendicular to the channel) provides very satisfactory result with respect to measurement data, because carriers are mostly controlled by the gate voltage V_{gs} in MOSFETs.

3.2 Different Compact Models Ever Recognized

Poisson's equation depicts the relation between potential and carrier concentration and the equation of current under drift and diffusion condition, describes the current flow mechanism in different operating conditions. The current continuity equation can be used

to calculate the electron current in the *y*-direction assuming that generation and recombination current, as well as hole current, are insignificant under normal circuit operation. In other words, total drain-to-source current I_{ds} is constant along the channel. The electron current density at a point (*x, y*) within the device can be calculated for n-MOSFET as

$$J_n(x,y) = -q\mu_n n(x,y)\frac{d\phi_f(y)}{dy} \tag{3.4}$$

where $n(x,y)$ denotes electron concentration, u_n denotes electron mobility in the channel. Typical value of μ_n in channel is much lower as compared to bulk due to high surface scattering. Here $\phi_f(y)$ represents quasi Fermi potential. Eq. (3.4) includes both drift and diffusion current components. Eq. (3.4) is multiplied by the channel width *W* and integrated throughout the depth of the current-carrying layer to produce the total current at a point *y* along the channel. The integration is performed from $x = 0$ to x_i, where x_i is the inversion layer thickness.

$$I_{ds}(y) = qW\int_0^{x_i}\mu_n n(x,y)\frac{d\phi_f(y)}{dy}dx \tag{3.5}$$

The change in sign indicates I_{ds} is from drain to source side. Eq. (3.5) can be re-written as

$$I_{ds}(y) = qW\mu_n\frac{d\phi_f(y)}{dy}\int_0^{x_i} n(x,y)dx \tag{3.6}$$

Its integration over the inversion layer gives the inversion charge per unit gate area, Q_i

$$Q_i(y) = -q\int_0^{x_i} n(x,y)dx \tag{3.7}$$

Substituting Eq. (3.7) into Eq. (3.6),

$$I_{ds}(y) = -\mu_{eff}W\frac{d\phi_f}{dy}Q_i(y) = -\mu_{eff}W\frac{d\phi_f}{dy}Q_i(\phi) \tag{3.8}$$

In Eq. (3.8) Q_i is represented as a function of ϕ_f; ϕ_f and *y* are interchangeable because ϕ_f is a function of *y*. So,

$$\int_0^L I_{ds}dy = \mu_{eff}W\int_0^{V_{ds}} -Q_i(\phi_f)d\phi_f \tag{3.9}$$

Simplifying

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_0^{V_{ds}} -Q_i(\phi_f) d\phi_f \tag{3.10}$$

Q_i can be obtained in a different form if $n(x,y)$ can be expressed as a function of (ϕ,ϕ_f).

$$n(x,y) = n(\phi,\phi_f) = \frac{n_i^2}{N_a} e^{q(\phi-\phi_f)/kT} \tag{3.11}$$

Combining Eq. (3.11) in Eq. (3.7)

$$Q_i(\phi_f) = -q \int_{\phi_s}^{\delta} n(\phi,\phi_f) \frac{dx}{d\phi} d\phi = -q \int_{\delta}^{\phi_s} \frac{\frac{n_i^2}{N_a} e^{q(\phi-\phi_f)/kT}}{E(\phi,\phi_f)} d\phi \tag{3.12}$$

Here ϕ_s represents surface potential at x=0, namely at source side. E denotes electric field along x-direction. δ represents very small potential but not zero.
Substituting Eq. (3.12) in Eq. (3.10),

$$I_{ds} = q\mu_{eff} \frac{W}{L} \int_0^{V_{ds}} \left(\int_{\delta}^{\phi_s} \frac{\frac{n_i^2}{N_a} e^{q(\phi-\phi_f)/kT}}{E(\phi,\phi_f)} d\phi \right) d\phi_f \tag{3.13}$$

Eq. (3.13) is referred to as Pao and Sah's double integral equation. It is possible to numerically evaluate this double integral. This approach is primarily of theoretical significance because of the lengthy computing time required.

If the inversion charge density Q_i can be written only as a function of ϕ_s, Pao and Sah's double integral can be reduced to a single integral. The charge-sheet concept (Brews, 1978, G. Baccarani, 1978, F. van der Wiele, 1979) [31] is based on the idea that the inversion layer is situated extremely close to the silicon surface like a thin sheet of charge is used to achieve this. Across the narrow inversion layer, there is a sudden increase in the field (spatial integration of volume charge density), while the potential barely changes (spatial integration of field). Thus, both the surface potential and the depletion charge density remain relatively unchanged after strong inversion. The key point for charge-sheet model is depletion charge density Q_{dep} can be extended even strong inversion is attained, which is written as

$$Q_{dep} = -qN_a W_d = -\sqrt{2\varepsilon_{si} qN_a \phi_s} \tag{3.14}$$

This leads to

$$Q_i = Q_g - Q_{dep} = -C_{ox}(V_{gs} - V_{fb} - \phi_s) + \sqrt{2\varepsilon_{si} q N_a \phi_s} \tag{3.15}$$

The Eq. (3.10) can be transformed to a function of ϕ_s.

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_{\phi_{s0}}^{\phi_{sL}} -Q_i(\phi_s) \frac{d\phi_f}{d\phi_s} d\phi_s \tag{3.16}$$

where ϕ_{s0} and ϕ_{sL} represents the value of the surface potential at the source and drain side respectively. Substituting Eq. (3.16) in Eq. (3.15)

$$I_{ds} = \mu_{eff} \frac{W}{L} \int_{\phi_{s0}}^{\phi_{sL}} \left[C_{ox}(V_{gs} - V_{fb} - \phi_s) + \sqrt{2\varepsilon_{si} q N_a \phi_s} + \frac{2kT}{q} \frac{C_{ox}^2 (V_{gs} - V_{fb} - \phi_s) + \varepsilon_{si} q N_a}{C_{ox}(V_{gs} - V_{fb} - \phi_s) + \sqrt{2\varepsilon_{si} q N_a \phi_s}} \right] d\phi_s \tag{3.17}$$

Eq. (3.17) expresses I_{ds} in a single integral. Still, it is complicated to carry out the integral to solve Eq. (3.17). A further approximation is introduced to obtain an analytical expression for drain current. As observed carefully, the last term in the square bracket contains a multiplying factor kT/q. Therefore, it can be neglected compared to other two terms in the square bracket. Now it is easier to carry out integral analytically:

$$I_{ds} = \mu_{eff} \frac{W}{L} \left\{ C_{ox} \left(V_{gs} - V_{fb} + \frac{kT}{q} \right) \phi_s - \frac{1}{2} C_{ox} \phi_s^2 - \frac{2}{3} \sqrt{2\varepsilon_{si} q N_a} \phi_s^{3/2} + \frac{kT}{q} \sqrt{2\varepsilon_{si} q N_a \phi_s} \right\} \Bigg|_{\phi_{s0}}^{\phi_{sL}} \tag{3.18}$$

The equation covers all the operating regions (subthreshold, linear and saturation) in a single, continuous function. So, it becomes the primary equation for surface-potential-based model.

3.2.1 Meyer Model

The first MOSFET model ever developed for circuit simulation is the Meyer model [32]. This model describes MOSFET characteristics as a function of applied voltage considering only drift contribution originally developed by Sah [33].

$$I_{ds} = \mu_{eff} \frac{W}{L} \left\{ \left(V_{gs} - V_{th} \right) V_{ds} - \left(\frac{1}{2} + \frac{\sqrt{2\varepsilon_{si} q N_{sub}}}{4C_{ox}} \sqrt{2\Phi_B} \right) V_{ds}^2 \right\} \tag{3.19}$$

where $V_{th} = V_{fb} + 2\Phi_B - \frac{\sqrt{2\varepsilon_s q N_{sub} 2\Phi_B}}{C_{OX}}$

Here $2\Phi_B$ is the surface potential at threshold condition. Eq. (3.19) can be derived from Pao and Sah drift-diffusion model by putting ϕ_{S0} and ϕ_{SL} equal to $2\Phi_B$ and $2\Phi_B+V_{ds}$ respectively. It can be seen that the drift contribution alone leads to an extremely simplified approximation of the surface potentials and a correspondingly limited validity. Meyer equivalent capacitance model is shown in Figure 3.2.

At the early stage of the IC technology development, the accuracy of the Meyer model was satisfactory. However, two major problems became apparent with advancing technologies. One is existence of discontinuities in the model description and the other is the difficulty to correctly incorporate the modeling of the enhancing short-channel effects.

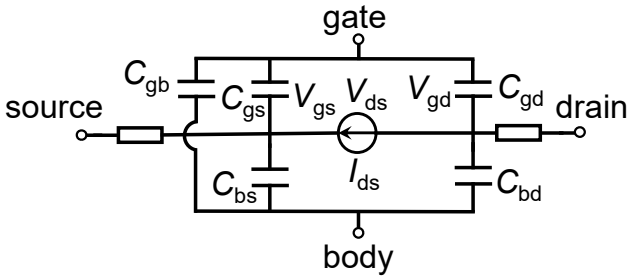

Figure 3.2: Meyer equivalent capacitance model for bulk n-MOSFET.

3.2.2 BSIM (Berkeley Short-channel IGFET Model)

Despite various disadvantages of Meyer model, BSIM (Berkeley Short-channel IGFET Model) MOSFET model is developed based on this model due to the ease with which new device models could be easily included. For circuit simulation, some models, including several earlier iterations of BSIM [34–35], have been developed and implemented in SPICE (Simulation Program with Integrated Circuit Emphasis). These models used separate model expressions for device operation regimes like subthreshold and strong inversion. Within each individual region of operation, the expressions can precisely describe how each device behaves although transition zones between the well-described subthreshold and strong inversion regions becomes a headache to be resolved.

BSIM4 was developed to resolve this issue to some extent. Continues channel charge density Q_{ch0}, representing conventional Q_i, expression was derived from separate expression for subthreshold and strong inversion for small V_{ds}.

$$Q_{ch0} = C_{ox}(V_{gs} - V_{th}) \quad \text{for } V_{gs} > V_{th} \tag{3.20}$$

$$Q_{ch0} = \sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\phi_s}}.\beta^{-1}\exp\left(\frac{V_{gs} - V_{th} - V_{off}}{n\beta^{-1}}\right) \qquad \text{for } V_{gs} < V_{th} \tag{3.21}$$

where $\beta=(kT/q)^{-1}$, V_{off} represents small V_{th} difference in subthreshold and strong inversion region.

At the transition between subthreshold and linear region a discontinuity exists, which is smoothed numerically by transforming the physical V_s into an effective V_{gseff},

$$V_{gseff} = \frac{\frac{2n}{\beta}\ln\left[1+\exp\left(\beta\frac{V_{gs}-V_{th}}{2n}\right)\right]}{1+2nC_{ox}\sqrt{\frac{2\Phi_B}{q\varepsilon_{si}N_{ch}}}.\exp\left(-\beta\frac{V_{gs}-V_{th}-2V_{off}}{n}\right)} \tag{3.22}$$

where N_{ch} is the channel doping concentration. Another discontinuity occurs at the transition between the linear and the saturation region. It is caused by the assumption that V_{ds} is small in order to derive Eq. (3.19). This is again smoothed numerically by introducing an effective V_{dseff}.

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}\right) \tag{3.23}$$

where V_{dsat} is the saturation voltage and δ is a fitting parameter. These effective voltages are also applied for describing the charges, however, the correct modeling approach is to model the charges first. As a result, a number of defects are built into and persist in the piece-wise models. The lacking of the dynamic charge partitioning between source and drain is another example. Thus,

$$Q_{ch0} = C_{ox}V_{gseff} \quad \text{for all } V_{gs}. \tag{3.24}$$

Eq. (3.24) achieves smooth transition between subthreshold and strong inversion region.

The discontinuities inherently occur due to application of the drift approximation. Eq (3.19) is valid in principle only in the linear region. I_{ds} is extended to the subthreshold region with fitting parameters

$$I_{ds} \propto \{1-\exp(-\beta V_{ds})\}.\exp\left(-\beta\frac{V_{gs}-V_{th}-V_{off}}{n}\right) \tag{3.25}$$

where n is the subthreshold swing, and V_{off} is the offset voltage in the subthreshold region. However, it has to be noticed that the important information about the device technology can be observed exactly in n, which is treated only as a fitting parameter here and is not properly related to the physical device parameters.
A continuous mobility model is also achieved by extending the strong inversion mobility model with the smoothing function in Eq. (3.22)

$$\mu_{eff} = \frac{\mu_0}{1+U_a\left(\frac{V_{gseff}+2V_{th}}{T_{ox}}\right)+U_b\left(\frac{V_{gseff}+2V_{th}}{T_{ox}}\right)^2+U_cV_{bs}} \tag{3.26}$$

where μ_0, U_a, U_b, and U_c are extracted parameters. T_{ox} is the thickness of gate oxide. In the subthreshold region, this mobility expression takes on a constant value, guaranteeing no mobility discontinuity.

3.2.3 HiSIM (Hiroshima-University STARC IGFET Model)

Conventional MOSFET models are threshold voltage based, often referred to as piece-wise models. Depending upon the operating region (subthreshold and saturation), it solves different sets of equations. V_{th} based model only considers drift equation which indicates this model is only valid for strong-inversion condition. It makes the equations simpler for neglecting diffusion contribution. The main disadvantage of this model is current discontinuity at the boundary of two operating regions. In surface potential-based drift-diffusion model this issue has been eradicated by considering a unified equation for both subthreshold and inversion region. Two further simplifications are made, under charge-sheet approximation and gradual-channel approximation. Even though simplified surface potential based modeling has been demonstrated by the three affiliations in the end of 70's, the main compact models have been developed based on the Meyer model. The reason is how to calculate surface potentials and how to extend for advanced

MOSFETs, such as short-channel effect, were still missing. HiSIM (Hiroshima university STARC IGFET Model) is the first complete surface potential-based model that is applied to circuit simulation extensively. Using 2D-device simulation, reliability of this simple drift-diffusion based model has been verified. The reason is that MOSFET operation is still governed by V_{gs} and the known characteristics are mostly retained in advanced MOSFETs.

3.2.3.1 Drain Current Formulation

Current density j_n described by drift-diffusion model for n-MOSFET is (see Eq. (3.2)) [30]

$$j_n = -q\mu_n n\frac{\partial \phi}{\partial y} + qD_n \nabla n \tag{3.27}$$

Combing with Einstein relation, Eq. (3.28) modifies to

$$j_n = -q\mu_n n\left(\frac{\partial \phi}{\partial y} - \frac{1}{\beta}\frac{d\ln n}{dy}\right) \tag{3.28}$$

Considering charge-sheet approximation, I_{ds}

$$I_{ds} = Wq\mu_{eff} n(y)\left(\frac{d\phi_s(y)}{dy} - \frac{1}{\beta}\frac{d\ln n(y)}{dy}\right) \tag{3.29}$$

Here *n(y)* is carrier density along channel which can be obtained integrating along *x* direction with inversion layer thickness.

Measuring quasi-Fermi-potential ϕ_f from substrate fermi-level as reference Eq. (3.29) is rewritten as

$$I_{ds} = Wq\mu_{eff} n(y)\frac{d\phi_f}{dy}$$

Here $\frac{d\phi_f}{dy} = \frac{d\phi_s(y)}{dy} - \frac{1}{\beta}\frac{d\ln n(y)}{dy}$. (3.30)

The first term in Eq. (3.30) denotes the drift current which is the carrier flow due to the electric field along the channel. The second term denotes the diffusion current which exists due to a difference in charge concentration gradients. Charges diffuse from regions of high charge concentration to low concentration giving rise to electric current. Using the gradual channel approximation and assuming uniform channel doping, HiSIM derives a drain current equation as a function of the surface potentials as

$$I_{\rm ds} = \frac{W_{\rm eff}}{L_{\rm eff}} \cdot \mu \cdot \frac{I_{\rm dd}}{\beta} \tag{3.31}$$

$$\begin{aligned} I_{\rm dd} &= C_{\rm OX}\left(\beta V'_{\rm G}+1\right)\left(\phi_{\rm SL}-\phi_{\rm S0}\right)-\frac{\beta}{2}C_{\rm OX}\left(\phi_{\rm SL}^2-\phi_{\rm S0}^2\right)-\frac{2}{3} \\ &\quad -\frac{2}{3}const0\left[\left\{\beta\left(\phi_{\rm SL}-V_{\rm bs}\right)-1\right\}^{\frac{3}{2}}-\left\{\beta\left(\phi_{\rm S0}-V_{\rm bs}\right)-1\right\}^{\frac{3}{2}}\right] \\ &\quad +const0\left[\left\{\beta\left(\phi_{\rm SL}-V_{\rm bs}\right)-1\right\}^{\frac{1}{2}}-\left\{\beta\left(\phi_{\rm S0}-V_{\rm bs}\right)-1\right\}^{\frac{1}{2}}\right] \end{aligned} \tag{3.32}$$

$$V'_{\rm G} = V_{\rm gs} - V_{\rm fb} - \Delta V_{\rm th}$$

$$const0 = \sqrt{\frac{2\varepsilon_{\rm Si} q N_{\rm sub}}{\beta}}$$

3.2.3.2 Surface Potential Calculation

Surface potential is calculated from the Poisson Equation as follows

$$\frac{d^2\phi_{\rm s}(y)}{dy^2} = -\frac{\rm q}{\varepsilon_{\rm si}}\left[p_{\rm p0}\left\{\exp(\beta\phi_{\rm f}-1)\right\}-n_{\rm p0}\left\{\exp(\beta\phi_{\rm f}-1)\right\}\right] \tag{3.33}$$

Here $n_{\rm p0}$ and $p_{\rm p0}$ denote the electron and hole concentration respectively at thermal equilibrium. Thus, electric field at lateral direction can be obtained as

$$\varepsilon(y) = \frac{d^2\phi_{\rm s}(y)}{dy^2}$$

$$= \pm\frac{\sqrt{2}kT}{qL_{\rm D}}\left[\left\{\exp(\beta(\phi_{\rm s}(y)-V_{\rm bs}))+\beta(\phi_{\rm s}(y)-V_{\rm bs})-1\right\}+\frac{p_{\rm p0}}{n_{\rm p0}}\left\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y)))+\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y)))\right\}\right]^{1/2}$$

(3.34)

Using the Gauss theorem, Q_s becomes

$$Q_s(y) = \varepsilon_{\mathrm{Si}}\varepsilon_{\mathrm{s}}$$
$$= qN_{\mathrm{sub}}L_{\mathrm{D}}\left[\left\{\exp(-\beta(\phi_{\mathrm{s}}-V_{\mathrm{bs}}))+\beta(\phi_{\mathrm{s}}-V_{\mathrm{bs}})-1\right\}+\frac{p_{\mathrm{p0}}}{n_{\mathrm{p0}}}\left\{\exp(\beta(\phi_{\mathrm{s}}(y)-\phi_{\mathrm{f}}(y)))+\exp(\beta(\phi_{\mathrm{s}}(y)-\phi_{\mathrm{f}}(y)))\right\}\right]^{1/2} \tag{3.35}$$

From Eq. (3.35) surface potential is calculated iteratively, where initial values are calculated by analytical equations derived under specific bias conditions.

3.2.3.3 Mobility Model

In HiSIM, at low electric field, carrier mobility μ_0 is modelled following the physically unified contributions with Coulomb scattering μ_{CB}, phonon scattering μ_{PH} and surface roughness scattering μ_{SR}

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\mathrm{CB}}} + \frac{1}{\mu_{\mathrm{PH}}} + \frac{1}{\mu_{\mathrm{SR}}} \tag{3.36}$$

Carrier collisions with charged (ionized) impurity atoms are accounted for by Coulomb scattering. Carrier collisions with the silicon lattice, mostly by acoustic phonons, are accounted for by phonon scattering. Surface roughness is detected when carriers are distributed close to the surface at high vertical electric fields. Each contribution is modelled as follows:

$$\mu_{\mathrm{CB}} = \mathrm{MUECB0} + \mathrm{MUECB1}\frac{Q_{\mathrm{i}}}{q.10^{11}} \tag{3.37}$$

$$\mu_{\mathrm{PH}} = \frac{\mathrm{MUEPH1}}{(T/300)^{\mathrm{MUETMP}}\varepsilon_{\mathrm{eff}}^{\mathrm{MUEPH0}}} \tag{3.38}$$

$$\mu_{\mathrm{SR}} = \frac{\mathrm{MUESR1}}{E_{\mathrm{eff}}^{\mathrm{MUESR0}}} \tag{3.39}$$

MUECB0, MUECB1, MUEPH1, MUEPH0, MUETMP, MUESR0, MUESR1 are fitting parameters. The mobility universality is preserved by MUEPH0=0.3 and MUESR0=2 for electrons and 1 for holes. The effective electric field is given by

$$\varepsilon_{\mathrm{eff}} = \frac{\mathrm{NDEP}.Q_{\mathrm{b}} + \mathrm{NINV}.Q_{\mathrm{i}}}{\varepsilon_{\mathrm{Si}}} \tag{3.40}$$

where NDEP=1 and NINV is 1/2 for electrons and 1/3 for holes. This important finding is called “universal mobility” verified by Sabnis and Clemens in 1979 [36].

The lateral electric field increases as the drain voltage increases. The carrier velocity increases near the drain region until it reaches carrier velocity saturation. The high-field electron mobility is modelled in this case as

$$\mu_{\text{eff}} = \frac{\mu_0}{\left(1+\left(\frac{\mu_0 \varepsilon_y}{v_{\max}}\right)^{BB}\right)^{1/BB}} \tag{3.41}$$

BB is 2 and 1 for NMOS and PMOS [36], $v_{\max}$ is $6\text{x}10^6$ cm/s for conventional MOSFETs, which can increase beyond the value called carrier velocity overshoot.

3.3 Compact Models for SOI MOSFETs

As SOI-MOSFET was aware of its advantages for advanced circuits, a physics-based SOI MOSFET compact model that serves as a bridge between the manufacturing process and circuit design was required for successful use of SOI technologies. Such a model must faithfully reproduce the device characteristics specific for SOI technology, such as reduced junction capacitance, dynamic threshold voltage shifts associated with the floating body effect (FBE), and the corresponding increase in the I_{on}/I_{off} ratio, which is beneficial for low-power CMOS applications. Here, compact models, which have been used for circuit designs, are briefly reviewed.

3.3.1. BSIM-SOI Model

BSIM-SOI model is also threshold voltage based as bulk MOSFET model BSIM. It shares the same fundamental equations as the bulk model, preserving the smoothness and physical characteristics of BSIM4 [37]. The most important challenge was to model dynamic change between fully depleted condition and partially depleted condition during circuit operation. The combined efforts of the BSIM Team at UC Berkeley and the IBM Semiconductor Research and Development Center (SRDC) at East Fishkill resulted in the inclusion of numerous improved features in BSIM-SOI 2010s. Some of the most important features of BSIM-SOI are as follows:

1. Simulation of floating body characteristics. It affects body potential which is determined by balance of all body current components.
2. A more accurate model of the parasitic bipolar current for modelling history effect. Improvements in the different diode leakage components, second order effects

(high-level injection and the Early effect), the diffusion charge equation, and the temperature dependence of the diode junction capacitance are all included.

3. A more accurate model of the impact-ionization current.
4. A thin-oxide SOI technology model for gate-to-body tunneling current.
5. The modeling of distributed body-resistance is made simpler by the introduction of an external body node.
6. Inclusion of self-heating effect by introducing additional node for thermal coupling with other devices.

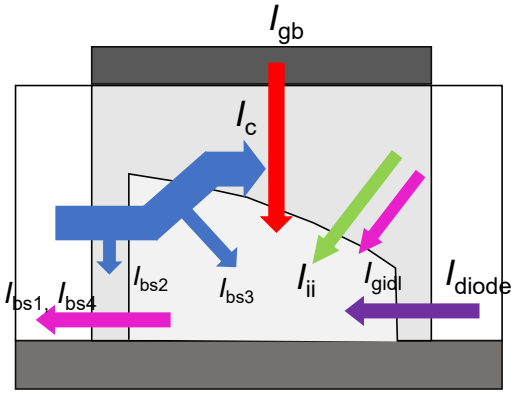

Figure 3.3: Modeling of current component inside the body for BSIMSOI. I_c, (I_{bs1}, I_{bs2}, I_{bs3}, I_{bs4}), I_{ii}, I_{gidl}, I_{gb} and I_{diode} denote parasitic bipolar transistor current, body to source diode current, impact ionization generated current, gate induced drain leakage current and drain to body diode current.

In BSIM-SOI floating body effect is determined through body current as depicted in Figure 3.3. All current components together contribute to produces body current, which captures newly introduced body potential.

All current equations are a function of effective node potentials. For example, the intrinsic drain current equation is expressed as

$$I_{ds,MOSFET} = \frac{I_{ds0}}{1+\frac{R_{ds}I_{ds0}}{V_{dseff}}}\left(1+\frac{V_{ds}-V_{dseff}}{V_A}\right) \tag{3.42}$$

where

$$I_{ds0} = \frac{\beta V_{gsteff}\left(1-A_{bulk}\frac{V_{dseff}}{2\left(V_{gsteff}+2v_t\right)}\right)V_{dseff}}{1+\frac{V_{dseff}}{E_{sat}L_{eff}}}$$

and $\beta = \mu C_{ox} \frac{W_{eff}}{L_{eff}}$

where V_{dseff}, R_{dseff} and μ respectively denote effective drain to source bias, drain to source series resistance and mobility. E_{sat} denotes critical electric field at velocity saturation and V_A accounts for channel length modulation.

3.3.2. PSP-SOI Model

PSP (Pennsylvania State University and Philips) SOI-MOSFET model for bulk-MOSFET is extended for SOI-MOSFET [38]. PSP is a surface-potential-based model, where analytical description is used for the surface-potential calculation. In PSP-SOI model, intrinsic drain current is computed from the charge-sheet model.

$$I_{ds} = \mu W \frac{C_{ox}}{\left(L_{eff} + L_{sat}\right)} \left(Q_i + \alpha\beta^{-1}\right)\left(\phi_{sd} - \phi_{ss}\right) \tag{3.43}$$

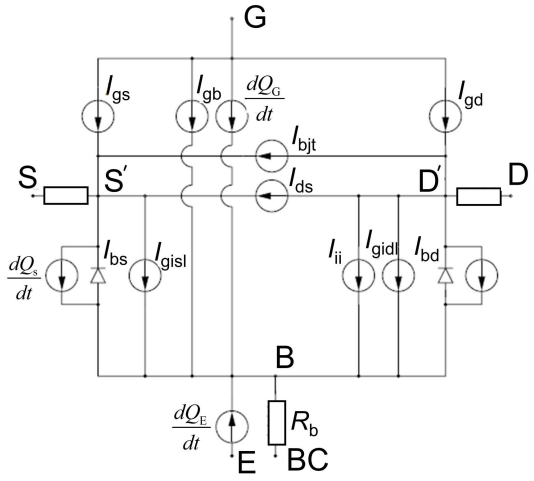

Figure 3.4: PSP-SOI circuit representation. I_{ds} stands for intrinsic drain current, I_{bjt} for parasitic bipolar current, I_{ii} for impact ionization current, and I_{gidl}/I_{gisl} for gate-induced drain/source leakage. I_{bs}/I_{bd} stands for source/drain junction current. Source, drain, gate, and back-gate charges are represented by Q_S, Q_D, Q_G, and Q_E respectively. For body-contacted SOI, an additional node (BC) connects internal body node (B) voltage through a body resistance R_B.

where μ denotes effective mobility, Q_i represents inversion charge at potential midpoint and $\beta^{-1} = kT/q$. ϕ_{ss} and ϕ_{sd} denotes surface potential at source and drain side respectively. L_{eff} is effective channel length and L_{sat} is saturation velocity dependent constant. The actual drain current (see Figure 3.4) is obtained by considering the contribution from junction capacitance at source/SOI and drain/SOI junctions, floating body effect due to

impact ionization generated holes and gate to body tunneling current.

Equivalent circuit model depicted in Figure 3.4 describes all current contributions, which are a function of node potentials together with body potential, similar to BSIM-SOI. The body potential is also determined by all current contributions. Modeling the floating body effects in SOI, such as the "kink" effect and history dependence of propagation delay, is done by using a junction model, including Shockley-Read-Hall recombination/generation, trap-assisted tunneling, and band-to-band tunneling currents. By improving the junction model, it was shown that SOI-MOSFET specific characteristics can be modeled accurately.

3.3.3 HiSIM SOI MOSFET Model

HiSIM-SOI model is the first complete potential-based model valid for any structural variations as well as any bias conditions, which has been published in 2002 [39]. The fundamental focus of this model is how to calculate potential distribution, which provides fundamental metrics for describing device properties. HiSIM-SOI captures the dynamic depletion-condition change according to both the bias condition and the device structure.

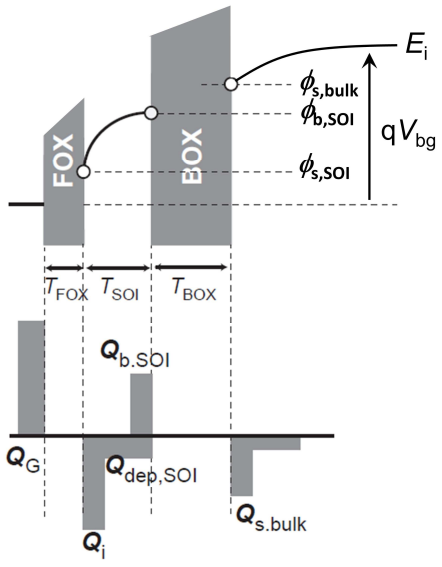

Figure 3.5: Three surface potentials along with induced charges in SOI MOSFET. Surface potentials are measured as band bending from intrinsic Fermi energy level E_i at the substrate to the surface. Therefore, conduction band and valance band are not shown for simplistic representation. Band offset between the insulator and semiconductor is not to scale to highlight E_i more precisely.

The Poisson equation is iteratively solved in HiSIM-SOI from the surface to the bulk substrate. The surface potential value ϕ_s together with the ϕ_b, solved by the Poisson equation, establishes whether the device is operating in fully depleted (FD) or partially depleted condition (PD).

HiSIM-SOI MOSFET model at early stage considers three surface potentials $\phi_{s,SOI}$, $\phi_{b,SOI}$ and $\phi_{s,bulk}$ in SOI structure as shown in Figure 3.5. All surface potentials are measured from intrinsic Fermi energy level E_i at the substrate. It induces different charges within SOI layer and substrate (Q_s, Q_b, Q_{bulk}). Using the Poisson equation together with the Gauss law the relation between charges and potential are obtained as follows

$$V_{gs} - V_{fb} = \phi_{s,SOI} - \frac{Q_{s,SOI} + Q_{b,SOI} + Q_{dep,SOI} + Q_{s,bulk}}{C_{FOX}} \tag{3.44}$$

Using boundary condition, the following relation is obtained.

$$\phi_{s,bulk} = \phi_{b,SOI} + \frac{Q_{s,bulk}}{C_{BOX}} \tag{3.45}$$

Here, $C_{FOX} = \varepsilon_{OX}/T_{FOX}$ and $C_{BOX} = \varepsilon_{OX}/T_{BOX}$. The charges are determined as a function of surface potential [39]. Thus, HiSIM-SOI captures advanced SOI MOSFET phenomenon such as floating body effect, punch-through effect, self-heating effect. The next generation of HiSIM-SOI considers back-gate charge Q_b explicitly, which enabled to capture accurate modeling for V_{bs} variation.

Chapter 4

Investigation for Dual Gate Control Mechanism

The increased popularity of ultrathin-film transistors is because of their superior short-channel control and suppression of device variability due to dopant fluctuation [40,41]. Planar thin-film transistor is more compatible with current CMOS technologies, making it easier to transfer existing circuit designs. These transistor topologies were created for extremely low power applications, and one of them is DG-MOSFET as mentioned in chapter 2. This device reduces power loss and process variation effect by controlling threshold voltage through ultra-thin buried oxide through back-gate voltage (V_{bg}) variation. Not only this, DG-MOSFET has been successfully investigated for 0.4V circuit operations [42, 43]. It has been verified that the 0.4V operation can be achieved without sacrificing circuit performance [44]. Back-gate contact can be utilized as an additional control gate in case of reduced T_{BOX}, which leads to extended design flexibility due to adjustability of V_{th}. The low-voltage circuit operation has been achieved by applying a positive bias on the back gate, whereby low threshold voltage (V_{th}) is realized. This type of thin-SOI- and thin-BOX-layer MOSFET is regarded as the most significant contribution to MG-MOSFET structures [45] with independent gate control. To take advantage of these new devices for circuit design, an accurate compact model must be developed. The potential distribution must be explicitly considered from the surface to the bottom of the substrate to precisely represent all induced charges, making the construction of compact models for ultrathin-film devices exceedingly challenging. Both the BOX thickness and the substrate impurities concentration have a significant impact on the potential value at the surface of the front gate.

Although well-established V_{th} models exist for the bulk MOSFET, the presence of an additional back gate makes it challenging to develop an accurate V_{th} model for such a generation of thin-layer MOSFETs, where a V_{th} shift is accompanied with the subthreshold swing. An analytical model for swing degradation has been developed based on the volume-inversion effect by considering the potential distribution along the device depth direction. Under such a condition, the back-gate control on the potential distribution

is the major concern. Another V_{th} description has been developed by considering both the front- and back-gate contributions explicitly [46-49]. However, all possible induced charges are not explicitly considered yet. Thus, our purpose of the present investigation is the development of a closed-form V_{th} description for a dual-gate MOSFET structure with independent gate control by considering the whole potential distribution to include all possible charge distributions.

4.1 Structure Parameter for DG-MOSFET

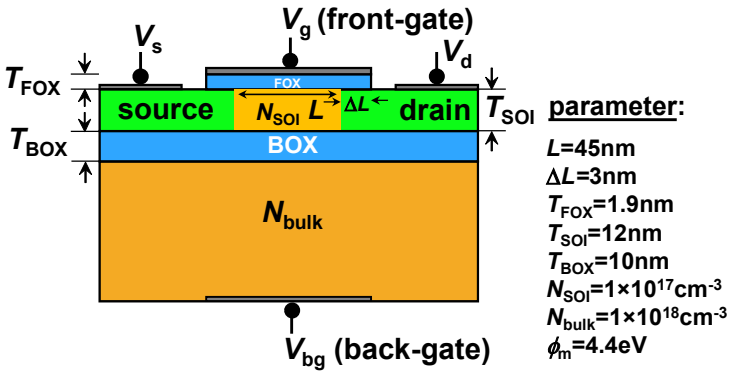

Figure 4.1: Structural description of thin-BOX DG MOSFET. Thinner BOX layer makes it suitable for low voltage applications.

The thin-BOX DG-MOSFET structure for our investigation is shown in Figure 4.1. Structural parameters are considered in such a way so that it follows conventional scaling rules to avoid extraordinary short-channel-effects. SOI and BOX layer thickness is 12nm and 10nm respectively. Channel length of the device is L=45nm, greater than 2.5xT_{SOI}. It is interesting to note that both SOI-layer and substrate are p-type and have doping concentration 1x10^{17}cm^{-3} and 1x10^{18}cm^{-3} respectively. Work-function of the gate material is 4.4eV, suitable for low voltage applications.

4.2 Important Device Characterization

As a substitute for measurement data, 2D-device simulations [50] have been used for our analysis of the V_{bg}-control properties. Figure 4.2 shows simulated I_{ds}-V_{gs} characteristics of the studied structure. Models adopted for the device simulation are the Lombardi mobility with the field dependency, the SRH (Shockley-Read-Hall) generation and the

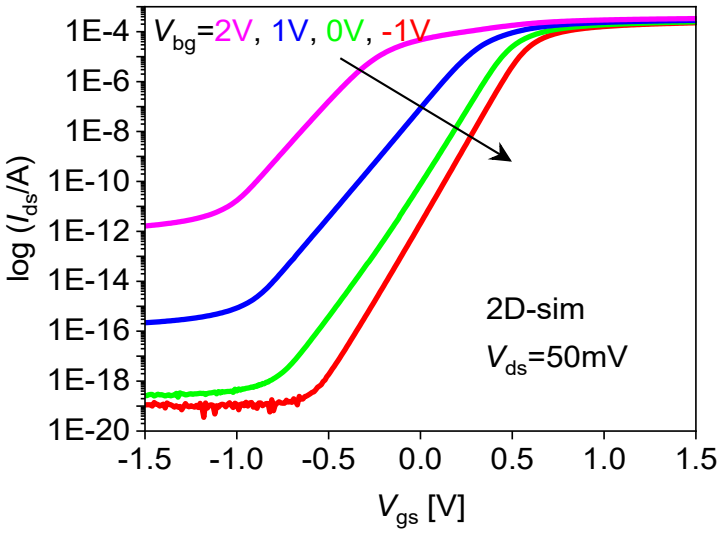

Figure 4.2: Simulated I_{ds} -V_{gs} characteristics for different V_{bg} at V_{ds}=50mV.

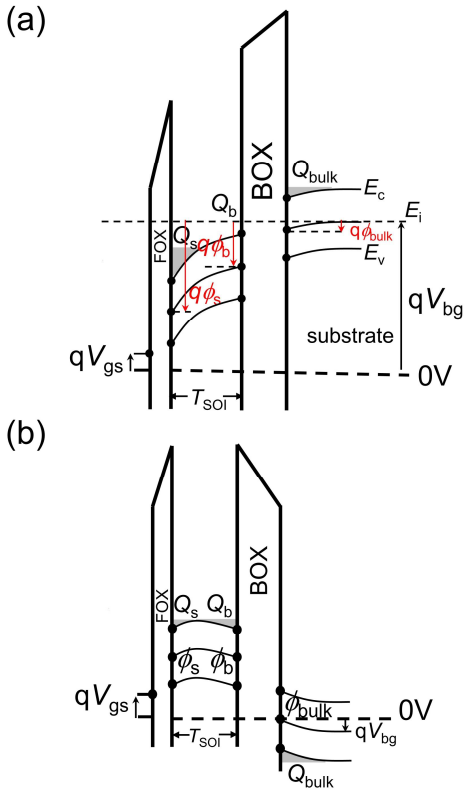

Figure 4.3: Energy distribution perpendicular to the device surface at the channel middle (a) for Q_{bulk}<0 and (b) for Q_{bulk}>0. Surface potentials at the front and back-gate (ϕ_s,ϕ_b) along with bulk (ϕ_{bulk}) are shown which influence charge generations within body (Q_s, Q_b) and bulk (Q_{bulk}), respectively. All surface potentials are measured from intrinsic Fermi energy level E_i at the substrate.

Auger recombination together with the bandgap narrowing. Charges at interfaces are ignored. The V_{th} shift is enhanced, when V_{bg} becomes increasingly positive biased. The compact model HiSIM_DG has been previously developed on the basis of the potential

distribution within the thin-substrate layer for common controlling of the front and back gates [39]. This concept is further developed here for general thin-layer MOSFET structures under independent gate control by considering the V_{bg} contribution explicitly [51]. Figure 4.3 depicts all charges (Q_s: front-gate charge, Q_b: back-gate charge, Q_{bulk}: bulk charge) induced within the device schematically under the condition of strong charge coupling between front gate and back gate. These charges are function of potential distribution (ϕ_s: front-gate potential, ϕ_b: back-gate potential, ϕ_{bulk}: bulk potential) along

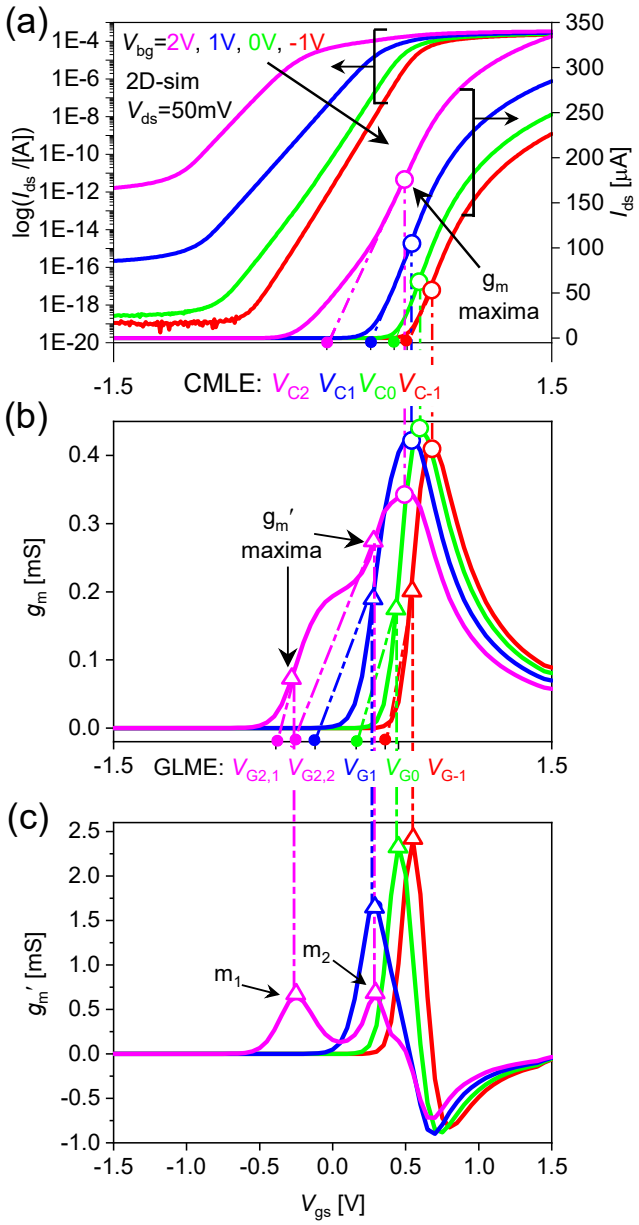

Figure 4.4: (a) I_{ds}-V_{gs} characteristics for different V_{bg} values at low drain voltage (V_{ds}=50mV), where open circles denote V_{th} by the CLME method. (b) Transconductance (g_m) plot, revealing non-monotonicity for higher V_{bg} before reaching the maximum due to the back-gate-inversion-charge (Q_b) contribution, where open triangles denote V_{th} by the GLME method. (c) g_m derivatives, which verify a double-peak structure due to the non-monotonicity.

device depth direction perpendicular to the channel (see Figure 4.3a).

4.3 Threshold Voltage (V_{th}) Extraction

Although V_{th} extraction methods for bulk technology [52-54] already exist, a corresponding analytical description for thin-layer MOSFETs is still missing.

The V_{th} of a thin-BOX-layer SOI-MOSFET can be easily adjusted by the back-gate voltage V_{bg}, a property which is utilized to realize low power circuits. Therefore, the accurate knowledge of V_{th} as a function of V_{bg} is important for device and circuit designers. The V_{th} extraction as well as the modeling of bulk-MOSFETs have been already developed and verified even with advanced technologies. However, a corresponding investigation for thin-layer DG-MOSFETs is still missing.

Previously, different V_{th} extraction methods have been developed for bulk MOSFETs. The most frequently applied methods are the constant-current linear-extrapolation method at the V_{gs} providing the maximum transconductance (g_m) (CMLE) [22, 23] and the *g*m-linear extrapolation at the maximum of the *g*m-derivative (*g*m′) with respect to *V*gs (GMLE) [54], as illustrated in Figure 4.4. The extracted V_{th} values by the two different methods are depicted together. They are distinguished by "C" and "G" for the CMLE method and the GMLE method, respectively. The extraction results are compared as a function of V_{bg} in Figure 4.5. The values are summarized in Table 4.1. The difference between the two methods becomes quite obvious for positive V_{bg} values. The CMLE method extracts the V_{gs} value where the mobility degradation has already started as the V_{th} value. The g_m peak occurs due to the balance between the carrier-density

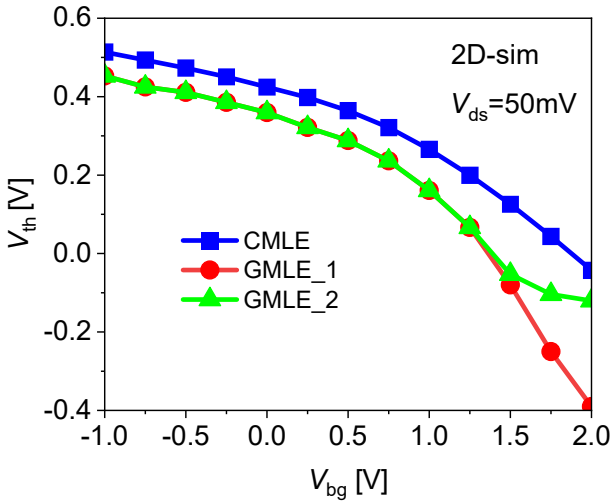

Figure 4.5: V_{th} variation as a function of V_{bg}. V_{th} degradation rate is higher after V_{bg}=1V due to the presence of inversion charges at BOX and SOI interfaces.

increase and the carrier-mobility reduction. On the other hand, the GMLE method extracts without this balance effect [54]. For V_{bg}≤1V, as can be seen in Figure 4.4b, g_m increases monotonically before reaching its maximum, as conventionally observed. With the further rise in V_{bg}, however, g_m exhibits non-monotonicity, showing a shoulder before reaching the maximum, which is reflected in gm' by two distinguishable maxima m_1 and m_2 (see Figure 4.4c). The first maximum (m_1) corresponds to the current component from the back-gate inversion charge Q_b, while the second maximum (m_2) corresponds to the additive contribution from the front-gate inversion charge Q_s on top of Q_b, as discussed in more detail with Figure 4.7 of the next section. Using the GMLE method these two maxima result in two different V_{th} values (see $V_{G2,1}$ and $V_{G2,2}$ in Figure 4.4).

Figure 4.6 shows 2D-device-simulation results for a relationship between I_{ds} and Q_{bulk} (charge induced below BOX, see Figure 4.3) as a function of V_{gs} for different V_{bg} values. It can be seen, that Q_{bulk} becomes independent of V_{gs} beyond the extracted V_{th} with the GMLE method. The reason is, that the inversion charge at the front gate Q_s is completely located close to the surface, so that the V_{gs} influence becomes a local effect, leaving Q_{bulk} only dependent on V_{bg}. As can be seen also in Figure 4.6, V_{th} extracted by GMLE for V_{bg}≤1V coincides with the V_{gs} voltage, above which Q_{bulk} starts to become independent of V_{gs}. For V_{bg} =2V, however, Q_{bulk} is not yet sufficiently independent of V_{gs} at $V_{G2,1}$. It rather becomes independent only at the higher value of V_{gs}=$V_{G2,2}$. Thus, it can be concluded that the two different V_{th} values determine different device conditions. $V_{G2,1}$ is the starting point with sufficient current for the circuit operation. V_{gs}=$V_{G2,2}$ is the starting point of the conventional MOSFET control by V_{gs}, without further changes of Q_{bulk}. Therefore, we can conclude that the GMLE method can provide a meaningful V_{th} extraction, reflecting the physical device condition, even for an advanced DG-MOSFET generation.

Table 4.1: Extracted V_{th} for Different V_{bg} Values with Two Different Extraction Methods

V_{bg} [V]	V_{th} CMLE [V]	V_{th} GMLE [V]
2	V_{C2}=-0.04	$V_{G2,1}$=-0.39 $V_{G2,2}$=-0.12
1	V_{C1}=0.26	V_{G1}=0.16
0	V_{C0}=0.42	V_{G0}=0.36
-1	V_{C-1}=0.51	V_{G-1}=0.45

Device characteristics of the studied device are determined not only by the charge induced at the front gate Q_s but also at the back-gate charge Q_b (see Figure 4.3). Here, our focus is given on the Q_b contribution in the V_{th} determination under the front-gate control, which means that V_{gs} is swept while V_{bg} is kept fixed at different values. The

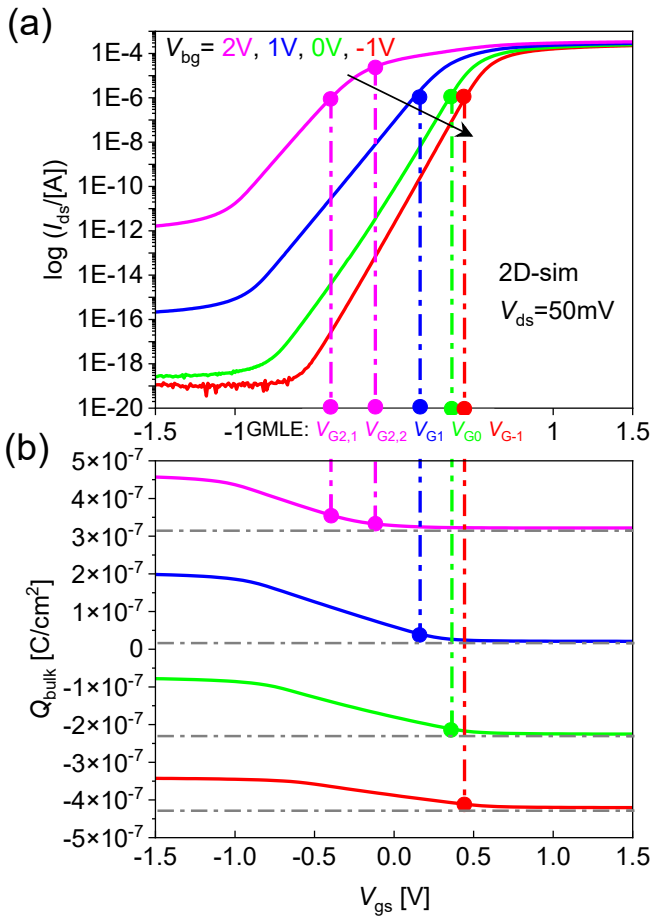

Figure 4.6: (a) I_{ds} -V_{gs} characteristics for different V_{bg} at V_{ds}=50mV. (b) V_{gs} dependency of Q_{bulk} diminishes beyond V_{th} leaving only dependency on V_{bg}.

front-gate potential ϕ_s and the back-gate potential ϕ_b, which are the origin of the device characteristics, are determined by a balance derived through the solution of the Poisson's equation together with the Gauss law [55, 56]. By solving these equations, the potential distribution as a function of applied voltages can be obtained. The potential characteristics of 2D-device-simulation results are depicted in Figure 4.7 as a function of V_{gs} for four different V_{bg} values. It is observed that ϕ_b becomes larger than ϕ_s for most V_{gs} biases as V_{bg} increases. However, ϕ_s always exceeds ϕ_{sb} when ϕ_s reaches the strong inversion condition.

V_{th} is conventionally determined as the V_{gs} where the carrier density reaches the impurity concentration, namely, the potential value of $2\Phi_B$ (= $2\beta^{-1}$ ln(N_{SOI}/n_i)), with n_i being the intrinsic-carrier density [57, 58]. It can be seen in Figure 4.7a, that the extracted V_{th} refers to either ϕ_s or ϕ_b values reaching $2\Phi_B$, even for the DG-MOSFET generation, except for $V_{G2,2}$. Figure 4.7b shows the carrier-density distributions, both for Q_s and Q_b. For V_{bg} =2V, first Q_b enters the inversion condition at ϕ_b=$2\Phi_B$ determining $V_{G2,1}$.

Afterwards strong inversion starts at ϕ_b=1.1x2Φ_B [59], determining $V_{G2,2}$. Additionally, at V_{gs}=$V_{G2,2}$, the bulk charge Q_{bulk} becomes independent of V_{bg}, namely, when ϕ_b reaches

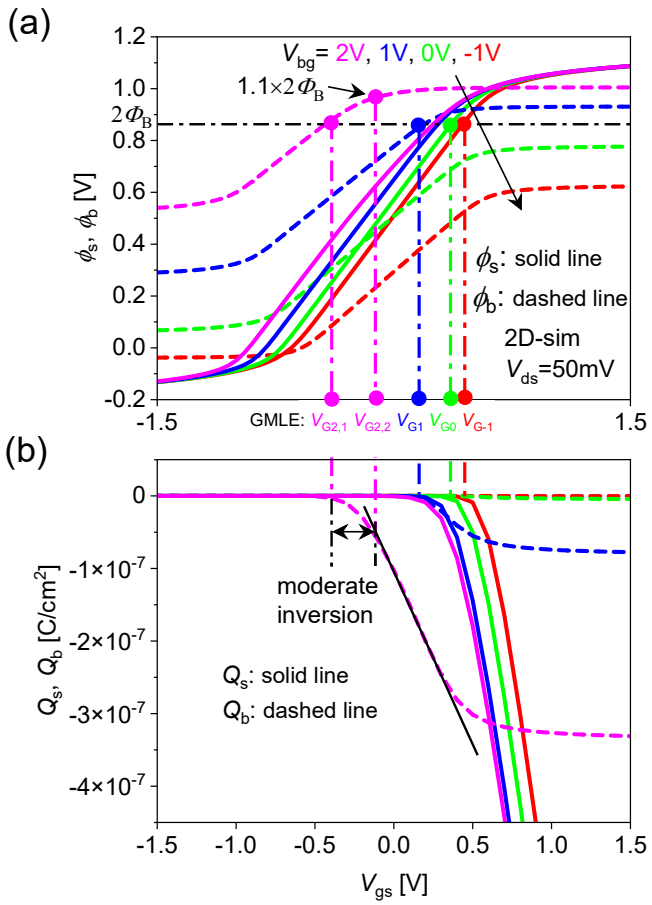

Figure 4.7: (a) Surface potentials at front gate and back gate (ϕ_s and ϕ_b) as a function of V_{gs} for different V_{bg}. (b) Q_s and Q_b as a function of V_{gs} for different V_{bg}.

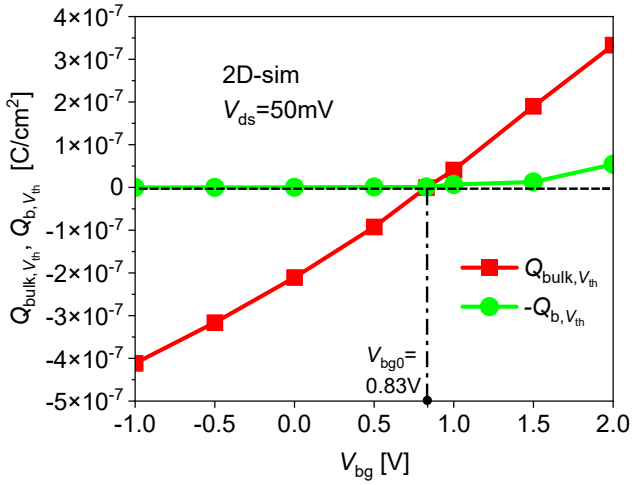

Figure 4.8: Comparative analysis of extracted $Q_{bulk,Vth}$, $Q_{b,Vth}$ as a function of V_{bg}. For V_{bg}>0.83V, $Q_{b,Vth}$ starts to pile up gradually and becomes comparable with $Q_{bulk,Vth}$.

1.1x2Φ_B (see Figure 4.7). This verifies, that ϕ_b enters the strong inversion conditions, so that ϕ_{bulk} is left unchanged. However, Q_b does not increase further as a function of V_{gs}, as usually observed for an inversion charge, but starts to saturate, because the two different peaks m_1 and m_2 are determined by contributions from two different charges (Q_s and Q_b). It can consequently be seen, that effective V_{th} is determined by both Q_s and Q_b, depending on the V_{bg} bias value. It can be also concluded, that Q_{bulk} will remain unchanged by V_{gs} beyond the V_{th} condition. Therefore, a key point for an analytical V_{th} description is the knowledge of the constant Q_{bulk} value as a function of V_{bg}.

4.4 Analytical V_{th} Description

Applying charge conservation principle in along depth direction perpendicular to the channel in MOSFET,

$$Q_g + Q_s + Q_b + Q_{dep} + Q_{bulk} = 0 \tag{4.1}$$

Using Gauss Law at the Oxide/Si interface,

$$E_{ox}\varepsilon_{ox} = E_s\varepsilon_s \tag{4.2}$$

where,

$$E_{ox} = \frac{(V_{gs} - V_{fb} - \phi_s)}{T_{FOX}} \tag{4.3}$$

The Poisson equation describes the relationship between the potential distribution and the total charge

$$\frac{\partial^2\phi}{\partial x^2} = -\frac{(Q_s + Q_b + Q_{dep} + Q_{bulk})}{\varepsilon_s} \tag{4.4}$$

which derives the field within semiconductor by integrating the equation once. It can be observed that field is position dependent. Combining Eq. (4.3) and (4.4), the final equation derives to,

$$V_{gs} - V_{fb} - \phi_s = -\frac{Q_s + Q_b + Q_{dep} + Q_{bulk}}{C_{FOX}} \tag{4.5}$$

Here, $C_{FOX} = \frac{\varepsilon_s}{T_{FOX}}$ In case of bulk MOSFET, Q_b and Q_{bulk} charge don't exists. So, Eq. (4.5) simplifies to

$$V_{gs} - V_{fb} - \phi_s = -\frac{Q_s + Q_{dep}}{C_{FOX}} \tag{4.6}$$

At threshold condition, Q_s is in the verge of entering strong-inversion condition, which resembles, magnitude of Q_s remains negligible to consider. So, Eq. (4.6) modifies to

$$V_{th} = V_{fb} + 2\Phi_B - \frac{\sqrt{2\varepsilon_s q N_{sub} 2\Phi_B}}{C_{OX}} \tag{4.7}$$

where $Q_{dep} = -q \times N_{sub} \times W_d$ and $W_d = \sqrt{\frac{2\varepsilon_s . 2\Phi_B}{qN_{sub}}}$

Here, ϕ_s is fixed to $2\Phi_B$ ($\Phi_B = \beta^{-1} \ln (N_{SOI}/n_i)$, $\beta^{-1} = KT/q$), C_{OX} is equal to C_{FOX}, and W_d is the depletion width, which is equal to T_{SOI} for a thin layer MOSFET. Although, channel starts to invert for ϕ_s larger than ϕ_f, true conductive channel exists at the surface when ϕ_s is equal to $2\Phi_B$ which resembles channel is inverted in such a way that free electron concentration in channel is identical to hole concentration in substrate. These minority carriers (free electrons) are attracted to the surface due to positive gate-biasing. However, our investigation in this study reveals for dual-gate MOSFET, Q_b and Q_{bulk} cannot be ignored under threshold condition. Therefore, at threshold, Eq. (4.5) modifies to

$$V_{th,MG} = V_{fb} + 2\Phi_B - \frac{Q_{dep,vth} + Q_{bulk,vth} + Q_{b,vth}}{C_{FOX}} \tag{4.8}$$

where $Q_{bulk,vth}$ and $Q_{b,vth}$ are the bulk charge and the back-gate charge at threshold condition. 2D-device simulations of these charges are compared in Figure 4.8 as a function of V_{bg}. It can be seen, that $Q_{bulk,vth}$ crosses the zero value at about V_{bg}=0.8V, and that Q_b starts to increase in positive direction beyond this V_{bg} value. By neglecting the inversion term, $Q_{bulk,vth}$ is thus written as [53, 55]

$$Q_{bulk,vth} = -Q_{0bulk} \sqrt{\exp(-\beta(\phi_{bulk} - V_{bg})) + \beta(\phi_{bulk} - V_{bg}) - 1} \tag{4.9}$$

where $Q_{0bulk} = \sqrt{2\varepsilon_{si} q N_{bulk} / \beta}$

In the following, Eq. (4.9) is further simplified according to conditions of the $Q_{bulk,vth}$

value.

4.4.1 Case of $Q_{\mathrm{bulk,vth}} \leq 0$

Under this condition, $Q_{\mathrm{bulk,vth}}$ is a depletion charge, which can be further simplified by neglecting the exponential term of Eq. (4.9).

$$Q_{\mathrm{bulk,vth}} = -Q_{0\mathrm{bulk}}\sqrt{\beta(\phi_{\mathrm{bulk}} - V_{\mathrm{bg}})} \tag{4.10}$$

The relationship for ϕ_{bulk} as a function of ϕ_{s}, derived by considering the boundary conditions, thus becomes

$$\phi_{\mathrm{bulk}} - \phi_{\mathrm{s}} = C_0 Q_{\mathrm{bulk,vth}} \tag{4.11}$$

where C_0 is a constant determined by device geometry (see Table 4.1). By substituting Eq. (4.5) into Eq. (4.6), ϕ_{bulk} is written as

$$\phi_{\mathrm{bulk}} = \frac{C_1 + 2\phi_{\mathrm{s}} - \sqrt{C_1^{\,2} + 4C_1(\phi_{\mathrm{s}} - V_{\mathrm{bg}})}}{2} \tag{4.12}$$

where $C_1 = C_0^{\,2} Q_{0\mathrm{bulk}}^{\,2}\beta$. Eq. (4.5) together with Eq. (4.10) derives the equation for $Q_{\mathrm{bulk,vth}}$ as

$$Q_{\mathrm{bulk,vth}} = -Q_{0\mathrm{bulk}}\sqrt{\beta\left(\frac{C_1 + 2\phi_{\mathrm{s}} - \sqrt{C_1^{\,2} + 4C_1(\phi_{\mathrm{s}} - V_{\mathrm{bg}})}}{2} - V_{\mathrm{bg}}\right)} \tag{4.13}$$

By substituting $Q_{\mathrm{bulk,vth}}$ into Eq. 8 with $\phi_{\mathrm{s}}=2\Phi_{\mathrm{B}}$, the final equation for $V_{\mathrm{th,MG}}$ can be written in the form

$$V_{\mathrm{th,MG}} = V_{\mathrm{fb}} + 2\Phi_{\mathrm{B}} - \frac{Q_{\mathrm{dep}} - Q_{0\mathrm{bulk}}\sqrt{\beta\left(\frac{C_1 + (2\times 2\Phi_{\mathrm{B}}) - \sqrt{C_1^{\,2} + 4C_1(2\Phi_{\mathrm{B}} - V_{\mathrm{bg}})}}{2} - V_{\mathrm{bg}}\right)}}{C_{\mathrm{FOX}}} \tag{4.14}$$

where all constants are summarized in Table 4.2.

Table: 4.2 Constants Used for Analytical V_{th} Description

Constants	Values	Remarks
C_0	$\left(\frac{1}{C_{BOX}}+\frac{1}{C_{SOI}}\right)$	$C_{BOX}=\varepsilon_{OX}/T_{BOX}$ $C_{SOI}=\varepsilon_{si}/T_{SOI}$
C_1	$C_0^{\,2}Q_{0bulk}^{\,2}\beta$	$\beta=(KT/q)^{-1}$
C_2	$\left(\frac{Q_{0bulk}\times\beta}{C_{BOX}}\right)$	$Q_{0bulk}=\sqrt{2\varepsilon_{si}qN_{bulk}/\beta}$
C_3	$\left(\frac{C_2}{\sqrt{2}}+1\right)$	
C_4	$\left(\frac{\beta\times C_2}{6\sqrt{2}}\right)$	
C_5	$4C_1-4\{C_1+(2\times 2\Phi_B)\}$	$2\Phi_B=2\beta^{-1}\ln(N_{SOI}/n_i)$
C_6	$(C_1+2\times 2\Phi_B)^2-C_1^2-(4C_1\times 2\Phi_B)$	

4.4.2 Case of $Q_{bulk,vth} > 0$

In this case Q_{bulk} is an accumulation charge and is written as

$$Q_{bulk,vth}=Q_{0bulk}\sqrt{\exp(-\beta(\phi_{bulk}-V_{bg}))+\beta(\phi_{bulk}-V_{bg})-1} \tag{4.15}$$

The results of a Taylor-series expansion of the root expression, with truncations at up to the 3rd-degree polynomial term, are shown in Figure 4.9 for evaluating the simplification of Eq. (4.10). Since the required potential differences ϕ_{bulk}-V_{bg} for the analytical equation are much smaller than -0.1V for realistic applications, consideration of up to the 3rd-degree polynomial term is judged as sufficient, and results in the simplified form of Eq. (4.11).

$$Q_{bulk,vth}=-Q_{0bulk}\beta(\phi_{bulk}-V_{bg})\left[\frac{1}{\sqrt{2}}-\frac{1}{6\sqrt{2}}\beta\left(\phi_{bulk}-V_{bg}\right)+\frac{1}{24\sqrt{2}}\beta^2\left(\phi_{bulk}-V_{bg}\right)^2\right] \tag{4.16}$$

The boundary condition at the BOX interfaces derives the relationship

$\phi_{bulk} - \phi_b = \frac{Q_{bulk,vth}}{C_{BOX}}$, which leads to

$$\phi_{bulk} - \phi_b = -C_2(\phi_{bulk} - V_{bg})\left(\frac{1}{\sqrt{2}} - \frac{1}{6\sqrt{2}}\beta(\phi_{bulk} - V_{bg})\right) \tag{4.17}$$

By solving the equation with respect to ϕ_{bulk} we obtain

$$\phi_{bulk} = \frac{C_3 - \sqrt{C_3^2 - 4C_4(\phi_b - V_{bg})}}{2C_4} + V_{bg} \tag{4.18}$$

Thus $Q_{bulk,vth}$ is written as

$$Q_{bulk,vth} = C_{BOX}\left(\frac{C_3 - \sqrt{C_3^2 - 4C_4(\phi_b - V_{bg})}}{2C_4} + V_{bg} - \phi_b\right) \tag{4.19}$$

where $Q_{bulk,vth}$ has been reduced to a function of ϕ_b and V_{bg}.

For V_{bg} >0.8V (see Figure 4.8), the inversion condition leads to a pile up of electrons at the BOX interface of the SOI layer, forming the inversion charge Q_b. A simplified equation for Q_b can be written as

$$Q_{b,vth} = -Q_{0SOI}\sqrt{2Q_{1SOI}e^{\beta\phi_b}} \tag{4.20}$$

where $Q_{0SOI} = \sqrt{2\varepsilon_{si}qN_{SOI}/\beta}$ and $Q_{1SOI} = n_i^2/N_{SOI}^2$, $\phi_b = 2\Phi_B$ for $V_{th,m1}$, and $\phi_b = 1.1x\Phi_B$

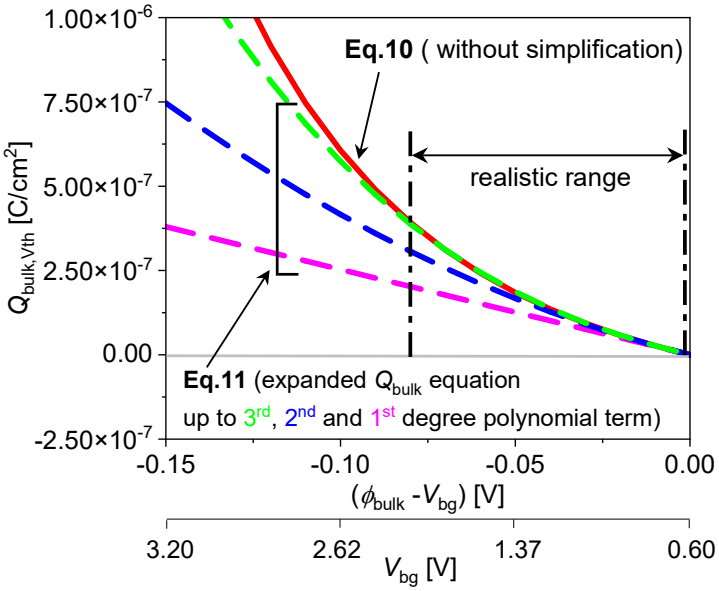

Figure 4.9: Comparison between Eq. 10 and its Taylor-series expansion up to 3rd, 2nd and 1st degree polynomial term as a function of ϕ_{bulk}-V_{bg}.

for $V_{th,m2}$ are valid. After substituting Eq. (4.14) and (4.15) into Eq. (4.3), the final $V_{th,MG}$ equation is written as

$$V_{th,MG} = V_{fb} + 2\Phi_B - \left[Q_{dep} + C_{BOX} \left\{ \left(C_3 - \sqrt{C_3^2 - 4C_4(2\Phi_B - V_{bg})} \right) \Big/ 2C_4 + V_{bg} - 2\Phi_B \right\} - Q_{0SOI} \sqrt{2Q_{1SOI} e^{2\beta\Phi_B}} \right] \Big/ C_{FOX} \quad (4.21)$$

An analytical equation for V_{bg} at $Q_{bulk,vth}$ =0 (=V_{bg0}) can be derived from Eq. (4.10) in the form

$$V_{bg0} = \frac{-C_5 \pm \sqrt{C_5^2 - 16C_6}}{8} \quad (4.22)$$

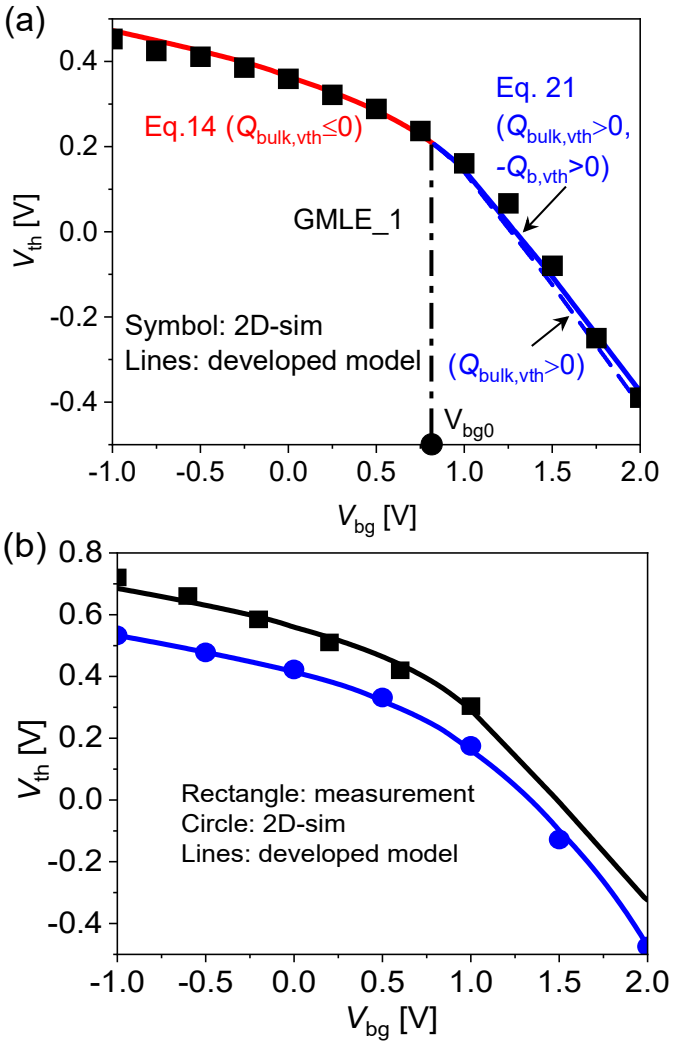

Figure 4.10: Comparison of simulated with 2D-device numerical simulator and modeled V_{th} for the DG-MOSFET structure (a) with T_{FOX}=1.9nm, T_{SOI}=12nm and T_{BOX}=10nm. For $Q_{bulk,vth}$>0, the solid line represents V_{th} including Q_b and dashed line without Q_b, (b) with T_{FOX}=1.9nm, T_{SOI}=8nm and T_{BOX}=6nm. For comparison measured result with T_{FOX}=1.9nm, T_{SOI}=12nm and T_{BOX}=10nm are also plotted.

For the studied device structure, V_{bg0}=0.83V is calculated, which accurately reproduces the extracted value from the 2D-device-simulation results (see Figure 4.8).

Figure 4.10a compares the extracted V_{th} values from 2D-device-simulations with the GMLE method to the results calculated with our developed analytical model without any fitting parameters. It can be seen, that a good overall agreement is achieved and that Eq. (4.14) has a transition to Eq. (4.21) without discontinuity at $V_{bg}=V_{bg0}$, where Q_{bulk} is equal to 0. According to Eq. (4.22), V_{bg0} becomes smaller for both T_{SOI} and T_{BOX} reduction. For comparison, another device structure has been investigated, as depicted in Figure 4.10b together with additional results for measured data taken from literature [60]. The good agreement confirms that the developed analytical model can be applied for any structure-type of a thin-layer MOSFET with independently controlled gates.

4.5 Summary

Our focus has been given on the contribution of induced charges in DG-MOSFETs at different gates under the threshold condition. It has been demonstrated, that the g_m-gradient maximum linear extrapolation method can provide physically reasonable results, even for MG-MOSFET generations. We have developed an analytical V_{th} model for such thin-layer MOSFETs with independent gate control by solving the Poisson equation together with the Gauss Law analytically, in a way that considers all possible induced charges. It has become clear, that the major surface-potential values at both front and back gate are contributing to the determination of the physically correct V_{th} value in a dynamic way. Additionally, it has been verified, that the threshold condition is given, when the potential bending reaches to $2\Phi_B$ at either the front-gate or the back-gate surface. However, it becomes 1.1x2Φ_B, when the major gate dominates the device control. The developed analytical model has been demonstrated to accurately describe the V_{th} characteristics of an advanced thin-layer MOSFET generation based on only the device parameters, so that it can be applied for both device optimization and circuit design. The developed model can be further extended to include the short-channel-effects by considering the potential distribution [61].

The V_{th} reduction due to application of a positive back-gate voltage has been used to achieve reliability in low voltage applications. Further, an analytical equation has been derived for V_{bg}, when Q_{bulk} becomes zero, namely, the flat-band condition for the back-gate control V_{bg0}. This value is mainly determined by the impurity concentration N_{bulk} of the substrate. Since the V_{th} reduction for $V_{bg}>V_{bg0}$ becomes more efficient, a reduction of

N_{bulk} is appropriate for the low-voltage operation. However, N_{bulk} reduction causes a potential drop in the substrate, which must be optimized in accordance with the requirements of the targeted circuitry.

Chapter 5

Dual-Gate MOSFET for Low-Voltage Application

5.1 Introduction

From the previous chapter, it is learnt that positive back-gate biasing reduces V_{th} for DG-MOSFET, which is suitable for low voltage applications. Moreover, back-gate control improves subthreshold swing compared to its bulk counterpart with identical bias condition. So, influence of the back-gate control is an important factor for performance and power-loss optimization. Besides, supply-voltage (V_{dd}) scaling is also one of the most effective ways to reduce dynamic power loss, as it has a quadratic relationship with the switching loss [62], [63]. However, scaling down the supply voltage weakens the front-gate control over the channel, especially for short-channel-length devices, due to the lateral-field dominance, produced by the source/drain junction depletion extension [61], [64]. This degrades the subthreshold slope. Therefore, to significantly strengthen the vertical electric field dominance over lateral field, a contribution from the back-gate is essential, and this is what multi-gate structure offers. In a DG-MOSFET structure, both front- and back-gate-controlled currents constitute the overall drain current (I_{ds}). In the subthreshold condition, a weaker front-gate-controlled-current contribution is inadequate for fast switching operation. Positive back-gate biasing is essential to increase the back-gate-controlled current. However, the efficiencies of front- and back-gate-current control by V_{gs} and V_{bg}, respectively, are vastly different in nature, due to different oxide thicknesses (FOX and BOX) and presence of an additional substrate region underneath BOX. Although positive back-gate biasing increases the drain current, its efficiency varies over a wide range of values [65].

Our investigation focuses on V_{bg}-control efficiency for back-gate-current generation and its impact on circuit performance. The near- or sub-threshold region is specifically analyzed, as it is highly attractive for the purpose of improving energy efficiency. As a substitute for measurement data, 2D-device simulations [50] are used in

the analysis. By applying the developed compact model HiSIM_DG [66], the key factors for optimizing circuit performance and device structure are clarified. It is demonstrated that an independent control of the DG-MOSFET gates provides the necessary optimization freedom for simultaneously achieving the requirements of both low switching loss and sufficiently high switching speed.

The SOTB-MOSFET structure, applied in our investigation, is shown in Figure 4.1, where also the device parameters and their values are listed. Figure 5.1a depicts the I_{ds}-V_{gs} characteristics of 2D-device simulation for different back-gate voltages (V_{bg}). The extracted threshold voltage V_{th} is plotted in Figure 5.1b as a function of V_{bg}. This extraction is done with the GMLE method, which has been verified to provide reliable results for advanced MOSFET generations [54]. It can be seen, that V_{th} is reduced drastically for $V_{bg}>0$, which is used to realize low-power operation [67]. The main effect of a positive V_{bg} is the additional formation of a back-gate charge Q_b, as schematically depicted in Figure 5.3. The surface potentials ϕ_s and ϕ_b at front and back gate are compared in Figure 5.2b as a function of V_{gs} for different V_{bg} values. The threshold condition occurs, when either of the potential values ϕ_s and ϕ_b reaches $2\Phi_B$. It can be seen roughly, that the threshold condition is mainly determined by the back-gate potential ϕ_b for $V_{bg}>0$ and by the front-gate potential ϕ_s for $V_{bg}<0$.

5.2 Efficiency of Back-Gate Control in Circuit

We have developed the compact model HiSIM_DG, which is applicable for independent-gate control of DG-MOSFETs. The model can be utilized for common-gate control as well as for more advanced technologies such as those of SOTB-MOSFETs. Our main focus here is to analyze the Q_b contribution of the SOTB-MOSFET generation in circuits. For this purpose, all possible induced charges within the device are considered explicitly, together with the deep current flow near the BOX side. The Poisson's equation is used together with the Gauss law to derive the V_{gs} dependency of the total charge (see Eq. (4.5)). The Poisson equation is solved iteratively together with the boundary conditions at the different material junctions [69], [70]. Figure 5.1b reveals, that HiSIM_DG can

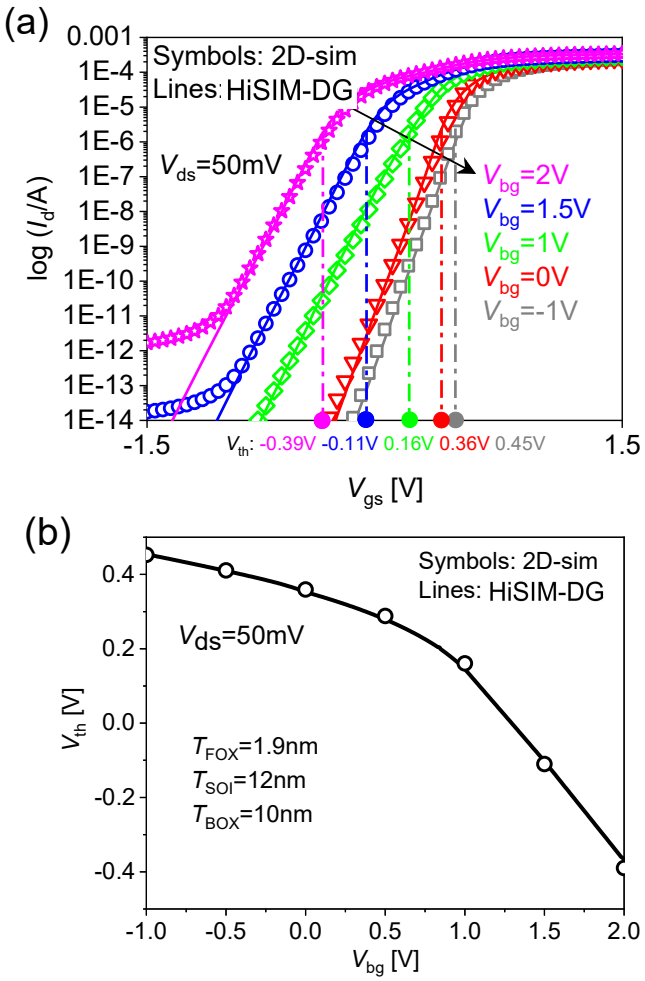

Figure 5.1: (a) I_{ds}-V_{gs} characteristics for different V_{bg} at drain voltage of 50mV, and (b) Extracted threshold voltage.

realize a good fit to the 2D device simulation results for any bias conditions.

For $V_{bg} \leq 0$, mostly ϕ_s dominates over ϕ_b (see Figure 5.2b), which indicates that the inversion charge Q_s at the front-gate side is giving the major contribution, while the influence of the back-gate-inversion charge Q_b is significantly smaller. Figure 5.3 depicts the charge distribution of Q_s and Q_b as a function of V_{bg}. An operation condition with smaller V_{bg} improves the subthreshold swing but reduces the gate overdrive (V_{gs}-V_{th}), because V_{th} increases as demonstrated in Figure 5.1a.

For V_{bg}>0, on the contrary, ϕ_b starts to increase as a function of V_{gs} first and ϕ_s follows, resulting in Q_b domination over Q_s for smaller V_{gs}. Under such a condition, the MOSFET has degraded subthreshold slope, because higher V_{bg} introduces a Q_b-originated current flow deep inside the SOI layer. Here, Q_b is not easily controlled by V_{gs} but rather by V_{bg} through T_{box}. The gate control is kept sufficiently high for a thin SOI-layer

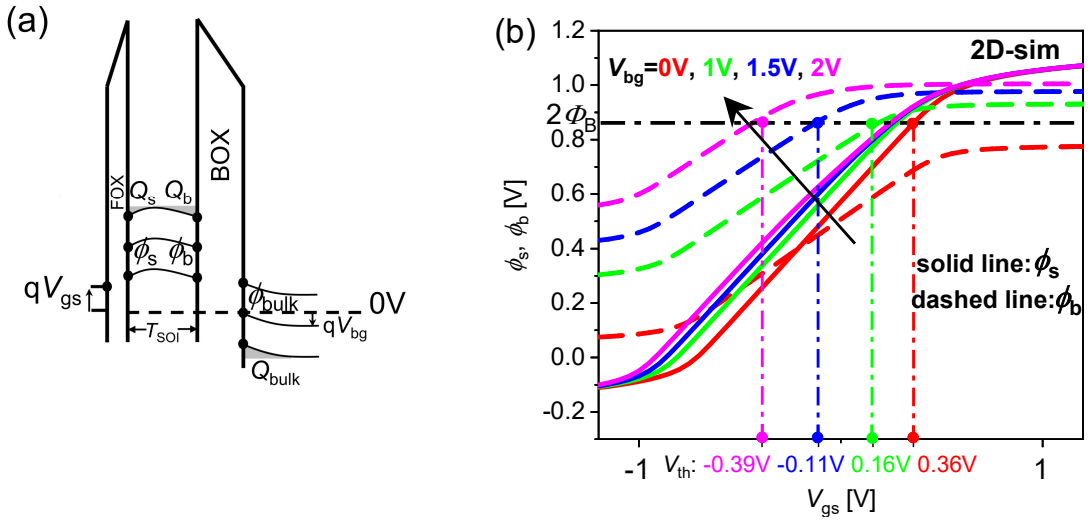

Figure 5.2: (a) Schematic energy distribution with charges along the vertical direction of device, (b)Surface- and back-gate potentials ϕ_s and ϕ_b as a function of V_{gs} for different V_{bg} values. Depending on the operating condition, the main control potential may be interchanged.

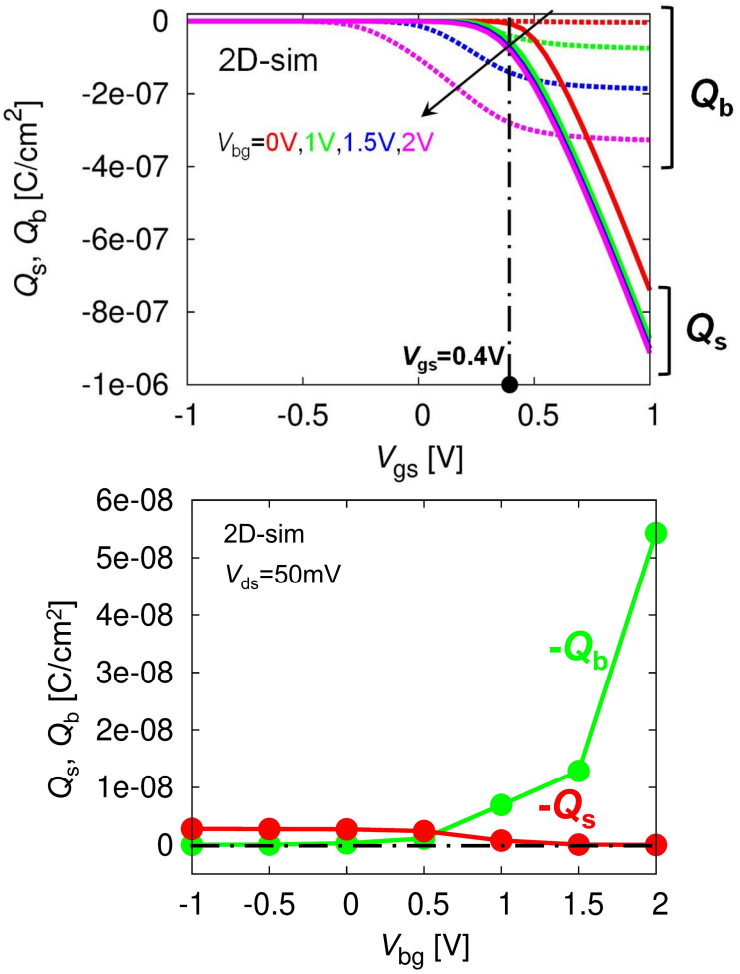

Figure 5.3: Induced charge densities at threshold condition as a function of V_{bg}. Both surface charge Q_s and back-gate charge Q_b contribute to the threshold condition. The Q_b contribution is much higher than that of Q_s under the threshold condition for $V_{bg}>0$, to balance the high Q_{bulk} density induced by V_{bg}.

thickness, however, so that the subthreshold slope degradation is not so obvious in our

studied case.

With the use of HiSIM-DG, a CMOS-inverter circuit (see Figure 5.4a) is investigated to analyze the switching- power loss with different V_{bg} values for high (1V) and low (0.4V) V_{dd} cases. Figure 5.5 shows the schematic explanation of the two different operation conditions with the simulated I_{ds}-V_{gs} characteristics, depicted in Figure 5.1a. As demonstrated, the voltage range of both $0 \leq V_{gs} \leq 1$V and $0 \leq V_{gs} \leq 0.4$V becomes insufficient to ensure lower static-power loss at higher V_{bg}. Thus, upper and lower limits of the gate-input pulse are scaled up and down by an input-voltage scaling ΔV_{in}, respectively, so that switching can complete while leakage currents are negligible, as shown in Figure 5.4b. Figure 5.6 depicts the power loss as a function of ΔV_{in} at low V_{dd}, separately for the switching-power loss (Figure 5.6a) and the static-power loss (Figure 5.6b). Even though the switching-power loss is only lightly dependent on ΔV_{in}, the static loss can be reduced drastically by adjusting ΔV_{in} for such a CMOS-inverter circuit.

The ΔV_{in} value is fixed to 0.6V hereafter to limit the static loss below 0.2μW, keeping an identical value for any bias conditions of V_{bg}. Figure 5.8 compares the simulated switching performance for the two V_{dd} conditions with various V_{bg} values. As can be seen in Figure 5.7a, higher-voltage operation of V_{dd}=1V, doesn't show any significant delay change for the inverter-output-voltage transition even at higher V_{bg}, which is explainable by the fact, that higher V_{dd} drives the MOSFET to operate far beyond the threshold condition, eliminating the V_{bg} dependence of ϕ_s, i.e., indicating a strong-inversion attainment. Rather, the V_{dd}=1V case is compromised by a substantial switching-power loss, being mostly due to the current increase, caused by the effective V_{gs} increase by ΔV_{in} (see also Figure 5.5). Namely, efficiently controlled ϕ_s (and hence Q_s) improves the transition delay significantly.

For low-voltage operation (V_{dd}=0.4V), the output-voltage transition happens in

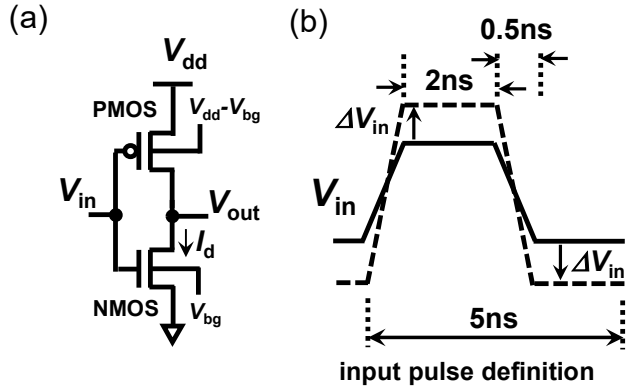

Figure 5.4: (a) Schematic of the studied circuit, (b) Input pulse together with the input-voltage scaling ΔV_{in}.

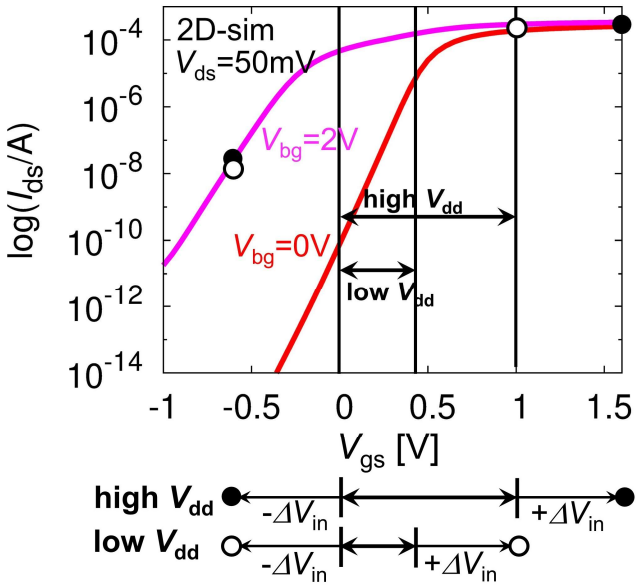

Figure 5.5: Schematic of relationship between the device operation condition and input-voltage scaling with ΔV_{in}.

the sub-threshold region, which provides more efficient V_{gs} control along with stronger V_{bg} dependence. At V_{bg} =0, the contribution of the surface charge Q_s still dominates during the transition. Therefore, relatively large V_{gs} is required, as reflected by the higher delay value in Figure 5.7b. On the contrary, Q_b starts to control the transition as V_{bg} increases, and the transition delay becomes smaller. Therefore, ample opportunities are available for 0V<V_{bg}≤2.0V to achieve optimization with respect to V_{bg}.

As discussed in the previous section, 0V<V_{bg}≤1.0V limits the generation of Q_b (see Figure 5.3), resulting in only small influence on the switching performance. Figure 5.8 illustrates the extracted results for delay time (τ_d) and averaged power loss ($P_{switching\ loss}$), using the simulation results shown Figure 5.7. For the low-V_{dd} case, it is evident that 1V<V_{bg}<1.5V is the optimum window, where delay-time (τ_d) reduction is possible while power-loss increase is kept small. Our investigation reveals that V_{bg} of 1.2V provides the lowest power loss with simultaneously short τ_d.

The results shown in Figures 5.7 and 5.8 are those at fixed ΔV_{in} of 0.6V. However, it is essential for low V_{th} devices, especially with negative V_{th}, to operate additionally with scaled input pulses for realizing an appropriate switching performance. Since the switching loss is not much dependent on ΔV_{in}, ΔV_{in} is optimized only for the static loss. Figure 5.9a depicts the minimum ΔV_{in} values, extracted from the result shown in Figure 5.6, as a function of V_{bg} together with the boundary condition of V_{gs} +ΔV_{in} > V_{th}. This $\Delta V_{in,min}$ is considered as the optimized value in accordance with V_{bg}, demonstrating that such an optimization can be done successfully as depicted in Figure 5.9b. It can be seen,

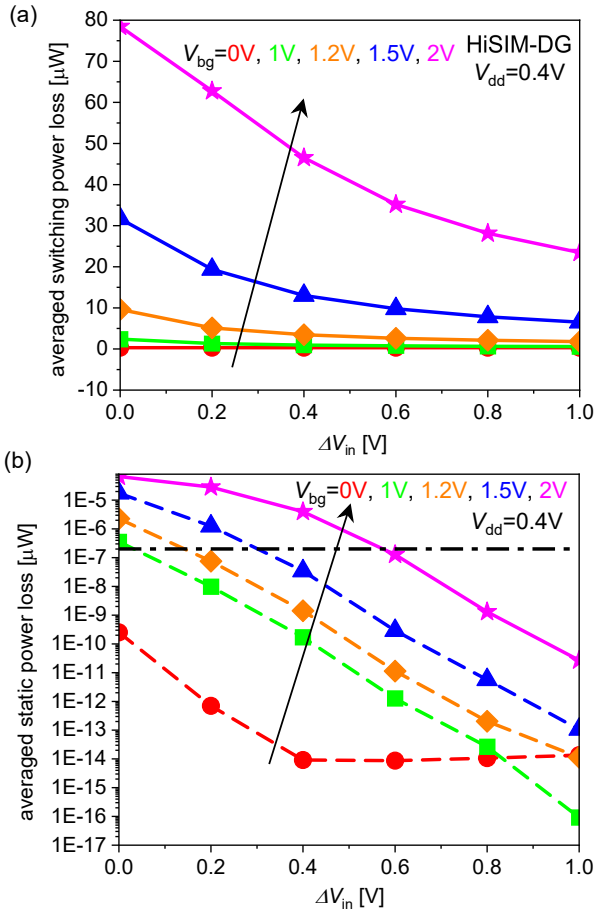

Figure 5.6: (a) The switching-power loss in CMOS-inverter remains weakly coupled with input-pulse scaling (increasing ΔV_{in}), as it doesn't influence the transition region apart from a slight slope deviation. (b) On the other hand, Static power loss reduces significantly for higher ΔV_{in} values. For V_{bg}>1V, without V_{in} scaling, static power loss is relatively high and comparable to the switching-power loss.

that the simultaneous optimization of ΔV_{in} sustains the power loss of the higher input voltage. As can be seen in Figure 5.3, both Q_s and Q_b are contributing for the formation of the threshold condition at 0V<V_{bg}≤1.5V. However, Q_b alone starts to contribute to the switching at V_{bg} =1.2V. Table 5.1 summarizes the scope of DG-structure back-gate biasing for high and low V_{dd} cases.

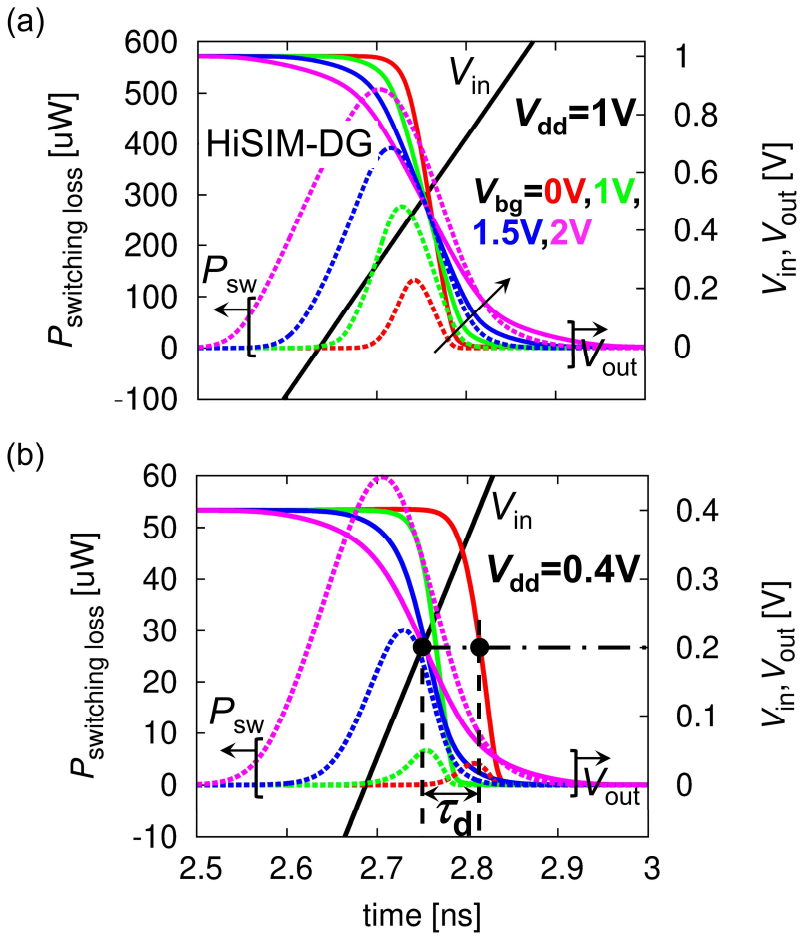

Figure 5.7: (a) Output voltage and switching loss for high V_{dd} of 1V, and (b) for V_{dd} of 0.4V. The transition delay (τ_d) at the switching transition is also depicted together.

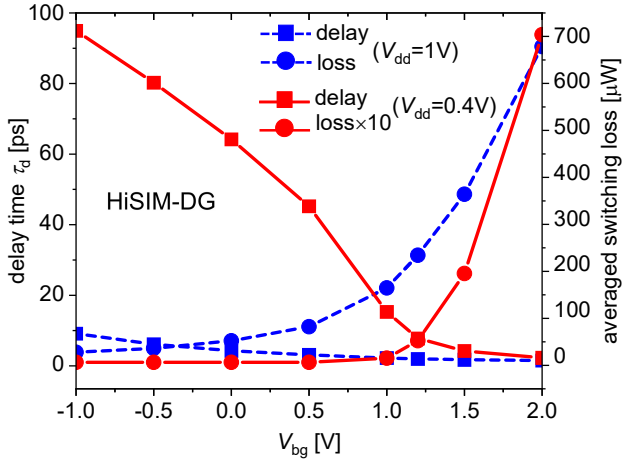

Figure 5.8: Extracted delay time (τ_d) and switching-power loss (P_{sw}) of one time-period as a function of V_{bg} for the CMOS-inverter-circuit studies. For the low-V_{dd} case, power-loss increment is minimal and τ_d improvement is maximum with $V_{bg} \leq 1$. For the high V_{dd} case and larger V_{bg}, the power loss increases significantly while improvement of τ_d is small.

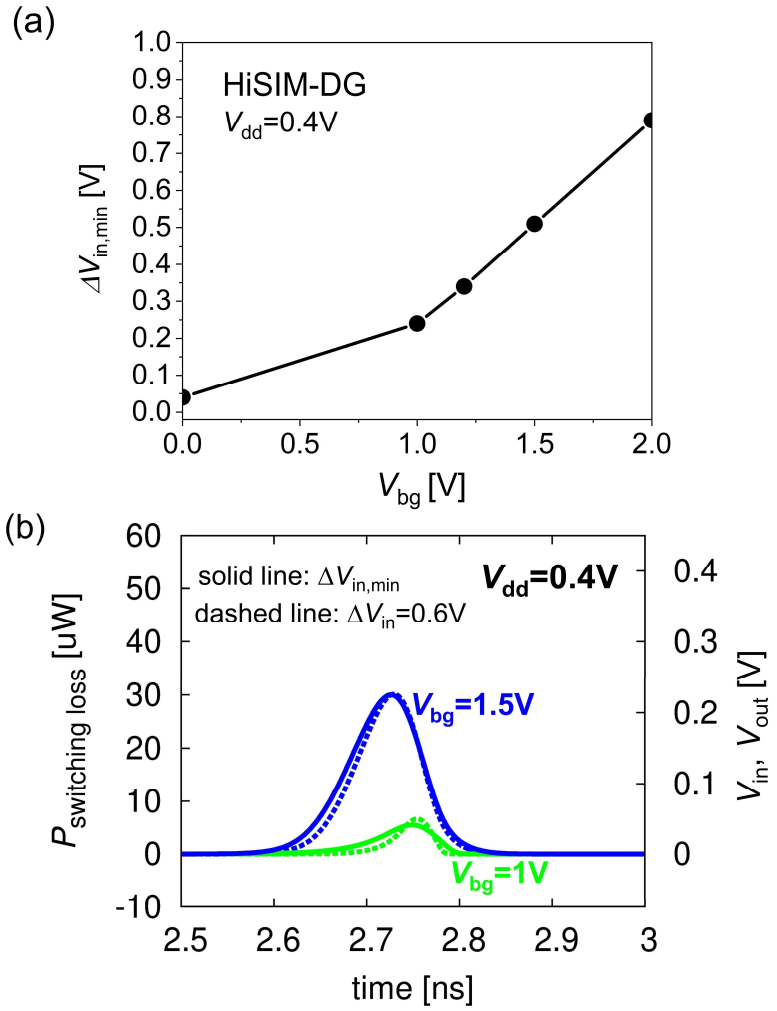

Figure 5.9: (a) Extracted D$V_{in,min}$ from the results shown in Fig. 6 as a function of V_{bg} (b) simulation results of output voltage V_{out} and switching power loss $P_{switching\ loss}$ with the extracted $\Delta V_{in,min}$ values for V_{bg}=1V and 1.5V, which are different for different V_{bg} values as can be seen in Fig. 9a. In spite of ΔV_{in} reduction, no power loss increase is observed.

Table: 5.1 Scope for back-gate biasing in DG-MOSFET

V_{bg}	**-1V to 0V**	**0V to 1.2V**	**1.2V to 2V**
High	• Suitable for low power application although inefficient power-loss scaling. • $Q_s > Q_b$, $Q_{bulk} < 0$		• No latency degradation but power-loss increase • $Q_b > Q_s$, $Q_{bulk} > 0$
Low V_{dd}	• Small power-loss but high latency. • $Q_s > Q_b$, $Q_{bulk} < 0$	• Small power-loss and improved latency. • $Q_s \approx Q_b$, $Q_{bulk} < 0$ • g_m remains high.	• Latency improvement but power-loss increase • $Q_b > Q_s$, $Q_{bulk} > 0$

5.3 Structural Optimization for Low Power Loss

Table: 5.2 Structural scaling parameters

Parameters	Original	Optimized
T_{SOI}	12nm	8nm
T_{BOX}	10nm	6nm

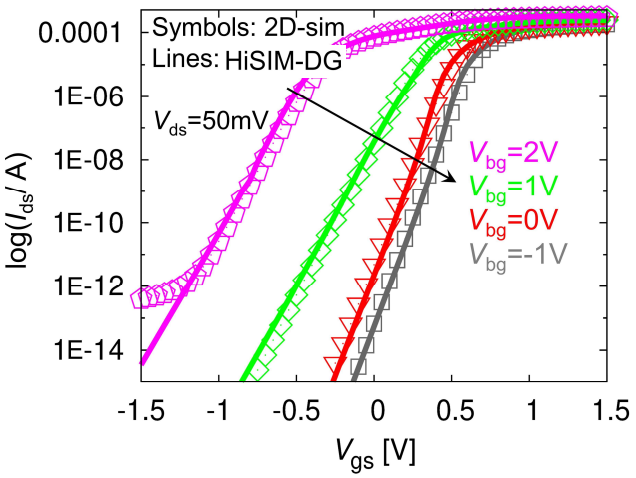

Figure 5.10: I_{ds}-V_{gs} characteristics of optimized structure (T_{FOX}=1.9nm, T_{SOI}=8nm, T_{BOX}=6nm) for different V_{bg} at drain voltage of 50mV. All model-parameter values are kept the same as those shown in Figure 5.1b, except for the device-structure parameters.

For further improvement of the power loss, the validity of a structural optimization is investigated. To reduce the switching loss, V_{gs} controllability must be improved. At the same time the Q_b contribution must be increased to enable the low voltage application. To fulfil these contradicting requirements, T_{BOX} is reduced together with T_{SOI}. The modifications are summarized in Table 5.2, where the rest of the overall device size is kept the same. I_{ds}-V_{gs} characteristics for the optimized structure are depicted in Figure 5.10 and show good agreement with 2D-simulation results, using identical model parameters as for the original structure (see Figure 5.1a), except for the device-structure parameters. This verifies the accuracy of the developed model. Figure 5.11 compares the results for the 2 device structures. Down-scaling of the T_{SOI} layer allows Q_b to be decreased due to increased V_{gs} control. Contradictorily, T_{BOX} scaling allows Q_b to be increased. At lower V_{bg} ($0V<V_{bg}\leq1.2V$), the T_{SOI}-scaling contribution dominates over that of T_{BOX} due to the relatively small Q_b (see Figure 5.3), whereas for higher V_{bg} the reverse holds true because Q_b becomes more important. The magnitude of Q_b is strongly dependent on V_{bg} and T_{SOI}. As observed in Figure 5.11a, I_{ds} decreases for the scaled structure with higher V_{th} when $0V<V_{bg}\leq1.2V$. Beyond that, I_{ds} increases with lower V_{th}. Figure 5.12 summarizes the V_{th} values as a function of V_{bg}. The reduction of V_{th} as a

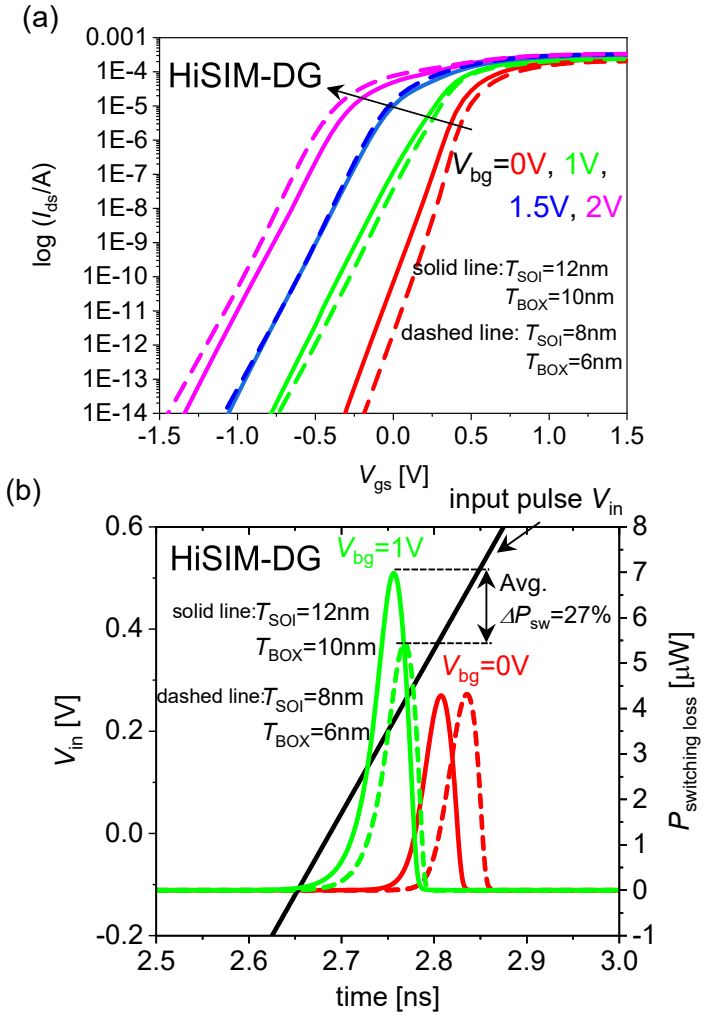

Figure 5.11: (a) Comparison of the calculated I_{ds}-V_{gs} characteristics of the originally studied structure (T_{SOI}=12nm, T_{BOX}=10nm) with a scaled structure (T_{SOI}=8nm, T_{BOX}=6nm). (b) Impact of the device scaling on the switching performance.

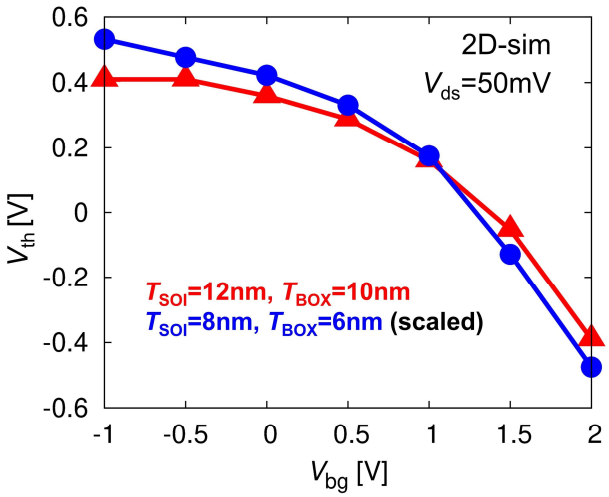

Figure 5.12: Extracted threshold voltage V_{th} from the simulation results shown in Figure 5.10a with scaled device structure in comparison to that with the original structure.

function of V_{bg} is quite drastic for the scaled structure. Hence, in regards of switching-loss improvements, $0V<V_{bg}\leq 1V$ is a comfortable region for circuit operation with scaled devices, without sacrificing a small power loss. Figure 5.11b demonstrates, that a switching-loss reduction of 27% can be achieved with the studied structure scaling at constant V_{bg}=1V, which would not be possible for V_{bg}=0V.

5.4 Summary

The SOI-MOSFET with thin SOI and BOX thicknesses was investigated with HiSIM_DG, to verify the back-gate-voltage V_{bg} contribution for low power operation. It was found, that the relative electrostatic controllability of carriers within the SOI layer by front gate and back gate varies depending on the operating region when increasing V_{bg}. It is further shown, that the back-gate charge Q_b increases as V_{bg} increases, which results in a switching-power-loss increase mostly due to the slow transition in a CMOS inverter. It is shown that the input-voltage scaling is additionally efficient to achieve the desired low-power operation. A specific range of V_{bg} ($1V<V_{bg}\leq 1.5V$ for the studied case), where both performance and power loss are optimal, is validated to be suitable for low-voltage operation. This refers to the condition, where Q_b is still kept under the weak-inversion condition. Within this V_{bg}-bias range, multi-stage cascaded circuits can be operated without ΔV_{in} scaling and with minimal switching-power loss. Structural device optimization in high-density circuits is found to yield 27% lower switching loss for about 30% reduced substrate thicknesses. It is also demonstrated, that the DG-MOSFET optimization can be successfully performed by applying the compact model HiSIM_DG.

Chapter 6

Floating Body Effect in SOI-MOSFET

6.1 Introduction

Silicon-On-Insulator (SOI) MOSFET is one of the most popular device technologies capable of providing high-density, high-performance logic circuits for smaller feature size below 22nm [9]. Compared to bulk-MOSFET, it has lower leakage, better subthreshold slope, less capacitance and superior gate control over the channel. Therefore, it has been utilized for low power applications [71]. Though the FinFET technology realizes the highest integration density, the SOI-MOSFET technology provides the best low power performance among thin film transistors. However, it is known that SOI-MSOFET mostly suffers the history effect causing unstable circuit performance [72]. The purpose of our present investigation is to study feature of the effect and to analyse influence on circuit performances. The device optimization to reduce the history effect is also discussed.

Conventional SOI-MOSFET is a three-terminal device as shown in Figure 6.1b different from the four-terminal bulk MOSFET shown in Fig. 1a. The body is confined within the front oxide (FOX) and the back oxide (BOX). Thus, one of the major structural differences between SOI and bulk MOSFET is that the SOI-MOSFET body is floating due to the BOX isolation. During high drain voltage V_{ds} application, larger than the band-gap, the impact ionization occurs. Though electron-hole pairs are generated due to the impact ionization, electrons are swept away through the drain contact instantaneously for nMOSFET, but holes consume certain time to be discharged through the source contact due to the built-in potential at the source/channel junction. This holes accumulation within the body results in some adverse effects like the kink effect, the history effect, hysteresis, as well as negative conductance. The amount of the accumulated hole density

depends on the operation condition determined by circuits as well as the device structure applied [73].

According to the V_{ds} increase, the impact ionization increases. In turn, strong hole accumulation will take place within the SOI layer. Figure 6.2 shows measured switching-on characteristics for different V_{ds} values by fixing the gate voltage V_{gs} is equal to 1V [74]. Figure 6.2a shows the result for the floating-body case, and Figure 6.2b is that for the body-tie case. It is seen that the drain current increases gradually until it reaches the final vales. The final current values are dependent on V_{ds} values as expected from the conventional MOSFET characteristics. However, the current stays nearly constant for the body-tie case.

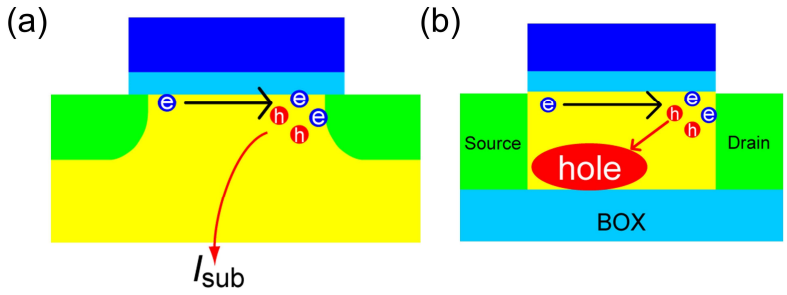

Figure 6.1: MOSFET structures, (a) the bulk type, and (b) the SOI type.

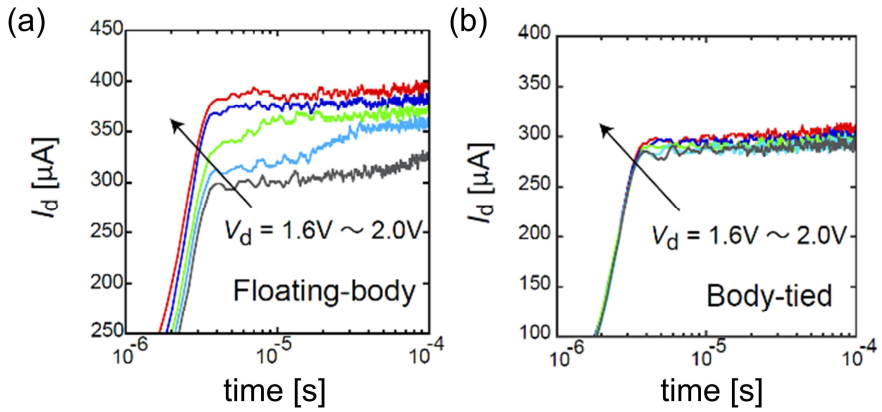

Figure 6.2: (a) Measured switching-on characteristics for different V_{ds} values, where Vgs is switched on to 1V. For comparison measured results for the body-tie type of SOI-MSOFET are depicted in (b).

6.2 Origin of Floating Body Effect

2D numerical device simulation is performed to investigate the impact-ionization effect on SOI nMOSFET [50]. Figure 6.3a and b show 2D potential distributions within the device under V_{gs}=0.2V and 1.2V, respectively, by fixing V_{ds} at 1.2V. The device structure

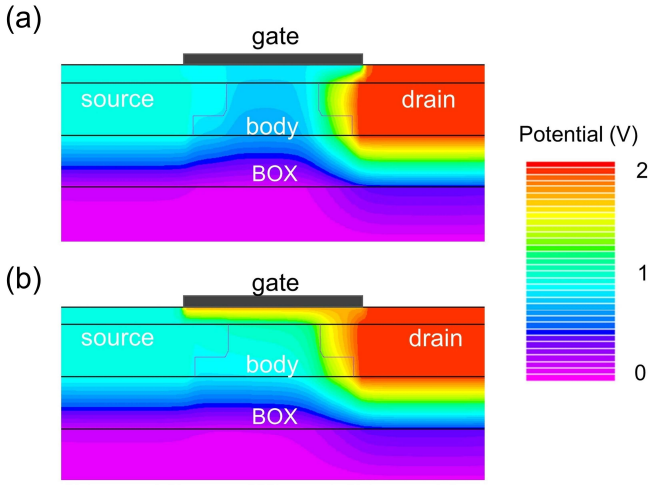

Figure 6.3: 2D Potential distribution (a) for V_{gs}=0.2V and (b) for 1.2V with V_{ds}=1.2V. The SOI-layer thickness T_{SOI} is set to 10nm with the gate oxide of 3.5nm and the BOX of 10nm. The impurity concentration in the SOI layer N_{SOI} is set to $1x10^{17}cm^{-3}$.

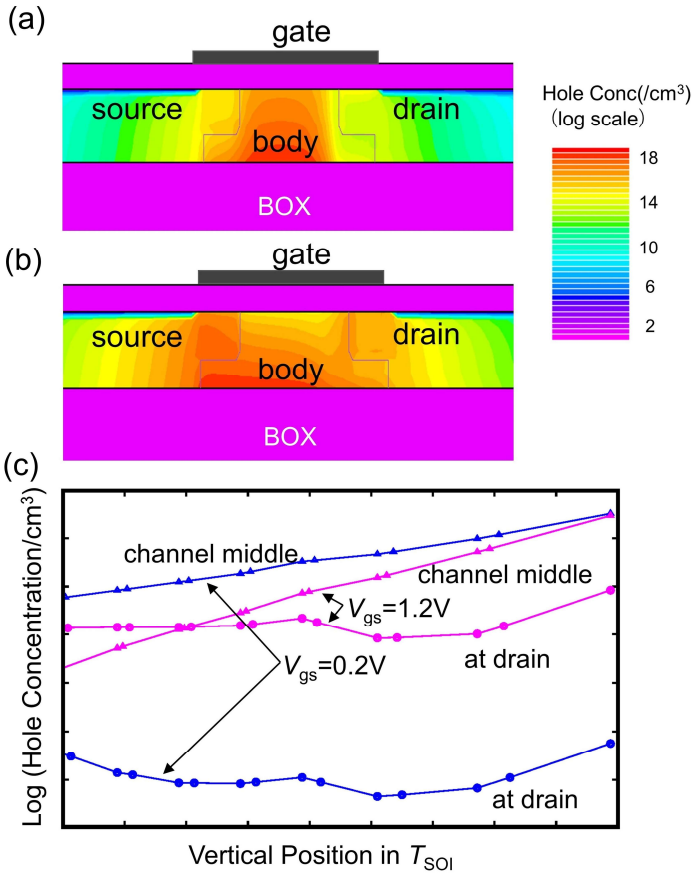

Figure 6.4: The same comparison as shown in Figure 6.3 for hole distributions (a) for V_{gs}=0.2V and (b) for V_{gs}=1.2V by fixing V_{ds}=1.2V. (c) Hole concentrations along the vertical direction in the channel middle and at the drain contact are compared for V_{gs} =0.2V and 1.2V.

applied for the investigation is summarized in the figure caption of Figure 6.3. Figure

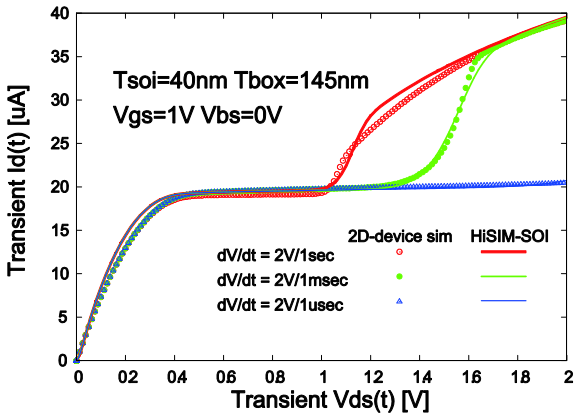

Figure 6.5: Measured I_{ds}-V_{ds} characteristics with different sweep speeds.

6.4a and b show simulated hole distributions within the SOI layer for the two different V_{gs} cases at V_{ds}=1.2V. It is seen that the low hole density is observed in the whole SOI layer for V_{gs} =0.2V, which means that the SOI layer is still partially depleted. On the contrary, the hole density exceeds the impurity concentration of N_{SOI}=1x10^{17}cm^{-3} for the V_{gs} =1.2V case. The hole density is a factor of ten larger than N_{SOI} for the case in the whole SOI layer. This refers to the hole accumulation phenomenon. Figure 6.4c shows the hole distribution along the vertical direction at the channel middle as well as at the drain contact. It is seen that the holes are mostly accumulated at the bottom first, and it extends to the surface as the density becomes high.

Transient features are investigated to characterize the carrier dynamics occurring during switching-on. Figure 6.5 shows measured I_{ds}-V_{ds} characteristics with different sweep speeds of V_{ds}, where the sweep-speed dependent characteristics are observed. If the sweep is very fast (the dV/dt=2V/1μsec case), the impact ionization cannot be happened due to the short bias apply time. On the contrary, the slow sweep (the dV/dt=2V/1sec case) causes sufficient impact ionization to be expected from the applied bias condition. The phenomenon can be understood together with the measurements shown in Figure 6.2. The fast sweep results in no hole generation due to too short time for the impact ionization. This refers to the low V_{ds} in Figure 6.2a. On the contrary, the slow sweep refers to the high V_{ds}, resulting in the high hole generation. Thus, the time required to reach the stable current value is shorter for larger V_{ds} value. This confirms that the hole accumulation requires time, and this is the reason for the phenomenon called the history effect. With use of the measured result, it was found that the time required to complete the accumulation is an inverse function of the substrate current, namely the strength of the impact ionization [74]. We call this time the delay time τ. If the sweep speed is slow (the dV/dt=2V/1sec case), the impact ionization takes place sufficiently

resulting in the accumulated charge density Q_h of the amount observed under the DC measurement. Therefore, the amount of the accumulation charge Q_h as well as the delay time τ must be considered in predicting the SOI-MOSFET circuit performance accurately.

6.4 Modeling Approach

The history effect has been implemented into HiSIM_SOI [39]. The accumulated charge density Q_h is modeled as a function of the substrate current I_{sub}, which is usually measured with the body-tie structure. The final Poisson equation with the Gauss law is written as

$$V_{gs} - V_{fb} = \phi_{s,SOI} - \frac{Q_i + Q_{dep} + Q_{b,SOI} + Q_{s,bulk} + Q_h}{C_{FOX}} \tag{6.1}$$

which is solved iteratively to achieve self-consistent solution of the potential distribution. All physical quantities are determined in [39]. The Q_h charging delay is modeled with the time constant τ, which is implemented in the form as

$$\begin{aligned} &Q_{h,nqs}(t_i) = Q_{h,nqs}(t_{i-1}) \\ &+Q_{h,nqs}(t_{i-1})\frac{\Delta t}{\Delta t + \tau_d}\{(Q_{h,qs}(V(t_i) - Q_{h,nqs}(t_{i-1})\} \end{aligned} \tag{6.2}$$

The calculated potential values are compared to those without Q_h in Figure 6.6a for three potential values (see Figure 6.6b) in comparison to 2D-device simulation results [60]. The definition of the different potentials is given in Figure 6.6b. It is seen that V_{gs} increase causes the surface-potential $\phi_{s,SOI}$ increase as usual. The potential value $\phi_{b,SOI}$ at the bottom of the SOI layer at BOX also increases by the impact ionization contribution. Whereas the potential value $\phi_{s,bulk}$ in the substrate at BOX stays nearly unchanged due to the studied structure with a rather thick BOX of 150nm thickness. Figure 6.7 shows the inversion charge Q_i as a function of V_{ds} for different V_{gs} values. It is seen that the inversion charge Q_i increases for V_{ds} >1V, which is originated by Q_h. Thus, it is seen that the hole accumulation causes current increase. The potential-barrier reduction caused by the V_{gs} increase makes the hole accumulation reduction (see Figure 6.6a). The sudden increase in the drain current I_{ds} observed in Figure 6.5 is called the kink effect, which is the evidence of the hole accumulation causing the history effect. Increase in the bottom of

the SOI layer potential due to the accumulated hole is associated with the reduction in the threshold voltage which in turn increases the drain current.

6.5 Influence of FBE on Circuits

An inverter-chain circuit with several stages is usually investigated for evaluating the history effect mostly for measuring circuit performance accurately [75]. Here we apply a two-stage inverter circuit as depicted in Figure 6.8a to simplify the theoretical investigation. Figure 6.9 shows calculated transient-delay characteristics of the studied circuit. Table 1 summarizes the device parameter values applied for the calculation. The propagation delay is measured as the difference between the input wave form and that of

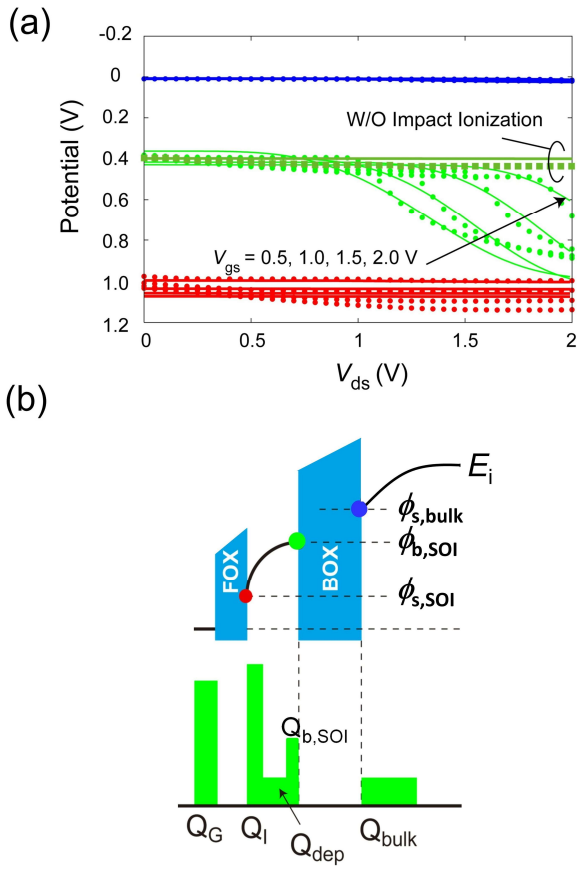

Figure 6.6: (a) Influence of Q_h on important potential values where dotted lines are those of 2D-device simulation results and solid lines are HiSIM calculation results; (b) The definition of the potential values with the history effect. Surface potentials are measured as band bending from intrinsic Fermi energy level E_i at the substrate to the surface. Conduction band and valance band are not shown for simplistic representation. Band offset between the insulator and semiconductor is not to scale to highlight E_i more precisely.

the output as depicted in Figure 6.8b. For comparison two different starting bias conditions are applied as shown in Figure 6.8b. One is the high bias starting (high start)

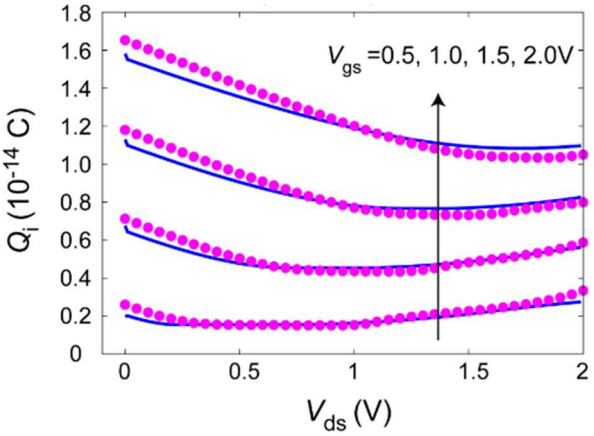

Figure 6.7: 2D device simulation results of the inversion charge Q_i dependence on V_{ds} with the impact ionization for different V_{gs} values. Solid lines are calculation results with HiSIM_SOI.

and the other is the low bias starting (low start). Figure 6.8b determines also four different propagation delays. The simulation results shown in Figure 6.9 consider the history effect with the same amount of Q_h for both nMOSFETs and pMOSFETs. It is seen in Figure 6.9a that the four different propagation delays split into four different values at the beginning of the circuit operation, which merges into two values after a certain time. At the high-start case, nMOSFET and pMOSFET are under the on- and the off-condition, respectively. Therefore, pMOSFET is stressed by V_{DD}, causing the impact ionization. The induced electrons are accumulated within the SOI layer as Q_h. At the low-start condition, on the contrary, holes are accumulated in nMOSFET. The charge accumulation results in improvements of *I-V* characteristics as observed in Figure 6.2 and 6.7. For the high-start case, thus, the electron accumulation in pMOSFET due to the V_{ds} stress at the beginning stage of the circuit operation increases the pMOSFET driving capability, resulting in the reduction of T_{HL} due to the current increase. For the low-start case, on the contrary, the hole accumulation in nMOSFET increases the nMOSFET driving capability, resulting in the reduction of T_{LH}. The reason is that the pMOSFET is responsible for the TpHL case, which is improved by the electron accumulation within the substrate. For the calculation same amount of the Q_h accumulation for both nMOSFET and pMOSFET is assumed. In reality either the pMOSFET or nMOSFET improvement results in the degradation of the opposite device performance in CMOS. Therefore, T_{LH} in the high-start case and T_{HL} in the low-start case are also influenced. Figure 6.9b shows the same calculation results but without the Q_h contribution for comparison. Thus, it is seen that the existence of Q_h is origin of the delay split observed in Figure 6.9a, and the split is reduced as the duration of the circuit operation increases. This means Q_h accumulated at the beginning stage of the circuit operation is discharged during the circuit operation.

To verify the Q_h influence on circuits, the Q_h magnitude is varied. To distinguish the Q_h effect of the nMOSFET and pMOSFET on circuit, the original delay difference of nMOSFET and pMOSFET (see Figure 6.9) is increased by degrading only the pMOSFET feature. For the variation the pMOSFET mobility is decreased by three times. The result is shown in Fig. 10a without the Q_h contribution. Simulation results with the same amount of Q_h applied for the results shown in Figure 6.9a are shown in Figure 6.10b. Additionally Q_h in pMOSFET is varied. It is seen that the analysis obtained by the investigation shown in Figure 6.9a is also confirmed in the results shown in Figure 6.10b, namely the four delays are splitted into four curves. The split is enhanced by increasing Q_h. For pMOSFET, T_{HL} and T_{LH} of high start are mostly influenced and T_{LH} and T_{HL} of low start is calm changed. The T_{HL} and T_{LH} of high start are determined both mostly by pMOSFET, where the device performance is improved by the electron accumulation.

During switching-on -off repetition Q_h increases as well as decreases, depends on the bias condition as well as the time constant τ. Figure 6.11 shows the simulation result, where the charging/discharging time constant τ is reduced by a factor of ten, referring the easy accumulation/dispersion of carriers in the SOI layer. The Q_h amount is kept the same as shown in Figure 6.9. It is seen that the history effect disappears shortly after the circuit operation start. This concludes that the reduction of Q_h is the key to avoid the history effect. To realize the Q_h reduction to reduce T_{SOI} is one possibility [9]. Another possibility is to reduce V_{ds} so that less impact ionization occurs. From this point of view, it can be concluded that the circuitry advantage of SOI-MSOFET can become obvious under the low-power operation.

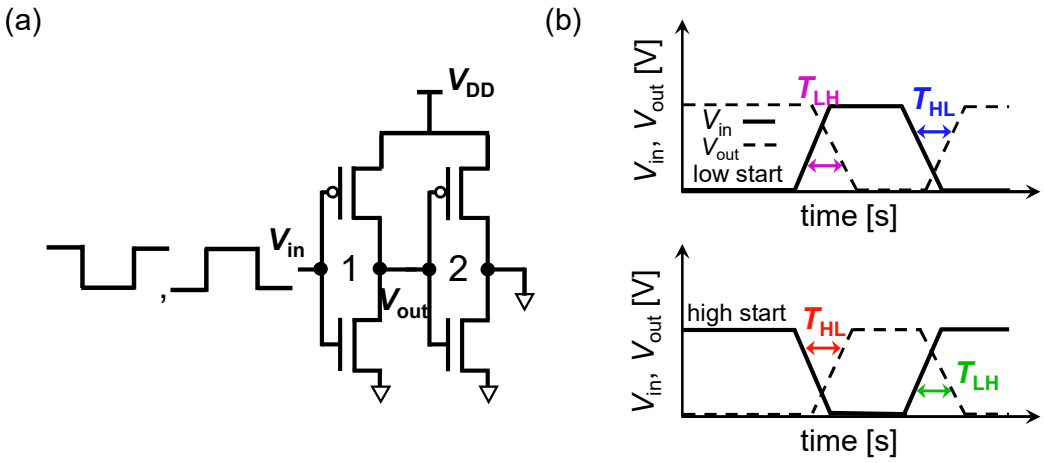

Figure 6.8: (a) Inverter chain circuit studied, and (b) definition of delay measurements.

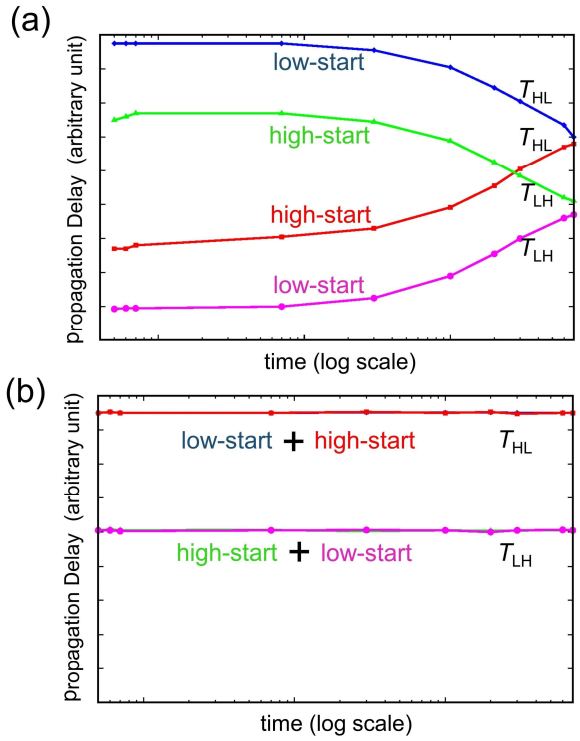

Figure 6.9: (a) Simulation delay characteristics with Q_h both in nMOSFET and pMOSFET, (b) without Q_h.

Table 6.1 Device parameter values applied for the delay simulation.

Parameter name	Parameter value
Front oxide thickness (TFOX)	3.5nm
SOI layer thickness (TSOI)	10nm
Buried oxide thickness (TBOX)	110nm
SOI layer impurity conc. (NSUBS)	$3x10^{17}cm^{-3}$

6.6 Summary

In this work, influence of the history effect on a simple inverter circuit is investigated. The origin of the history effect is modeled by considering the amount of the accumulated charge together with the time constant required for the accumulation. Simulation results with the model reveals that the large amount of the accumulation charge Q_h causes the large history effect, which makes the circuit operation unstable. The time constant increase due to a large amount of Q_h is another origin of an enhanced influence of the history effect. As a conclusion, thin SOI-MOSFET under low-power operation reduce the effect, which brings the most circuitry advantage of SOI-MSOFET.

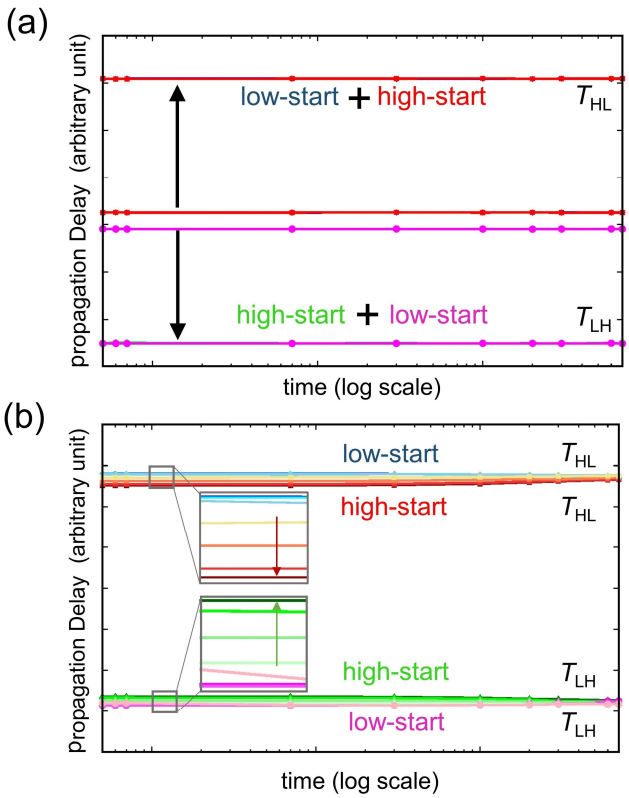

Figure 6.10: Simulation delay characteristics (a) without Q_h, (b) with Q_h, for both nMOSFET and pMOSFET. The Q_h amount only in pMOSFET is varied.

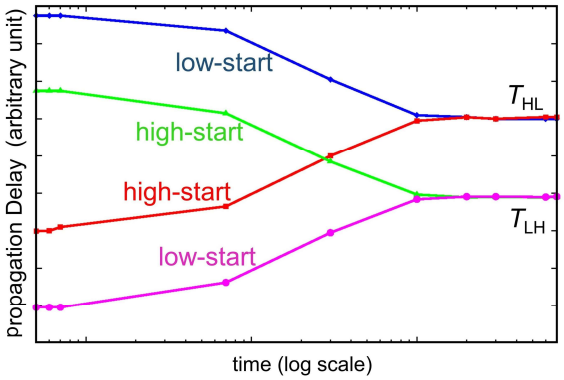

Figure 6.11: Simulation delay characteristics with the same amount of Q_h both in nMOSFET and pMOSFET as those shown in Figure 6.9 but the time constant τ is reduced by a factor of 10.

Chapter 7

Advanced SOI-MOSFET for RF Applications and Its Modeling

7.1 Introduction

Modern cellular technology is shifting its focus from GaAs based High-electron-mobility transistor (HEMT) to Si-based SOI MOSFET technology due to high volume manufacturing advantage because of mature process node. High frequency RF applications (4G, 5G and higher) require highly linear device performance for wide range of frequency spectrum. SOI technology has the ability to maintain high device-linearity due to availability of high-resistive silicon substrate (HR-Si), which bulk CMOS technology lacks by its structural limitation. This facilitates achieving lower crosstalk between active and passive devices in ICs. Figure 7.1 depicts two closely located rectangular metal interconnects, one of which carries high frequency signals, are affected by substrate coupling induced crosstalk due to rather low-resistive substrate. This causes nonlinear feature of upper devices.

Nonlinearity is undesirable in a system chain, because they introduce signal

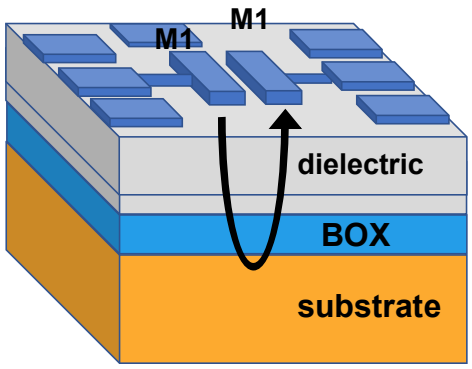

Figure 7.1: Crosstalk between two metal interconnects through common substrate.

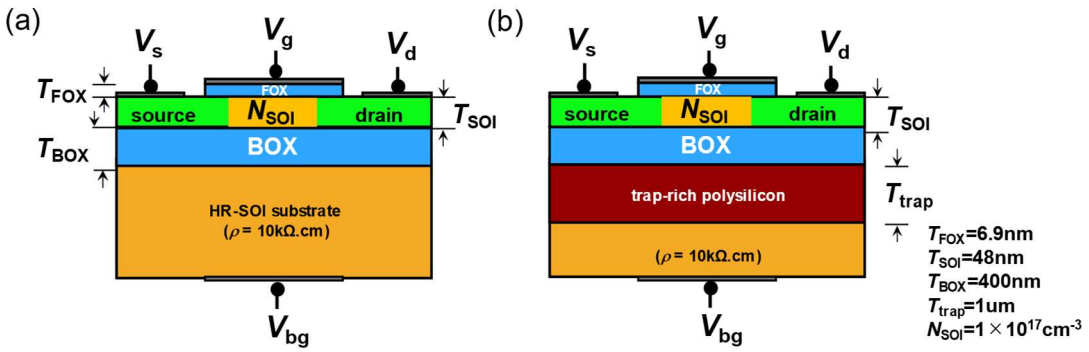

Figure 7.2: Structural description of (a) High resistive (HR) SOI and (b) trap-rich (TR) SOI MOSFET for channel length 0.3um.

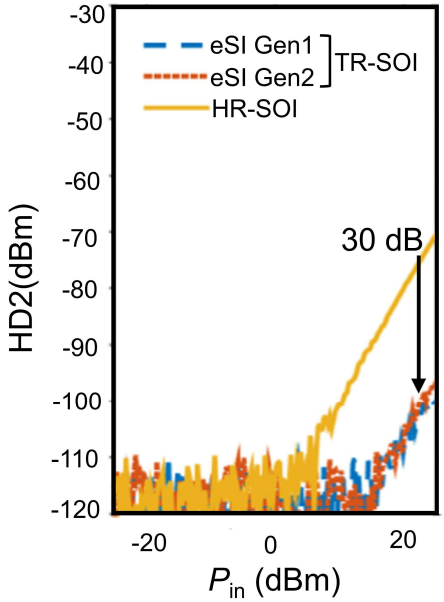

Figure 7.3: Measured 2nd (HD2) harmonic distortions of a crosstalk structure with zero DC substrate bias.

distortion in output waveforms. This results in additional spectral components in the frequency domain with multiple frequencies of original input frequency. This is called harmonic distortion causing entanglement of information. Therefore, stringent linearity specifications are applied to all levels of the RF chip in advanced telecommunication schemes from active devices to the substrate material. For SOI-MOSFET with HR-Si substrate, resistivity remains in the order of 5-10 kΩ.cm. Although highly resistive Si-substrate improves linearity, it still suffers from resistivity lowering effect at the interface between BOX/substrate due to natural high carrier concentration in the substrate. This reduces resistivity by a factor of 10^3–10^6, which is known as parasitic surface conduction (PSC). It has been demonstrated that the most effective method to eradicate PSC is to

introduce a trap-rich polysilicon layer in the substrate at the BOX/substrate interface. This type of SOI layer is referred to as trap-rich (TR)-SOI. The purpose of introducing polysilicon layer is to capture the free carriers responsible for surface conduction and keep substrate nominal high resistivity. Measurement data [76] shown in Figure 7.3 depicts 30dBm reduction in the second harmonic magnitude for TR-Si substrate. Investigations have been performed by Prof. J.P Raskin and his team using SOITEC HR-SOI and TR-SOI substrate to analyze DC and frequency domain characteristics both theoretically and experimentally [77], [78]. The trap-density dependence on the RF-performance improvements has been verified. Although, carrier distribution in the substrate and its frequency dependency of the TR layer under circuit operation is yet to be explored in detail. This chapter of the thesis covers those analysis which clarifies the essence of the TR layer to incorporate more accurate device physics to realize accurate compact model for the technology. For investigation purposes, HiSIM_DG MOSFET model has been utilized together with 2D-device simulation [50]. Device structures for investigation purposes are depicted in Figure 7.2.

7.2 Modeling of Trap Distribution in Polysilicon Layer

Polysilicon is trap enriched polycrystalline material which has been studied for its technology dependent characteristics. It contains grains of different sizes. When two grains of different orientation come closer together, lattice strain is created which changes bond length and angles. This leads to formation of broken bonds. These broken bonds create energy states within bandgap, known as trap states. Depending on the nature of trap-state feature, the trap state is categorized as acceptor-like and donor-like trap state. Acceptor-like trap state remains neutral in nature and becomes negatively charged when

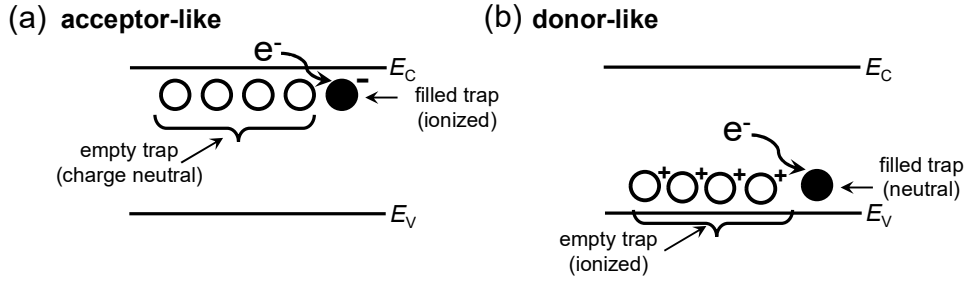

Figure 7.4: (a) Acceptor-like trap ionization state. It remains neutral when empty and becomes negatively charged when occupied with electrons. (b) Donor-like trap ionization state. It remains ionized when empty and becomes charge neutral when occupied with electrons.

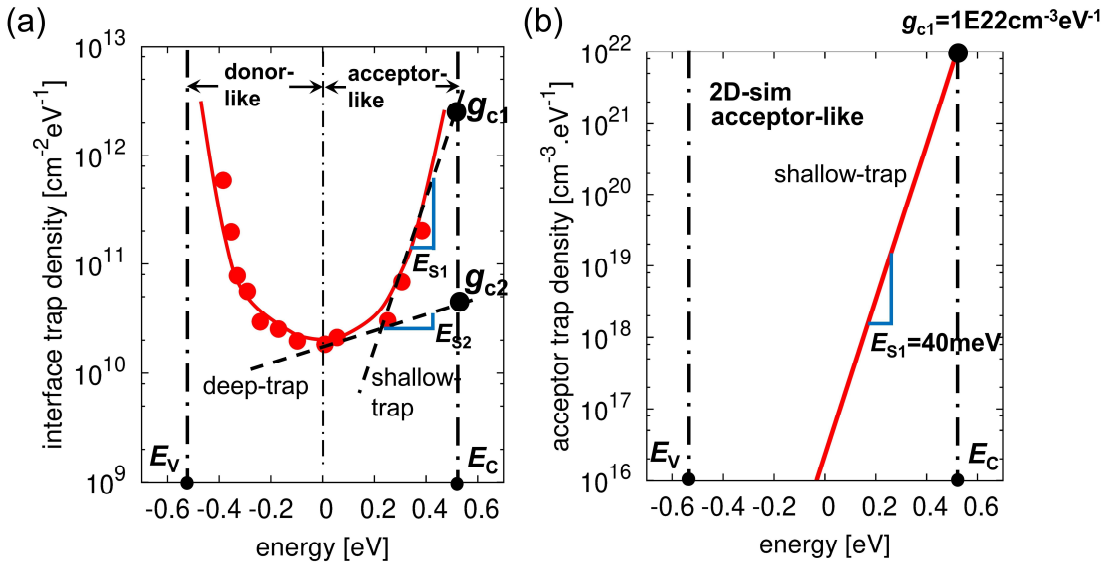

Figure 7.5: (a) Measured interface trap density in Si-SiO_2 interface. Energy states are maximum at band edge and reduces gradually at mid-gap. Depending on the slope, it can be classified in two categories. 1. Shallow-trap 2. Deep-trap. (b) Shallow-trap distribution profile considered for our investigation in 2D-simulation.

filled with electrons (See Figure 7.4). Donor-like trap state remains positively charged in nature, and it becomes neutral when it is filled by electrons. Here our focus is given only on the acceptor-like trap modeling. Figure 7.5a shows measured trap density distribution at Si-SiO_2 interface as a typical bulk-MOS structure [57]. Trap density is maximum at band edges and reduces gradually at midgap. The measured trap-distribution is modeled with two independent distributions, shallow- and deep-level distribution. Here our focus is given only on the acceptor-like trap modeling. The distribution is modeled with two model parameters, g_c denoting conduction-band edge intercept trap density and E_s denoting characteristics of decay energy at which trap density decays within the energy domain. Two trap levels consider different values of g_c and E_s. It is known that the poly silicon trap density is much higher than that of crystal Si, and for simplification only one distribution is considered in modeling as depicted in Figure 7.5b. The trap density reduces exponentially when it moves away from conduction-band edge to midgap, thus the distribution is written as a function of energy E

$$g_A(E) = g_c \exp\left(\frac{E - E_c}{E_s}\right) \tag{7.1}$$

To calculate total trap density N_{trap_A}, trap distribution is multiplied by existing probability function F and is integrated within the bandgap.

$$N_{\text{trap\_A}} = \int_{E_V}^{E_C} g_{\text{A}}(E).F(E,\vec{r})dE \qquad \text{for acceptor-like} \tag{7.2}$$

which leads to an analytical description under an approximation that traps are mostly located at E=E_{f}

$$N_{\text{trap\_A}} = N_0 \exp\left(\frac{E_{\text{f}} - E_{\text{c}}}{E_{\text{s}}}\right) \tag{7.3}$$

$$N_0 = g_{\text{c}} E_{\text{s}} \frac{\frac{kT}{E_{\text{s}}}}{\sin\left(\frac{kT}{E_{\text{s}}}\right)} \tag{7.4}$$

where k and T are the Boltzmann constant and temperate in kelvin, respectively. Total trap charges can be expressed as

$$Q_{\text{trap}} = -q \times N_{\text{trap\_A}} \tag{7.5}$$

Using charge neutrality condition within the device,

$$Q_{\text{g}} + Q_{\text{s}} + Q_{\text{b}} + Q_{\text{dep}} + Q_{\text{bulk}} + Q_{\text{trap}} = 0 \tag{7.6}$$

where Q_{g} denotes gate charge, Q_{s}, Q_{b}, Q_{dep}, Q_{bulk} are front-gate, back-gate, depletion and bulk charge, and Q_{trap} designates trap charge. Each charge distribution within the device is depicted in Figure 7.6. It is seen that all charges are a function of potential distribution along the device.

The Poisson equation, together with the Gauss law, derives the V_{gs} dependency of the total charge induced within semiconductor as

$$V_{\text{gs}} - V_{\text{fb}} - \phi_{\text{s}} = -\frac{Q_{\text{s}} + Q_{\text{b}} + Q_{\text{dep}} + Q_{\text{bulk}} + Q_{\text{trap}}}{C_{\text{FOX}}} \tag{7.7}$$

The potential distribution can be obtained by solving the above equation together with boundary conditions [55], [56].

7.3 Potential and Carrier Distribution for HR- and TR-SOI

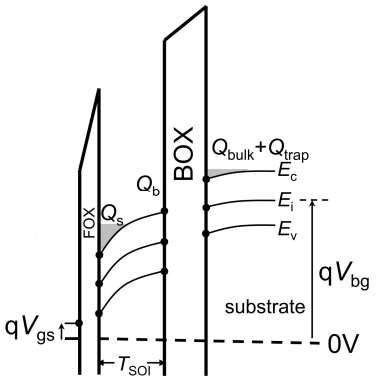

Figure 7.6: Energy distribution perpendicular to the device surface at the channel middle. All the charges combined maintains charge neutrality condition in the device.

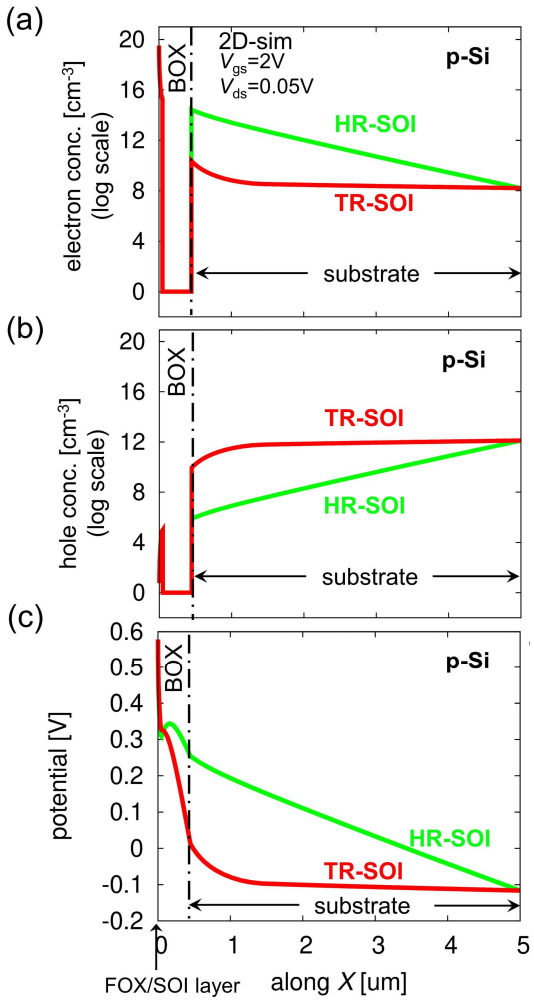

Figure 7.7: (a) electron concentration (b) hole concentration (c) potential distribution along X in substrate for HR-SOI and TR-SOI.

Due to incorporation of trap-rich layer, potential and carrier distribution are influenced significantly. In Figure 7.7a, 2D-simulation result for HR-SOI along device depth direction perpendicular to the channel depicts high density of electron concentration at the BOX/substrate interface to compensate positive charges inside SOI layer. These free electrons contribute to surface conductivity. In case of TR-SOI, free electron concentration is reduced due to carrier trapping within polysilicon layer. Conversely, hole concentration is higher at BOX/substrate interface in case of TR-SOI compared to HR-SOI as seen in Figure 7.7b. This affects the potential distribution as shown in Figure 7.7c. When a small sinusoid signal is applied at the source side of the MOSFET (here add a figure with the small-signal input), existing free electrons at the interface react to this sinusoidal bias variation. Therefore, electron rich PSC layer conductivity becomes a time varying quantity which conducts source-side input signal to the drain side with distortion. This existence of parasitic surface conduction originates different undesired harmonic components of output signal at drain contact. TR-SOI substrate reduces these harmonics with the dismissal of surface conduction at the interface. As seen in the Poisson equation, charge compensation between Q_{trap} and free carrier included in Q_{bulk} is accomplished. As a result of the charge compensation the potential value at the BOX/substrate is reduced, resulting in the improvement of harmonic distortions.

7.4 Fermi-Energy Feature in HR- & TR-SOI

The charge neutrality (Eq. 7.6) describes a balance among charges, and all charges are function of potential distribution (see Figure 7.7c). Here, a new physical quantity to be characterized for calculation is quasi-fermi energy E_f in the TR layer, as seen in the trap-density equation (see Eq. 7.3). For this purpose, 2D-device simulation is performed here. Figure 7.8a shows cross-sectional device structure studied with 2D-device simulation. Two different devices are analyzed with 2D-device simulation under identical bias condition to characterize E_f in TR-SOI for improving RF performance.

1. HR-SOI: substrate without any trap: $g_A(E)=0$.
2. TR-SOI: substrate with trap density $g_A(E)$.

As schematically depicted in Figure 7.8b, Fermi level is at different energy state for HR- and TR-SOI. Below $g_c=1x10^{18}cm^{-3}eV^{-1}$, trap-density is negligibly small to change E_f, and substrate is treated as HR-SOI. Extracted E_f from 2D-simulation shown in Figure 7.8c as a function of g_c, which depicts Fermi level shifts away from conduction band towards midgap as g_c increases. Thus, it can be concluded that E_f is strongly coupled with g_c, the trap density value. At higher g_c probability of occupancy of free electrons is reduced

within energy state between conduction band and midgap.
Fermi energy E_f for polysilicon is described as [79]

$$E_F = E_{i0} + akT \ln\left(\frac{N}{n_i}\right) \tag{7.8}$$

where N is the average active dopant concentration at grain boundaries and n_i is the intrinsic carrier concentration for polysilicon. E_{i0} is the intrinsic Fermi level, and a = 1 for donor-type dopants or - 1 for acceptor-type dopants. From the equation it is expected that E_f reduced as N increases. It is challenging, however, to obtain the values of N and n_i

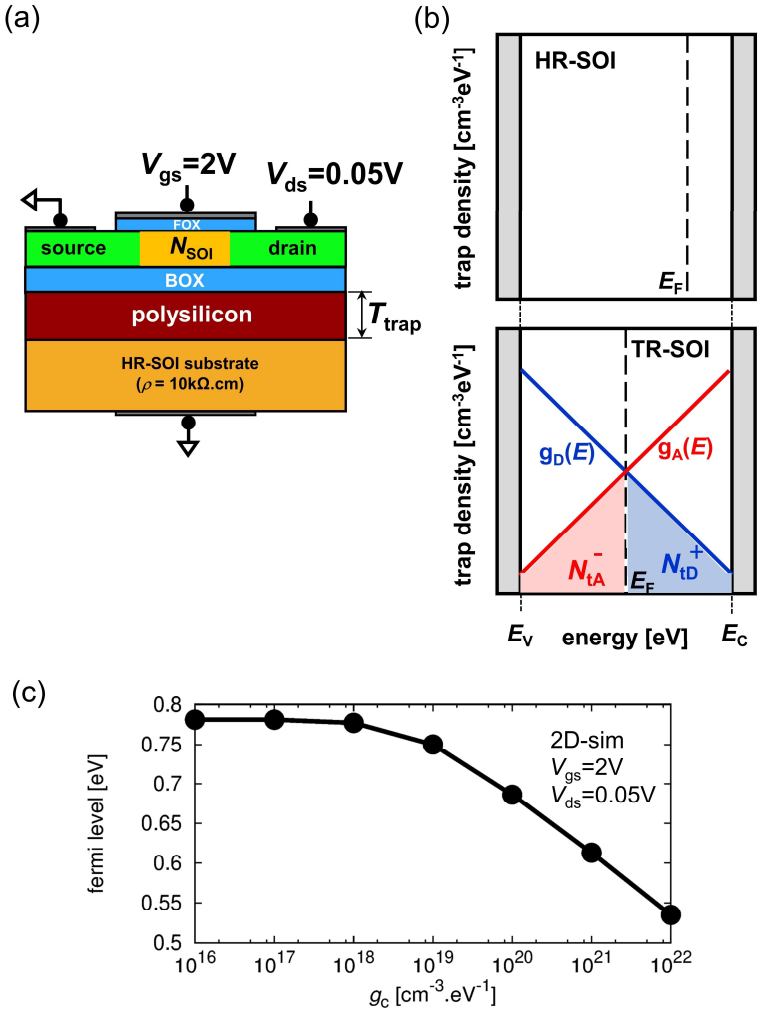

Figure 7.8: (a) RFSOI MOSFET with MOS-Capacitance configuration. (b) Trap-density as a function of band-gap energy. For HR-SOI, fermi-level is closer to conduction band in the substrate. This indicates PSC-layer is formed which reduces substrate resistivity. In case of TR-SOI, fermi-level is very close to midgap, reflecting that free electrons are not induced at the BOX/substrate junction and therefore, nominal resistivity is maintained. (c) Extracted data from 2D-sim of fermi level shift towards midgap for higher values of g_c.

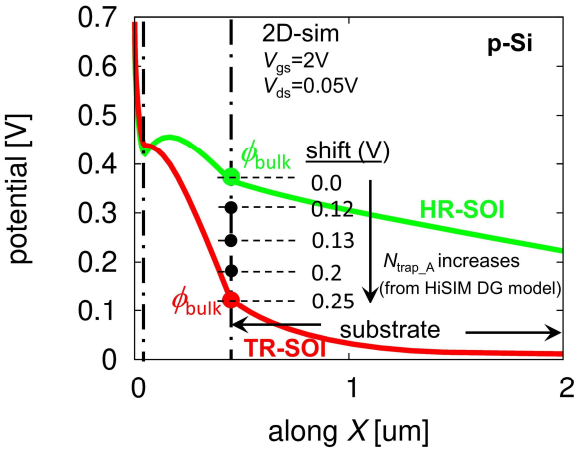

Figure 7.9: ϕ_{bulk} reduces as N_{trap_A} increases (obtained from HiSIM DG MOSFET model).

for polysilicon, because the polysilicon characteristics are strongly dependent on technology. To resolve this issue E_f is treated as model parameter in compact-modeling purpose. Thus using Eq. 7.3, for different values of gc, N_{trap_A} can be calculated, which predicts improvement of RF performances as observed in Fig. 7.3. 2D-device simulation results of E_f are depicted in Fig. 7.8b as an example.

From the measurement data shown in Figure 7.3, higher order harmonic amplitude can be measured for different trap densities in polysilicon layer which show different improvements in frequency domain. Origin of harmonic amplitude is nonlinearity of carrier response to bias variation, where it is known that carrier scattering is the major cause. Due to the carrier scattering, number of carriers varies. Carrier mobility at the BOX/substrate interface is of course affected by Q_{trap}. However, the major cause for reduction of RF performance is the reduction of the carrier concentration within substrate for the TR case. Trap-site increase reduces E_f, resulting in increase of trap density. The increase causes the change of potential distribution. Figure 7.9 demonstrates calculated most sensitive potential values for different trap densities. It is seen that the trap density decreases ϕ_{bulk} potential, which results in reduction of carrier density in bulk Q_{bulk}. It suggests that the new HiSIM_DG captures the physical phenomenon correctly.

7.5 Summary

Crosstalk is the effect caused by neighboring circuits communicating via a common substrate. Crosstalk reduction has been verified for high-resistive silicon substrates (HR-Si). It has been shown that a thin trap-rich polysilicon layer beneath the BOX (Buried Oxide) can reduce crosstalk by capturing free carriers at the BOX/substrate interface

caused by substrate coupling. Reducing free charge carriers reduces carrier scattering and thus lowers undesirable harmonic distortions. The trap charge under the BOX is now consistently included in the Poisson equation, which is solved iteratively within the HiSIM_DG framework. The trap-density dependence on RF-performance improvements has been validated using this improved model.

Chapter 8

Future Perspective

This thesis work will contribute to understanding and exploring next generation thin layer DG transistors and trap rich RFSOI MOSFETs for advanced circuit application.

From my first investigation on "Analytical V_{th} Description under DG Control", developed analytical V_{th} equation is a structural parameter dependent standalone equation which doesn't require any fitting parameter. So, this equation is not only limited to HiSIM DG MOSFET model, but it can also be applied to other MOSFET models such as BSIM and PSP. Therefore, the model is universal and has wider influence on future research.

The old SOI MOSFET models, which ignored back-gate bias dependency for V_{th} description, can be modified with newly developed V_{th} equation with accurate V_{bg} dependence. It will eliminate non-essential parameters required to fit accurate back-gate bias dependence for the old models and enhance computational efficiency.

From the second investigation on "Device Optimization for Low-Power Applications", circuit designer can calibrate operating point for thin layer DG MOSFET to obtain high gate overdrive with efficient parameter extraction. For low power circuit applications (e.g. V_{dd}=0.4V), it will be very encouraging work for future.

From the third investigation on "Advanced SOI-MOSFET for RF Application" developed trap density model is extendable for RFSOI aging analysis considering lower E_s (characteristics decay energy) and g_c (band edge intercept trap density). Additionally, this work will give an insight on trap stability (trapping and de-trapping) and its influence on MOSFET transient characteristics.

Chapter 9

Conclusions

In this thesis, the HiSIM_DG compact model has been improved by investigating new device physics induced by new device technologies on following aspects:

1. Modeling and observation of Dual-Gate MOSFET characteristics important for low voltage applications and its implementation into HiSIM_DG and investigation of circuits-performance improvement for low power applications.
2. RF-performance improvements with a new SOI-MOSFET technology suppressing non-linear effect induced by crosstalk.

Chapter 1:
This chapter focuses on history of transistor invention and motivation of my research.

Chapter 2:
In this chapter SOI technology development history is described. Additionally, it includes how SOI MOSFET has evolved to multi-gate MOSFET generation.

Chapter 3:
This chapter highlights importance of compact modeling along with different compact models for bulk and SOI MOSFET.

Chapter 4:
In this chapter focus has been given to figure out contribution of induced charges under threshold condition of Dual-Gate MOSFETs. Analytical threshold voltage V_{th} description has been developed for thin-layer SOI-MOSFET based on the charge distribution written by potential distribution induced within the device. Previously developed V_{th} model didn't include back-gate bias dependency. It has been ignored as back-gate effect is decoupled by the neutral body due to thicker SOI layer. For advanced thin layer structure existing equation is not sufficient to successfully describe threshold condition. The Poisson equation including all charges along with the Gauss law is solved analytically under the

threshold condition, which successfully derives closed form analytical threshold-voltage equation for thin layer Dual-Gate MOSFET for the first time . This equation is based on only device structural parameters and requires no fitting parameters. So, it is applicable universally in stand-alone condition, therefore independent of any compact model. This equation is valid for both thinner and thicker SOI layer. Through the investigation it has been found that the surface-potential values at the front and back gates under the threshold condition are alternatively determining to the V_{th} characteristics for thin-layer SOI-MOSFET generation. Furthermore, it has been confirmed that the threshold condition is met when the potential bending at either the front-gate surface or the back-gate surface reaches $2\Phi_B$ ($\Phi_B = 2\beta^{-1}\ln(N_{SOI}/n_i)$, determined by device parameter values). When the major gate predominates the device control, it reaches even to $1.1x2\Phi_B$ to dominate over the minor gate control. The developed closed form equation describes even exchange bias condition, when dominating control gate is exchanged. Thus, the developed analytical model can be used for both device optimization and circuit design. For a particular back-gate biasing of V_{bg0}, flat-band condition at the back gate is attained, which refers to $Q_{bulk}=0$. This value provides very important information for V_{bg} value to achieve efficient V_{th} reduction for low-power applications (e.g. $V_{dd}=0.4V$). Namely, for the V_{bg} value larger than V_{bg0} efficient V_{th} reduction is realized. The closed form V_{bg0} equation is dependent only on structural parameters T_{BOX} and T_{SOI}. By reducing T_{BOX} and increasing T_{SOI}, V_{th} reduction efficiency can be improved further.

Chapter 5:

The developed model has been verified for low-power applications with the DG-MOSFET technology. Although, $V_{bg}>V_{bg0}$ is suitable for low voltage application, there is a limit up to which back-gate bias voltage can be increased without significant power-dissipation increase in real circuits. It is demonstrated with a CMOS inverter circuit. The optimized operating condition is shown to keep the back-gate charge Q_b under the weak-inversion condition. A specific range of V_{bg} ($V_{bg0}<V_{bg}\leq V_{bg1}$), where both performance and power loss are optimal, is validated to be suitable for the purpose. It is also demonstrated that an input-voltage optimization accompanies the back-gate-voltage optimization, sustaining the optimized low power loss with low input voltage. Circuit-performance improvement of 27% by about 30% reduction of SOI-layer thickness, while keeping switching-power loss small, is also verified.

Chapter 6:

Despite the SOI MOSFET structure being well suited to low power applications, the

history effect is observed due to floating-body effect, where carriers are dynamically accumulated within the SOI layer during circuit operation. Influence of the history effect on a simple inverter circuit is investigated using the HiSIM_SOI model. HiSIM_SOI simulation results show that larger accumulation charge Q_h causes a large history effect, making the circuit operation unstable. The reason is that time constant for charging and discharging of impact ionization generated charges is much longer than circuit operation cycle, responsible for the circuit-operation instability.

Chapter 7:

Although the SOI technology suffers from some of its limitations such as the floating body effect, it is still considered to be the best candidate for reducing crosstalk in RF applications. The monolithic integration technology has been realizing integration of different circuit blocks on the common substrate, which causes change in carrier dynamics within the common substrate, called crosstalk. Reduction of the crosstalk is a major concern for RF circuits which has been verified for high-resistive silicon substrate (HR-Si). It has been demonstrated that thin trap-rich polysilicon layer underneath the BOX (Buried Oxide) can improve the crosstalk influence by capturing free carriers in the BOX/substrate interface induced by substrate coupling, origin of the crosstalk. Reducing free charge carriers lowers carrier scattering, therefore lowers undesired harmonic distortions. For modeling the trap charge under the BOX has been newly included in the Poisson equation in a consistent way, which is solved iteratively within the HiSIM_DG framework. Using this improved model, trap-density dependence on the RF-performance improvements has been validated. The improved HiSIM_DG model is under investigation to achieve high performance RF circuit design by optimizing trap density characteristics.

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(1) Analytical V_{th} Modeling for Dual-Gate MOSFETs with Independent Gate Control.
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