論文の要旨
（Thesis Summary）

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論文題目(Thesis Title)
Compact Modeling of Dual-Gate-Control Mechanism in Thin-Layer-MOSFETs for Advanced Circuit Applications
(高性能回路設計に向けた薄膜 MOSFET におけるデュアルゲート制御機構のコンパクトモデル開発)

In this thesis, the HiSIM_DG compact model has been improved by investigating new device physics induced by new device technologies on following aspects:

1. Modeling and observation of Dual-Gate MOSFET characteristics important for low voltage applications and its implementation into HiSIM_DG and investigation of circuits-performance improvement for low power applications.
2. RF-performance improvements with a new SOI-MOSFET technology suppressing non-linear effect induced by crosstalk.

Chapter 1:
This chapter focuses on history of transistor invention and motivation of my research.

Chapter 2:
In this chapter SOI technology development history is described. Additionally, it includes how SOI MOSFET has evolved to multi-gate MOSFET generation.

Chapter 3:
This chapter highlights importance of compact modeling along with different compact models for bulk and SOI MOSFET.

Chapter 4:
In this chapter focus has been given to figure out contribution of induced charges under threshold condition of Dual-Gate MOSFETs. Analytical threshold voltage V_{th} description has been developed for thin-layer SOI-MOSFET based on the charge distribution written by potential distribution induced within the device. Previously developed V_{th} model didn't include back-gate bias dependency. It has been ignored as back-gate effect is decoupled by the neutral body due to thicker SOI layer. For advanced thin layer structure existing equation is not sufficient to successfully describe threshold condition. The Poisson equation including all charges along with the Gauss law is solved analytically under the threshold condition, which successfully derives closed form analytical threshold-voltage equation for thin layer Dual-Gate MOSFET for the first time . This equation is based on only device structural parameters and requires no fitting parameters. So, it is applicable universally in stand-alone condition, therefore independent of any compact model. This equation is valid for both thinner and thicker SOI layer. Through the investigation it has been found that the surface-potential values at the front and back gates under the threshold condition are alternatively determining to the V_{th} characteristics for thin-layer SOI-MOSFET generation. Furthermore, it has been confirmed that the threshold condition is met when the potential bending at either the front-gate surface or the back-gate surface reaches $2\Phi_B$ ($\Phi_B = 2\beta^{-1}\ln(N_{SOI}/n_i)$, determined by device parameter values). When the major gate predominates the device control, it reaches even to $1.1x2\Phi_B$ to dominate over the minor gate control. The developed closed form equation describes even exchange bias condition, when dominating control gate is exchanged. Thus, the developed analytical model can be used for both device optimization and circuit design. For a particular back-gate biasing of V_{bg0}, flat-band condition at the back gate is attained, which refers to Q_{bulk}=0. This value provides very important information for V_{bg} value to achieve efficient V_{th}

reduction for low-power applications (e.g. V_{dd}=0.4V). Namely, for the V_{bg} value larger than V_{bg0} efficient V_{th} reduction is realized. The closed form V_{bg0} equation is dependent only on structural parameters T_{BOX} and T_{SOI}. By reducing T_{BOX} and increasing T_{SOI}, V_{th} reduction efficiency can be improved further.

Chapter 5:
The developed model has been verified for low-power applications with the DG-MOSFET technology. Although, $V_{bg}>V_{bg0}$ is suitable for low voltage application, there is a limit up to which back-gate bias voltage can be increased without significant power-dissipation increase in real circuits. It is demonstrated with a CMOS inverter circuit. The optimized operating condition is shown to keep the back-gate charge Q_b under the weak-inversion condition. A specific range of V_{bg} ($V_{bg0}<V_{bg}\leq V_{bg1}$), where both performance and power loss are optimal, is validated to be suitable for the purpose. It is also demonstrated that an input-voltage optimization accompanies the back-gate-voltage optimization, sustaining the optimized low power loss with low input voltage. Circuit-performance improvement of 27% by about 30% reduction of SOI-layer thickness, while keeping switching-power loss small, is also verified.

Chapter 6:
Despite the SOI MOSFET structure being well suited to low power applications, the history effect is observed due to floating-body effect, where carriers are dynamically accumulated within the SOI layer during circuit operation. Influence of the history effect on a simple inverter circuit is investigated using the HiSIM_SOI model. HiSIM_SOI simulation results show that larger accumulation charge Q_h causes a large history effect, making the circuit operation unstable. The reason is that time constant for charging and discharging of impact ionization generated charges is much longer than circuit operation cycle, responsible for the circuit-operation instability.

Chapter 7:
Although the SOI technology suffers from some of its limitations such as the floating body effect, it is still considered to be the best candidate for reducing crosstalk in RF applications. The monolithic integration technology has been realizing integration of different circuit blocks on the common substrate, which causes change in carrier dynamics within the common substrate, called crosstalk. Reduction of the crosstalk is a major concern for RF circuits which has been verified for high-resistive silicon substrate (HR-Si). It has been demonstrated that thin trap-rich polysilicon layer underneath the BOX (Buried Oxide) can improve the crosstalk influence by capturing free carriers in the BOX/substrate interface induced by substrate coupling, origin of the crosstalk. Reducing free charge carriers lowers carrier scattering, therefore lowers undesired harmonic distortions. For modeling the trap charge under the BOX has been newly included in the Poisson equation in a consistent way, which is solved iteratively within the HiSIM_DG framework. Using this improved model, trap-density dependence on the RF-performance improvements has been validated. The improved HiSIM_DG model is under investigation to achieve high performance RF circuit design by optimizing trap density characteristics.