博 士 論 文
（Doctoral Thesis）

Investigation on the Mechanism of Millisecond Solid Phase Crystallization of Silicon Films Formed by Micro-Thermal-Plasma-Jet and Their Application to Bottom-Gate Thin Film Transistors

（大気圧マイクロ熱プラズマジェット照射によるシリコン薄膜のミリ秒結晶化メカニズムの解明とボトムゲート型薄膜トランジスタへの応用）

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Chapter 1

Introduction

1.1. Background

1.1.1. Introduction to thin film transistors [1,2,3]

A thin film transistor (TFT) is a key technology for developing active-matrix flat panel displays (AMFPDs). It is a special type of field effect transistor formed by placing thin films of the dielectric layer as well as an active semiconductor layer and metallic contacts onto a supporting substrate [1,2,3].

Thin film transistor differs from metal oxide semiconductor field effect transistor (MOSFET) in certain way. Firstly, TFT works in accumulation layer while MOSFET works under inversion layer. Secondly, TFT is amorphous in nature as compared to MOSFET, which is crystalline in nature. Thirdly, TFT is undoped while MOSFET is mostly Si-doped [1]. The applied gate voltage (V_G) controls the electrons flow from source to drain. For positive gate voltage, electrons attract towards the bottom side of the semiconductor layer and conduct a channel. Then, the voltage applied between the two terminals results in current flow. The current flow occurs from drain to source.

Thin film transistor can be worked in depletion mode or enhancement mode depending on whether it requires a gate voltage to induce the channel conduction. When no gate voltage is applied, the channel conductance is low for enhanced mode of operation. Therefore, a low carrier density in the channel is essential to achieve this mode. A channel has to be induced in case of enhancement mode. In this mode, channel enhances on increasing the gate source voltage. Then applying voltage between the drain and source terminals causes the drain current to flow. While in case of depletion mode, if we apply the drain source voltage, the drain current will flow for zero gate source voltage. In this type of MOSFET, there is an implanted channel[1].

Based on position of the electrodes, we can classify to four basis configurations of TFT as: top gate bottom contact, top gate top contact, bottom gate top contact, and bottom gate bottom contact. Although using the exact same materials, different TFT structures can display

quite different device characteristics. The illustrations of TFT configurations are shown in Fig. 1.1.

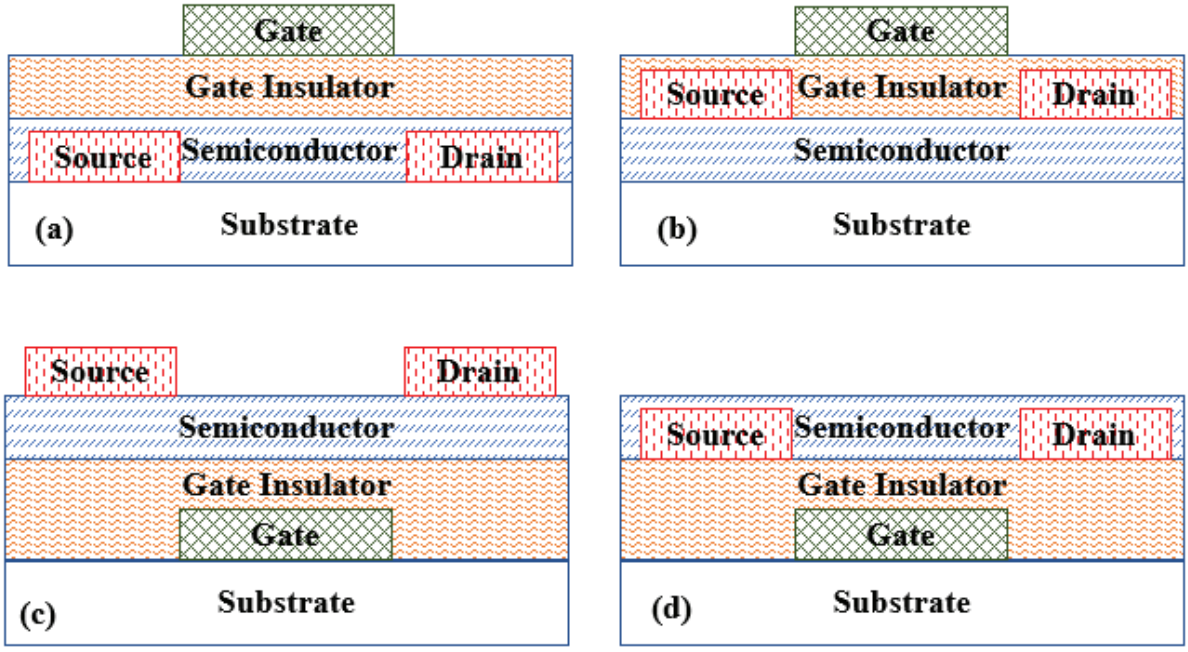

Fig. 1.1. TFT configuration: (a) top gate bottom contact, (b) top gate top contact, (c) bottom gate top contact, and (d) bottom gate bottom contact.

Different processes taken for the TFT fabrication typically determines the selection of a particular structure. The deposition of semiconductor channel layer is firstly made in coplanar top gate structure, while deposition on insulator layer is firstly made in the bottom gate structure. Both of them can fabricate in self-aligned structure, therefore the parasitic overlap capacitance between the gate and source/drain terminals is reduced. However, bottom gate structure needs smaller masks number for photolithography process. As a result, in view of mass production, it will help to reduce the production's cost.

There are two common bottom-gate TFT structures as back-channel-etched (BCE) and etch-stop (ES). These have different fabrication processes which is discussed below. Figure 1.2. shows an example of the main steps in fabricating BCE hydrogenated amorphous silicon (a-Si:H) TFT. The first stage is gate formation: metal deposition, photolithography and etching

by using mask M1. The gate is coated by a stack of three consecutively deposited films of a-SiN_x : H, intrinsic a-Si:H, and doped a-Si:H by using plasma enhanced chemical vapor deposition (PECVD). The film thicknesses for commercial TFTs are typically 300 nm a- SiN_x : H, 200 nm intrinsic a-Si:H, and 50 nm doped a-Si:H [(4)]. In the second patterning stage, M2, the triple stack is defined into the individual TFT islands. Next is the deposition of the source and drain contact metals and photolithography by mask stage M3. The gate is used as an etch mask to remove the doped layer from those areas of the TFT island stack where it is not protected by the metal. The fabrication process is completed by the deposition of a final capping/passivation layer of a-SiN_x : H, which is patterned by mask M4 into contact holes down to the source, drain and gate pads. In summary, the BCE process consists of four mask stages, two PECVD depositions, and two metal sputter deposition stages [(2)].

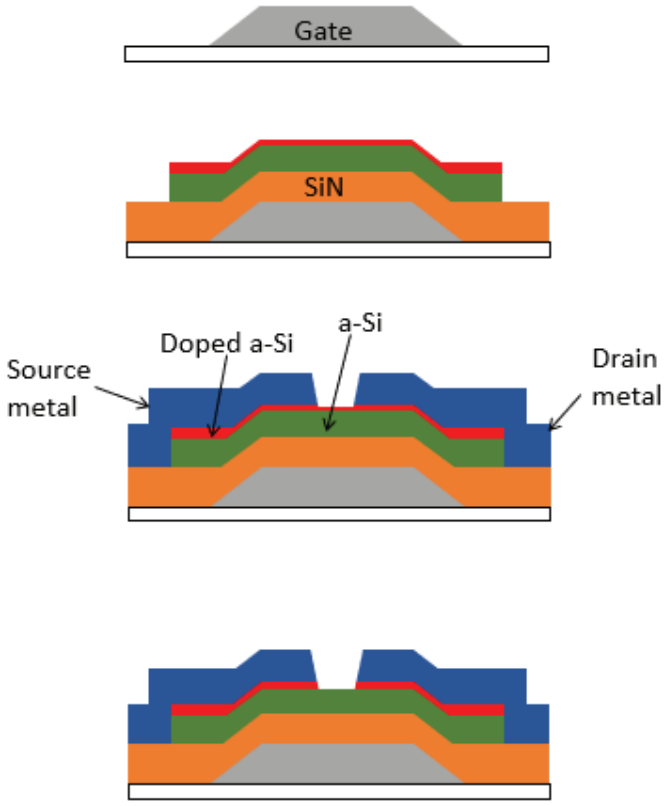

Fig. 1.2. Illustration of main steps in BCE a-Si:H TFT fabrication.

Similarly, Fig. 1.3 shows an example of the main steps in ES a-Si:H TFT fabrication. The main difference between two structure is the present of an a-SiN_x : H pack above the edges of the doped regions. It gives better etch selectivity between the etching of the doped region and the underlying a-SiN_x : H, therefore avoiding the need to use a critical etching time. However, by using this way, the fabrication process is more complex. In summary, the ES process requires 5 mask stages, and three PECVD depositions. It is clear that, providing the back channel etch is well controlled, the BCE process is simpler, with fewer steps. As the consequence, it can take higher manufacturing throughput and lower overall cost and is extensively implemented in production facilities [(2)].

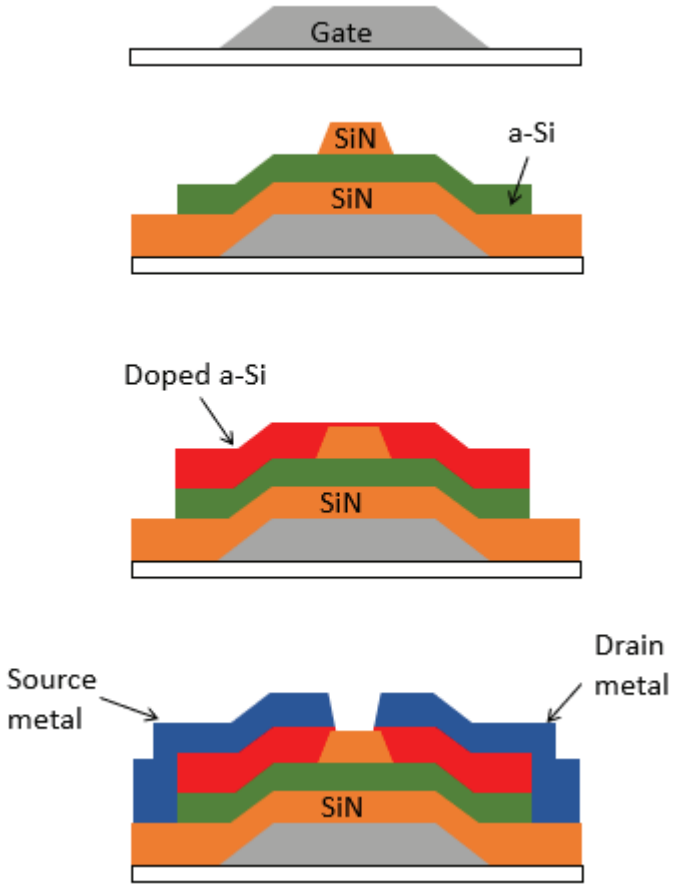

Fig. 1.3. Illustration of main steps in ES a-Si:H TFT fabrication.

1.1.2. Review about conventional TFT channel's material

In the past several years, the TFT technology has progressed intensely, especially in the low temperature, large-area, high throughput fabrication process [2]. To date, difference types of TFTs with the improved mobility, novel structures or flexible material properties have been reported for application in displays, sensors, imagers, detectors, flexible electronics, etc [2]. In this section, we will review some conventional TFT channel's materials.

1.1.2.1.Hydrogenated amorphous silicon

Hydrogenated amorphous silicon (a-Si:H) is an alloy of Si with ~10% hydrogen. Hydrogen plays a key role both in defect passivation within the material, by reducing the dangling bond density from ~ 10^{20} cm^{-3}, in H-free a-Si, to ~ 10^{16} cm^{-3} [5] and in the a-Si:H deposition process itself.

Hydrogenated amorphous silicon is well suited for active-matrix liquid crystal displays (AMLCDs) because it is easy to deposit over large areas at low temperature that are fully compatible with glass or plastic substrates by using plasma enhanced chemical vapor deposition (PECVD). Because of a high dark resistivity, it makes TFTs having low leakage currents. It can be made *n*- or *p* – doped a-Si:H, therefore the fabrication of low-resistance contacts is available. The processing of a-Si:H TFTs is similar to the crystalline silicon metal oxide-semiconductor (MOS) integrated circuited technologies, which make AMLCDs more mature than other technologies, for example organic displays based on light-emitting devices. Finally, a-Si:H technology benefits from the tremendous investment in a-Si:H solar cells made several years ago, and so has become the dominant player in the active-matrix display world. However, its low mobility, < 1 cm^2/Vs,[6,7] is perfectly suitable to TFTs within each pixel but is unsuitable for the faster switching circuits needed for addressing the rows and columns in the display itself.

1.1.2.2. Transparent amorphous oxide semiconductors

Transparent amorphous oxide semiconductors, in particularly a-InGa-aZnO (a-IGZO), are attracting increasing attention as TFT material for large sized active-matrix organic light emitting diode (AMOLED) displays. Because of an electron mobility ~ 10 times higher than a-Si:H [8,9], it is more easily able to deliver the large drive currents needed for OLEDs. Due to amorphous material, devices show good uniformity and promise a simpler processing schedule. However, the current TFTs are only n-channel, and integrated logic circuits made in this material will be slower and consume more power than the complementary pair circuits available with polycrystalline silicon (poly-Si) TFTs. The device structure is typically either inverted staggered ES or inverted coplanar, which can be made with a 5 or 4 mask process, respectively. In principle, this is a low temperature process, including the deposition of a-IGZO by DC sputtering at room temperature, although post-deposition anneals are required to stabilize the material. Device performance is sensitive to ambient oxygen and water, and effective passivation of the structure is essential for the fabrication of high quality TFTs with stable long-term operation.

1.1.2.3. Polycrystalline silicon

The interest in poly-Si as an alternative TFT material started soon after a-Si:H TFTs became recognized as the most promising technology for the large-scale production of active-matrix LCDs. In contrast to the carrier mobility in a-Si:H, which does not change to much over last 20 years or so, the electron mobility in poly-Si has increased, over the same period, from <5 to ~ 120 cm^2/Vs with routine processing, and up to ~ 900 cm^2/Vs with innovative techniques yielding quasi-single-crystal large-grain material [10]. Several ways have been examined for the formation of these TFTs such as direct deposition methods as well as conversion using a-Si film.

The principal technique for the direct deposition of poly-Si is by low-pressure chemical vapor deposition (LPCVD) using silane in nitrogen carrier gas. Practical deposition rates of 1 – 10 nm/min are obtained over temperature range 540 – 620 °C. For typical silane pressures of 100 – 200 mTorr, films will be deposited at upper temperature in a fine grain columnar form. The grain size is typically 100 nm and with a preferred (110) orientation. At the lower temperature the films are more likely to be amorphous, but the precise structure of the film depends upon both pressure and temperature. Films deposited in the amorphous state and then crystallized into poly-Si have been shown to have higher carrier mobilities due to larger grain size compared with film deposited in the polycrystalline state. The use of amorphous films as precursor material has meant that large-area plasma-enhanced CVD is also used. Crystallization of the amorphous material is achieved either by solid-phase crystallization (SPC) at temperature of ~ 600 °C or by the use of a laser.

Directly deposited columnar poly-Si was the material of initial interest in this area. However, columnar structure with typical grain size as 100 nm limited the electron field effect mobility μ_{FE} of 5 cm^2/Vs [11,12]. Meakin *et al.* [6] reported that deposited at a reduced pressure of < 10 mTorr at 630 °C can yield larger-grain material, with fewer intragrain defects and a higher μ_{FE} of ~ 10 cm^2/Vs. The interrelationship between silane pressure, growth mechanism, grain structure and surface morphology has been comprehensively studied. In the lower-pressure regime (< 10 mTorr), the large high-quality grains are only obtained in films thicker than ~ 0.5 μm, which is likely to result in large TFT off-currents. In addition, these large-grained films also show considerable surface roughness which has been demonstrated to degrade carrier mobility as well as the long-term stability of the devices. Although this work has considerably increased the understanding of the grain growth mechanisms, the film roughness has limited its application.

The poly-Si film via SPC using precursor a-Si film increase μ_{FE} comparing with directly deposited poly-Si film. For film deposited at temperatures below 600 ºC, thermal crystallization for 20 h at 600 ºC was required to convert them into their final polycrystalline form. The grains resulting from this process are generally elliptical in shape due to preferential growth in the <112> direction, and dendritic dur to the formation of twins along boundaries. Grain size dimension in excess of 1 μm have been obtained by this technique. Due to the low temperatures used (in order to keep the process compatible with the use of glass substrates) long crystallization times of several hours are necessary. Grain size has been reported to increase with film thickness in crystallized amorphous LPCVD silicon, probably due to grain nucleation occurring at the back of the film. In addition to the use of LPCVD a-Si precursor material, similar results have been obtained from use of PECVD a-Si:H deposited at significantly lower temperatures, such as 250 ºC. This exploits the use of large-area deposition equipment available for a-Si:H TFTs and also benefits from the higher deposition rates achievable with this technique compared with LPCVD a-Si (typically hundreds of angstroms per minute and tens of angstroms per minute respectively). Large dendritic grains are obtained after SPC, the major difference from LPCVD a-Si being a longer regrowth time due to a combination of a lower degree of inherent structural order in the film (due to the lower deposition temperature) and to the effect of the higher impurity density found in PECVD material. One of the practical limitations to the SPC process to the SPC process at ~ 600 ºC has been the long thermal anneal cycles necessary for the regrowth of the films. Some techniques are introduced to reduces this cycle time such as the use of metal induced crystallization [13-15]. However, film contamination by either the metal itself or the metal silicide are their issue. Excimer laser annealing (ELA) has been widely utilized and provides high-crystallinity Si films with low thermal damage to substrate by melting and crystallizing Si films within nanoseconds [16]. However, the high density of Si films crystallized by ELA results in large

variation of TFTs characteristics. In addition, the application of ELA to large area processing leads to difficulties in reducing the process cost due to high initial investment and operating costs.

The content of this section is summarized in Table 1.

Table 1. The summary of properties of some conventional bottom gate TFTs channel materials.

Material	Properties
a-Si:H	- Large scale production of AMLCDs - μ_{FE} < 1 cm^2/Vs, not suitable for faster switching circuit.
Amorphous transparent oxide (especially a-InGaZnO)	- Better overall performance than a-Si:H - μ_{FE} only around 10 cm^2/Vs, ES bottom gate architecture is preferred, therefore it not good for mass production.
Poly-Si	- Direct deposition (LPCVD): μ_{FE} = 5 ~ 7 cm^2/Vs but crystallized film has columnar structure. - Advance process as excimer laser annealing, μ_{FE} > 100 cm^2/Vs, large grain size. However, the devices show non-uniformity and have difficulty in large area application because of high initial investment and operating costs. - Solid phase crystallization using precursor a-Si film: μ_{FE} ~ 20 cm^2/Vs, devices show good uniformity, easy for large area application but long thermal cycle is limited its application in technology.

1.1.3. Published researches on mechanism of solid phase crystallization[20]

Completed research on the kinetics of SPC based on classical nucleation theory has been carried out since the 70s of the last decade [17-21]. These publications only focused on the low crystallization temperature region of a-Si, from 550 to 700 ^oC [22-25]. Hong *et al.* studied the kinetics of SPC by annealing a-Si films in a tube furnace when the temperature changed from

560 to 1000 °C [26]. Because of the heating-rate-limitation of the conventional method, they did not give the evidence for SPC crystallization at temperatures higher than 800 °C.

In this section the classical theory of solid-phase nucleation and growth in a homogeneous amorphous material is reviewed. The activation energies associated with transient time, nucleation rate, and growth velocity are found in relation to thermodynamic parameters of the classical theory.

According to classical theory, micro-crystallites (containing only a few atoms) will nucleate frequently. Because of a large surface-to-volume ratio, these tend to shrink. From thermodynamic considerations, however, a few will become large enough that further growth is energetically favorable. Growth in the microcrystalline regime occurs by the same basic mechanism as growth in the macrocrystalline regime: the rate at which each atom at an amorphous-crystalline interface makes a transition between the amorphous state and the crystalline state is a function of the energy levels of the two stages. Growths is energetically favorable when the free energy of the system is lowered by the transition of an interface atom from the amorphous to the crystalline state. In the classical model of nucleation, the Gibbs-free-energy ΔG, the barrier energy an atom must pass across to transfer from amorphous phase to crystalline phase, as a function of number of atoms in the cluster is given by:

$$\Delta G = -\Delta g_v \frac{4\pi r^3}{3a^3} + \sigma_{ca}, \qquad (1.1)$$

where Δg_v is the difference of free energy between amorphous phase and crystal phase, σ_{ca} is the interfacial free energy at the crystal – amorphous interface, r is the cluster radius, and a is the average atomic distance (0.27 nm). The maximum free energy, denoted as ΔG^*, occurs at a critical grain radius of r^*. The smaller clusters, with $r < r^*$, tend to shrink, and the larger clusters, with $r > r^*$, tend to grow.

The forward reaction rate is the rate that a cluster grows from n to $n + 1$ atoms. The reverse reaction rate is the rate that a cluster shrink from $n + 1$ to n atoms. These rates are found by defining an unbiased atomic jump frequency ν at the amorphous phase, it can be characterized by the activation energy of self-diffusion in amorphous silicon E_d. Because all reaction rates are proportional to ν, E_d enters into the activation energies for transient time t_o (time before the onset of nucleation), steady-state nucleation rate r_n, a characteristic crystallization time t_c (measured from t_o) and growth velocity v_g.

In each case a characteristic time t_t associated with transient nucleation was found to have the same temperature dependence. By assuming that the free energy of formation is a weak function of temperature, the form is

$$t_t \sim T/k_n^* \tag{1.2}$$

where k_n^* is the forward (or reverse) reaction rate at the critical cluster size. Kashchiev's theoretical results, which are in good agreement with experiment, indicate that t_o is proportional to t_t:

$$t_o \sim T \exp(\frac{E_d}{kT}) \tag{1.3}$$

The linear temperature term in Eq. 1.3 contributes kT to E_{to} (defined here as the slope of t_o on an Arrhenius plot.

$$E_{t_o} = E_d - kT \tag{1.4}$$

The theorical temperature dependence of the steady state nucleation rate is

$$r_n \sim (1/T) exp[-(E_d + \Delta G_n^*)/kT] \tag{1.5}$$

activation energy for nucleation rate is the absolute slope of r_n on an Arrhenius plot.

The growth rate can be found from the net forward reaction rate for a large cluster. Addition of one atom to a large cluster will not significantly change the surface energy. The change in free energy is – ΔG'.

$$v_g \sim exp[-(E_d - \Delta G'/2)/kT] \tag{1.6}$$

The Gibbs-free-energy difference between the amorphous and crystalline phases is

$$\Delta G' = 2\left(E_{v_g} - E_d\right) \quad (1.7)$$

where E_{v_g} is the activation energy of the growth velocity.

A number of analyses of activation energies for t_o, r_n, t_c, v_g of SPC Si film at low temperature regime (500 – 700 °C) have been published[22-25]. According to Iverson *et al.* [23] , activation energy for transient time is 2.7± 0.15 eV. Activation energy for nucleation rate is 5.1 ± 0.15 eV following research of Iverson *et al.* [23]; Zellama *et al.* [24] and Koster *et al.* [25] show an activation energy of 4.9 eV at 570 ºC. The characteristic crystallization time is also the function of temperature. The activation energy is 3.9 ± 0.25 eV from Iverson *et al.* [23], 3.1 eV from Blum and Feldman[22]. This activation energy is not related to a particular crystallization process, but rather, is the result of number of processes. The growth velocity also depends on temperature. Iverson *et al.* [23] shows activation energy as 3.3 ± 0.35 eV. Also, some data from several sources as 2.9 eV from Koster [25], 2.4-4.9 eV from Zellama *et al.* [24].

1.1.4. Micro thermal plasma jet irradiation

As we mentioned before, it is required a lower cost crystallization technique for large area electronics. We previously proposed the application of an atmospheric-pressure direct current (DC) arc discharge micro thermal plasma jet (μ-TPJ) to the millisecond crystallization of a-Si films on quartz substrate [27]. Figure 1.4 shows the experimental set up. The wolfram W cathode and the water – cooled copper Cu anode separated 2 mm each other is connected to a supplied power. Arc discharge was performed by supplying DC bias between electrodes with an argon Ar gas flow. The thermal plasma is blown out through an orifice with diameter ϕ as 600μm. The substrate was moved linearly by a motion stage with a scanning speed *v*.

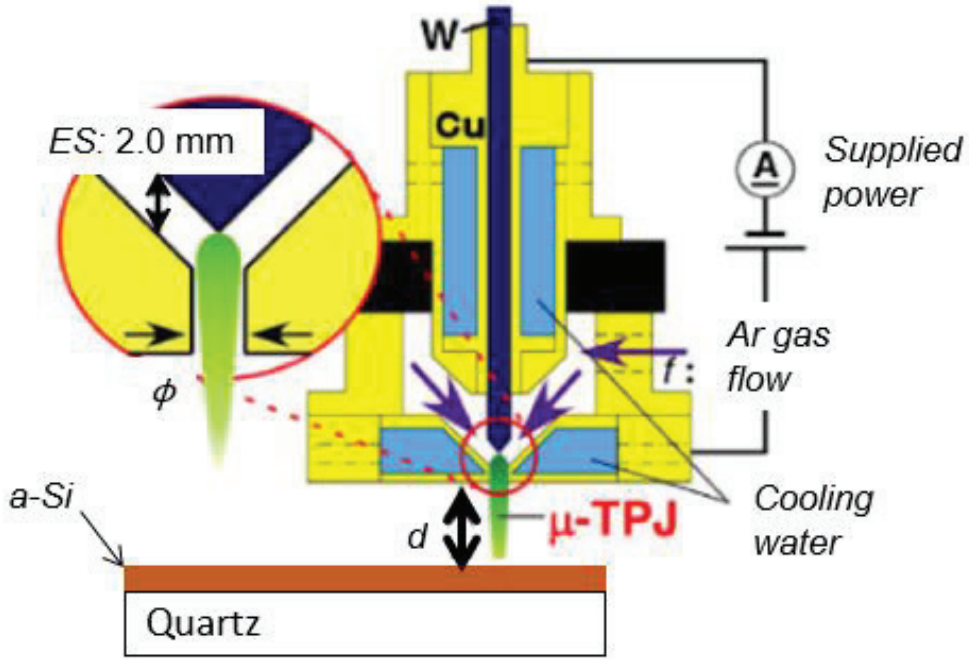

Fig. 1.4. Schematic of μ-TPJ experimental set-up.

The crystallized Si films formed by μ-TPJ shows good quality. The crystalline volume fraction R_c estimated from Raman spectra reaches 100 % in case of recrystallized from liquid phase and 70% in case of solid phase crystallization [28].

Surface morphologies were observed by atomic force microscopy (AFM) [29]. The typical grain size and root mean square (RMS) were ~ 20 and 0.5 nm, respectively, are obtained when Si films crystallized in SPC. In contrast, the melting and solidification that occurred in the Si film resulted in large grains 300 – 600 nm in size. This crystallization was called "liquid phase crystallization (LPC)" in a previous study [29] because it was induced via a liquid phase. The grain size in LPC is close to that of Si films formed by ELA.

1.1.5. Direct observation of phase transformation

We introduced a new in situ observation technique of phase transformation using high-speed camera (HSC) with a microsecond time resolution [30]. The substrate was linearly moved by a motion stage in front of the μ-TPJ with a scanning speed v changing from 500 to 2500

mm/s. The distance between the plasma source and substrate (*d*) was varied from 1.0 to 1.5 mm. For the *in-situ* observation of grain growth of a-Si film during μ-TPJ irradiation, an optical microscope and a HSC was set on the motion stage on the backside of the substrate. The frame rate (R_f) was varied from 3000 to 1650000 frames per second (fps) [30].

Phase transformation of the Si film induced by μ-TPJ irradiation was very clearly observed. Figure 1.5 shows the HSC snapshots during μ-TPJ irradiation under conditions of f_{Ar} = 1.6 L/min, P = 1.12 kW, v = 1500 mm/s, d = 1.0 mm, ES = 2.0 mm.

Fig.1.5. HSC snapshots of Si film taken by HSC during μ-TPJ irradiation. μ-TPJ conditions were f_{Ar} = 1.6 L/min, P = 1.12 kW, v = 1500 mm/s, d = 1.0 mm, ES = 2.0 mm.

Since liquid Si shows very high reflectivity due to free carriers, which called the molten region (MR). A SPC formed in front of the molten Si was clearly distinguished from amorphous phase. Following the movement of MR, grains grew perpendicularly to a liquid-solid interface, called high speed lateral crystallization (HSLC). It should be noted that a region showing a wave-like pattern exists between MR and SPC region. In previous research, it is called leading wave crystallization (LWC) because it exhibits a periodic and repeating structure like waves [30].

Furthermore, a new crystallization mechanism named LWC was discovered. Grain growth with a velocity measured as high as 4500 mm/s intermittently propagates into SPC regions. As a result, LWC formed periodic and repeating-structure-like waves, and LWC-Si films showed a very high crystalline volume fraction of 100%. The length of LWC increased with the increase of thickness of Si film and scanning speed *v*. This result suggests that not only heat conducted from μ-TPJ but also latent heat plays a very important role in LWC. The growth mechanism in LWC is well understood on the basis of a model including the explosive propagation of a thin liquid layer driven by released latent heat at the liquid-solid interface.

1.1.6. Contactless temperature measurement

By obtaining the transient reflectivity of quartz substrate during μ-TPJ irradiation, we developed the method for measuring its temperature [31]. The transient reflectivity was measured by irradiating the quartz substrate with He-Ne laser (633 nm) or yttrium aluminum garnet (YAG) laser (532 nm) from the backside of the substrate and detecting the reflected light intensity using a photodiode through a band pass filter. Other route was used to investigate the phase transformation of Si films. The oscillating transient reflectivity of He-Ne laser light relates to sample temperature. The number of oscillations increases with decreasing *v*, which suggests that the increase in the number of oscillations reflects an increasing surface

temperature. The transient reflectivity oscillates by the interface of the incident light reflected multiple times between the top and bottom surfaces of the substrate. The oscillation was reproduced in numerical simulation of heat diffusion and optical interference [31]. The simulation was based on a two-dimensional heat diffusion equation [32],

$$\frac{\partial T(x,y)}{\partial t} = \frac{\kappa}{\rho c}\left(\frac{\partial^2 T(x,y)}{\partial x^2} + \frac{\partial^2 T(x,y)}{\partial y^2}\right) + \frac{S}{\rho c} \qquad (1.8)$$

where x is the position along the plasma jet scanning direction, y is the depth from the substrate surface, T is the temperature, t is the time, κ, ρ and c are the thermal conductivity, the density and the specific heat of the quartz substrate, respectively, and S is the thermal incidence. The details of the analysis have been reported elsewhere[32]. Using the analysis of transient changes in optical reflectivity of quartz substrates, the temperature during TPJ process is measured within 30K error. In this analysis, we can well reproduce the observed waveforms with double-Gaussian shapes of the TPJ profile. From the analysis of transient changes in optical reflectivity of quartz substrates exposing to the Ar TPJ, the maximum surface temperature and the annealing duration were evaluated under different annealing conditions. We have found that maximum surface temperature can be controlled in the range of 980 to 1780K with almost constant annealing duration at ~ 3 ms by changing the Ar gas flow rate and distance between the plasma source and the substrate d. This technique was also applied to Si wafers and conventional glass substrate [33,34].

1.2. Overview of thesis

1.2.1. Motivation and purpose

Bottom gate TFTs fabricated with SPC – Si films show high mobility as 20 cm^2/Vs[35] and good uniformity. Hence, it is suitable for large area applications. However, the conventional methods for SPC film fabricating as LPCVD, PECVD or furnace need long

thermal cycle which is main drawback when applying in industry. By using metal induced crystallization, this annealing time is reduced, but the film is contaminant by metallic. Based on experience to make SPC-Si film with good characteristics by μ-TPJ irradiation, we propose millisecond SPC Si film formed by μ-TPJ is an alternative material for TFT's channel.

Based on our knowledge, due to the limitations of conventional method, the millisecond SPC Si films formed in at temperature around 1000 ºC have not been studied in detail. In this thesis, we will propose a new method for observing the phase transformation and temperature SPC Si film formed in millisecond region by μ-TPJ at temperature around 1000 ºC. The characteristics of millisecond SPC Si film are investigated by optical microscopy, Raman spectra, Hall effect measurement, atomic force microscopy (AFM), and high-resolution transmittance electron microscopy (HRTEM). Then, bottom gate TFTs fabricated with millisecond SPC film are prepared. Our target is TFTs mobility as high as 20 cm^2/Vs and small variation in transfer characteristics.

1.2.2. Composition

My thesis consists of two main points. First is about mechanism of millisecond SPC Si film annealed by μ-TPJ at high temperature. Second is characteristics of millisecond SPC Si film and its application to bottom gate TFTs. Beside the background presented in chapter 1, my research is presented in four chapters with title listed as below,

Chapter 2: Simultaneous Observation of Phase Transformation and Temperature of Silicon Film during Millisecond Annealing

Chapter 3: Temperature Calculation and Growth Mechanism of Millisecond Solid Phase Crystallization Silicon Film

Chapter 4: Characteristics of Millisecond Solid Phase Crystallization Phosphorous Doped Silicon Films

Chapter 5: Application of Millisecond Solid Phase Crystallization Silicon Film for Bottom-Gate Thin Film Transistors Fabrication

Content of chapter 2 and 3 mainly comes from Main Paper 1 and that of chapter 4 and 5 comes from Main Paper 2.

In the last, some conclusions are presented.

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Chapter 2

Simultaneous Observation of the Phase Transformation and Temperature of Silicon Film during Millisecond Annealing

2.1. Principle of measurement

The temperature dependence of the optical properties of solids has been the focus of many studies[1, 2].

As known, the refractive index *n* of material depends on temperature, called thermo-optic-coefficient (TOC), in details:

$$n = a + b \times T \tag{2.1}$$

$$TOC = \frac{dn}{dT} = b \tag{2.2}$$

When a light comes through interface between two media, the reflectivity appears with the reflectivity coefficient *r* depends on refractive index *n* as following equation:

$$r = \frac{n_1 - n_2}{n_1 + n_2} \tag{2.3}$$

with n_1, n_2 are the refractive index of media when the light come in and come out, respectively. It is cleared that the changing in reflectivity depends on temperature of sample. Hence, by obtaining the transient reflectivity of Si film during μ-TPJ irradiation, the transient temperature can be extract by applying inference phenomena inside the thin film.

Based on our experienced, an idea for direct observation phase transformation and temperature of Si film at high temperature simultaneously is supposed. A laser light is introduced to objective lens of HSC and focuses on the a-Si films surface during μ-TPJ annealing. The Fig. 2.1 shows the illustration of optical path inside the sample.

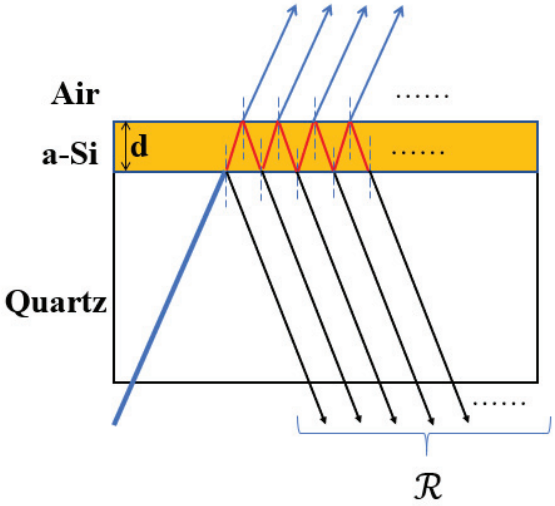


Fig. 2.1. Illustration of optical path inside the thin film

The interference phenomenon inside quartz substrate is neglected. The reflectivity which comes from interference of multiply reflected light at the top and the bottom surfaces of a-Si film is collected by an oscilloscope. From the reflected signal during annealing and TOC of a-Si film, we can extract the temperature. In this chapter, we present the phase transformation and transient reflectivity of Si film during μ-TPJ irradiation. The temperature extracted from reflectivity is presented in Chapter 3.

2.2. Experimental procedure

150-nm-thick a-Si films were deposited on 525-μm-thick quartz substrate by PECVD using SiH_4 and H_2 at 250 °C. Dehydrogenation was performed by N_2 annealing at 450 °C for 1 h. Before the μ-TPJ annealing experiments, the samples were cleaned simply by acetone for 10 minutes to remove inorganic contaminants on the sample surface. Figure 2.2 shows the schematic diagram of the experimental setup. The system is consisted of μ-TPJ to irradiate the samples and HSC set on a motion stage which moved linearly with a sample in front of μ-TPJ with v ranging from 350 to 2020 mm/s. The distance between two electrodes (ES) was 2.0 mm, P was from 0.5 to 1.2 kW, f_{Ar} was 1.0 L/min, and d was 1.0 mm. The μ-TPJ was generated by blowing out the thermal plasma through an orifice with 600 μm in diameter. He-Ne laser light

with 632.8 nm in wavelength was introduced to the objective lens of HSC, focused on the surface of a-Si film and located at the center of crystallization area. The changes in reflectivity $\mathcal{R}$ of the sample during μ-TPJ irradiation was detected by a photodiode connected with a fast oscilloscope. Strong light from the μ-TPJ was cut off by a bandpass filter. In addition, a part of reflected light from top surface of Si film comes to CCD of HSC, the phase transformation will be collected. By this method, we can observe the phase transformation and transient $\mathcal{R}$ of Si film during μ-TPJ irradiation simultaneously.

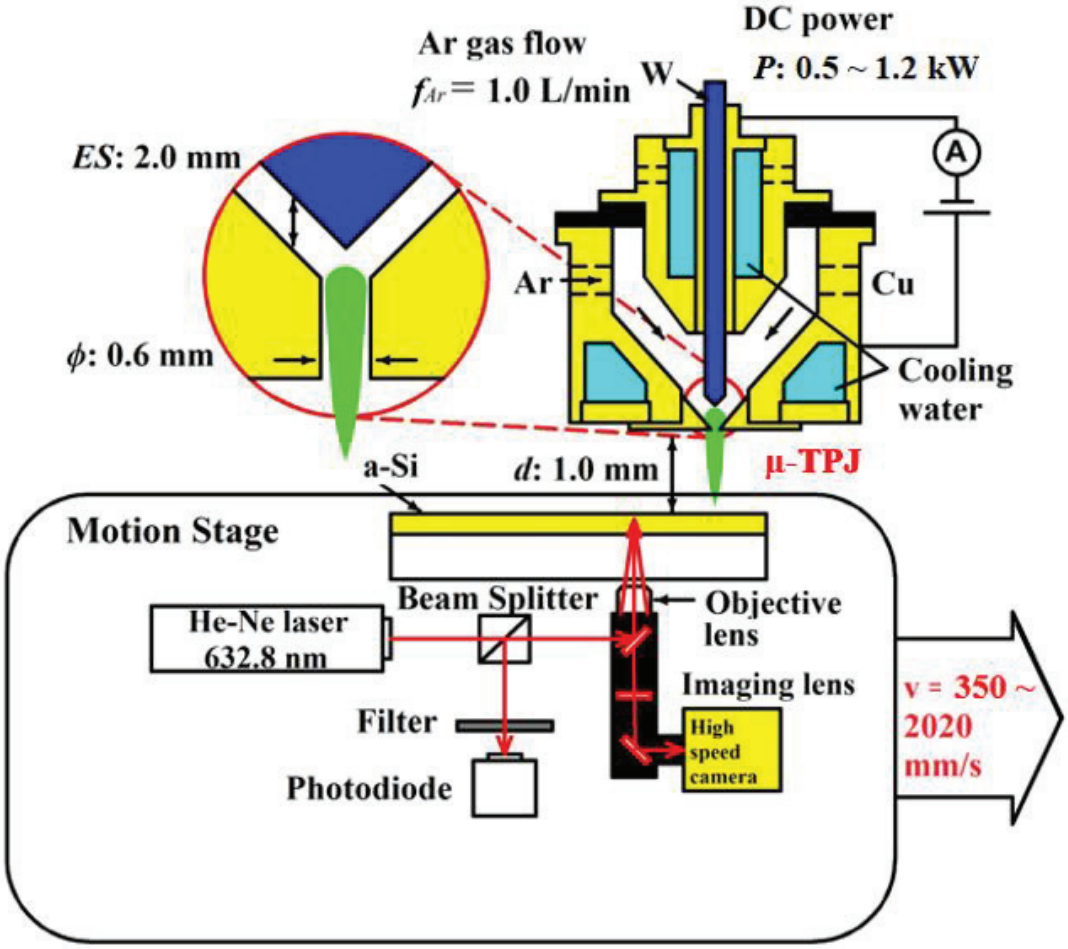


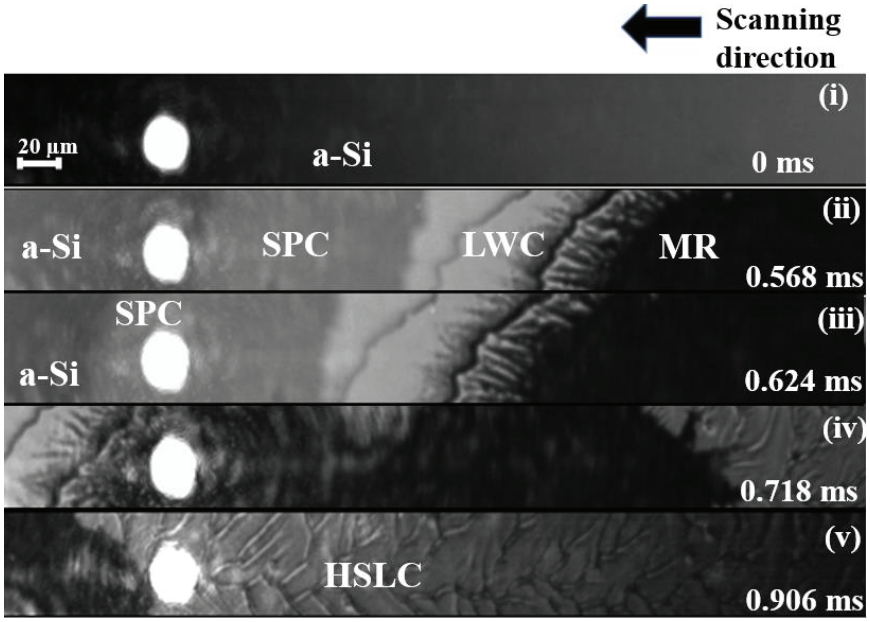
Fig. 2.2. Experimental setup for direct observation of phase transformation and non-contact temperature measurement of Si films during μ-TPJ irradiation [(3)].

2.3. Results and discussions

2.3.1. HSC snapshots and transient reflectivity of Si film during μ - TPJ irradiation

To have full sight of what happens with Si film during μ-TPJ irradiation, Fig. 2.3 shows (a) a typical example of HSC snapshots and (b) the transient $\mathcal{R}$ of a-Si film when the film is totally melted during μ-TPJ annealing under the conditions of P = 1.06 kW, d = 1.0 mm, f_{Ar} = 1.0 L/min, and v = 1680 mm/s. The He-Ne laser spot can be seen in a bright spot which is about 20 μm in diameter in Fig. 2.3 (a). The phase transformation of a-Si film during annealing was observed comprehensively. The SPC was formed before the leading wave crystallization (LWC) [(2)] which part had a wave-like form. It is clearly different from SPC and a-Si. Molten region (MR) went after the LWC. The part that has dendritic morphology following MR is called high-speed lateral crystallization (HSLC) [(4)]. The transient $\mathcal{R}$ waveform of a-Si film during μ-TPJ irradiation taken simultaneously with Fig. 2.2 (a) is shown in Fig. 2.2 (b) and arrows (i) to (v) correspond to the HSC captures of Fig. 2.2 (a) (i) to (v). Before the onset of SPC, $\mathcal{R}$ of a-Si gradually increases during the annealing process ((i) to (ii)). It is related to the changing of a-Si film temperature because the refractive index of a-Si depends on temperature, called the thermal-optic coefficient (TOC). From (ii) to (iii), the decrease of $\mathcal{R}$ relates to the phase transformation process from amorphous to crystalline. The trending between (iii) and (iv) relates to the appearance of LWC. A significant increase in $\mathcal{R}$ was perceived after LWC, the maximum $\mathcal{R}$ reached around 70 % (at point (iv)). It comes from the free carrier generation in molten Si. When the laser spot touches the HSLC region (at point (v)), $\mathcal{R}$ moves downward. It relates to the solification of molten silicon.

(a)



(b)

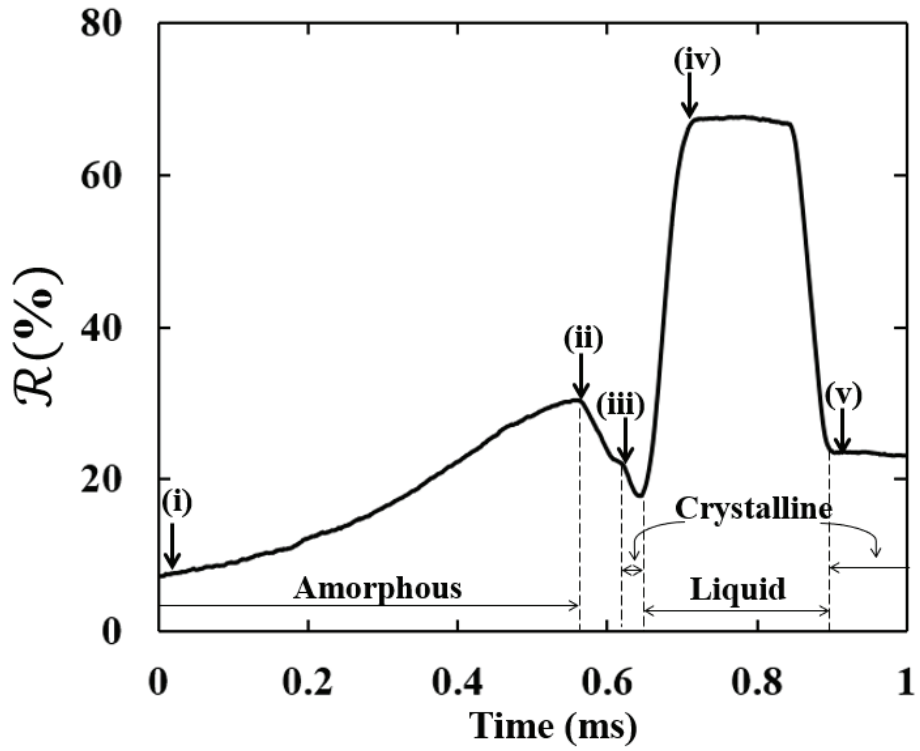


Fig. 2.3. (a) HSC snapshots of 150-nm-thick Si film during μ-TPJ irradiation under conditions of P = 1.06 kW, d = 1.0 mm, f_{Ar}= 1.0 L/min, and v = 1680 mm/s, respectively and (b)its transient $\mathcal{R}$ during μ-TPJ irradiation taken simultaneously with Fig. 2.3(a). (i) to (v) corresponds to the HSC snapshots shown in (a) [3].

Next, the millisecond SPC film is focused on. A typical example of transient $\mathcal{R}$ waveforms observed during μ-TPJ irradiation to a 150-nm-thick a-Si film under annealing conditions of P = 0.61 kW, d = 1.0 mm, f_{Ar} = 1.0 L/min, and v = 500 mm/s is shown in Fig.2.4. The points (i), (ii), and (iii) correspond to point (i), (ii), and (iii) of HSC snapshots in the inset. Under this condition, a-Si film is crystallized in solid phase because we see no abrupt increase in $\mathcal{R}$ due to melting.

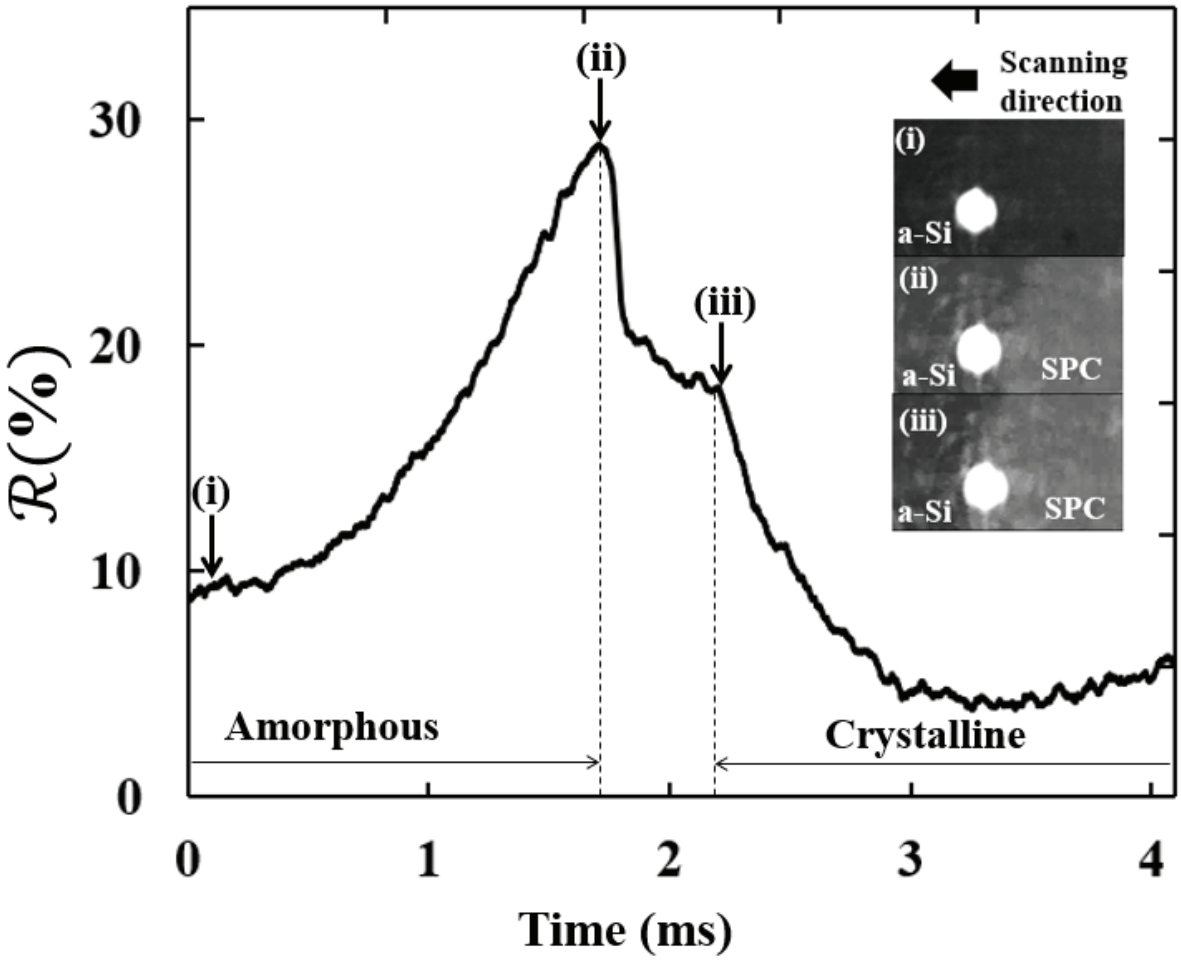


Fig. 2.4. The transient $\mathcal{R}$ of 150-nm-thick a-Si film observed during μ - TPJ irradiation (P = 0.61 kW, f_{Ar} = 1.0 L/min, d = 1.0 mm, v = 500 mm/s) when SPC occurs [3].

As mentioned in Section 2.1, the increase in transient $\mathcal{R}$ from (i) to (ii) is due to the changing of refractive index, meaning as the changing in film temperature in amorphous phase. Nucleation occurs at (ii) and phase transformation from amorphous to crystalline proceed until

(iii). We can interpret the decrease in $\mathcal{R}$ from (ii) to (iii) as the change in crystalline volume fraction (R_c). Therefore, by obtaining the temperature variation of a-Si from (i) to (ii), we can determine T_c. In addition, we can extract the transient variation of R_c from (ii) to (iii) and can determine t_c. It will be discussed in detail in Chapter 3.

2.3.2. Crystallinity

Micro-Raman spectroscopy analysis was performed to determine R_c of crystallized silicon films. The Ar laser with wavelength as 514.5 nm was used for measurement. Figure 2.5 indicates the micro-Raman scattering spectra of μ-TPJ crystallized films under conditions of P = 0.61 kW, d = 1.0 mm, f_{Ar} = 1.0 L/min, and v from 480 – 520 mm/s together with precursor a-Si and single crystalline Si.

In our experiments, d was kept constant and v was changed 20 mm/s for SPC condition, the heating rate is not too different between three Raman samples [(1)]. R_c is extracted from Raman spectra by using the equation shown as

$$R_c = \frac{S_c + S_m}{S_c + S_m + S_a} \qquad (2.4).$$

Here, S_c, S_m, and S_a are transverse optical (TO) phonon peak area of crystalline-Si (c-Si) (~ 520 cm^{-1}), microcrystalline-Si (μc-Si) (~ 500 cm^{-1}), and a-Si (~ 480 cm^{-1}).

As can be seen in Fig. 2.5, when v = 520 mm/s, SPC–Si film shows a peak position of 514.8 cm^{-1}, full width half maximum (FWHM) of 7.6 cm^{-1}, and R_c of 65 %. When we decreased v to 500 mm/s, SPC – Si film displays a peak at 515.3 cm^{-1}, FWHM of 7.4 cm^{-1}, and R_c of 82 %. HSLC film formed under v at 480 mm/s shows a peak position of 515.4 cm^{-1}, FWHM of 6.3 cm^{-1}, and R_c of almost 100 %. The result is suitable with our previous publications [(5,6)]. The c-Si TO phonon peak of both crystallized Si shifted to lower wavenumber because of tensile stress, grain size, and the composition of crystalline and microcrystalline phase. By decreasing v, FWHM gradually decreased and the peak positions were close to that of single c-Si at 520

cm^{-1}. From these results, the crystallinity of millisecond SPC-Si film was improved by μ-TPJ crystallization with slow v because of the low nucleation temperature T_c and larger grain size as discussed in the following sections.

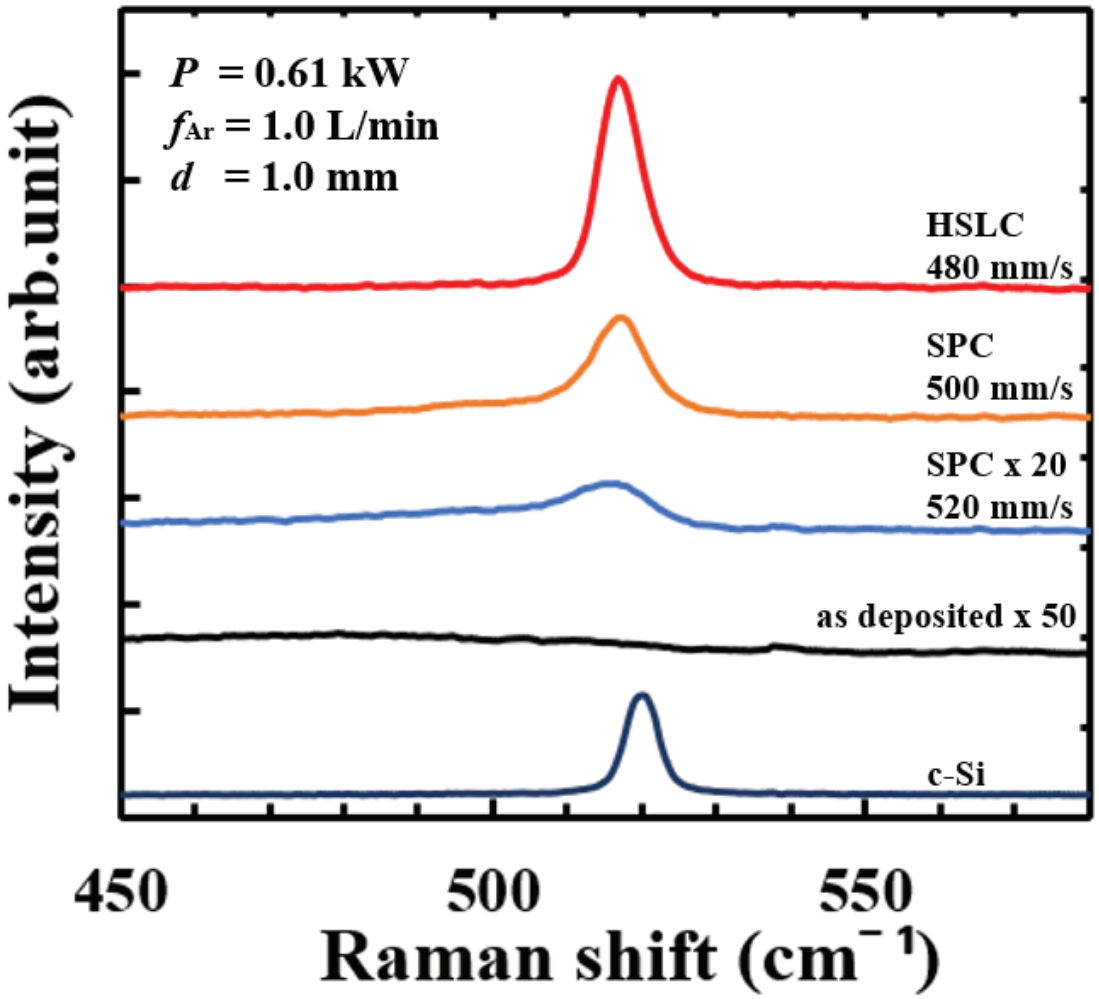


Fig. 2.5. Micro-Raman scattering spectra obtained from 150-nm-thick crystallized films formed by different experiment conditions [3].

2.4. Summary

This work gives a new method to directly observe the phase transformation and measure the transient $\mathcal{R}$ of Si film during μ-TPJ irradiation simultaneously. The phase transformation of a-Si film during annealing was observed clearly. When film is melted, the millisecond SPC comes before LWC, next is MR, and HLSC follows MR. In case of 150-nm-thick Si film, $\mathcal{R}$

gradually increases before the onset of SPC. When phase transformation process from amorphous to crystalline occurs, the decrease of $\mathcal{R}$ is observed. The significant increase in $\mathcal{R}$ appeared when film was melted and recrystallized from liquid phase. Micro-Raman spectroscopy analysis indicates the crystallinity of millisecond SPC films is higher than 65 % and it grows up with the decreasing of v.

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Chapter 3

Temperature Calculation and Growth Mechanism of Millisecond Solid Phase Crystallization Silicon Film

3.1. Introduction

As we mentioned in Chapter 2, from the TOC of a-Si combined with transient reflectivity obtained during μ-TPJ irradiation, the transient temperature will be calculated. Moreover, based the changing of transient reflectivity during phase transformation process, characteristic crystallization time is found out. In this section, theory for calculation is introduced.

3.1.1. Optical interference

In addition, when a light passed an interface between two media, it is affected by reflectance and transmittance. The optical model is shown in Fig.3.1.

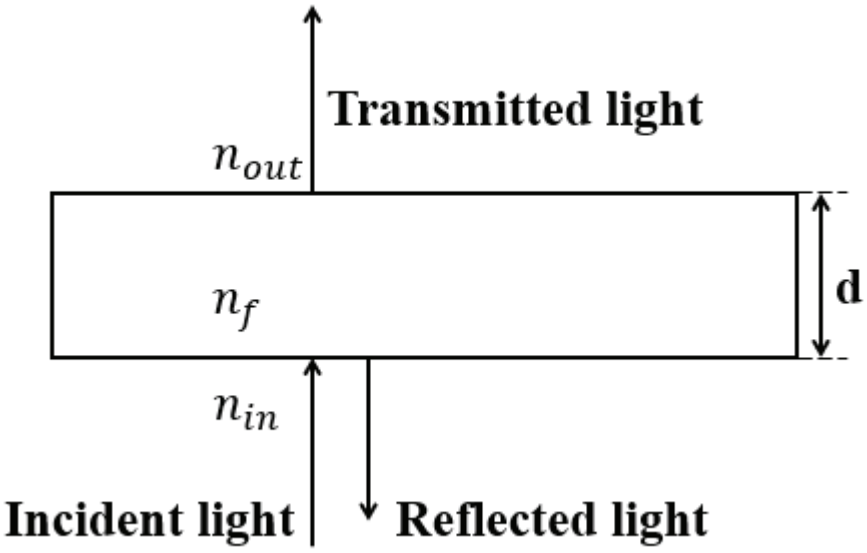


Fig. 3.1. Reflection and transmission phenomena when a light passed through two media.

The Fresnel's equation for these phenomena as below was applied:

- Reflectivity coefficient

$$r = \frac{n_{in} - n_{out}}{n_{in} + n_{out}} \qquad (3.1)$$

- Transmittance coefficient

$$t = \frac{2n_{in}}{n_{in} + n_{out}} \tag{3.2}$$

The phase difference $2\delta_f$ between a reflection from interface 1 and a transmission from the film following reflection from interface 2 is represented by the following equation

$$2\delta_f = \frac{4\pi}{\lambda} N_f d \tag{3.3}$$

This equation is based on Snell's law and a simple geometrical consideration. Considering the phase difference, amplitude reflectance and amplitude transmittance are calculated from a summation of reflectance or transmittance.

Amplitude reflectance

$$= \frac{r_1 + r_1 \exp(-2i\delta_f)}{1 + r_1 r_2 \exp(-2i\delta_f)} \tag{3.4}$$

Amplitude transmittance

$$= \frac{t_1 + t_1 \exp(-2i\delta_f)}{1 + r_1 r_2 \exp(-2i\delta_f)} \tag{3.5}$$

By multiple with complex conjugation of amplitude reflectance and amplitude transmittance, we can calculate the energy reflectance and energy transmittance as follow,

Energy reflectance

$$= 1 - \frac{8n_0 n_1^2 n_2}{(n_0^2 + n_1^2)(n_1^2 + n_2^2) + 4n_0 n_1^2 n_2 + (n_0^2 - n_1^2)(n_1^2 - n_2^2)\cos 2\delta_f} \tag{3.6}$$

Energy transmittance

$$= \frac{8n_0 n_1^2 n_2}{(n_0^2 + n_1^2)(n_1^2 + n_2^2) + 4n_0 n_1^2 n_2 + (n_0^2 - n_1^2)(n_1^2 - n_2^2)\cos 2\delta_f} \tag{3.7}$$

In case of no absorptance, the total of energy reflectance and transmittance need to be equal 1.

When consider an absorptance, the complex refractive index of medium is: $N_i = n_i - i.k_i$, with n_i is the refractive index, k_i is extinction coefficient. Fresnel coefficients in Equation (3.1) and (3.2) become:

$$r = \frac{N_{in} - N_{out}}{N_{in} + N_{out}} \tag{3.8}$$

$$t = \frac{2N_{in}}{N_{in} + N_{out}} \tag{3.9}$$

3.1.2. The usage of time-resolved reflectivity in studies of random nucleation and growth

Because the indices of refraction of a-Si and c-Si are different, reflectivity measurement can be used to detect to formation of crystalline material in an amorphous matrix, even in the absence of epitaxy. In the present work, time-resolved reflectivity (TRR) was used to study the random nucleation and solid phase growth of crystalline grains within amorphous films deposited onto quartz. The measured reflectivity as a function of time was used to calculate the volume fraction of crystallized material as a function of time. From this information, the kinetic parameters governing random crystallization, such as crystallization time and activation energy were determined. To extract the kinetics of random crystallization from the reflectivity data we modelled the crystallizing films as a homogeneous mixture of amorphous and crystalline material, and its index of refraction was treated as a linear combination of the amorphous and crystalline indices. In a more accurate treatment, the polarizabilities rather than the indices of refraction would be treated as linear in the volume fraction, but for the purpose of extracting crystallization times, it is not significant different between the two approaches.

In this chapter, the TOC of our a-Si film is measured, from that we determine the relationship between the reflectivity and temperature. Combined with transient reflectivity of Si films obtained during μ-TPJ irradiation in Chapter 2, we estimate the nucleation temperature T_c and characteristic crystallization time t_c. In the last part, we will suggest a simple theorical model for explain mechanism of millisecond SPC formed at high temperature region.

3.2. TOC measurement experiment

We have measured the TOC of our a-Si films which used in experiments in Chapter 2. Figure 3.2 shows the experimental set-up of TOC measurement.

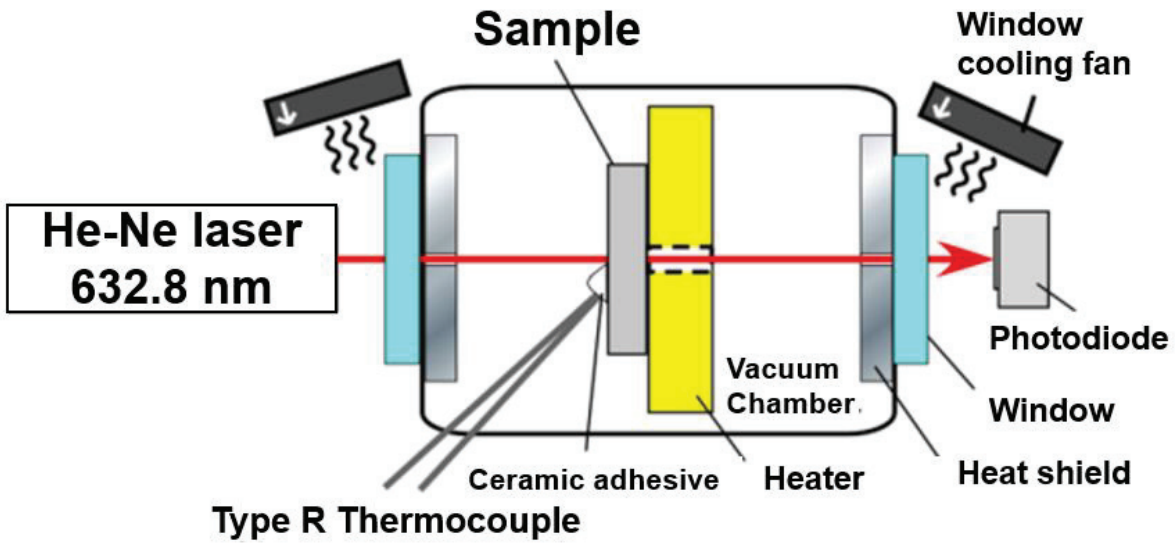


Fig. 3.2. Schematic of TOC measurement experimental set-up.

A He-Ne laser with wavelength as 632.8 nm is used to irradiate sample and the transmissivity $\mathfrak{I}$ is measured. The chamber is evacuated to 1 Pa and the 1 x 1 cm^2 a-Si film (or quartz) is heated gradually at 5 K/min by a plate heater while maintaining thermal equilibrium and the transmissivity and sample temperature are measured at 0.25 s intervals. A 0.05-mm-diameter type-R thermal couple is used to avoid effects due to the heat capacity and conduction of the wire. The chamber windows are covered by aluminum heat shields to prevent a thermal

radiation wave from the heater, and the TOC is extracted from the measured waveform of the transmissivity [1]. In this time of experiment, we performed measure the TOC of quartz substrate and a-Si film deposited on the quartz substrate separately.

3.3. Results and discussion

3.3.1. TOC measurement

The measured $\mathcal{T}$ *(T)* value is converted to *n (T)* and *k(T)* by using the Fresnel formula when considering the interference phenomena of quartz substrate and a-Si film. In this simulation, we introduced the thermal expansion coefficient of a-Si and quartz as 3 x 10^{-6} and 5 x 10^{-7} $^{o}C^{-1}$ [2, 3], respectively.

The $\mathcal{T}$ (*T*) and simulated optical model of quartz is shown in Fig.3.3 (a) and those of a-Si deposited on a quartz substrate is shown in Fig.3.3 (b). The oscillation in Fig.3.3 (a) comes from the interference of multiply reflected light at the top and the bottom surfaces of quartz. In Fig. 3.3 (b), the number of oscillation and amplitude of $\mathcal{T}$ are slightly changed, which is the effect of TOC of quartz. By applying the optical interference equation as described in section 1, the refractive index of quartz and a-Si film is found as

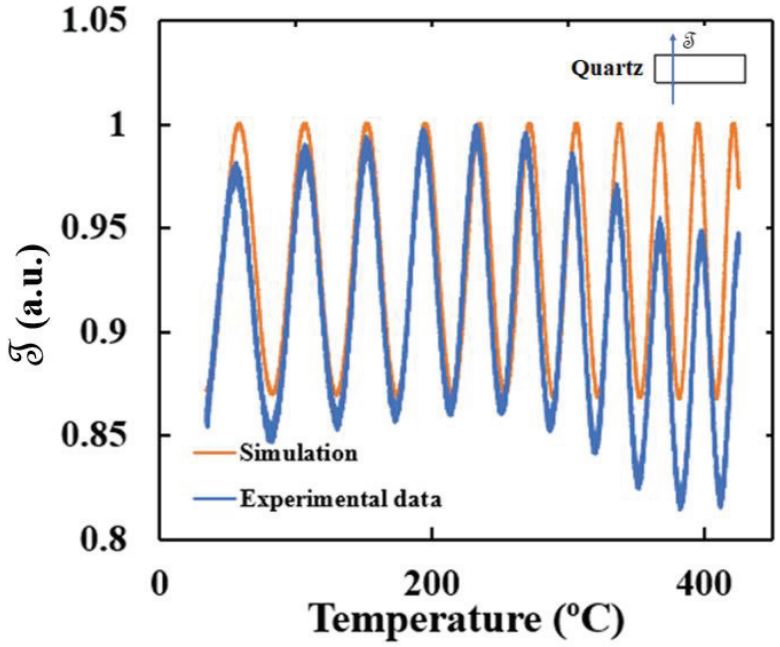
$$n_{quartz} = 1.457 + 1.12 \times 10^{5}T + 0.7 \times 10^{-9}T^{2} + 21 \times 10^{-12} \times T^{3} \quad (3.10)$$

$$n_{a-Si} = 4.19 + 7 \times 10^{-4}T \quad (3.11)$$

We extracted the TOC of a-Si as dn/dT=7×10^{-4} $^{o}C^{-1}$. This value is suitable with the publication of Smets *et al.* [4].

According to Hong et al., when the annealing time comes to around 800 ^{o}C, a-Si films crystallize in less than 1 s [5]. It is impossible to measure the TOC at a temperature higher than 800 ^{o}C by the present method. Therefore, we estimated TOC of a-Si film at high-temperature by extrapolating the measured value at the low-temperature regime.

(a) Quartz



(b) a-Si deposited on quartz

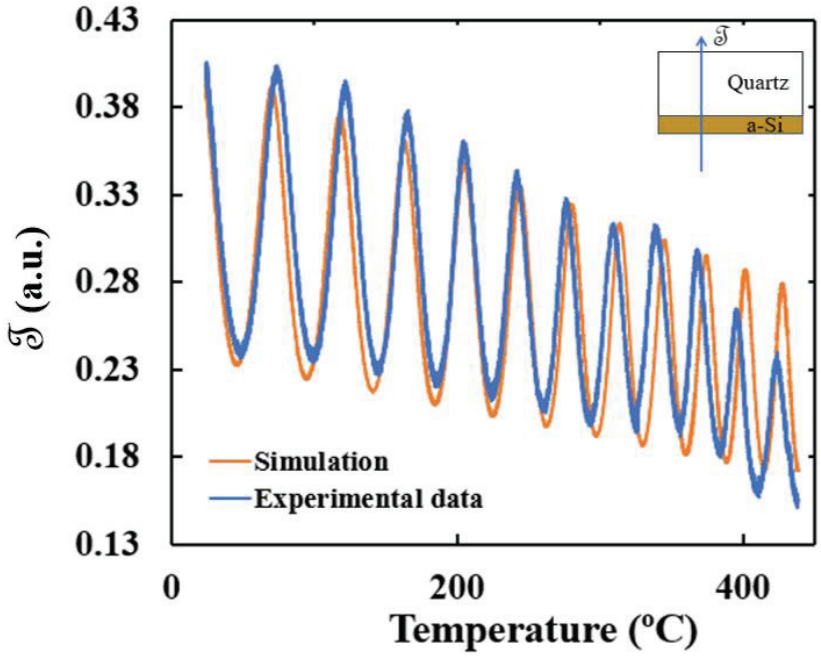


Fig. 3.3. The transient $\mathfrak{I}$ of quartz (a) and a-Si films deposited on quartz substrate (b) with respect to the sample temperature [6].

Based on the TOC, we calculated the reflectivity as a function of temperature $\mathcal{R}(T)$ for 150-nm-thick a-Si film as shown in Fig.3.4.

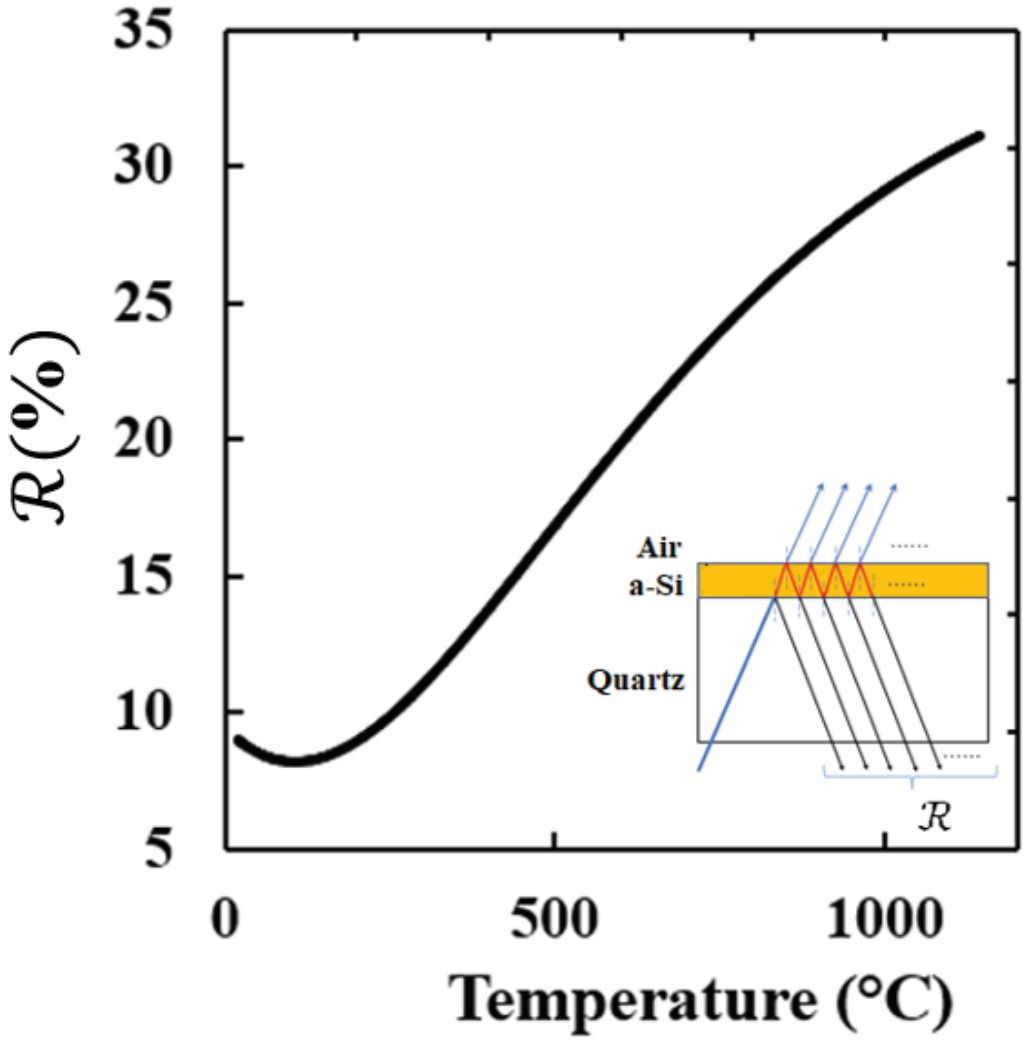


Fig. 3.4. $\mathcal{R}$ of 150-nm-a-Si/quartz sample as a function of temperature calculated based on interference phenomena inside the a-Si film. The inset shows the optical model of calculation [6].

Because the laser light is focused on the surface of a-Si film deposited on quartz substrate in the *in-situ* measurement (see Fig. 2.2), we only consider the multiple reflection and interference inside the a-Si film. The interference effect in quartz substrate can be neglected. The optical model to calculate $\mathcal{R}(T)$of a-Si films is shown in inset figure of Fig. 3.4. Since thickness of a-Si film is very thin, we obtain only a small portion of the oscillation in Fig. 3.4. $\mathcal{R}(T)$ follows the equation as below:

$$\mathcal{R}(T)=9.26 - 2.15\times10^{-3}\times T+10^{-4}\times T^2 - 10^{-7}\times T^3+4\times10^{-4}\times T^4 \quad (3.12),$$

where T is expressed in degree Celsius and $\mathcal{R}$ is in percentage.

3.3.2. Estimation of nucleation temperature

Equation 3.12 combined with the transient $\mathcal{R}$ as a function of time from Fig. 2.3 (i) to (ii) gives us the dependence of a-Si film temperature on time.

Figure 3.5 shows the transient variation of $\mathcal{R}$ and temperature of a-Si before the onset of SPC deducted from Fig. 2.4 (i) to (ii). The μ-TPJ conditions were P = 0.61 kW, f_{Ar} = 1.0 L/min, d = 1.0 mm, and v = 500 mm/s. From this result, we can estimate the T_c to be 991 °C. The time for temperature increases from room temperature to T_c was 1.708 ms, namely, the average R_h was 5.66×10^5 K/s. As mentioned above, the laser spot size is 20 μm, the distribution of temperature inside the laser spot can be neglected.

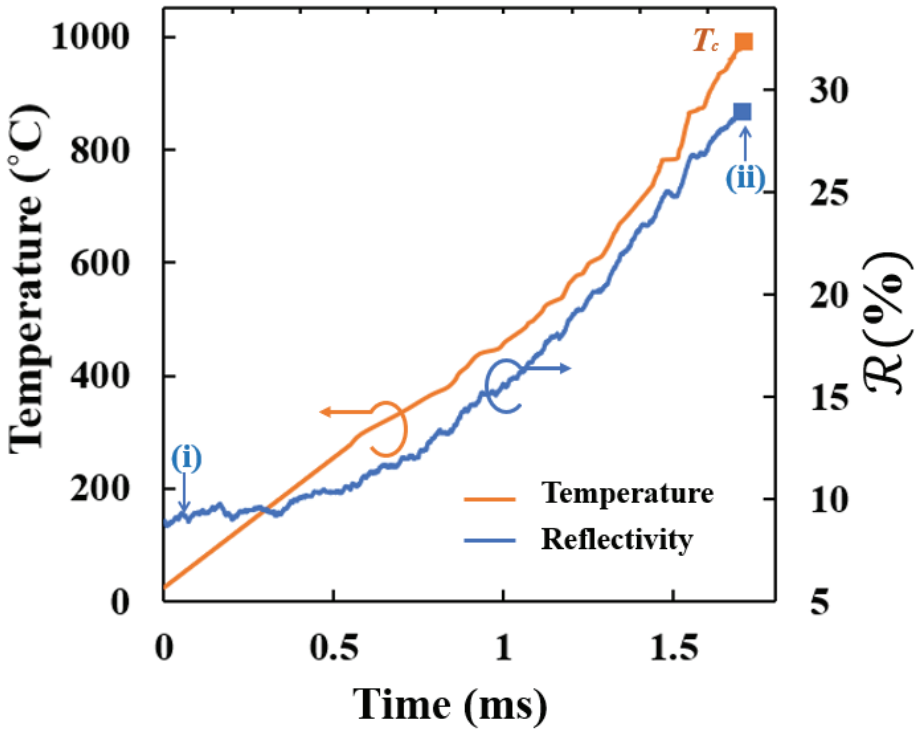
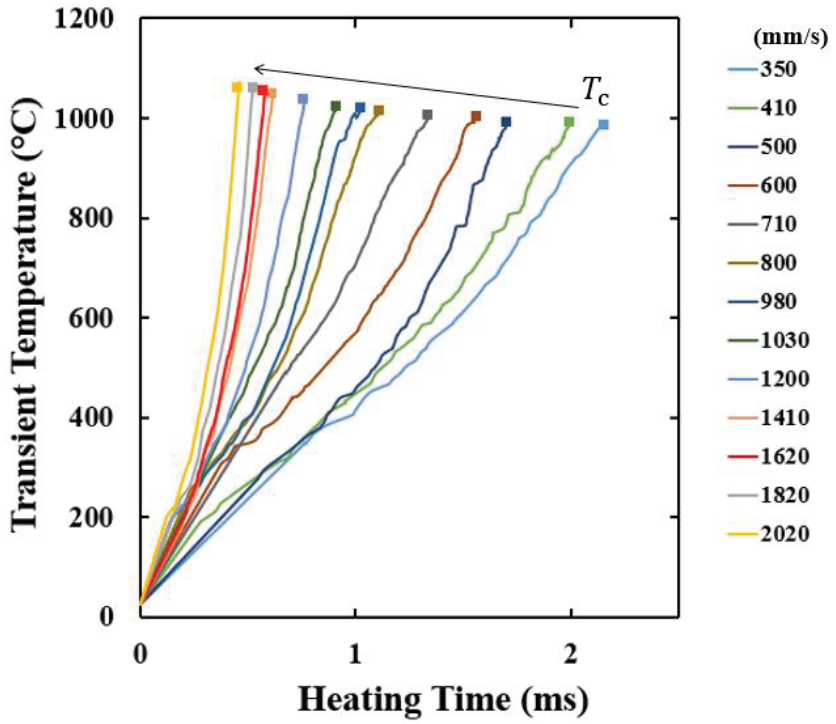


Fig.3.5. Transient variation of temperature and the transient $\mathcal{R}$ of a-Si film depend on heating time before the onset of SPC deducted from Fig. 2.4 (i) to (ii). The μ-TPJ conditions were P = 0.61 kW, f_{Ar} = 1.0 L/min, d = 1.0 mm, and v = 500 mm/s [6].

We applied the present temperature analysis method to millisecond SPC samples crystallized at different v and P, the dependence of T_c on R_h are summarized in Fig. 3.6.

(a)



(b)

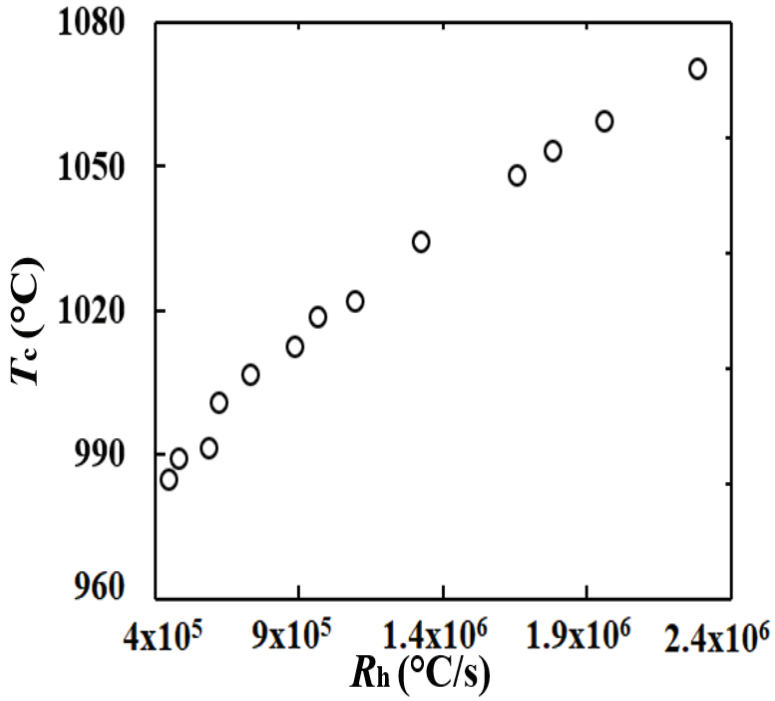


Fig.3.6. (a) the transient variation of a-Si temperature measured under different v and P depends on heating time, ■ marks indicate the T_c, (b) dependence of T_c on R_h [6].

The Fig. 3.6 (a) shows the transient variation of a-Si temperature measured under v from 350 to 2020 mm/s. It is clearly seen that the T_c increases from 985 to 1071 ºC with the decreasing heating time from 2.155 to 0.458 ms. In other words, the R_h increases from 4.45×10^5 to 2.28×10^6 K/s. For our knowledge, this is the first experiment result reporting the temperature of nucleation in millisecond annealing.

As we know, SPC of a-Si involves two distinct processes, namely the nucleation of seeds (formation of clusters of crystalline silicon) and their growth to polycrystalline films[7]. According to classical nucleation theory, only seed nuclei increase to critical sizes can transfer to polycrystalline, other nuclei come back to amorphous phase. The time for nuclei gets critical sizes called incubation time. The incubation time reduces with the increase of heating rate.

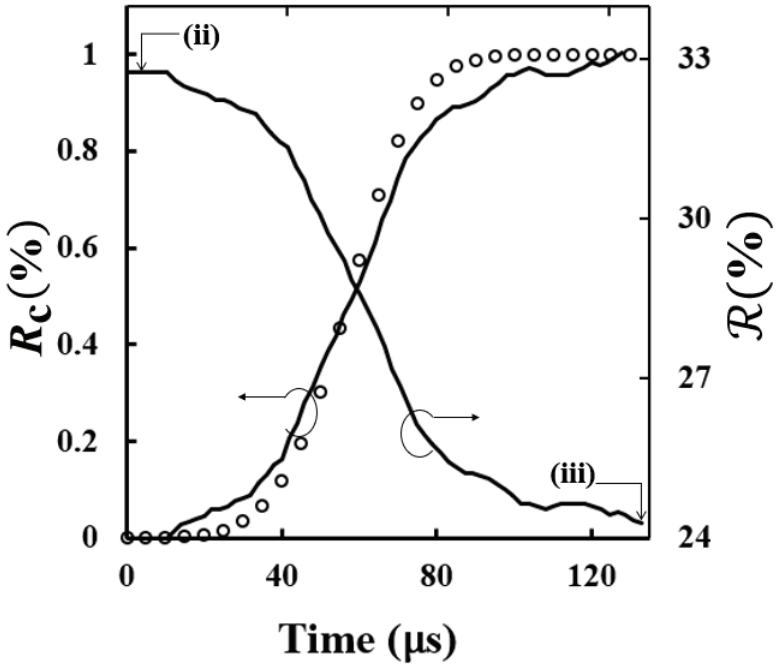
As reported in other publications, the concentration of hydrogen also effects on crystallization process [8]. Budini *et al.* [8] claimed that a higher hydrogen concentration leads to a faster crystallization. The presence of Si-H_n bonds leads to the production of atomic H during the SPC process. The interaction between H and Si-H bonds gives as a result minuscule crystallites in a very high density which prevent grains to grow to a considerable size, resulting in a nanocrystalline material with grain sizes in the rage of 24 - 28 nm[8]. In our experiments, a-Si films were prepared by using PECVD with SiH_4 and H_2 at 250 ºC, then dehydrogenation was carried out in N_2 ambient at 450 ºC in 1 hour. According to Budini *et al.*[8], after dehydrogenation process, hydrogen concentration in samples is lower than 5 %. However, the further research about the influence of hydrogen concentration on crystallization process at high temperature is not carried out in this thesis.

3.3.3. Characteristic crystallization time

Characteristic crystallization time t_c is the time required to crystallized 67 % volume of sample.

In Fig. 2.3, the transient $\mathcal{R}$ from point (ii) to (iii) reflects the phase transformation of amorphous to crystalline. We consider the film as a homogeneous optical medium with an optical constant equal to a linear combination between amorphous and crystalline Si values [9]. We assumed that at point (ii), the total volume is in an amorphous state, at point (iii) all the volume is transferred to polycrystalline. Based on the above assumption, the measured $\mathcal{R}$ can be converted into volume fraction of crystalline. Figure 3.7 (a) and (b) show examples of $\mathcal{R}$ and R_c as functions of time during phase transformation when SPC film was formed by μ-TPJ irradiation under v at 500 mm/s and 800 mm/s, respectively. From these figures, we can find the t_c as 60 and 36 μs when v as 500 and 800 mm/s, respectively.

(a) v = 500 mm/s



(b) v = 800 mm/s

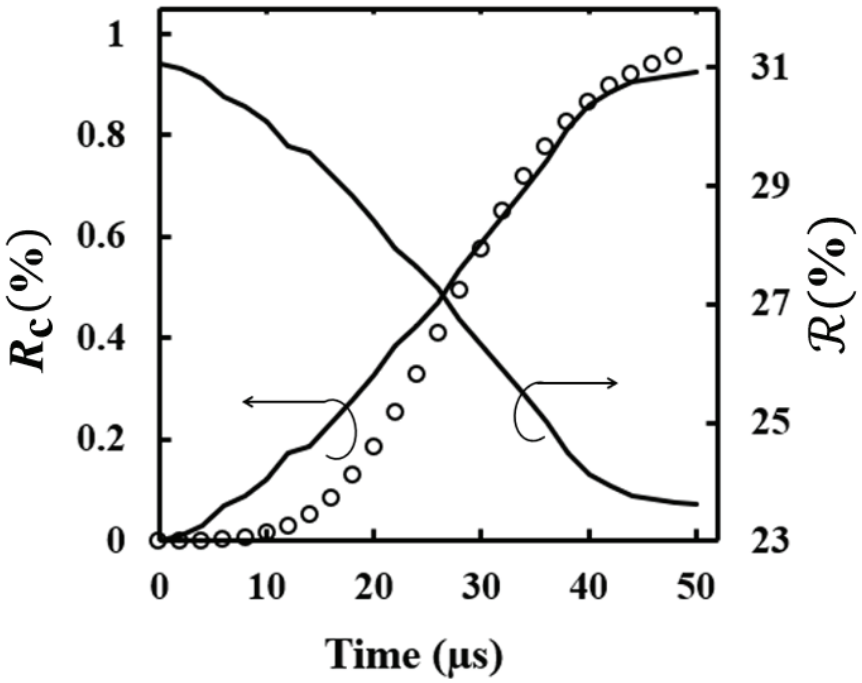


Fig. 3.7. $\mathcal{R}$ and R_c as a function of time during phase transformation when the a-Si film was annealed by μ-TPJ under v as 500 mm/s (a) and 800 mm/s (b), respectively. Solid lines show transient $\mathcal{R}$ shown in Fig. 2. 3 (ii) to (iii) and extracted crystalline volume fraction R_c. The dotted line is the calculation data of R_c based on the proposed model in section 3.3.3 [(6)].

The t_c as a function of T_c, determined in the same way, is plotted in Fig. 3.8. The value of t_c decreases from 95 to 20 μs when the T_c increases from 985 to 1071 ºC. It is extremely shorter than that at 600ºC. The activation energy E (solid line) is 2.9 eV. According to the definition of t_c in classical nucleation theory, it is proportional with the product of nucleation rate (r_n) and growth velocity (v_g) as $t_c \sim \left(r_n \times v_g^2\right)^{-1/3}$ [9]. Therefore, the E found from Fig. 3.8 relates to both nucleation and crystal growth.

According to Iverson et al., at low temperatures regions the maximum free energy ΔG* for the cluster formation is 2.4 eV and activation energy for growth process is 3.3 eV[9]. Therefore, at high temperature region, the nucleation process with high nucleation frequency is a primary process. As a result, the final grain size will be small.

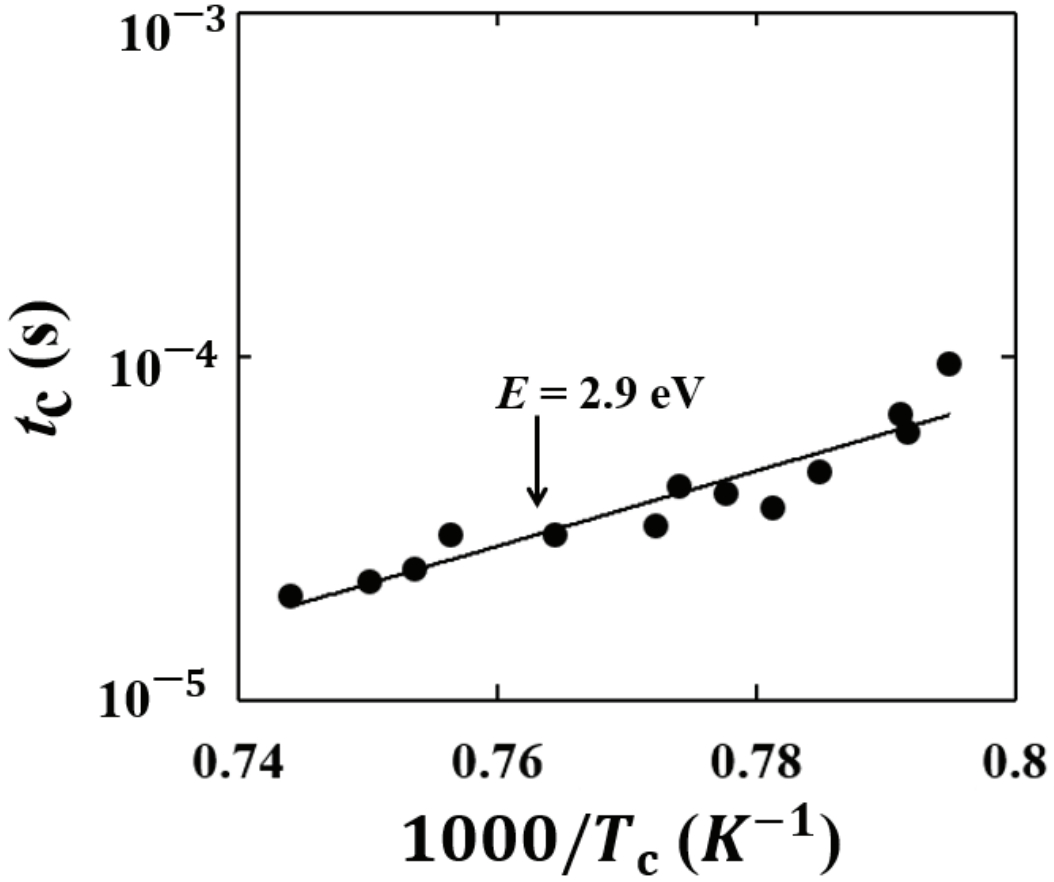


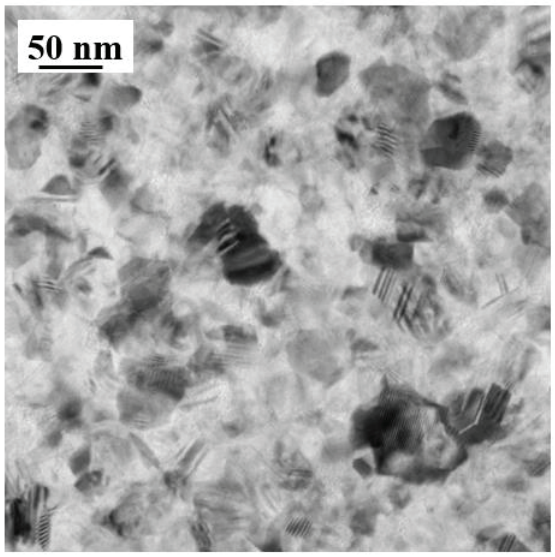
Fig. 3.8. Characteristic crystallization time t_c as a function of T_c. The solid line was fit to the data of this work and corresponds to an activation energy of 2.9 eV [6].

3.3.4. Grain size

HRTEM observation was performed to investigate the grain size of millisecond SPC films. To perform HRTEM measurement, the area of 1.0 x 1.0 cm^2 was crystallized by overlapping the scanning steps with a 50 μm pitch. Two samples with v as 500 and 800 mm/s were prepared. Figure 3.9 (a) shows the HRTEM image of SPC films when v is 500 mm/s (R_h = 5.66 x 10^5 K/s) and Fig. 3.9 (b) show that of sample when v is 800 mm/s (R_h = 8.86 x 10^5 K/s).

From the HRTEM images, we can observe very small grains, however, it is difficult to determine exactly the average value of grain size from these images. When v is 500 mm/s, a rough estimation of grain size distribution from 30 to 60 nm. When v increases to 800 mm/s, the most of grain is smaller than 20 nm. It is clearly seen that the decrease in grain size is related to increasing of v.

***(a) v* = 500 mm/s**



***(b) v* = 800 mm/s**

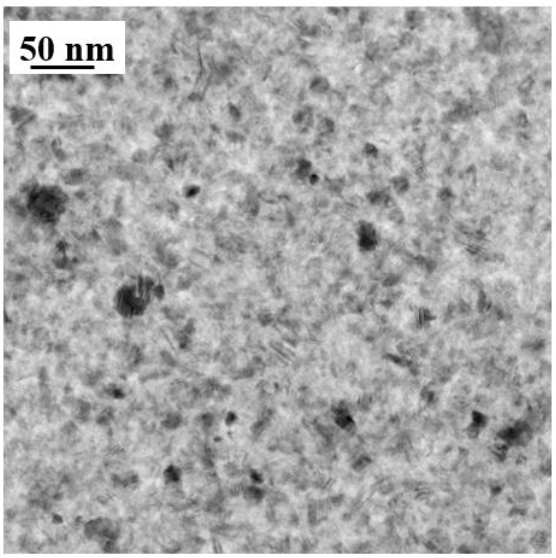


Fig. 3.9 HRTEM images of solid-phase crystallized a-Si films annealing by μ-TPJ at *v* of 500 mm/s (a) and 800 mm/s (b), respectively [(6)].

Figure 3.10 shows the selected area electron diffraction patterns for SPC film crystalized at *v* of 500 mm/s (a) and precursor a-Si film (b).

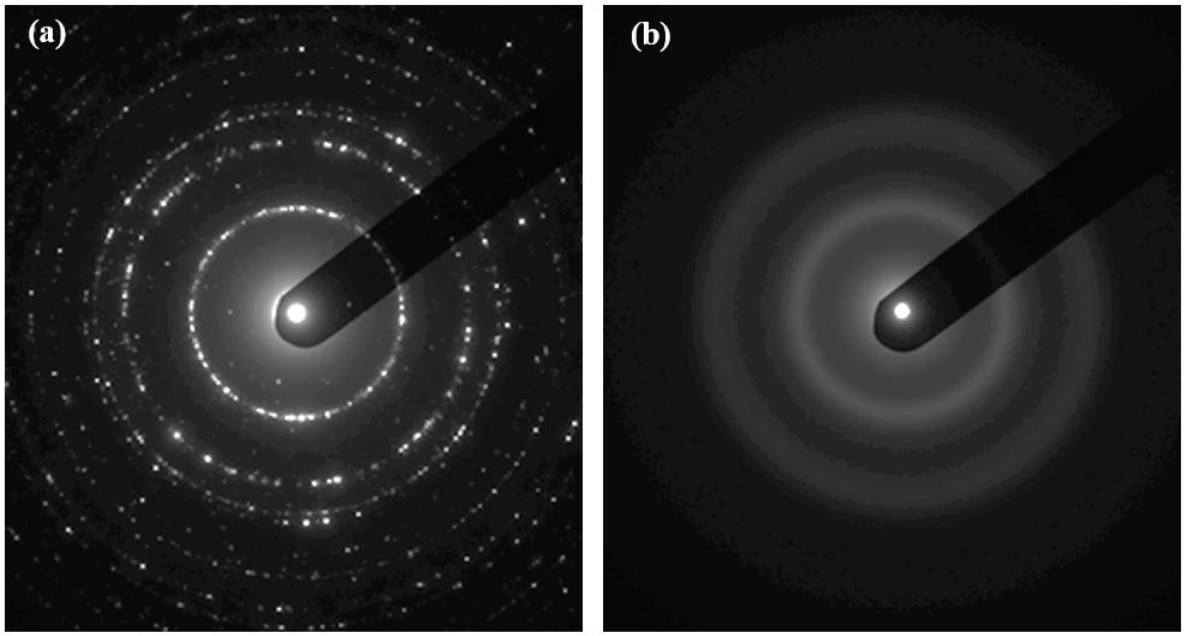


Fig. 3.10. The selected area electron diffraction patterns for SPC film crystalized at *v* of 500 mm/s (a) and precursor a-Si film (b) [(6)].

We can confirm many bright spots in Fig. 3.10 (a) reflecting diffraction from each crystalline grain. Here we see no halo rings. This means the film is in crystalline at least from a microscopic viewpoint. Because the heat flow from μ-TPJ is the highest in a center part and decreases when going to the edges of the crystallization area, there is a distribution of crystallinity. Due to very small beam spot, HRTEM can concentrate on the sample surface position which has the highest crystallinity. However, the Raman measurement with the laser spot size as 10 μm, which is much larger than electron beam spot, the spectra reflect both the area with low crystallinity and amorphous phase outside the 100-μm-crystallization area. This is reason why the Raman and HRTEM result indicate different crystallinity.

3.3.4. Growth mechanism

We suppose a simple physical model to estimate the crystal grain size based on the classical nucleation theory. Iverson *et al.* [(9)] gave the equation showing the dependence of r_n on temperature T as $r_n=10^{37}\exp(-5.1\ \text{eV}/kT)$ (events/cm^{3}s), where k is Boltzmann constant. In

addition, v_g as function of temperature was indicated by Zellama *et al.* [11], $v_g=10^{13}\exp(-2.4\ \text{eV}/kT)$ (nm/s). We assume that R_h will be constant during the phase transformation process. The time for completed crystallization is divided into small fractions with step Δt. At the $t_o = 0$ μs, the temperature of a-Si film reaches T_c (corresponds to Fig. 3.6), no crystal inside the volume. After Δt μs, temperature increases, the number of nuclei N_1 appears inside the volume and grows with velocity $v_{g1,}$ and the volume of a-Si reduces. After $2\Delta t$ μs, the temperature raises up, N_2 nuclei additionally appear and grow with velocity v_{g2}. In addition, N_1 nuclei in the previous time step continue to grow with the same velocity v_{g2}. The volume of a-Si keeps on reducing. This process will be continued until the crystal grains fill out the considering volume and no appearance of a-Si.

The volume of crystal (V_c) is calculated as follows

At $t = t_o = 0$: temperature $T_o = T_c$: before the onset of nucleation.

At $t_1 = t_o + \Delta t$: temperature $T_1 = T_o + R_h\Delta t$: nucleation starts.

The length of crystal growth or grain size $l_1^0 = v_{g1}\Delta t$ (nm).

During this time, the number of nuclei N_1 in considering volume V is $r_{n1}V\Delta t$ (nuclei).

The V_{c1} at t_1 is

$$V_{c1} = \frac{4}{3}\pi\left(\frac{l_1^0}{2}\right)^3 N_1 \qquad (3.\ 13).$$

At $t_2 = t_o + 2\Delta t$: temperature $T_2 = T_o + 2R_h\Delta t$,

The length of crystal growth or grain size l_2^0 is $v_{g2}\Delta t$ (nm).

The number of nuclei N_2 in the rest of considering volume V is $r_{n2}(V - V_{c1})\Delta t$ (nuclei).

N_2 nuclei occupies a volume as

$$\frac{4}{3}\pi\left(\frac{l_2^0}{2}\right)^3 N_2 \qquad (3.\ 14).$$

In addition, N_1 nuclei in the previous time step continue to grow with v_{g2} and reach the size $l_1^1 = l_1^0 + v_{g2} \times \Delta t$.

The V_{c2} is

$$V_{c2} = \frac{4}{3}\pi\left(\frac{l_2^0}{2}\right)^3 N_2 + \frac{4}{3}\pi\left(\frac{l_1^1}{2}\right)^3 N_1 \quad (3.15).$$

……

The crystalline volume is calculated as

$$V_c = V_{cn} = V \quad (3.16).$$

Finally, we have a distribution of grain size. The final grain size r is average of grain size as following calculation

$$r = \frac{N_1 \times l_1^{n-1} + N_2 \times l_2^{n-2} + N_3 \times l_3^{n-3} + \cdots + N_n \times l_n^0}{N_1 + N_2 + N_3 + \cdots + N_n} \quad (3.17),$$

with l_1^{n-1}, l_2^{n-2},..., l_n^0 is the grain size of N_1, N_2,...,N_n nuclei at the final time step, respectively.

In addition,

$$R_c = \frac{V_c}{V} \quad (3.18).$$

Figure 3.11 shows an illustration of this model.

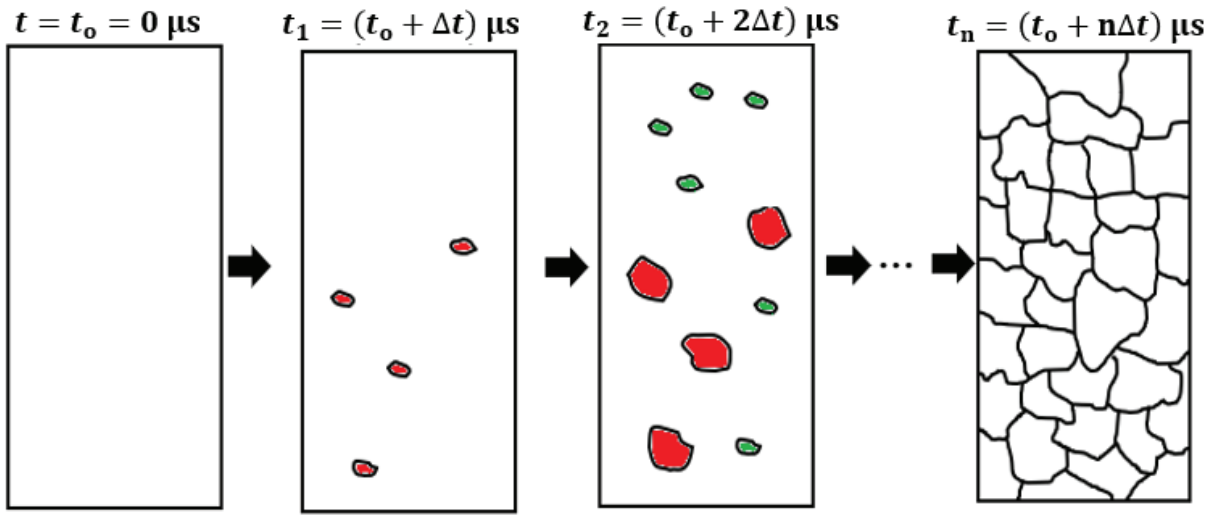


Fig. 3.11. Physical model of grain size estimation [6].

Based on the calculation, it is easy to obtain that R_c and r do not depend on the value of considering volume. In our experiments, a-Si films thickness was 150 nm, the length of crystallization region is 1 cm and its width is 100 μm due to the size of sample and diameter of μ-TPJ orifice. Thus, we consider the 1.5 x 10^{14}-nm^3-volume of sample. First, when v as 500 mm/s (R_h = 5.66 x 10^5 K/s) is considered. The chosen Δt is 5 μs. Using the equation of Iverson and Zellama, at t_1 is 5 μs, N_1 and l_1^0 are 683 nuclei and 0.01 nm, respectively. However, at this temperature, the critical radius of nuclei r^* at a critical cluster size i^* is

$$r^* = \sqrt[3]{\frac{3 \times i^* \times a^3}{4\pi}} = \sqrt[3]{\frac{3}{4\pi} \times \frac{32}{3} \pi \frac{\sigma_{ca}^3}{\Delta g_v^3} \times a^3} = 0.63 \text{ (nm)} \qquad (3.19)$$

with σ_{ca} = 0.105 eV/atom [25], Δg_v = 0.09 eV/atom [12-14]. Therefore, l_1^0 is much smaller than r^*. According to classical nucleation theory, the crystal with this size does not exist. Thus, the classical model needs to be modified in our cases. In this study, we increase the pre-exponential factors in r_n and v_g equation as r_{no} = 3.3 x 10^{40} nuclei/(cm^3s) and v_{go} = 4.2 x 10^{15} nm/s, respectively. In addition, when the volume of the sample is filled with crystal, the velocity growth will be decreased because of the collision between the crystals. Since we introduce the factor (1 - R_c) to v_g equation to describe the reducing of velocity. The dots in Fig. 3.7 shows the calculation results of R_c as a function of time when v is 500 mm/s (a) and 800 mm/s (b), respectively. The time step is 5 and 2 μs when v is 500 and 800 mm/s, respectively. These values are the same as the sampling time of transient $\mathcal{R}$ in two cases. As can be seen from these figures, the assuming v_{go} and r_{no} give the best fitting between experimental and simulation data. Moreover, these values are so sensitive. For example, if we keep the same value of Δt and r_{no}, only v_{go} is changed to 4.0 x 10^{15} or 4.5 x 10^{15} nm/s, the error increases significantly and the fitting to the experimental curve obviously degrades.

From the theoretical calculation, when v is 500 mm/s (R_h = 5.66 x 10^5 K/s,) the grain size varies from 3 nm to 36 nm, and r is 20 nm. In case v is 800 mm/s (R_h = 8.86 x 10^5 K/s), the grain size varies from 1 nm to 20 nm, and r is 16 nm. The r decreases with the increase of R_h. In our assumption, the Δt can be explained as incubation time because it is the time required for the growing of nucleation, during Δt the nucleation is prohibited. When R_h increases, the Δt decreases. It is explained by the required time for nuclei growing decreases at high temperature. This estimated r is fairly agreed with HRTEM observation shown in Fig.3.9.

3.4. Summary

Based on the transient reflectivity obtained in Chapter 2, we succeed in estimate the T_c of a-Si films and t_c. When R_h increases from 4.45×10^5 to 2.28×10^6 K/s the T_c increases from 985 to 1071 °C. The small size of the laser spot, 20 μm, makes the results more confident. The t_c was pointed out by using the TRR method as the function of T_c corresponds to activation energy 2.9 eV. A simple theorical model is suggested to explain the kinetics of millisecond SPC film formed by μ-TPJ at high temperature. The calculated results from our model are quite suitable with experimental results.

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Chapter 4

Characteristics of Millisecond Solid Phase Crystallization of Phosphorous Doped Silicon films

4.1. Introduction

In chapter 2 and 3, the mechanism of millisecond SPC film formed by μ-TPJ at high temperature was investigated. Based on that, when films are annealed at high v, r_n and v_g are high, it makes the smaller grain size. Therefore, we can control the grain size of the crystallized films by controlling experimental conditions such as v. The average grain size of millisecond SPC film is smaller than 50 nm [(1)].

A μ-TPJ annealing technique was applied to activate dopants for the source/drain (S/D) region of TFTs [(2)]. The crystallization and activation can be performed simultaneously by μ-TPJ irradiation to intrinsic Si films on heavy-doped S/D island. In previous studies[(2)], 60-nm-thick phosphorous-doped a-Si films were prepared by PECVD using SiH_4 and PH_3 gases diluted with H_2. The doped a-Si films were annealed by μ-TPJ under different conditions. By this method, the dopant activation efficiency achieved 82 % at a 1 % PH_3 concentration of 31 % [(2)]. It suggested that many phosphorous atoms with above the thermal equilibrium solid soluble limit were activated by non-equilibrium phase transformation of Si film. The cooling rate after annealing affected the carrier concentration accompanying with the activation rate [(2)]. The results indicate that TPJ millisecond annealing is very effective for activating dopants in S/D regions of TFTs.

In this chapter, the characteristics of millisecond SPC of double layer structure as phosphorous doped silicon (P-doped-Si) deposited on a-Si films induced by μ-TPJ will be investigated.

4.2. Experimental procedure

In our research, sample structure is 30-nm-thick of a-Si film deposited on 30-nm-thick of phosphorous-doped a-Si film (a-Si/P-doped a-Si) deposited on 525-μm-thick quartz substrate. After the wet chemical cleaning of quartz substrate, 30-nm-thick of P-doped a-Si was

deposited by using PECVD with SiH_4, H_2, and PH_3 at a substrate temperature of 200 °C. Then, PECVD was performed once more to make 30-nm-thick non-doped a-Si film using SiH_4 and H_2 at a substrate temperature of 250 °C. After dehydrogenation in N_2 ambient at 450°C for 1 hour, the samples were crystalized by µ-TPJ under different experimental conditions. The illustration of experimental set-up for annealing samples is indicated in Fig. 4.1. The samples were fixed in a motion stage which moved linearly in front of µ-TPJ. The *P* changed from 0.73 to 1.05 kW. The *ES* was 2.0 mm and the *d* was fixed at 1.0 mm. The f_{Ar} was 1.0 L/min. The thermal plasma was blowing out through an orifice with the diameter (ϕ) of 600 µm. The crystallized films were formed by overlapping the scanning steps with a 50 µm pitch. Then, the characteristics were investigated by optical microscopy, micro-Raman spectra, atomic force microscopy (AFM), and Hall effect measurement.

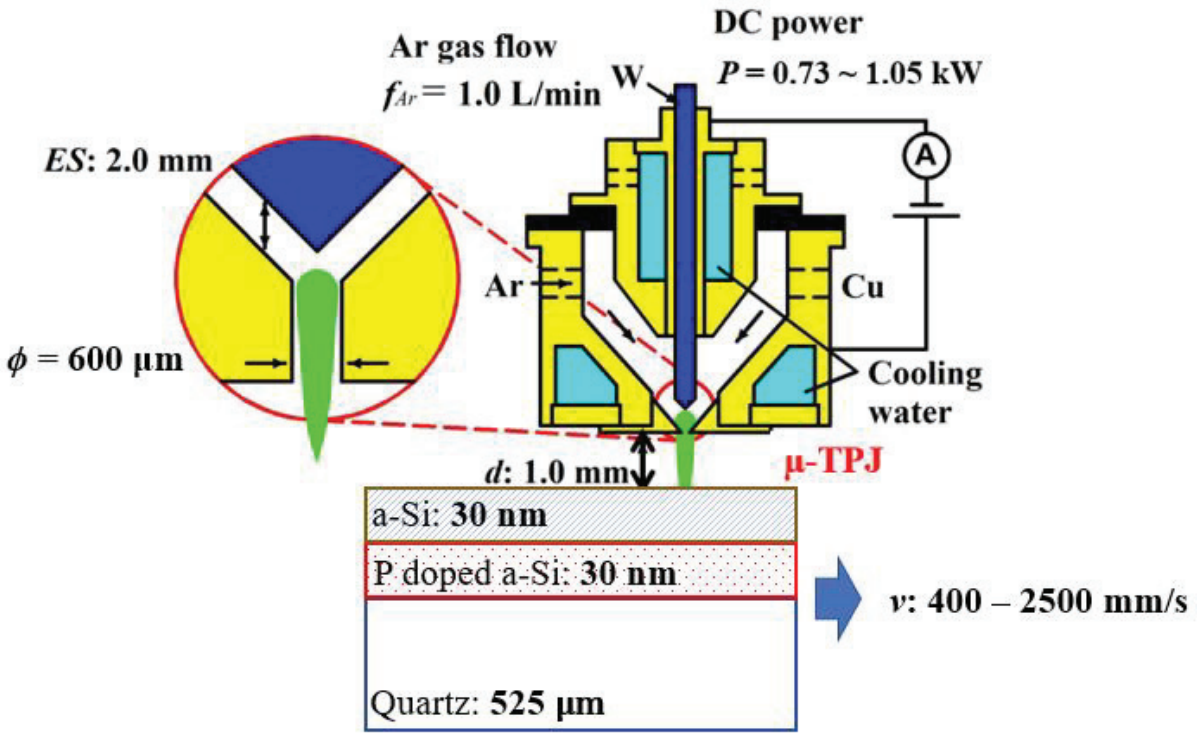

Fig. 4.1. Illustration of experimental set-up for annealing samples by µ-TPJ [3]. (Copyright (2021) The Japan Society of Applied Physics)

4.3. Results and discussion

4.3.1. Phase diagram

The phase diagram of μ-TPJ irradiated a-Si/P-doped a-Si film with respect to *P* and *v* is indicated in Fig. 4.2.

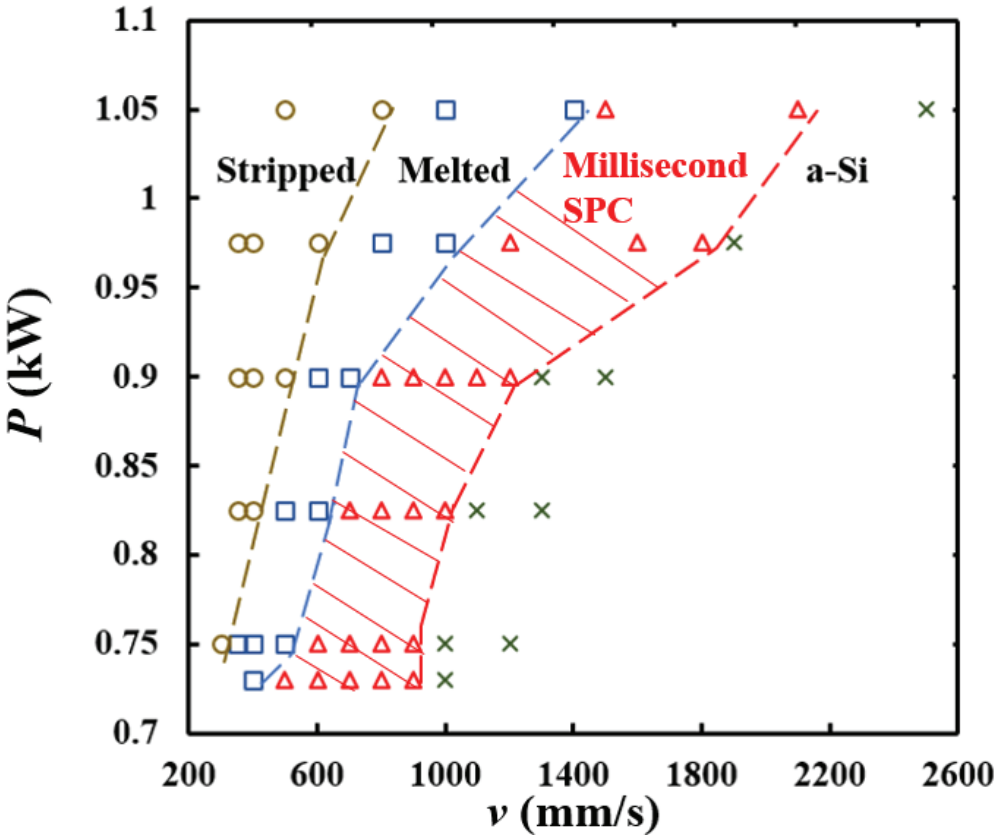

Fig. 4. 2. Phase diagram of μ-TPJ irradiated a-Si/P-doped a-Si films with respect to *P* and *v* [3]. (Copyright (2021) The Japan Society of Applied Physics)

As can be seen, with an increase in annealing temperature, namely increase *P* or decreased *v*, the phase of the film changes in the order of amorphous, millisecond SPC, melt and regrowth, and stripped. The millisecond SPC is always formed in between conditions of amorphous and melt and regrowth. It is easily to obtain that each crystallized Si film was independently formed by control of μ-TPJ irradiation conditions such as *P* and *v*. According to Nguyen *et al.* [1], the millisecond SPC film formed under slow *v* gives us better quality of

crystallinity and grain size. Therefore, in this research, we focused on crystallized film under conditions of μ-TPJ as *P* of 0.73 kW and *v* changed from 400 to 900 mm/s. Based on phase diagram, when *v* as 400 mm/s, the film was melted. When condition of *v* changed from 500 to 900 mm/s, the crystalized film was formed by millisecond SPC. The films are a-Si when crystallized under condition of *v* larger than 900 mm/s.

The optical microscopy images of crystallized film formed by conditions of *v* as 400 and 500 mm/s are shown in Fig. 4.3(a) and (b) respectively. We confirmed dendritic morphology, which is frequently observed when the grain growth is induced by lateral movement of the molten region as show in Fig. 4.3(a) [(4)]. In contrast, millisecond SPC film show no remarkable morphology because of the small grain size as shown in Fig. 4.3(b).

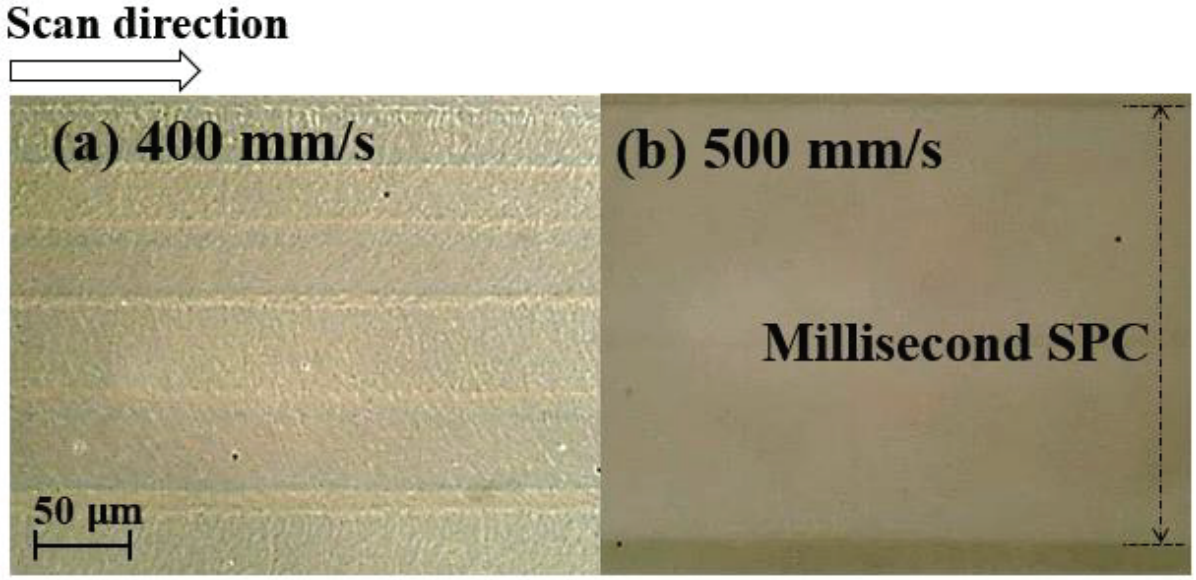

Fig. 4. 3. Optical microscopy images of crystallized samples annealed by μ-TPJ irradiation under *v* of (a) 400 mm/s and (b) 500 mm/s [(3)]. (Copyright (2021) The Japan Society of Applied Physics)

4.3.2. Surface roughness

AFM images of crystallized samples under the condition of *v* as 400, 500, and 600 mm/s are indicated in Fig. 4.4 (a), (b), and (c), respectively. Root mean square (RMS) roughness was obtained using 5x5μm^2 scan window size. When *v* as 400 mm/s, film was melted, and the value of RMS is 2.56 nm. When *v* = 500 and 600 mm/s, namely that millisecond SPC film was formed, RMS values is largely decreased to 0.61 and 0.31 nm, respectively. The maximum heights of the surface feature were 19, 5, and 3 nm when condition of *v* as 400, 500, and 600 mm/s, respectively. It can be easily to obtain, millisecond SPC samples surface reduces more than 76 % roughness compared to the case of melted sample. The evolution of the surface morphology of thin film can show scaling characteristics that are directly related to the growth processes occurring during film growth. When *v* is 400 mm/s, film is melted and recrystallized from liquid phase. A long grain growth was caused by a strong lateral temperature gradient of the molten region. Therefore, the sample surface is rough. As mentioned before, the increase of *v* makes the increase of nucleation temperature. For that reason, the final grain size of crystallized films induced at high *v* is smaller and surface is smoother. As reported in our previous work [(1)], in case of *v* = 500 mm/s, the grain size distribution was from 30 to 60 nm.

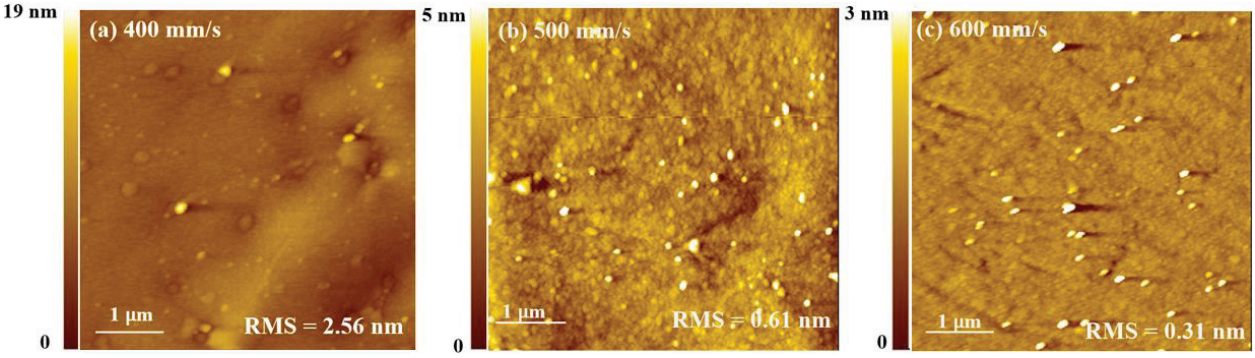

Fig. 4.4. Atomic force microscopy results of crystallized samples under the conditions of *v* as (a) 400 mm/s, (b) 500 mm/s, and (c) 600 mm/s [(3)]. (Copyright (2021) The Japan Society of Applied Physics)

4.3.3. Crystallinity

The crystallinity of film is estimated from micro-Raman spectroscopy which was shown in Fig. 4.5. We used Ar laser with wavelength at 514.5 nm, laser power of 23 mW and laser spot size of 10 μm. The melted film under *v* of 400 mm/s shows a peak position of 511.4 cm^{-1}, a FWHM of 8.87 cm^{-1}, and R_c of 72 %. It is easily observed that the Raman peak intensity is decrease, more asymmetric, and the width is larger with the increase of *v*. Therefore, the R_c degrades with the increase of *v*. It is caused by millisecond SPC films composed of microcrystalline grain with the typical size of ~ 20 nm[5, 6]. However, when millisecond SPC film formed under condition of *v* of 500 mm/s, R_c still reached up to 61% with peak position of 511.7 cm^{-1} and FWHM of 9.14 cm^{-1}. This result suggests that millisecond SPC film formed at slow *v* have good crystalline quality. Comparing with conventional SPC at typical temperature as 630 ºC, it takes 5 hours to make SPC film with crystalline fraction of 28% [7]. According to results in Chapter 3, the nucleation temperature of millisecond SPC films formed by μ - TPJ is very high as 1000 ºC.

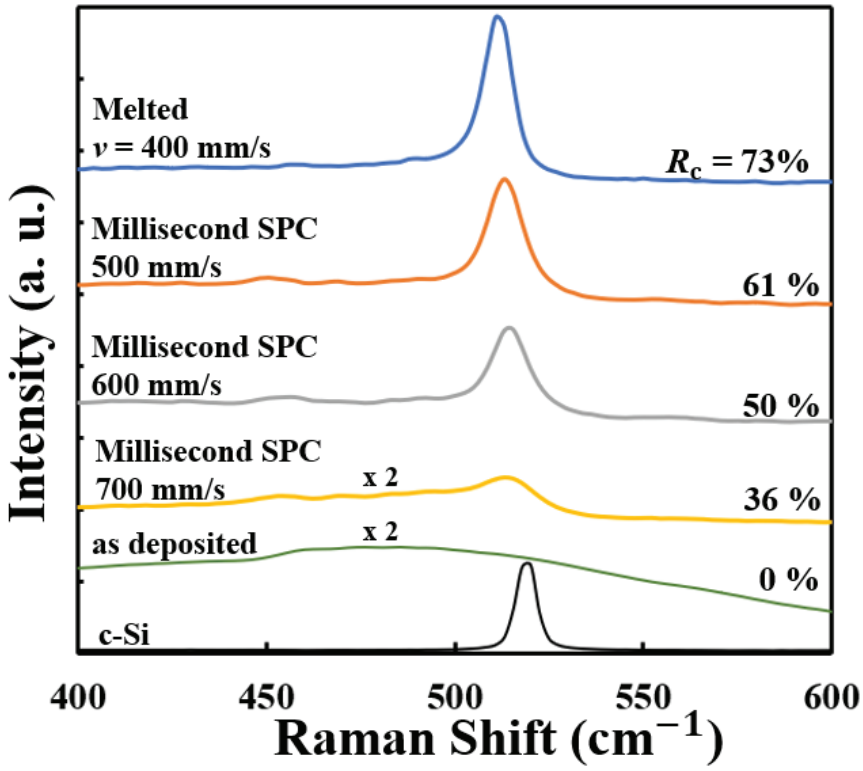

Fig. 4.5. Raman scattering spectra obtained from crystallized films formed by μ-TPJ under the different conditions of v [3]. (Copyright (2021) The Japan Society of Applied Physics)

As our knowledge, SPC Si films formed in millisecond annealing at high temperature have not been studied in detail. Therefore, present study gives us a new insight that millisecond SPC Si films formed at high temperature could have high crystallinity closer to that of Si films formed by melting and solidification process. Millisecond SPC is a new approach and a new finding that we can obtain fairly high crystallinity.

4.3.4. Hall effect measurement's results

Resistivity, carrier concentration and carrier mobility were obtained from Hall effect measurement. Resistivity measurements confirm the high activation level of dopant element. The evolution of the resistivity with v is shown in Fig. 4.6 (a).

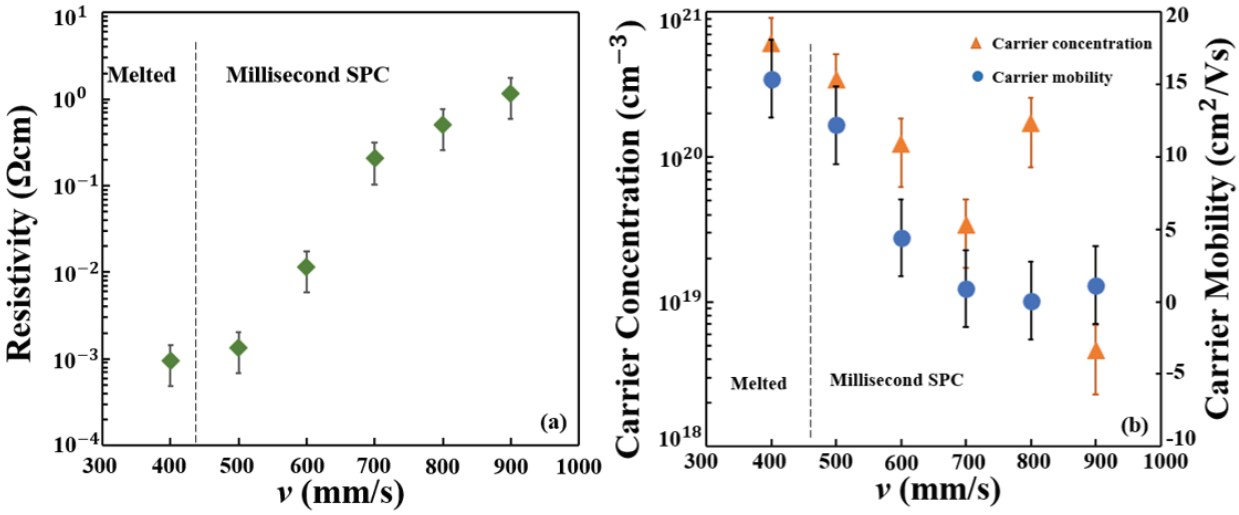

Fig. 4.6. (a) resistivity (b) carrier concentration and carrier mobility of melted sample and millisecond SPC samples obtained from Hall effect measurement. The μ-TPJ conditions were P = 0.73 kW, f_{Ar} = 1.0 L/min, d = 1.0 mm, ES = 2.0 mm, v = 400 – 900 mm/s [3]. (Copyright (2021) The Japan Society of Applied Physics)

The resistivity significantly increases with the increase of v. This behavior is caused by the diffusion and subsequent activation of phosphorus atoms into silicon. However, it is easily observed that there is not significant different in resistivity when crystallized films were formed under melted condition with v at 400 mm/s and millisecond SPC condition with v at 500 mm/s. The value of resistivity is 9.6 x 10^{-4} and 1.36 x 10^{-3} Ωcm when condition of v as 400 and 500 mm/s, respectively. These values are a little higher than resistivity of poly-Si film formed by other low temperature poly-silicon process. For instance, according to T. Noguchi [8], the lowest resistivity of P-doped -Si film formed by excimer laser annealing with pulse energy density of 350 mJ/cm^2 is 4.2 x 10^{-4} Ω.cm. In principle, these values are suitable for transistor fabrication. Carrier concentration and carrier mobility are shown in Fig. 4.6 (b). Both increase with the decrease of v. This behavior can be attributed to an increase in the solubility of phosphorous into silicon and the increase in activation efficiency. The value of carrier concentration was 6.09 x 10^{20} cm^{-3} when v as 400 mm/s and 4.61 x 10^{18} cm^{-3} when v as 900 mm/s. In case of

carrier mobility, it is 16.3 cm^2/Vs when *v* as 400 mm/s, and comes to 1.15 cm^2/Vs when *v* as 900 mm/s. However, both of quantities is still high when millisecond SPC film was formed under *v* as 500 mm/s, carrier concentration is also around 3.41 x 10^{20} cm^3 and carrier mobility is 12.2 cm^2/Vs. Based on these results, the millisecond SPC film formed under *v* as 500 mm/s is potential material for small grain poly-Si TFTs.

4.4. Summary

We succeed in activation doped element in millisecond SPC film by μ - TPJ. The crystallized films formed under conditions closed with melted conditions shows high carrier concentration as 3.41 x 10^{20} cm^{-3}, high mobility as 12.2 cm^2/Vs , low resistivity as 1.36 x 10^{-3} Ωcm , and high crystallinity as 60%. When the *v* increases, the characteristics of crystallized films are worst.

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Chapter 5

Application of Millisecond Solid Phase Crystallization Silicon Film for Bottom-Gate Thin Film Transistors

5.1. Introduction

Bottom-gate TFTs have attracted much attention because of their advantages in industry [1-5]. As mentioned in Chapter 1, by using backside exposure of photoresist on the top of the plate, bottom gate acts as a mask to define the channel length [6,7]. With this approach, it only needs four masks which is the smallest mask number for TFTs fabrication process. Moreover, it is possible to fabricate bottom-gate TFTs, without ion implantation, by sequentially depositing doped amorphous silicon (a-Si) and intrinsic a-Si and removing the doped a-Si from the channel region [8-10]. Therefore, the product cost is reduced.

Based on our knowledge about millisecond SPC from previous chapters, in this chapter, the bottom-gate TFTs with millisecond SPC film as S/D and channel are fabricated. Our objective is that μ_{FE} of devices is larger than 20 cm^2/Vs and transfer characteristics show a small variation.

5.2. Experimental procedure

N-type bottom-gate TFTs were fabricated using millisecond SPC Si film crystallized by μ-TPJ irradiation by the procedure as shown in Fig. 5.1. 525-μm-thick quartz was used as the substrate. After RCA cleaning process, Mo film as gate was deposited by sputtering system. Its thickness was 100 nm. The gate pattern was formed by photolithography and wet etching by H_3PO_4 : HNO_3 : CH_3COOH : H_2O solution. Next, 200-nm-thick SiO_2 as an insulator layer was formed by remote PECVD at 350 ºC. Then, 30-nm-thick of P-doped a-Si was deposited by PECVD using SiH_4, H_2 and PH_3 with substrate temperature as 200 ºC. After back exposure with gate as a mask, chemical dry etching (CDE) using CF_4 and O_2 was done to remove P-doped a-Si film in the channel path. An intrinsic a-Si film with thickness of 10 nm was deposited by PECVD with SiH_4 and H_2 at 250 ºC. Photolithography and CDE were performed to make channel patterns. After dehydrogenation in N_2 ambient at 450 ºC for 1 h, a-Si/P-doped

a-Si was transferred to millisecond SPC by using μ-TPJ under conditions of P = 0.73 kW, f_{Ar} = 1.0 L/min, ES = 2.0 mm, d = 1.0 mm, and v from 400 to 900 mm/s. The electrodes of gate, source, and drain were formed by Al evaporation after opening the contact holes.

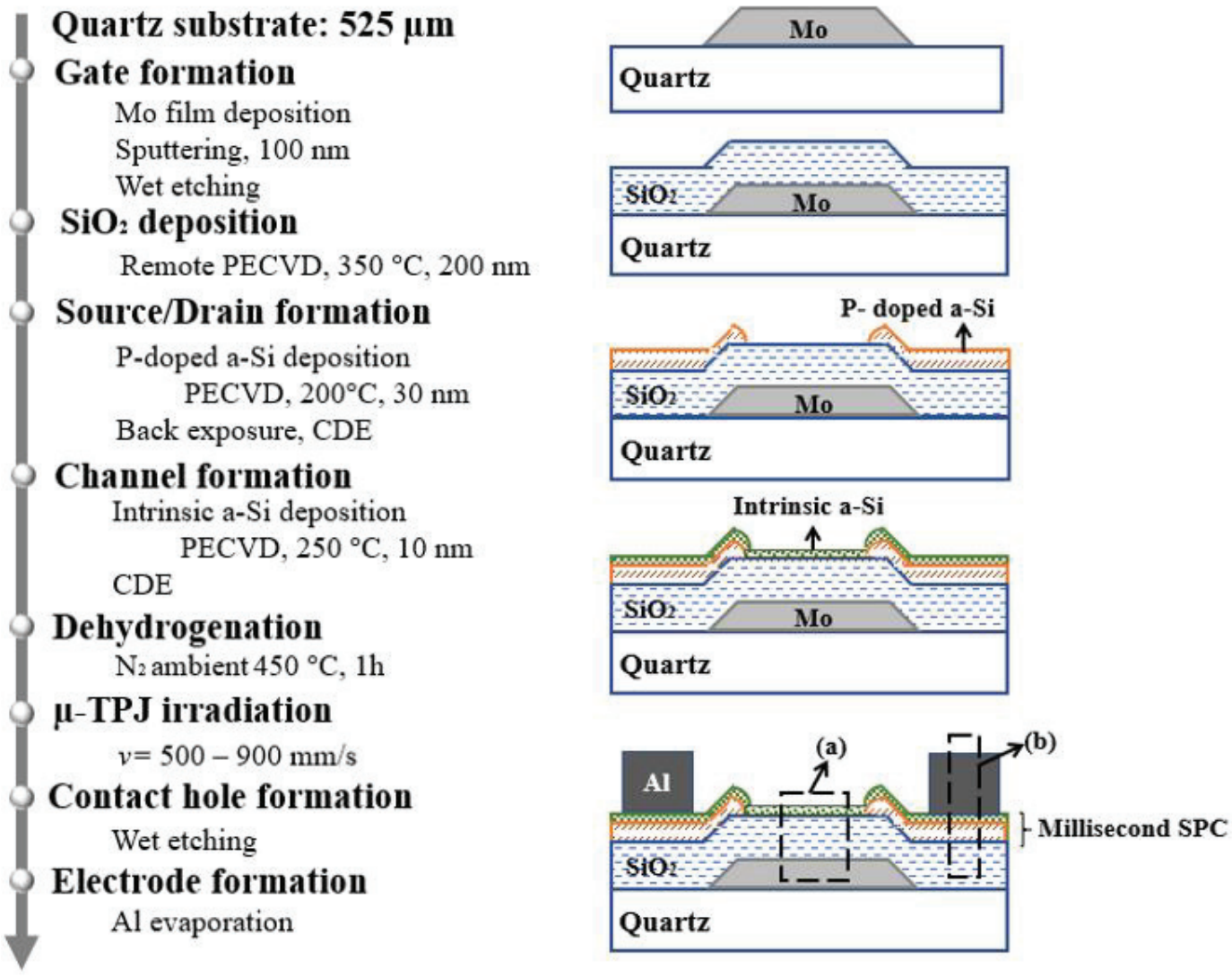


Fig. 5.1 Bottom-gate TFTs fabrication process and structure diagram of transistors [11]. (Copyright (2021) The Japan Society of Applied Physics)

5.3. Results and discussion

5.3.1. Cross-sectional image of bottom-gate TFTs

A cross sectional transmittance electron microscopy (TEM) of bottom gate TFT fabricated with millisecond SPC formed under v as 500 mm/s is shown in Fig. 5.2 (a) and (b). Figure 5.2 (a) shows the channel position and Fig. 5.2 (b) shows the S/D position as indicated in Fig. 5.1. The upper Pt and C layers are for antistatic and surface protection of the sample during TEM observation. According to TEM observation, the thickness of each layer is as following: Mo layer as 132 nm, SiO_2 layer as 210 nm, P-doped Si layer as 27.8 nm, and intrinsic Si layer as 7.7 nm at source/drain position. As can be seen in Fig. 5.2(a), the Mo surface is not flat, therefore the roughness of SiO_2 and millisecond SPC film is large. In the in-surface direction of millisecond SPC film, the contrast caused by the diffraction of crystals such as black and white part can be confirmed. There is no doubt that it is a crystalline Si film. Since the film thickness is very thin, we suggest that the crystallinity in the depth direction in the millisecond SPC film is very uniform. Due to very thin millisecond SPC - Si layer, it is very difficult to observe the interface by TEM.

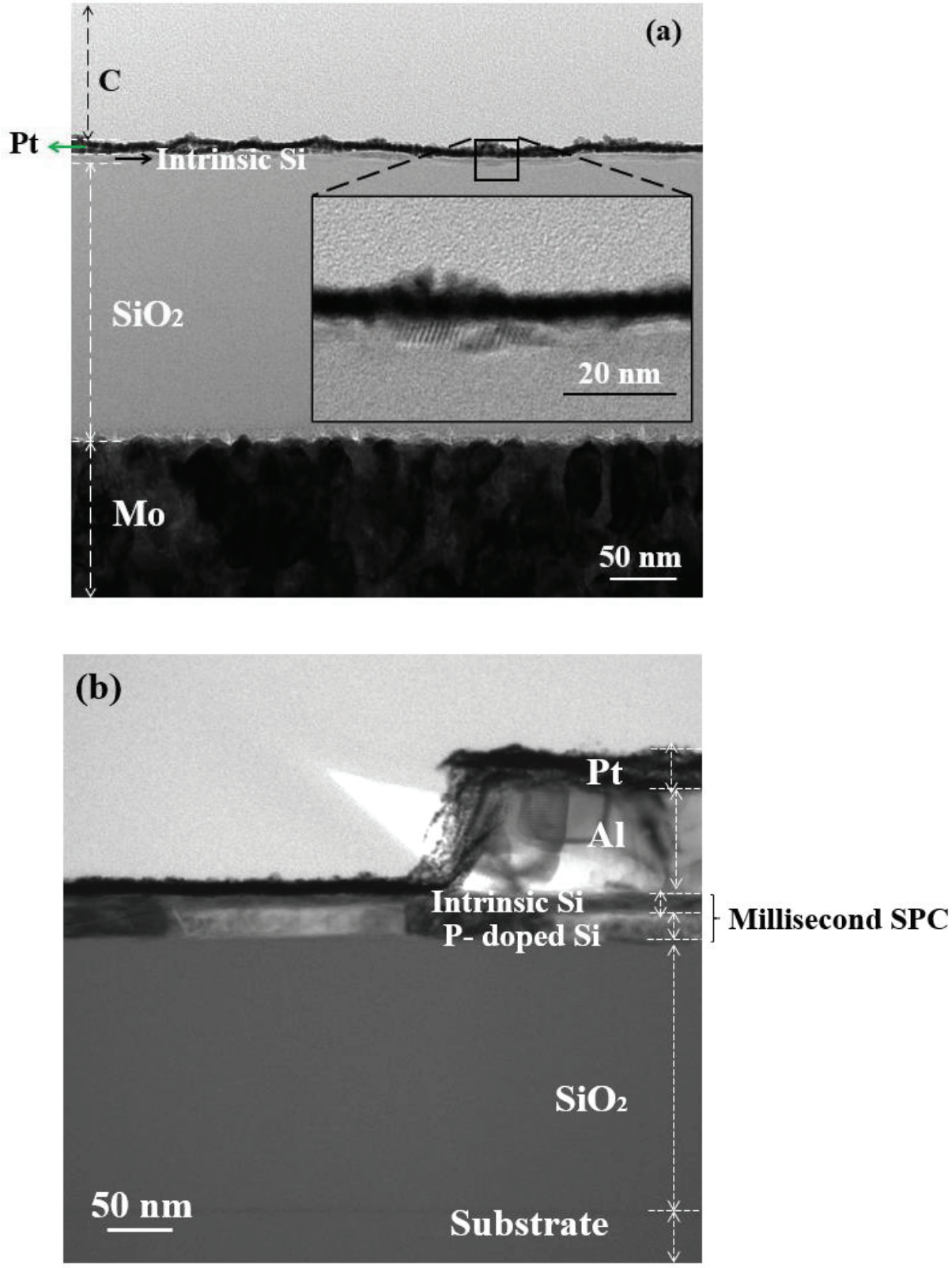


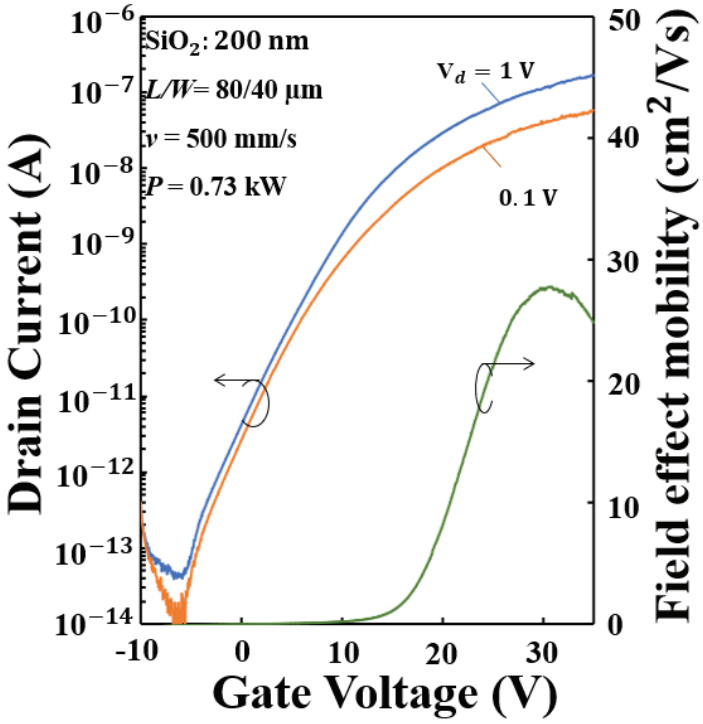
Fig. 5.2. A cross sectional TEM image of (a) channel position and (b) source/drain position of bottom gate TFT fabricated with millisecond SPC film formed under *v* of 500 mm/s [(11)]. (Copyright (2021) The Japan Society of Applied Physics)

5.3.2. Transfer characteristics

Transfer characteristics, μ_{FE}, and output characteristics of bottom-gate TFT with dimension as L/W = 80/40 μm fabricated with millisecond SPC film are indicated in Fig. 5.3 (a) and (b).

The millisecond SPC film was formed by μ-TPJ under v of 500 mm/s. The millisecond SPC-Si TFTs show high μ_{FE} of 28 cm^2/Vs, which is ~ 4 times higher than direct deposition poly-Si by using LPCVD method[12,13]. The mobility changes in inverse proportion to the impurity concentration. In case of Hall effect measurement, millisecond SPC film formed under v = 500 mm/s has high carrier concentration, around 10^{20} cm^{-3}. However, channel of TFTs is intrinsic Si layer, the carrier concentration is small. Therefore, μ_{FE} is higher than carrier mobility obtained from Hall effect measurement. The ratio between the on-state drain current (measured at a gate voltage of 35V) and the off-state drain current (minimum current) is defined as the on/off ratio. As can be seen in Fig. 5.3(a), the devices show the ratio of on/off current as 10^6, threshold voltage V_{th} were 14 V.

(a)



(b)

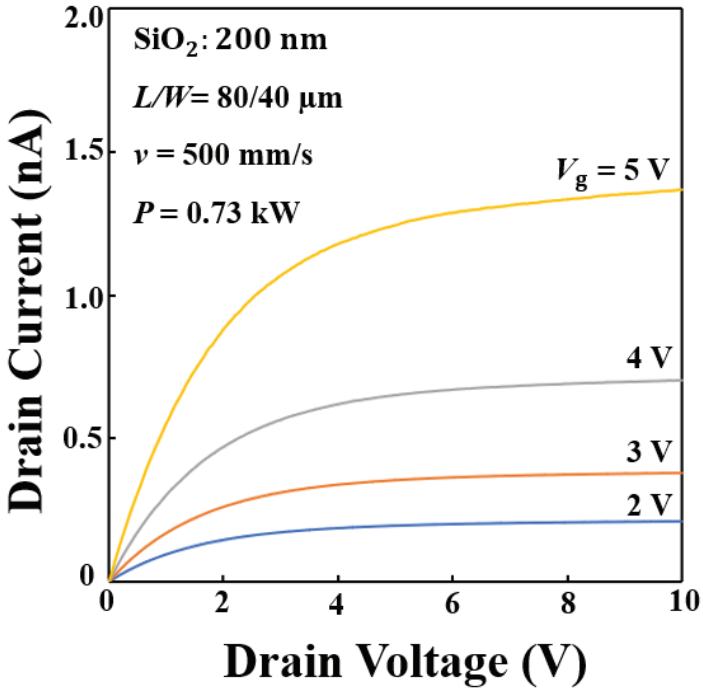
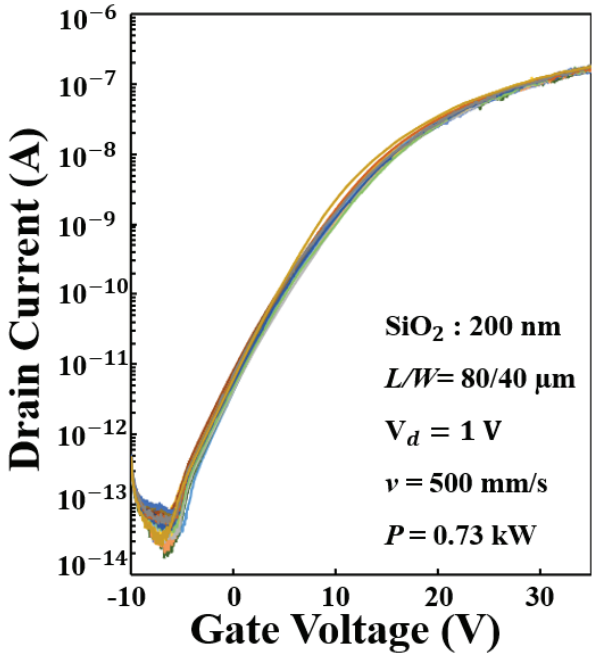


Fig. 5.3. (a) transfer characteristic and field effect mobility and (b) output characteristic obtained by bottom-gate TFTs fabricated with millisecond SPC film formed under *v* of 500 mm/s [(11)]. (Copyright (2021) The Japan Society of Applied Physics)

The characteristics of bottom-gate TFTs with millisecond SPC film as source-drain and channel annealed by μ-TPJ under different experimental conditions are shown in Fig. 5.4 (a) and (b). Figure 5.4 (a) shows the transfer characteristics of 50 devices fabricated with millisecond SPC film. The millisecond SPC films were formed under v as 500 mm/s, and TFT's dimension as L/W = 80/40 μm. The average μ_{FE} were 28.6 cm^2/Vs and the average threshold voltage V_{th} were 13.5 V. As shown in Fig. 5.4 (a), there is small variation among devices. The variations of μ_{FE} and V_{th} from the average value were 0.49 cm^2/Vs and 0.57 V, respectively. For these reasons, TFTs show good uniformity. It is the result of small grain size and random orientation of millisecond SPC film. Figure 5.4 (b) show the I_d - V_g curve of transistor with dimensions as L/W = 80/20 μm when the millisecond SPC formed under different condition of v. The performance of devices is worst when v increases. The maximum value of on current decreases 4 order in magnitude when v increases from 500 to 900 mm/s. This result is suitable with electrical characteristics of crystallized films collected from Hall effect measurement shown in Chapter 4. This result suggests millisecond SPC film formed close to melted condition is a good candidate for small grain bottom-gate TFTs fabrication.

(a)



(b)

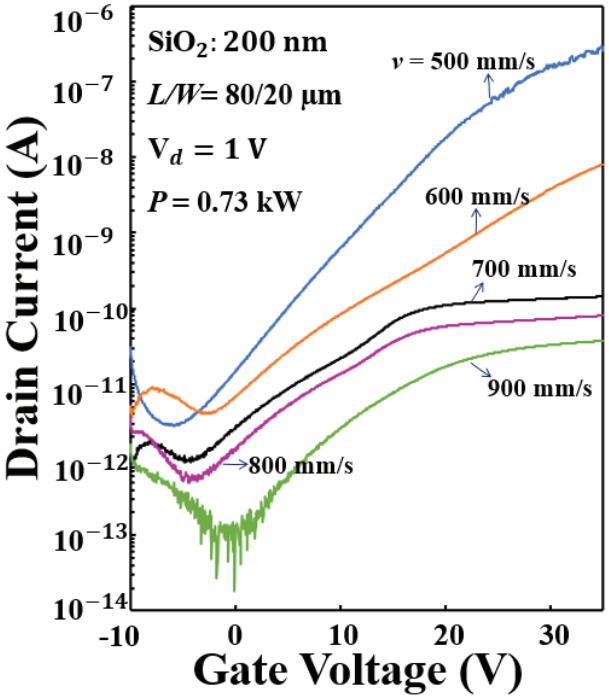


Fig. 5.4. (a) Transfer characteristic of 50 TFTs fabricated with millisecond SPC film annealed under *v* of 500 mm/s and (b) comparison of transfer characteristics of TFTs fabricated with millisecond SPC film annealed under different value of *v* [(11)]. (Copyright (2021) The Japan Society of Applied Physics)

In this time of fabrication, the TFTs fabricated at v = 400 mm/s did not work at all although the device showed normal appearance. We do not know the reason why at this moment. In future work, we will investigate the characteristic of bottom gate TFTs fabricated with melted film and compare with that of bottom gate TFTs fabricated with millisecond SPC film.

5.4. Summary

We succeed in make bottom gate TFTs with millisecond SPC film as S/D and channel. The devices fabricated with millisecond SPC film formed under conditions closed with melted condition show good performance as on/off ratio as high as 10^6 , high mobility as 28 cm^2/Vs and small variation in transfer characteristics. The performance become worst when the v is faster.

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CONCLUSION

The main objective of this research is investigation on the mechanism of millisecond SPC Si films formed at high temperature region by using μ-TPJ. After that, the ability of using it for bottom gate TFTs fabrication with high mobility as 20 cm^2/Vs and small variation in transfer characteristics.

A new method to directly observe the transient reflectivity of a-Si film and the phase transformation simultaneously during μ-TPJ irradiation is introduced. The SPC-Si film is produced in millisecond region, calling millisecond SPC. Phase transformation is observed in real time by using HSC which moved with sample during μ-TPJ irradiation. By introducing the He-Ne laser to objective lens of HSC, we obtained the transient reflectivity of Si film during μ-TPJ annealing. Raman spectra show high crystallinity as higher as 65%. HRTEM images show the distribution of grain size. In general, it is smaller than 60 nm and decreases with the increase of *v*.

In chapter 3, based on the interference phenomenon, the transient variation of Si film temperature during μ-TPJ irradiation is investigated from obtained reflectivity in chapter 2. The nucleation temperature is around 1000 ^oC, heating rate R_h is as high as 10^6 K/s. Both increase with the increase of scanning speed *v*. In addition, according to classical nuclear theorical, we suggested a simple physical model to explain the growth mechanism of millisecond SPC at high temperature region around 1000 ^oC. The results calculated from our theorical model are suitable with experimental results.

In chapter 4, phase diagram of μ-TPJ irradiated a-Si/P-doped a-Si films with respect to supplied power *P* and *v* is shown. Optical microscopy shows the different morphology of crystallization area when film is melted and millisecond SPC state. Characteristics of

millisecond SPC film is investigated by Hall effect measurement, Raman spectra microscopy, and atomic force microscopy. Millisecond SPC films formed at near melted condition show high crystallinity as 61%, low resistivity as 1.36 x 10^{-3} Ωcm, high concentration carrier as 3.41 x 10^{20} cm^{-3}, the carrier mobility as 12.2 cm^2/Vs and smooth surface. So, we succeed in dopants activation by μ-TPJ irradiation.

In chapter 5, we succeed in make bottom gate TFTs with millisecond SPC film as S/D and channel. The devices fabricated with millisecond SPC film formed under conditions closed with melted condition show good performance as on/off ratio as high as 10^6, high mobility as 28 cm^2/Vs and small variation in transfer characteristics. The performance become worst when the *v* is faster.

Based on our achievements in this research, we can conclude that millisecond SPC films formed by μ-TPJ are suitable for bottom-gate TFTs.

Publications and Awards

Academic papers

1. **H.T.K. Nguyen**, H. Hanafusa, Y. Mizukawa, S. Hayashi and S. Higashi: "Direct Observation of Ultra-Rapid Solid Phase Crystallization of Amorphous Silicon Films Irradiated by Micro-Thermal-Plasma-Jet", Materials Science in Semiconductor Processing, 121 (2021) 105357-1 – 105357-9.

2. **H.T.K. Nguyen**, H. Hanafusa, R. Kawakita, S. Hayashi, T. Sato and S. Higashi: "Investigation on Chracteristics of Millisecond Solid Phase Crystallized Silicon FIlms Annealed by Atmospheric Pressure DC Arc Discharge Micro-Thermal-Plasma-Jet and Their Application to Bottom-Gate Thin Film Transistors Fabrication", Japanese Journal of Applied Physics, In press (DOI: https://doi.org/10.35848/1347-4065/ac18ac)

International Conference

1. **H.T.K Nguyen**, H. Hanafusa, R. Kawakita, K. Segawa, and S. Higashi: "Chracteristics of Millisecond Solid Phase Crystallized Silicon Films Formed by Micro-Thermal-Plasma-Jet and Their Application to Bottom-Gate Thin Film Transistors", 2021 International Conference on Solid State Devices and Materials (SSDM2021), (Online, Sept. 6-9, 2021), Peer-Reviewed, Oral Presentation

2. **H.T.K. Nguyen**, H. Hanafusa, Y. Mizukawa, S. Hayashi and S. Higashi: "Characteristic of Rapidly Solid Phase Crystallized Amorphous Silicon Films Formed by Micro-Termal-Plasma Jet Irradiation", 2020 International Conference on Solid State Devices and Materials (SSDM2020), (Online, Sept.27-30, 2020) Peer-Reviewed, Oral Presentation.

Domestic Conference

1. **H.T.K.Nguyen**, H. Hanafusa, and S. Higashi: "Application of Millisecond Solid Phase Crystallization of Silicon Films Induced by Micro-Thermal-Plasma-Jet to Bottom-Gate Thin-Film Transistors", The 82nd JSAP Autumn Meeting 2021 23a-P06-3, Poster (2021.09.21-23, Hybrid)

2. **H.T.K. Nguyen**, H. Hanafusa, and S. Higashi: "Characteristics of Millisecond Solid Phase Crystallization of Phosphorus Doped Silicon Film Annealed by Thermal-Plasma-Jet Irradiation", The 68th JSAP Spring Meeting 18p-Z24-7, Oral Presentation (2021.03.16-19, Online)

3. **H.T.K. Nguyen**, H. Hanafusa, Y. Mizukawa, S. Hayashi, and S. Higashi: "Investigation on millisecond solid phase crystallization of amorphous silicon films induced by micro-thermal-plasma jet", Silicon Device and Materials SDM 2020-18, Oral Presentation (2020.10.22, Online)

4. **H.T.K. Nguyen,** Y. Mizukawa, H. Hanafusa, and S. Higashi: "Investigation on Rapid Solid Phase Crystallization of Amorphous Silicon Films Induced by Micro-Thermal-Plasma-Jet", The 81st JASP Autumn Meeting 10p-Z10-7, Oral Presentation (2020.9.8-11, Online)

5. **H.T.K. Nguyen,** Y. Mizukawa, H. Hanafusa, S. Higashi: "Investigation the Solid phase Crystallization kinetics at the high-temperature region by annealing amorphous silicon using micro-thermal-plasma jet", The 67th JSAP Spring Meeting 15a-PB3-1, Oral Presentation (2020.3.12-15, Sophia University, Yotsuya Campus)

6. **H.T.K. Nguyen,** Y. Mizukawa, H. Hanafusa, S. Higashi: " Direct Observation of Phase Transformation and Transient Reflectivity of Amorphous Silicon Film During Micro-Thermal-Plasma-Jet Irradiation", The 80th JASP Autumn Meeting, 18p-C309-6, Oral Presentation

(2019.9.18-21, Hokkaido University, Sapporo Campus)

Awards

1. **Hiroshima University Excellent Student Scholarship** in 2020

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September 2021,

Hoa Thi Khanh Nguyen

公表論文
（Articles）

(1) Direct Observation of Ultra-Rapid Solid Phase Crystallization of Amorphous Silicon Films Irradiated by Micro-Thermal-Plasma-Jet

H.T.K. Nguyen, H. Hanafusa, Y. Mizukawa, S. Hayashi and S. Higashi

Materials Science in Semiconductor Processing **121**, 105357 (2021)

(2) Investigation on Characteristics of Millisecond Solid Phase Crystallized Silicon Films Annealed by Atmospheric Pressure DC Arc Discharge Micro-Thermal-Plasma-Jet and Their Application to Bottom-Gate Thin Film Transistors Fabrication

H.T.K. Nguyen, H. Hanafusa, R. Kawakita, S. Hayashi, T. Sato and S. Higashi

Japanese Journal of Applied Physics**,** In press

参 考 論 文
（Thesis Supplements）

(1) Characteristics of Millisecond Solid Phase Crystallized Silicon Films Formed by Micro-Thermal-Plasma-Jet and Their Application to Bottom-Gate Thin Film Transistors.

H.T.K Nguyen, H. Hanafusa, R. Kawakita, K. Segawa, and S. Higashi

2021 International Conference on Solid State Devices and Materials, (Online, Sept. 6 – 9, 2021) Peer-Reviewed, Oral Presentation.

(2) Characteristic of Rapidly Solid Phase Crystallized Amorphous Silicon Films Formed by Micro-Termal-Plasma Jet Irradiation.

H.T.K. Nguyen, H. Hanafusa, Y. Mizukawa, S. Hayashi and S. Higashi

International Conference on Solid State Devices and Materials, (Online, Sept.27-30, 2020) Peer-Reviewed, Oral Presentation.