博士論文

A study on High-Mobility SiC MOSFETs with Interfacial Silicate Layer for Harsh Environment Electronics

（極限環境エレクトロニクス実現に向けた
界面ケイ酸塩層を有する
高移動度 SiC MOSFETs の研究）

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主論文

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Chapter 1

Introduction

1.1 Harsh environment electronics

In 1947, the point-contact transistor was invented by Bardeen, Brattain, and Shockley. Since then, a lot of semiconductor devices have been developed. Nowadays, we can see various electronic devices built of transistors (e.g., smartphone) in daily life.

Recently, some research groups attempt to develop electronics operable even under an extreme environment, where a conventional semiconductor device would fail such as high-temperature and high-radiation environments. The specialized technology and the science for this are called the harsh environment electronics.

Figure 1.1 charts end-use applications for radiation and high-temperature environments [1]. The horizontal axis shows a quantity of energy deposition per unit mass by ionizing radiations in applications. As indicated in the figure, several

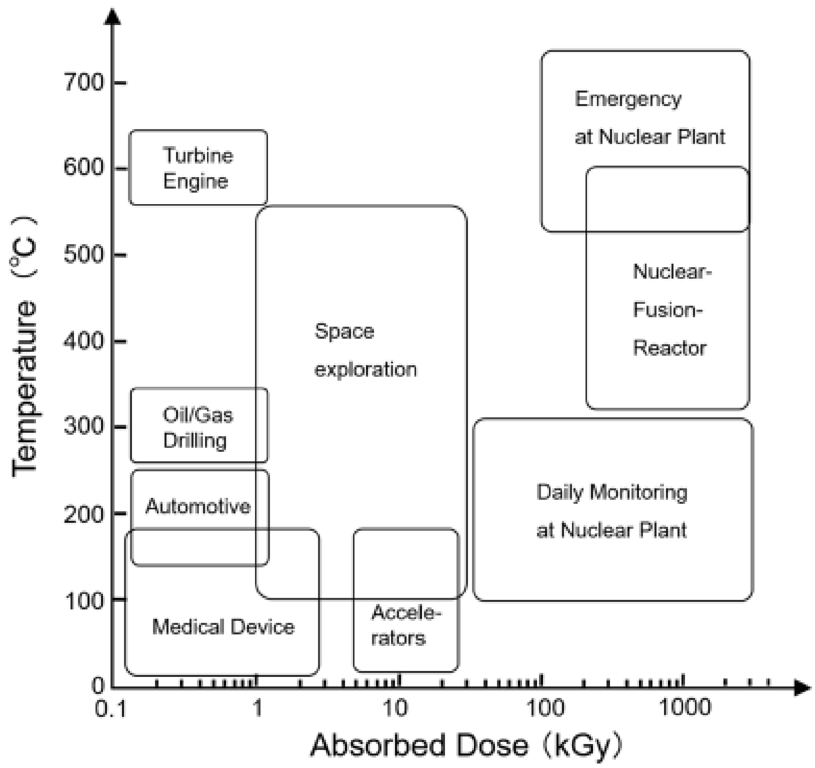

Fig. 1.1. Applications for the harsh environments.

applications and systems strongly require the harsh environment electronics. Among them, a nuclear power plant with a meltdown accident especially requires high radiation-hardness over 100 kGy and high-temperature reliability at a temperature over 500°C.

Before explaining how to enhance both hardnesses of semiconductor devices, the influences of the harsh environments on the devices are mentioned in subsections 1. 1. 1 and 1. 1. 2.

1.1.1 Radiation effects on semiconductor devices

Ionizing radiation is roughly categorized into three types by incident particles: a single highly energetic charged-particle (alpha particle, heavy ion), light particle (neutron, electron), photon (X-ray, γ-ray). These incident particles interact with some material in a semiconductor device. The dominant radiation responses are shown in Fig. 1.2. It is mainly changed by the type of incident particle, the kinetic energy, and an applied electric field.

The incident charged-particle causes the single event effects (SEEs) on the semiconductor region. An incident high-energetic particle generates a lot of electron-hole pairs along its path. The initial number of electron-hole pairs (N_p) is estimated with the formula:

$$N_p = E_k / E_{e\text{-}h}, \quad (1.1)$$

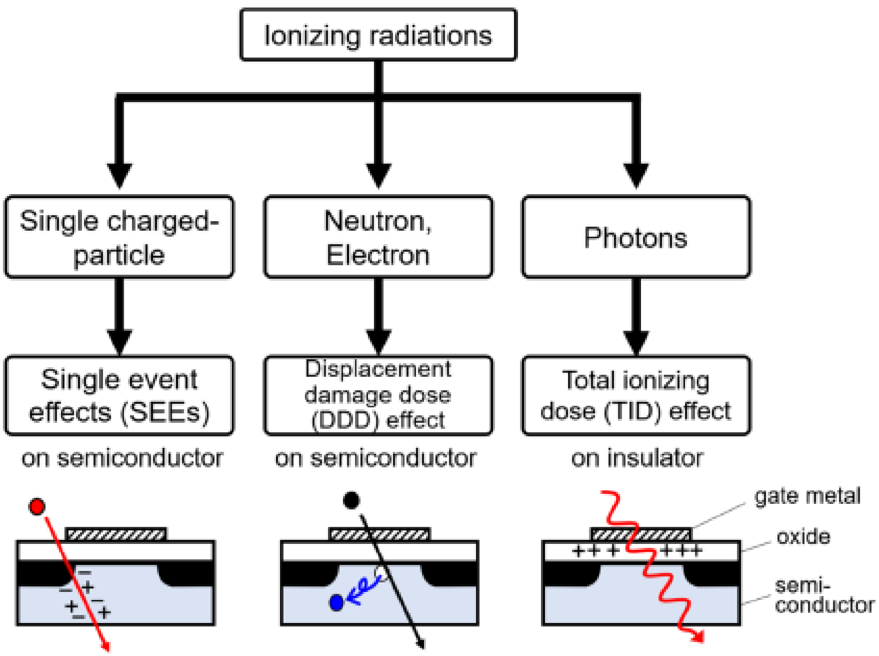

Fig. 1.2. Classification of the radiation and interaction mechanism.

where E_k and $E_{e\text{-}h}$ are the kinetic energy of the radiation and the pair creation energy. The created pair-line-density is high. In other words, the separation distance between electron-hole pairs is narrow, leading to much recombination (called the columnar recombination model) [2]. The yield of the pairs escaping recombination is enhanced by an electric field. Most of the pairs are separated by a reverse-biased of p-n junctions. As a result, a large current flow, thereby causing the single-event upset [3] and the single-event burnout [4]. These phenomena are collectively called SEEs.

The interaction of neutron strongly depends on kinetic energy. Slow neutron ($E < 0.1$ eV) creates a high-energy charged-particle via nuclear transmutation reaction. Hence, slow neutron causes SEEs as same as alpha particle. Slow neutron was reported to react with an impurity in the interlayer dielectric layer on transistors [5, 6]. On the other hand, fast neutron (0.5 MeV $< E < 20$ MeV) is much damaging a semiconductor substrate resulting from the knock-on effect with the host atom due to elastic and inelastic scattering [7]. This is called by displacement damage dose (DDD) effect. Unlike SEEs, DDD effect is a result of energy deposition in the bulk materials, causing the degradation of electrical characteristics [8].

X-ray and gamma-ray seriously do not make serious damages to a semiconductor. When photons pass through a semiconductor, electron-hole pairs are generated like the response of the charged-particle. However, the created charge density is lower than that of the charged-particle (called the geminate recombination model) [2]. Thus, the number of charges is insufficient to cause SEEs. However, the incident photons cause total ionizing dose (TID) effect, instead of SEEs, in an oxide.

TID effect mainly occurs in a gate-oxide of metal-oxide-semiconductor field-effect transistor (MOSFET) due to cumulative dose. Figure 1.3 shows the schematic energy band diagram for n-channel MOSFET with SiO_2 gate-oxide, where a positive gate bias is applied. The TID effect occurs in four stages. Firstly, electron-hole pairs in SiO_2 are generated by radiation. The radiation-induced electrons and holes move to the gate metal and semiconductor side, respectively. In SiO_2, the electron drift mobility is much higher than the hole mobility, and most of the electrons are swept out without via recombination process. As a result, residual holes are trapped in the oxide. In the case of SiO_2, the electron mobility is 20 $cm^{-2}V^{-1}s^{-1}$ and the hole mobility is 4×10^{-5} $cm^{-2}V^{-1}s^{-1}$ at room temperature [9, 10].

The hole trapping breaks Si-O bonds in SiO_2, generating oxygen vacancies (E′-center) [11]. The defects are gradually propagated into the MOS interface along a strain gradient around the MOS interface [12].

After reaching near the MOS interface, transported holes fall into trap states in the bandgap of the semiconductor. These trapped holes have a long life-time, act as fixed positive charges near the oxide/semiconductor interface. The positive charges are called oxide-trapped positive charges, and the build-up positive charges lead to negative threshold voltage shift and an increase in gate leakage current [2, 13].

The reached holes right at the MOS interface disorder the MOS interface. The interfacial hole-trapping breaks chemical bonds (e.g. Si-H bond, Si-Si bond) generating interface traps [12, 14]. These are called radiation-induced interface traps. The induced traps reduce the channel mobility in the inversion layer and increase the threshold voltage [15].

In summary, the incident photon induces the three major radiation effects: the build-up of oxide-trapped positive charge, generation of interface traps, and mobility degradation.

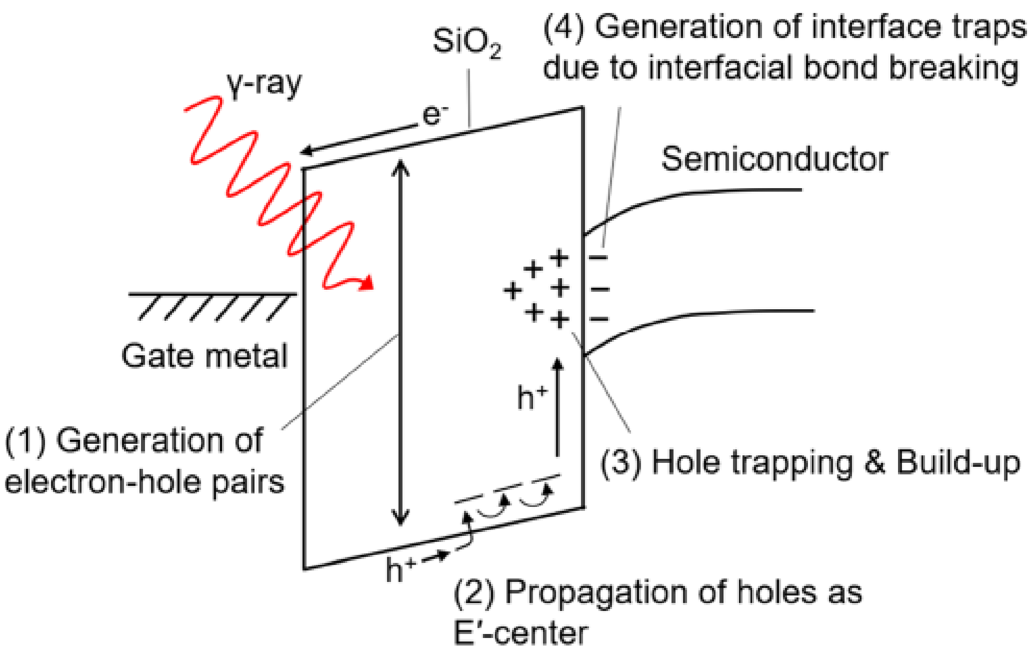

Fig. 1.3. Schematic energy band diagram and the processes of TID effect [2].

1.1.2 Performance of MOS devices under high-temperature

Temperature impacts on carrier density of semiconductor. In figure 1.4, electron density (n) is plotted as a function of the reciprocal temperature for a n-type silicon with donor impurity concentration (N_D) of 1×10^{15} cm^{-3} [16]. At low temperatures under 120 K, the thermal energy (kT) is lower than an ionization energy of the dopants, where k is the Boltzmann constant and T is temperate. Thus, most impurities are not ionized, and this range is called frozen-out region ($n < N_D$). As increasing T, the electron density becomes a constant ($n \approx N_D$) due to the full ionization. This stage is called saturation region. Almost all semiconductor devices utilize this region to maintain the carrier density.

At high temperatures beyond 500 K, the intrinsic carrier density (n_i) greatly contributes the electron density rather than the doping concentration because of ionization of silicon. The carrier density is expressed as follows:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{kT}\right), (1.2)$$

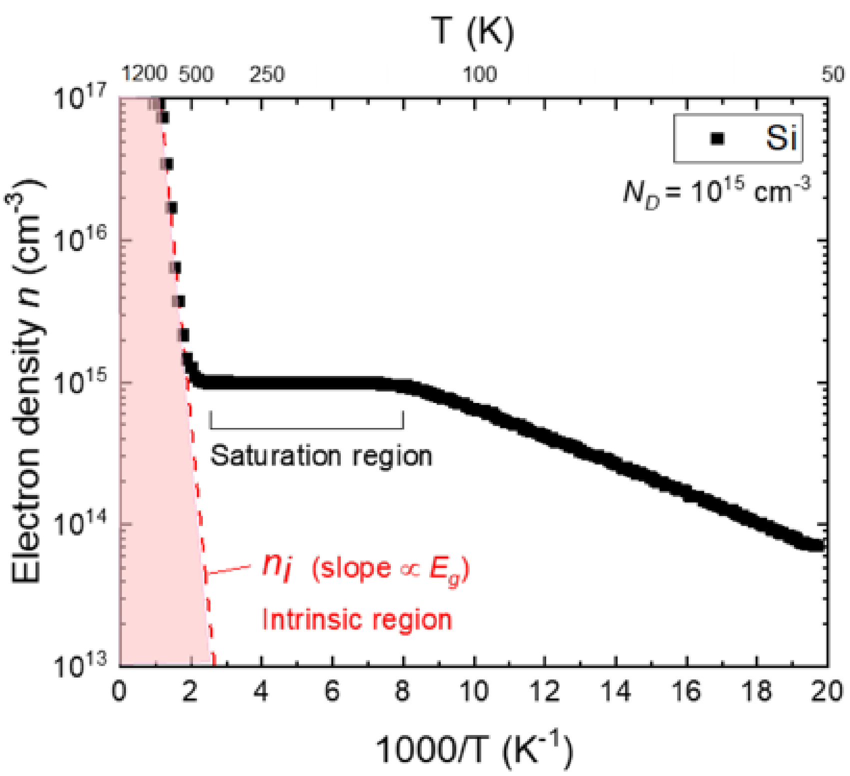

Fig. 1.4. Electron density as a function of temperature for silicon with donor impurity density of 1×10^{15} cm^{-3} [16].

where Nc, Nv are the effective densities of states in the conduction band and the valence band, respectively. Also, E_g is the bandgap of semiconductor. The electron density exponential increases with increasing the temperature. As a result, the semiconductor exhibits high conductivity like a metal, leading high leakage current through the device. Therefore, it is important to maintain the carrier density of semiconductor in order to extend the operational temperature range.

The operational range is limited by not only semiconductor but other components in a device. Beside semiconductor, the device consists of some metals and oxides. At high temperatures, diffusion or chemical reaction occur in both materials.

As one of examples, an interlayer dielectric erosion is described [17]. Figure 1.5 illustrates the cross-section of MOSFET with an Al-erosion on SiO_2 dielectric. Al and SiO_2 are typical materials for the interconnect metal and interlayer dielectric. At high temperatures around 500°C, the Al layer reacts and gradually erodes the underling SiO_2 layers. This reaction is expressed below:

$$2Al + 3/2\ SiO_2 \rightarrow Al_2O_3 + 3/2\ Si. \quad (1.3)$$

This phenomenon reduces the effective thickness of the interlayer, causing a short-circuit and device's failure.

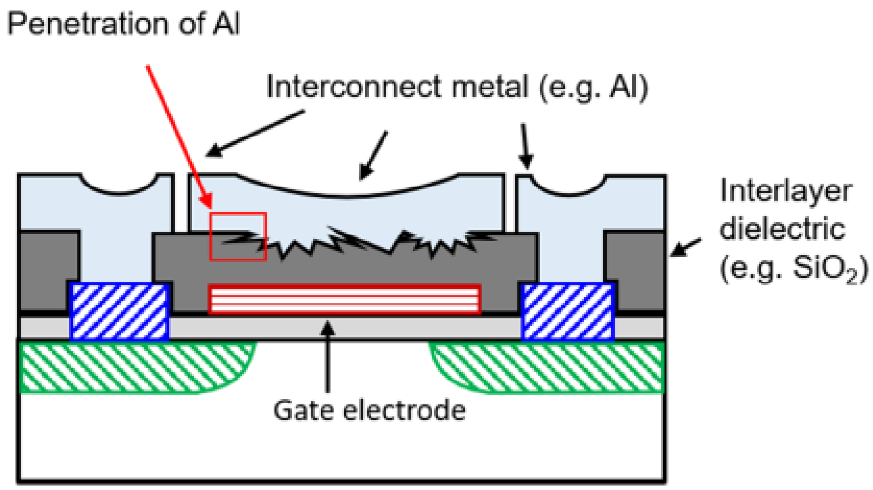

Fig. 1.5. Schematic cross-section of MOSFET and the erosion of Al-gate metal at high temperatures around 500°C.

1.2 Silicon carbide and its specialized applications

Silicon carbide (SiC) is one of the compound semiconductors which has been considered as a potential alternative to Si for power electronics [18]. Also, SiC is endowed with superior physical and electrical properties for the harsh environment electronics.

1.2.1 Physical properties

SiC has a lot of polymorphs; the popular polytypes are 3C-, 4H-, 6H-, 15R-SiC in Ramsdell's notation. 4H-SiC has the widest bandgap and exhibits the good spatial uniformity of electron-mobility. Hence, 4H-SiC attracts an attention and a hope for power electronics and the harsh environment electronics. The principle properties of 4H-SiC semiconductor and conventional Si semiconductor are summarized in Table 1.1. 4H-SiC is endowed with a wider bandgap, a higher electron-hole creation energy ($E_{e\text{-}h}$), and a higher threshold displacement energy (E_d). These properties enhance the radiation- and high-temperature hardnesses. More specific reasons are described in subsection 1.2.2 and 1.2.3.

Table 1.1. Physical properties of Si and 4H-SiC for the harsh environment electronics. All measurements at room temperature if not specified otherwise.

	Si	**4H-SiC**	**Ref.**
Bandgap, E_g (eV)	1.12	3.26	16, 18
Breakdown electric field, E_B (MV cm^{-1})	0.3	2.8	18
Electron mobility, μ_e (cm^2 V^{-1}s^{-1}) *	1350	1000*	18
Hole mobility, μ_h (cm^2 V^{-1}s^{-1})	500	120	18
Thermal conductivity, K (W cm^{-1} K^{-1})	1.5	4.9	18
Electron-hole pair creation energy, $E_{e\text{-}h}$ (eV)	3.62	7.78	19
Threshold displacement energy of a sublattice, E_d (eV)			
Silicon	15	21	20, 21
Carbon	—	18	21
$T_{intrisic}$ (K) at $N_D = 1 \times 10^{15}$ cm^{-3} **	530	1000	16
Melting point, T_m (K)	1600	2000	19

*perpendicular direction to *c*-axis. **$T_{intrinsic}$ is the temperature at switching from the saturation region to the intrinsic region.

1.2.2 Radiation hardened electronics

Radiation effects are divided into SEEs, DDD effect, and TID effect as described in the subsection 1.1.1. The higher $E_{e\text{-}h}$ and E_d lead to suppress SEEs, DDD effect, and TID effect.

The $E_{e\text{-}h}$ of 4H-SiC is two times higher than that of Si. Using Eq. (1.1), the estimated number of electron-hole is cut by half. Thus, when 4H-SiC is utilized as semiconductor substrate, the probability of SEEs can be reduced.

Note that circuit design and the layout also make a large contribution to minimize the probability of SEEs from a single-particle strike. It is called radiation hardness-by-design. Here, a triple modular redundancy (TMR) is explained. It is a design for improving the fault tolerance due to the single event upsets. The TMR design has three identical instances of hardware with a voting function at the output. The three systems perform a majority voting, producing a single output. If a single-particle strike affects one of the hardware instances, the logic circuits note the majority output with the initial information. Si devices for space applications adopt redundant structures like TMR for improving the tolerance of SEEs [3, 22].

Utilizing 4H-SiC also reduces the displacement damage by radiation. The E_d of 4H-SiC is 1.4 times higher than that of Si. The number of displacements per atom is inverse proportion to E_d [23]. Hence, 4H-SiC is expected to lead to the less displacement damage. Unlike SEEs, DDD effect is caused by the cumulative damage. Thus, radiation hardness-by-design is unable to prevent the displacement damage. Replacing semiconductor substrate is one of a few methods to manage the tolerance of DDD effect. Harris et al. reported the difference in the displacement damage between Si and SiC in the ref. [24].

Replacing the semiconductor substrate is also an approach to improve TID tolerance. TID effect mainly damages a gate-oxide and an interlayer dielectric, not semiconductor. Nevertheless, replacing the substrate to SiC reduces the number of the oxygen vacancies in the dielectrics, and prevents the generation of the interface states [25, 26]. Although the TID hardening by utilizing SiC has experimentally been revealed, the reason is not fully understood yet [27, 28]. Ohshima et al. reported the bandgap dependence on TID hardness; wider bandgap can provide lower threshold voltage shift by radiation [26].

1.2.3 High-temperature electronics

The operational temperature range is strongly affected by intrinsic carrier density (n_i) of semiconductor substrate, as expressed in Eq. (1.2). 4H-SiC is able to prevent the ionization of semiconductor, reducing n_i at high temperatures. Figure 1.6 shows electron densities of 4H-SiC and Si as a function of the reciprocal temperature. The saturation region of 4H-SiC is extended thanks to the wide bandgap. $T_{intrinsic}$ is defined as the temperature at switching from the saturation region to the intrinsic region. The values of $T_{intrinsic}$ are 530 K and 1000 K for Si and 4H-SiC at the same dopant concentration, 4H-SiC can act as semiconductor at the temperature of more than 500°C.

For commercial power devices, the maximum operating temperature is expressed as junction temperature (T_j), which is specified to determine the maximum permissible power dissipation under a continuous ON-sate of the device. T_j of commercial 4H-SiC MOSFETs is summarized in Table 1.2. The values of T_j are 150–200°C, and the manufacturer A provides the MOSFETs with the highest T_j.

As shown in Table 1.2, the current T_j is still below the $T_{intrinsic}$. That is, other components, not the semiconductor substrate, is the bottleneck. Only replacing the

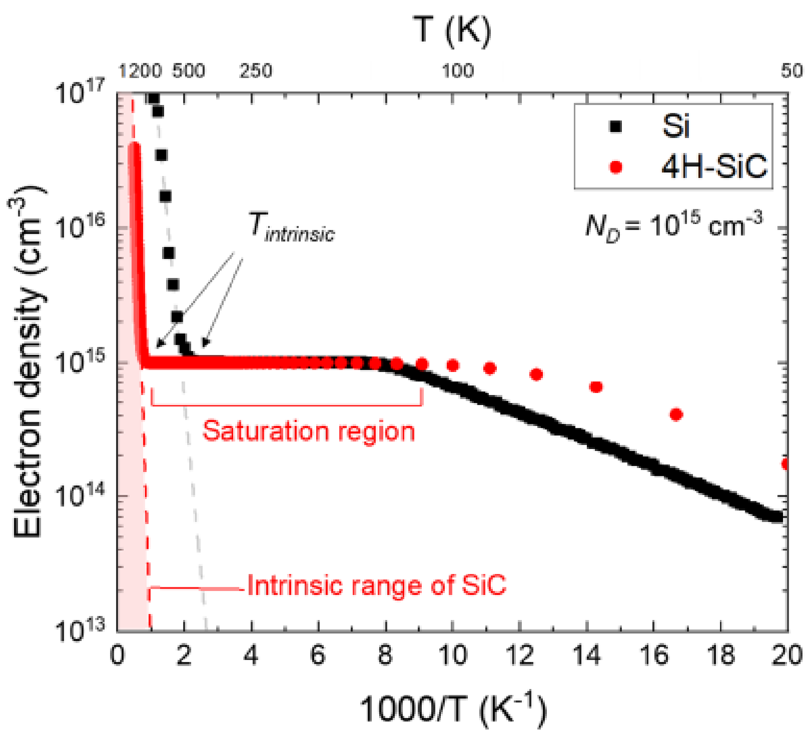

Fig. 1.6. Electron densities of Si and 4H-SiC as a function of reciprocal temperature.

substrate is insufficient to enhance the maximum operating temperate. The group of national aeronautics and space administration (NASA) demonstrated the stable operation of 4H-SiC junction field-effect transistor (JFET) with high-temperature reliability at temperatures above 800°C [29]. JFET has no gate-oxide to switch its channel conductivity. Thus, this structure suppresses the characteristic degradation due to the chemical reaction between gate-oxide and gate-metal at high temperatures.

Table 1.2. Maximum junction temperatures of commercial 4H-SiC MOSFETs.

	Blocking Voltage, V_B (V)	**On-resistance, R_{on} (Ω)**	**Maximum junction temperature, T_j (°C)**	**Package**
Manufacturer A	1200	0.69	200	HIP247
	1200	0.69	200	HIP247
	1200	0.239	200	HIP247
	1200	0.239	200	HIP247
	1200	0.1	200	HIP247
	1200	0.069	200	HIP247
Manufacturer B	1200	—	175	TO-220-2
	1200	0.016	175	TO-247-4
	1200	0.016	175	TO-247-3
	1200	0.021	175	TO-247-3
	1200	0.021	175	TO-247-4
	1200	0.025	150	TO-247-3
	1200	0.032	175	TO-247-4
Manufacturer C	1200	0.16	175	TO-247N
	1200	0.105	175	TO-247-4L
	1200	0.105	175	TO-247N
	1200	0.08	175	TO-247-4L
	1200	0.08	175	TO-247N
	1200	0.04	175	TO-247-4L

1.3 Optimization of SiC MOS interface

Both radiation and high-temperature hardnesses are improved by utilizing SiC as the substrate. Because of its special characteristics, SiC MOSFET has been developed for the harsh environment electronics. For example, the MOSFET-based integrated circuits were demonstrated up to 500°C [30].

Another advantage of SiC is that it can be thermally oxidized in the same manner as silicon. In early studies, the thermal-grown SiO_2 had been utilized as gate dielectric in MOSFET [31]. However, the thermal-grown SiO_2/SiC interface has high interface trap density (D_{it}), which is 100–1000 times higher than that of the hydrogen-terminated SiO_2/Si interface [32]. These defect states strongly limit channel mobility in MOSFET, and the mobility was far from a satisfactory level.

For mobility improvement, various methods have been suggested, shown in Fig. 1.7. It is categorized into two types; gate oxide engineering and channel engineering. The former method enhances channel mobility thanks to reducing D_{it}. The latter one is the method which enhances initial carrier mobility without improving the interface properties, for example, utilizing $(11\bar{2}0)$ face.

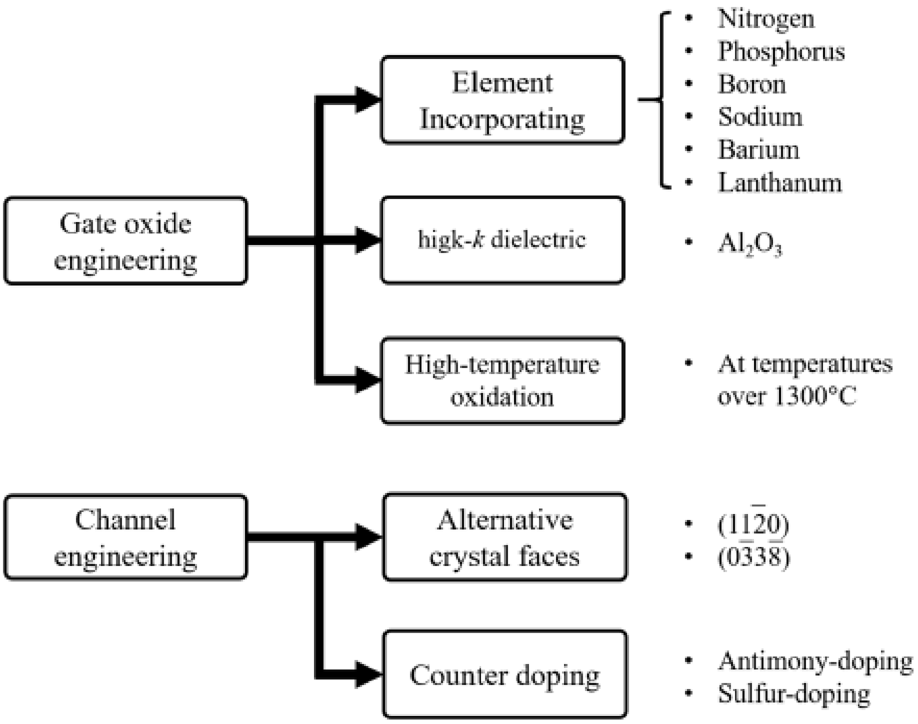

Fig. 1.7. Classification of mobility enhancement methods.

1.3.1 Gate oxide engineering

One of the popular approaches is to incorporate some element into the SiO_2/SiC interface to reduce D_{it}. Nitrogen, phosphorus, boron, sodium, barium, and lanthanum were effective for the passivation of the defects [33–38]. Incorporating nitrogen by annealing in the ambient of NO or N_2O provides reproducible mobility enhancement with a few drawbacks. Thus, it is widely used for fabricating state-of-the-art commercial SiC MOSFETs. Although the channel mobility is increased up to 25–35 $cm^2V^{-1}s^{-1}$, the resulting mobility is still lower than the ideal value expected by the bulk electron mobility [18, 39].

The gate insulator with a high dielectric constant (k) also enhances the mobility. Lichtenwalner et al. demonstrated high-mobility SiC MOSFETs with Al_2O_3 gate dielectric instead of the nitric oxide [40]. Besides Al_2O_3, AlSiO and AlN thin film are effective as the gate dielectric [41, 42]. High-temperature oxidation at temperatures over 1500°C assists to form high quality SiO_2/SiC interface [43, 44]. Kita et al. proposed the method to control the interface states by thermodynamic property of desorption of the carbon atoms when SiC is oxidized [43].

Table 1.3 shows the values of field effect mobility (μ_{FE}) improved by the gate oxide engineering. Moreover, the relationship between the μ_{FE} and threshold voltage (V_{th}) is shown in Fig. 1.8. There is a decreasing trend in μ_{FE} as increasing V_{th}. That is, it is still difficult to ensure both high μ_{FE} and V_{th}. This is because the element incorporating simultaneously leads to reduction of D_{it} and counter-doping on SiC surface. As a result, the net concentration on the channel region decreases, and the mobility dramatically increases as same as the counter doping using ion implantation. The counter-doping effect from the incorporated-oxide was revealed using scanning capacitance microscopy by Fiorenza et al. [45].

Table 1.3. Summary of field effect mobility (μ_{FE}) and interface trap density (D_{it}) in 4H-SiC MOS devices. The fabrication process of the gate oxide, the acceptor concentration (N_A) of the p-type channel region are also shown.

Process	**P-type body concentration N_A (cm^{-3})**	**Threshold voltage V_{th} (V)**	**Field effect mobility μ_{FE} (cm^{2}V^{-1}s^{-1})**	**Interface trap density D_{it} (cm^{-2}eV^{-1})**	**Ref.**
Non-incorporated thermal SiO_2	5.8×10^{16}	—	6	—	46
	5×10^{15}	4.9	6.6	4×10^{11}	47
	7×10^{15}	7.5	6	8×10^{12}	48
NO annealing	$1–4 \times 10^{16}$	5	37	2×10^{12}	39
	7×10^{15}	3.4	26	3×10^{12}	48
$POCl_3$ annealing	7×10^{15}	0.0	89	1×10^{11}	48
Boron diffusion	5×10^{15}	1.3	102	1×10^{11}	35
Na-contamination	5×10^{15}	1.8	140–180	1×10^{11}	36
Ba-incorporation	5×10^{15}	1	85	3×10^{11}	37
	5×10^{15}	0.5	110	3×10^{11}	49
	—	≈0	62	4×10^{11}	50
La-incorporation	5×10^{15}	3	130	2×10^{11}	51
	5×10^{15}	—	40–130	—	38
Al_2O_3	—	0.8	106	—	40
High temperature oxidation	1×10^{17}	−1	40	6×10^{12}	44

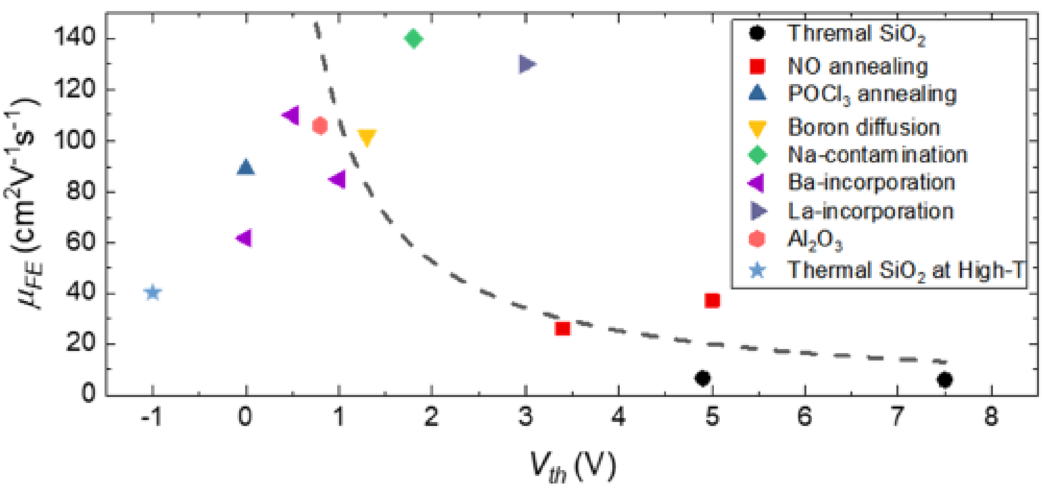

Fig. 1.8. Relationship between V_{th} and μ_{FE}. Data are taken from Table 1.3.

1.3.2 Channel engineering

Historically, the (0001) Si-face of SiC has been utilized to fabricate almost all SiC devices. In 2002, Yano et al. reported that $(11\bar{2}0)$ a-face resulted in 50 $cm^2V^{-1}s^{-1}$ of field effect mobility, showing that other faces could be utilized for the MOS device [52]. They also reported that the shallow interface state density on $(0\bar{3}\bar{3}8)$ m-face was lower than on (0001) [53]. Utilizing alternative faces is easy to combine the fabrication process of a vertical power MOSFET, which has a large drain current toward the SiC bulk substrate. Most of vertical MOSFET utilize this method.

Counter-doping into channel region by ion implantation is used to control V_{th} and μ_{FE}. The counter-doping reduces the net concentration of acceptor in channel region. As a result, Coulomb scattering due to the impurities is suppressed, enhancing the mobility. Antimony (Sb) and sulfur (S) are mainly used [54, 55], and in most cases, the gate oxide engineering is simultaneously performed to reduce D_{it}.

1.4 Motivation and purpose

In this dissertation, high-mobility and rugged SiC MOSFETs under the harsh environments were investigated. As mentioned in section 1.1, the decommissioning of nuclear power plants requires SiC devices with high radiation-hardness over 100 kGy and high-temperature reliability at temperatures over 500°C.

Nitrogen incorporation into MOS interface is one of the strong candidates to enhance the channel mobility, and it is used for fabricating state-of-the-art commercial SiC MOSFETs. Moreover, it has reported that stable operation of MOS devices with nitrogen incorporation at temperatures up to 500°C [30]. Although the resulting mobility is still low, nitrogen incorporation can satisfy the requirement for the high-temperature environment.

However, in the term of radiation-hardness, the nitrogen incorporation has a couple of drawbacks. The first one is to reduce TID hardness. The MOS interface with nitrogen has more hole-trap-centers than that of thermally-grown SiO_2 [56, 57]. It promotes trapping the holes generated by radiation, causing a large threshold voltage shift [27, 28]. The second one is to react with neutrons. Inside a nuclear power plant with a meltdown accident, an introduced SiC device is expected to suffer from both gamma-ray and neutron irradiations. ^{14}N, which makes up 99.636% of natural nitrogen, captures a neutron, changing to ^{14}C. This nuclear transmutation reaction is given:

$$^{14}N + n \rightarrow {}^{14}C + p + \gamma \text{ (0.58 MeV)}, \quad (1.4)$$

where n, p, and γ denote neutron, proton, and gamma-ray. The capture cross-section of the thermal neutron (~ 25 meV) is 2 barn, which is 20 times higher than that of ^{30}Si used neutron transmutation doping for Si-power device (1 barn = 1×10^{-24} cm^2) [58]. Thus, introducing nitrogen would gradually lose its original characteristic by capturing neutron.

In this dissertation, I focus on barium-incorporation proposed by Wolfspeeed, Inc. The resulting mobility was higher than that of nitrogen incorporation [37]. Moreover, ^{138}Ba, makes up 71.70% of natural barium, does not produce nuclear transmutation reaction against neutron. Thus, there is a possibility that barium incorporation overcomes the drawbacks of nitrogen incorporation, leading to more stable operations in the harsh environments. I fabricated SiC MOSFETs with barium, and then explored the potential of the Ba-incorporation method for harsh environment electronics.

1.5 Dissertation overview

This dissertation consists of six chapters, as shown below.

Chapter 1: The research background and the purpose are summarized. It is shown that the influences of the harsh environments on the semiconductor devices and the effectiveness of utilizing 4H-SiC substrate for the harsh environment electronics.

Chapter 2: It is shown that the thickness dependencies of SiO_2/BaO_2 layers on structural and interfacial properties of a layered gate-dielectric on 4H-SiC. The Ba-incorporation method utilizes not only Ba layer, but also a SiO_2 cap layer, which is deposited on a Ba/SiC substrate prior to oxidation. I conclude the roles in each layer in the mobility enhancement and discuss optimal thicknesses.

Chapter 3: High-temperature characteristics of the SiC MOSFETs with interfacial Ba-silicate is shown. Electrical characterization at high-temperatures from 27°C to 500°C was measured. At 500°C, the MOSFETs exhibited clear output characteristics. Moreover, the incorporated Ba atoms did not act as mobile ion at even 500°C.

Chapter 4: The chapters of radiation hardness is divided into chapter 4 and 5. In this chapter, the TID and DDD effects of the fabricated SiC MOSFETs are shown. N-channel SiC MOSFETs with Ba-silicate layer were irradiated with gamma-rays up to

850 kGy. Threshold voltage shift was observed due to TID effect. Moreover, drain-substrate leakage current flowed. This leakage current indicates the generation of a deep defect state on pn junction due to DDD effect.

Chapter 5: After irradiation over 600 kGy, the SiC MOSFET with Ba-silicate resulted in anomalous mobility enhancement: field effect mobility increased from 12 to 18 $cm^2V^{-1}s^{-1}$. The narrower channel MOSFET enhanced this effect. I discuss the geometric effect and the mechanism of this anomalous mobility enhancement.

Chapter 6: Summary of this dissertation is shown. Then, the potential of the Ba-incorporation method is concluded for harsh environment applications. In concluding remarks, future works and residual problems are mentioned.

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Chapter 2

Effects of SiO_2/BaO_2 layers on interfacial properties in Ba-incorporation method

2.1 Introduction

TID tolerance of MOSFETs depends on gate-oxide thickness. Thin oxide promotes the recombination of the generated holes through both thermal and tunneling electrons, improving the intrinsic TID robustness [1, 2]. In the case of Si-devices for space application, 3–10 nm-thick gate-oxide has been used [2–4].

Ba-incorporation method has two disadvantageous properties for the gate-oxide thickness. One is to promote catalytic oxidation. Alkali metal is known to act as a catalyst, promoting oxidation and nitridation on a semiconductor [5, 6]. This is because alkali metal, which has an s-orbital electron protruding into vacuum, can assist adsorption and dissociation of molecules [7]. Barium also has the 6s-electrons [8], and it promotes oxidation reaction [9, 10]. Figure 2.1 shows an oxidation growth rate by catalytic oxidation [11]. For 60 min of oxidation time, the SiO_2 thickness was 50 and 2 nm with and without barium; the growth rate became 25 times higher.

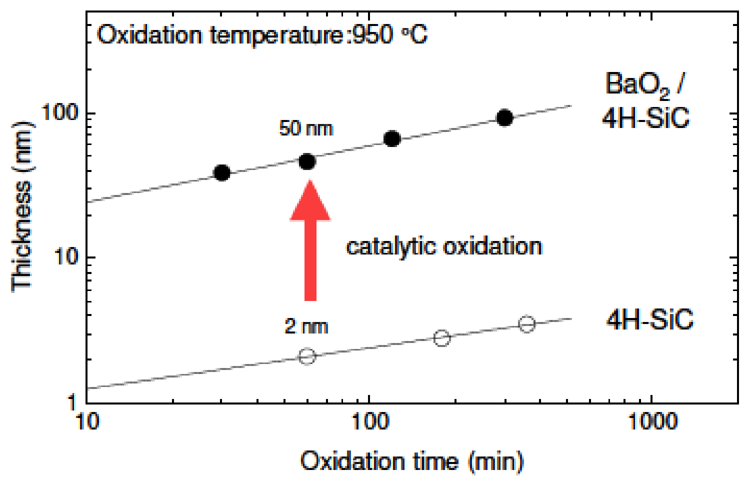

Fig. 2.1. Oxidation growth rate by catalytic reaction as a function of oxidation time.

The second disadvantage is to require a thick cap-SiO_2 layer. The Ba-incorporation method utilizes a SiO_2 cap layer, which is deposited on a Ba/SiC substrate prior to oxidation. The thicknesses of barium and cap-SiO_2 layers are summarized in Table 2.1 [12–17]. It includes the information of La-incorporation. Both methods utilize a thick SiO_2 cap layer over 30 nm. Thin gate-oxide (~10 nm) has not reported. For the Ba-incorporation method, a 4H-SiC MOS capacitor without cap-SiO_2 layer slightly reduced D_{it} (to 2×10^{12} cm^{-2}eV^{-1}), and it was not sufficient for improving mobility [10]. This report implies that the cap-SiO_2 layer is necessary for the Ba-incorporation method. However, its role has not been elucidated. Moreover, the optimal Ba thickness is also incompletely understood. The previous research was done with a thin Ba layer (0.1–0.8 nm) [12, 14, 18, 19].

In this chapter, I show the thickness dependencies of an interfacial Ba layer and an SiO_2 cap layer on the interface properties of a layered gate dielectric, in order to reveal the role of the SiO_2 cap layer. The effects of different thicknesses are investigated using four characterization techniques. Furthermore, I fabricated n-type MOS capacitors with different thicknesses and evaluated their electric characteristics.

Table 2.1. Summary of cap-SiO_2 thickness and the related parameters.

Process	Interface layer thickness (nm)	Cap-SiO_2 thickness (nm)	N_A (cm^{-3})	V_{th} (V)	μ_{FE} (cm^{2}V^{-1}s^{-1})	D_{it} (cm^{-2}eV^{-1})	Ref.
Ba-incorporation	0.6–0.8	30	5×10^{15}	1	85	3×10^{11}	12
	a few monolayers	30	5×10^{15}	0.5	110	3×10^{11}	13
	0.1	35		≈0	62	4×10^{11}	14
La-incorporation	1	30	5×10^{15}	3	130	2×10^{11}	15
	0.3–1.0	30	5×10^{15}	—	40–130	—	16
	2	50	—	—	—	7×10^{11}	17

2.2 Experimental

2.2.1 Sample preparation

An experimental procedure is shown in Fig. 2.2. N-type MOS capacitors were fabricated on 4° off-axis 4H-SiC (0001) wafers with an epitaxial n-type SiC layer, which had a dopant concentration (N_D) of 1×10^{16} cm^{-3}. After chemical surface cleaning, a layered gate dielectric was formed through the following processes. A barium peroxide (BaO_2) layer, which exhibits higher chemical stability than metal Ba, with a thickness in the range of 3–8 nm was deposited on the 4H-SiC substrate. Barium oxide also has the 6s-electrons protruding into the vacuum [20]. Subsequently, an SiO_2 cap layer with a thickness range of 0–30 nm was deposited on the BaO_2/SiC sample. Both the depositions were carried out by RF sputtering in the same vacuum chamber at room temperature.

The samples were then oxidized in O_2 ambient at 950 °C for 1 hour, forming a layered SiO_2/Ba-silicate/SiC structure. TID tolerance would be influenced by both oxidation and post-oxidation annealing temperatures [21]. Temperatures over 950°C cause a viscous shear flow in SiO_2, increasing the number of hole traps [22].

For all the samples, Ni silicide was formed by the deposition of Ni on the backside of the substrate, followed by annealing in N_2 ambient at 900 °C. Finally, aluminum was deposited on the sample as the gate electrode. The capacitance–voltage (C–V) characteristics were measured using an Agilent 4284A LCR meter and an Agilent 4294A impedance meter.

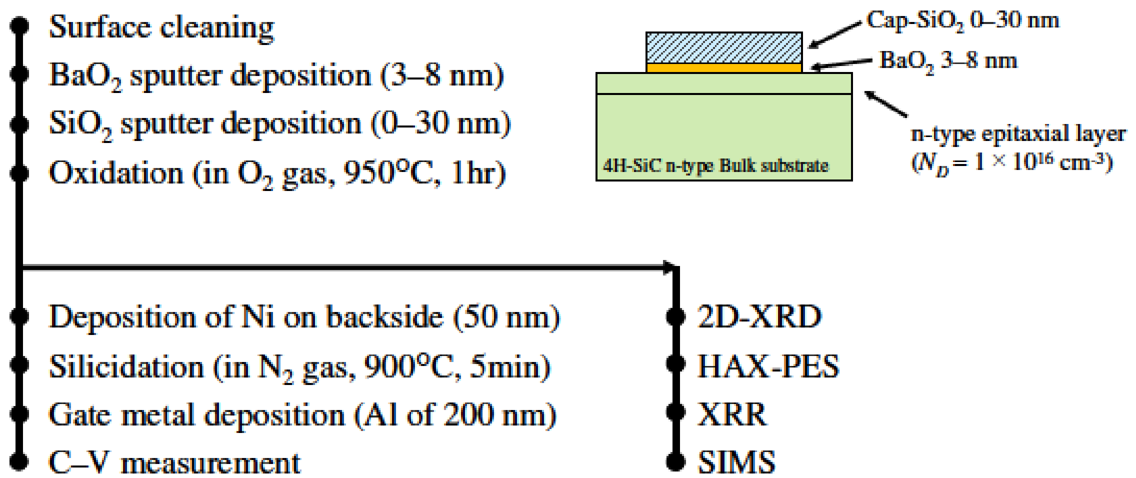

Fig. 2.2. Experimental procedure in Chapter 2.

2.2.2 Characterization

The effects of different thicknesses were characterized using four characterization techniques: two-dimensional X-ray diffraction (2D-XRD), hard X-ray photoelectron spectroscopy (HAXPES), secondary ion mass spectrometry (SIMS), and X-ray reflectivity (XRR).

2D-XRD and HAXPES were carried out at the beamline BL46XU of SPring-8, which is a synchrotron radiation facility in Japan. The incident X-ray energies were 12.4 and 7.94 keV, respectively. For the 2D-XRD measurement, the X-ray incident angle was set to 0.2°, and the diffracted X-rays were detected using a two-dimensional detector (PILATUS 300K, Dectris). The penetration depth of the incident X-ray is 1.1 μm, as shown in Fig. 2.3.

The HAXPES spectrum was measured using VG Scienta R4000 instrument, and take-off angle (TOA) was set to 80°. The TOA is defined as the angle between the path of the detected photoelectrons and the sample surface. The energy resolution was 280 meV. Binding energy of a core level peak was determined by fitting with Voigt function. C 1s core-level-peak of bulk SiC (283.25 eV) was used for charge correction.

Dynamic SIMS was carried out using a quadrupole mass spectrometer and a Duoplasmatron ion source (SIMS6650, ULVAC-PHI); the incident primary ions were O^{2+} with an acceleration voltage of 5 kV. Etching depth was estimated by a stylus surface profiler (Dektak3ST, ULVAC) after SIMS measurement.

The XRR was measured using an X-ray diffractometer (ATX-E, Rigaku). The incident X-ray (Cu*K*α line, 8.04 keV) was collimated using a Ge (220) channel-cut monochromator, with a divergence angle of 0.0057° and a beam width of 0.025 mm, as shown in Fig. 2.4. At a critical angle on SiO_2 (~0.215°), this experimental setup produced a 6.7 mm of the footprint on a SiO_2/4H-SiC chip.

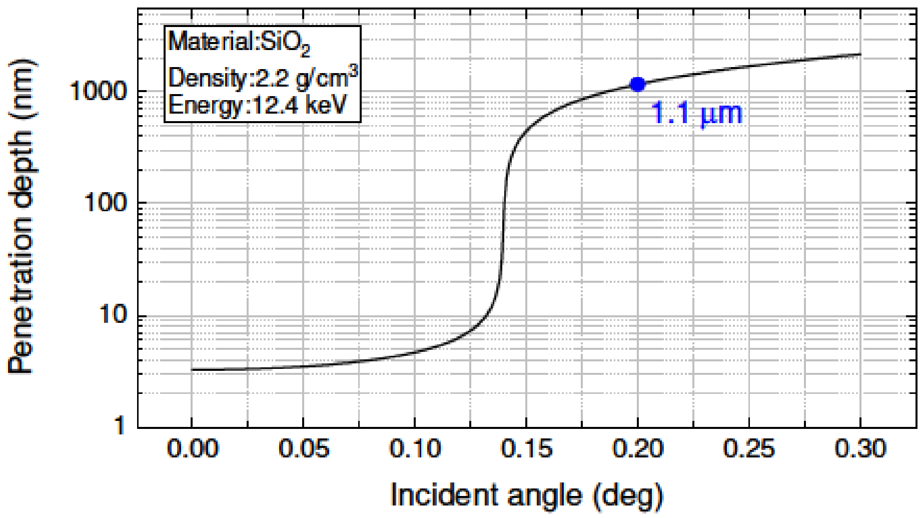

Fig. 2.3. Penetration depth versus incident angle of X-ray (12.4 keV).

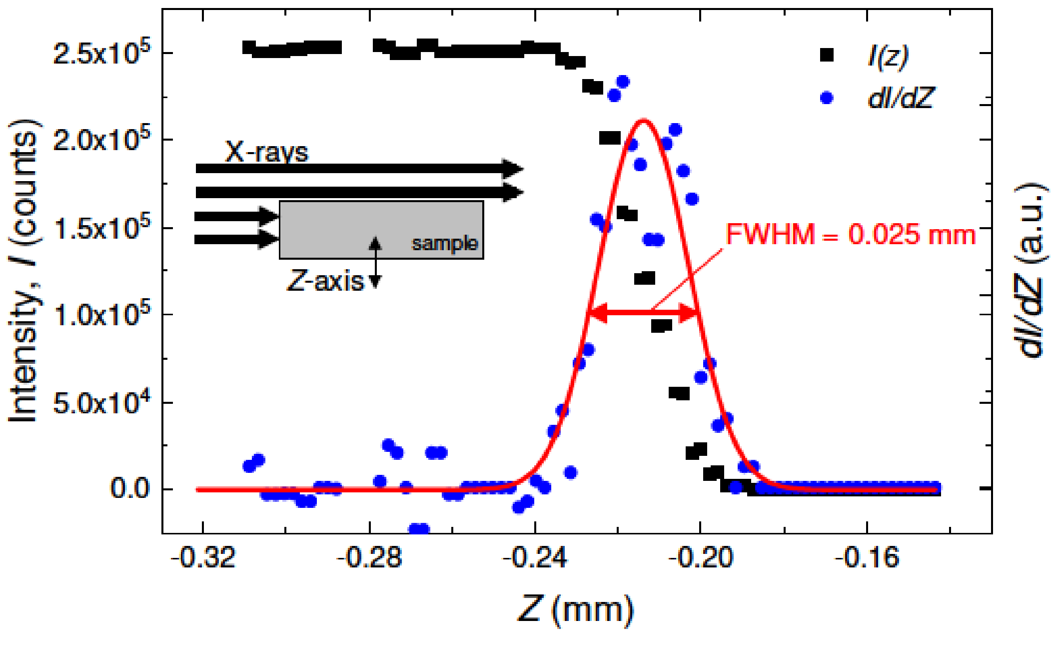

Fig. 2.4. X-ray intensity and scanning of *Z*-axis. FWHM (full width at half maximum) was estimated by Gaussian function.

2.3 Results and discussion

2.3.1 Structural and interfacial properties

Figure 2.5(a) shows the 2D-XRD images of the layered gate dielectrics with various cap-SiO_2/BaO_2 thicknesses. For a 3-nm-thick BaO_2 layer, crystal diffraction was not observed neither with nor without the SiO_2 cap layer. In other words, the gate dielectrics were amorphous. When the BaO_2 thickness was over 6 nm, annular Bragg diffractions appeared. The annular diffraction patterns indicate the presence of a polycrystalline structure in the dielectric. The diffraction pattern strongly depended on the cap-SiO_2 thickness, and poly-crystalline $Ba_5Si_8O_{21}$ [23] and $Ba_3Si_5O_{13}$ [24, 25] were formed at thicknesses of 0 and 20 nm.

Figure 2.5(b) shows the bidirectional C–V curves corresponding to the various SiO_2/BaO_2 thicknesses. All MOS capacitors exhibited a clockwise hysteresis due to electron injection, not mobile ion drift. The MOS capacitors with polycrystalline Ba-silicate exhibited a large frequency dispersion around the flat-band voltage, suggesting a high D_{it} value [26]. This trend is independent of the cap-SiO_2 thickness.

In contrast, the 3-nm-thick BaO_2 layer resulted in a smaller frequency dispersion around the flat-band voltage, only when the SiO_2 cap layer was used. Thus, the amorphous Ba-silicate interface is expected to have a low D_{it} value.

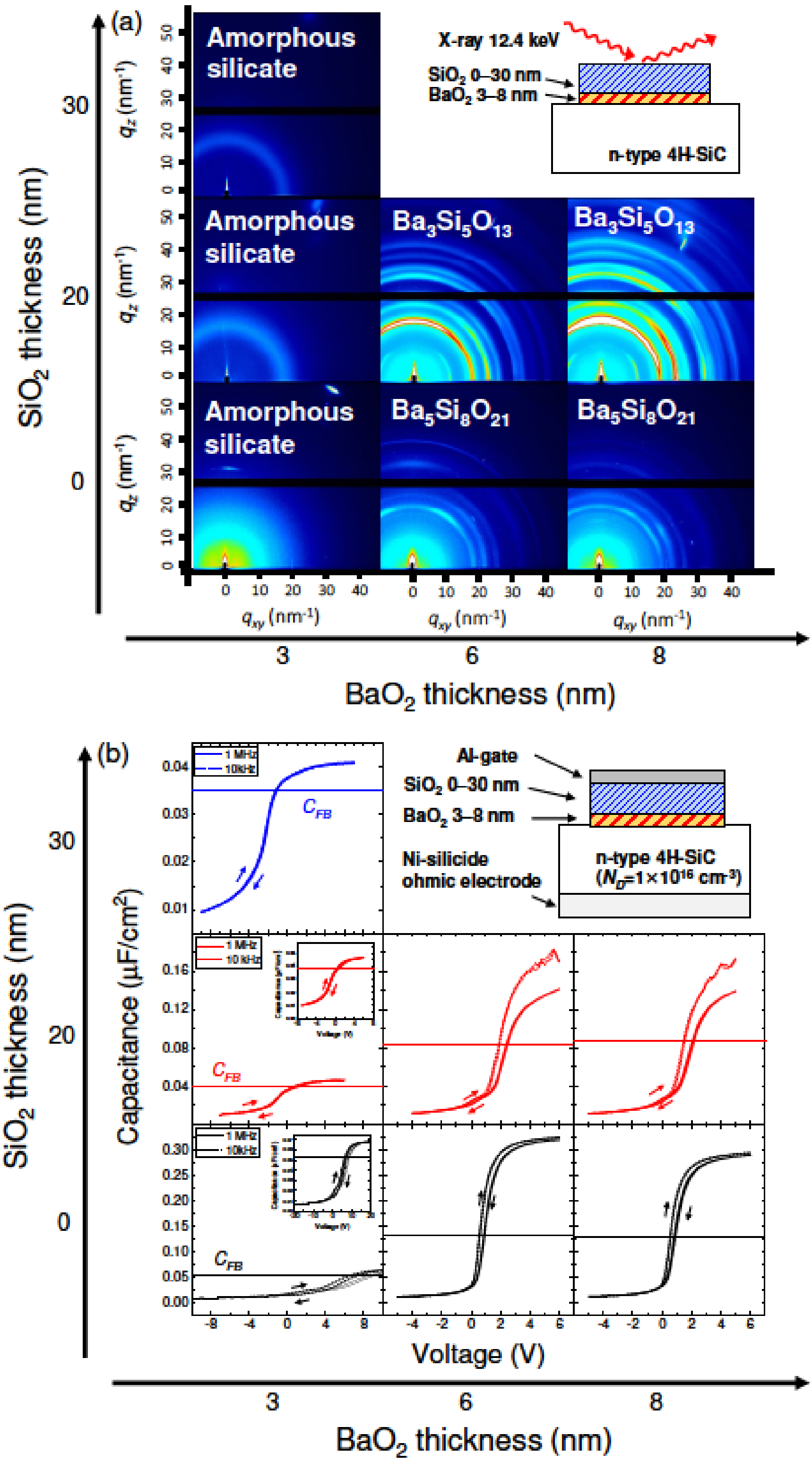

Fig. 2.5. Thickness dependences in SiO₂/BaO₂ layers on (a) 2D-XRD images and (b) bidirectional C–V characteristics. q_{xy} and q_z denote the horizontal and vertical scattering vectors. C_{FB} is the flat-band capacitance. The inset shows the schematic cross-section of the sample, and the deposited thicknesses prior to oxidation.

2.3.2 Evaluation of interface trap density

D_{it} was extracted by conductance method [27]. This method determines D_{it} value from conductance due to interface states of the MOS capacitor when biased in depletion. The interface-state-conductance, G_p/ω, is extracted from experimental data by

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}{}^2}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2}, \quad (2.1)$$

where G_p and ω are an equivalent parallel conductance and angular frequency; C_m, G_m are a measured capacitance and conductance per unit area, respectively; C_{ox} is gate-oxide capacitance per unit area. In this work, G_p/ω was measured as functions of frequency, gate bias, and measurement temperature. The temperature was varied from 25 to 200 °C to extend the measurable energy range.

G_P/ω curve can be simulated using the following equation [27, 28]:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \frac{\exp(\eta)}{\omega\tau_n} \ln\left(1 + \omega^2 \tau_n{}^2 \exp(-2\eta)\right) \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) d\eta, \quad (2.2)$$

where q, ω, τ_n, and σ_s are the elementary charge, angular frequency, time constant, and surface potential fluctuation, respectively. η is defined at $\eta = V_s - \langle V_s \rangle$, where V_s is the normalized surface potential to kT/q.

The surface potential, ψ_s, was determined by a semiconductor capacitance (C_s) [29]. It is expressed by

$$C_s = C_p - C_{it}, \quad (2.3)$$

$$C_p = \sqrt{\frac{C_{ox}{}^2 G_p}{G_m} - \frac{G_p{}^2}{\omega^2}} - C_{ox}, \quad (2.4)$$

$$C_{it} = \frac{qD_{it}}{2\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \frac{\exp(\eta)}{\omega\tau_n} \tan^{-1}(\omega\tau_n \exp(-\eta)) \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) d\eta. \quad (2.5)$$

C_{it} and C_p denote an interface-trap capacitance and an equivalent parallel capacitance. Figure 2.6 shows one example of the capacitances as a function of frequency. C_s was independent of frequency. In other words, the surface potential was determined only by gate bias, indicating the validity of this method.

Figures 2.7(a) and (b) show the G_p/ω curves at the energy levels of $E_t - E_i = 1.0$ eV and 1.4 eV, where E_t and E_i denote the energy levels of the interface traps and the intrinsic Fermi level, respectively. For comparison, G_p/ω curves of a thermally-grown SiO_2/SiC are included. The SiO_2 was grown at 1150 °C in dry O_2 ambient, and the thickness was 20 nm.

Figure 2.7(c) shows the D_{it} values as a function of the relative energy level. For the 20-nm thick cap-SiO_2, the D_{it} value was comparable with that of the thermal-grown SiO_2. Both the D_{it} values were 3×10^{12} cm^{-2}eV^{-1} at $E_t - E_i = 1.4$ eV. With increasing SiO_2 thickness, the D_{it} value decreased to 2×10^{11} cm^{-2}eV^{-1} at an energy level of 1.4 eV. These results indicate that the D_{it} value is affected not only by the BaO_2 thickness but also by the cap-SiO_2 thickness. The D_{it} value is not necessarily improved even though BaO_2 is incorporated into the interface.

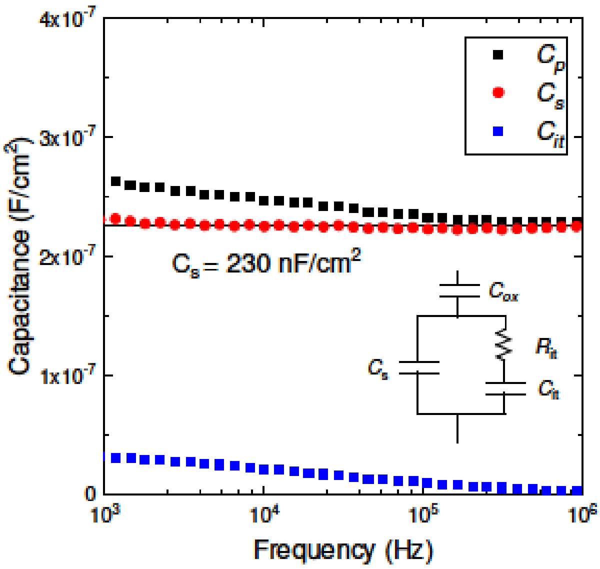

Fig. 2.6. C_p, C_s, and C_{it} characteristics as a function of frequency for MOS capacitor with SiO_2 30 nm and BaO_2 3 nm. R_{it} is a resistance due to the energy loss during electron transfer between interface states and the conduction band of 4H-SiC.

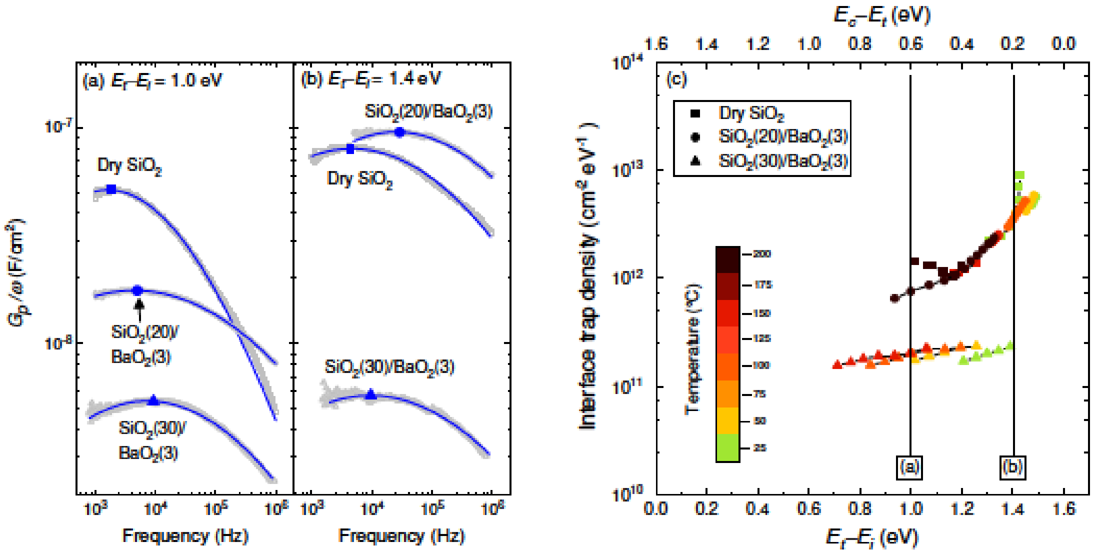

Fig. 2.7. G_p/ω curves at E_t-E_i = (a) 1.0 and (b) 1.4 eV. The symbols and solid lines indicate the experimental and simulation data, respectively. (c) Interface trap density (D_{it}) as a function of the energy relative to E_i. Each thickness is given in parentheses.

2.3.3 Distribution of Ba with and without cap-SiO_2 layer

Figure 2.8 shows the depth profile of Ba and the related elements with various cap-SiO_2 thicknesses; the BaO_2 thickness was fixed at 3 nm. The sample without capping exhibited two peaks in the Ba profile, as shown in Fig. 2.8(a). The intensity of the Ba ion took maximum on the gate-dielectric surface; moreover, the SiO_2/SiC interface had high intensity. This result indicates that the Ba distribution is segregated by oxidation into the dielectric surface and the dielectric/SiC interface. Without SiO_2 capping, most Ba-silicate is located on the surface; interfacial Ba is scarce. The MOS capacitor with this condition caused a large frequency dispersion, as shown in Fig. 2.5(b). The residual Ba concentration is inadequate for improving electric characteristics.

Figure 2.8(b) and (c) show the SIMS results with capping. The cap-SiO_2 thicknesses were 20 nm and 30 nm. Both the Ba profiles were similar; the intensity of the Ba ion was maximum at the dielectric/SiC interface, which increased further on approach to the dielectric surface. The high intensity near the surface implies the diffusion of Ba into the SiO_2 region during oxidation. With capping, most Ba-silicate remains intact at the interface even after oxidation. These SIMS profiles with and without capping are consistent with those reported by Chanthaphan et al. [10, 30].

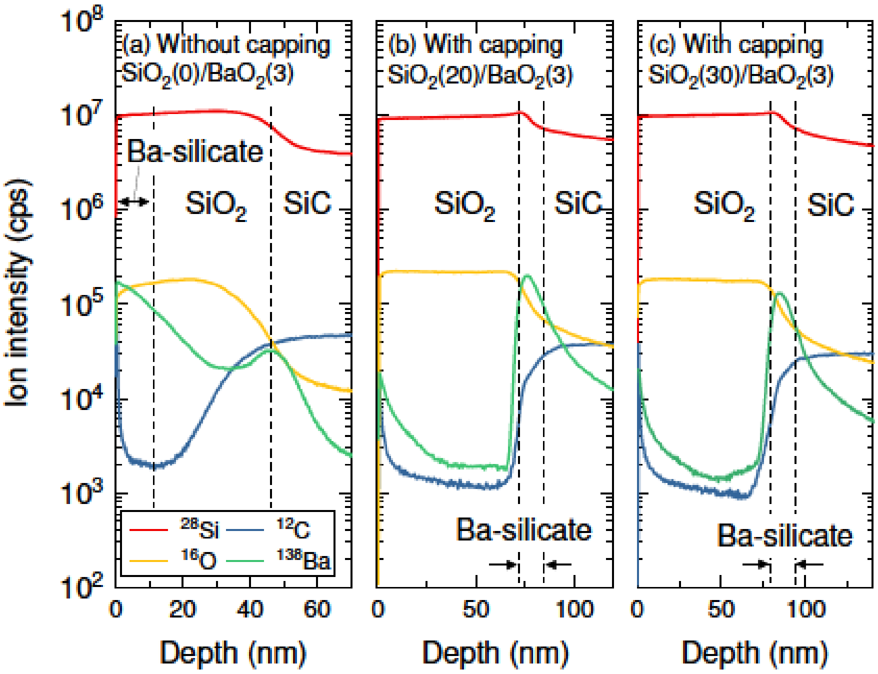

Fig. 2.8. SIMS depth profiles of layered dielectric/SiC samples with various cap-SiO_2 thicknesses. (a) 0 nm, (b) 20 nm, and (c) 30 nm. Each thickness is indicated inside the parentheses in the figure.

2.3.4 Stoichiometry of interfacial Ba-silicate layer

Using XRR, thickness of a layered gate dielectric is determined. Figure 2.9 shows one of the measured XRR profiles and a simulated curve. The thicknesses of the BaO_2 and SiO_2 layers were 3 and 20 nm. For the simulation, I employed a three-layer SiO_2/Ba-silicate/SiC model based on the SIMS results. Fitting parameters are summarized in Table 2.2.

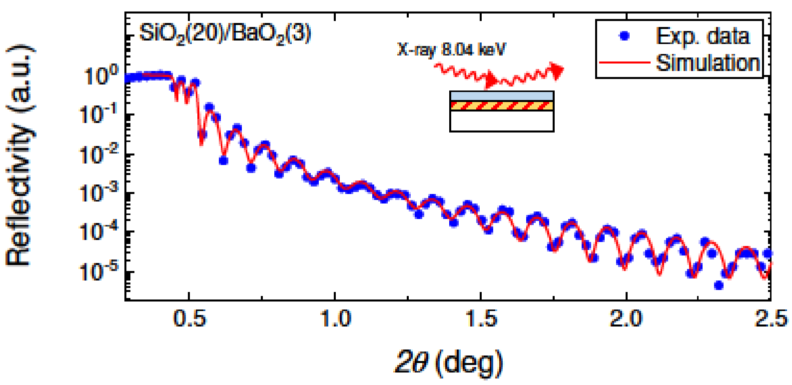

Fig. 2.9. an XRR profile and a simulated curve. Each thickness is given in parentheses.

Table 2.2. Structural parameters corresponding to the simulated curve in Fig. 2.9.

Material	Density (g/cm^3)	Thickness (nm)	Roughness (nm)
SiO_2	2.30	70.9	0.88
$Ba_5Si_8O_{21}$	3.31	3.07	0.46
4H-SiC	3.21	–	0.20

Figure 2.10(a) shows a summary of the fitting parameters of all the samples as a function of the SiO_2 cap thickness. The BaO_2 thickness was fixed at 3 nm. The thickness of the Ba-silicate ($d_{silicate}$) decreased from 3.1 to 1.8 nm with increasing cap-SiO_2 thickness, whereas the density ($\rho_{silicate}$) increased from 3.3 to 3.6 g/cm^3. The surface roughness increased from 0.46 to 1.7 nm. These variations imply the formation of different silicate structures with increasing cap-SiO_2 thickness.

Figure 10(b) shows the relationship between the cap-SiO_2 thickness and the binding energy of Ba $3d_{5/2}$ orbital. All the Ba 3d spectra exhibit a single peak. The binding energy slightly decreased from 781.1 to 780.6 eV with increasing cap-SiO_2 thickness. This chemical shift indicates a difference in the crystal structure of Ba-silicate. As a reference, the binding energies of three silicates ($Ba_5Si_8O_{21}$, $Ba_3Si_5O_{13}$, and BaO_2) are included in Fig. 10(b). The peak position of $Ba_3Si_5O_{13}$ is at 781.1 eV, which is higher than that of $Ba_5Si_8O_{21}$. The binding energy of BaO_2 was much lower than those of the other samples.

The mole percentages of BaO in $Ba_3Si_5O_{13}$ and $Ba_5Si_8O_{21}$ are 37.5 and 38.5 mol%, respectively. In other words, $Ba_5Si_8O_{21}$ contains more BaO than $Ba_3Si_5O_{13}$. Barium oxide shows an anomalous negative binding energy shift relative to the metal Ba [31]. Hence, it is predicted that BaO-rich silicate exhibits a lower binding energy. The thicker cap-SiO_2 layer led to a decrease in the binding energy, indicating the formation of a BaO-rich silicate structure with the deposition of the cap-SiO_2 layer.

BaO-rich silicate has a higher electron density than SiO_2-rich silicate. For example, the theoretical densities of $Ba_3Si_5O_{13}$, $Ba_5Si_8O_{21}$, and BaO_2 are 3.71, 3.73, and 5.39 g/cm^3, respectively [32]. The increasing trend in $\rho_{silicate}$ also supports the formation of a BaO-rich silicate structure. The dependence of SiO_2 thickness can be explained by the diffusion of oxygen. A thicker SiO_2 layer suppresses the diffusion of oxygen into the MOS interface during oxidation [33]. As a result, the thermal oxidation rate of SiC decreases, thus forming BaO-rich silicate at the interface.

Lichtenwalner et al. [12, 19] speculated that the ionic nature of Si-Ba bonding could enhance the flexibility of interfacial atoms and thereby improve mobility. BaO-rich silicate is expected to contain more ionic bonds and act as a buffer layer, thereby reducing the interfacial strain. Thicker cap-SiO_2 resulted in the reduction of D_{it} and formation of BaO-rich silicate. This result corroborates the mechanism proposed by Lichtenwalner et al.

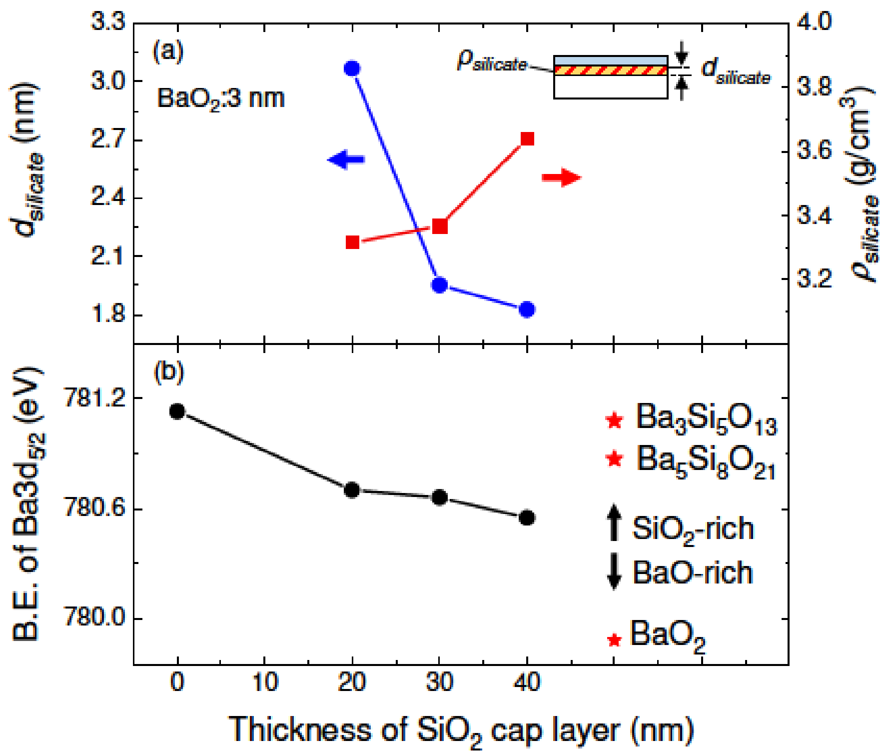

Fig. 2.10. (a) $d_{silicate}$, $\rho_{silicate}$, and (b) binding energy of Ba 3d $_{5/2}$ orbital as a function of cap-SiO_2 thickness.

2.4 Conclusions

In this chapter, the effects of cap-SiO_2 thickness on the structural and interface properties of a layered SiO_2/Ba-silicate gate dielectric was discussed. It is concluded that the SiO_2 cap layer plays two important roles in the formation of Ba-silicate; one is to ensure that Ba-silicate remains intact at the MOS interface even after oxidation. Without the cap layer, the most silicate is formed near the dielectric surface, whereas SiO_2 capping helps localize Ba-silicate at the MOS interface. The other role is to control the stoichiometry of interfacial silicate. A thicker cap-SiO_2 layer resulted in a more BaO-rich silicate structure. Moreover, the interface trap density reduced with increasing thickness.

It is also shown the poly-crystallization of Ba-silicate at BaO_2 thicknesses was induced over 6 nm. The poly-crystallization of Ba-silicate resulted in a large frequency dispersion around the flat-band voltage, even though the Ba-silicate layer was localized at the MOS interface.

An interfacial BaO-rich silicate is conducted to be necessary for improving the 4H-SiC MOS interface properties. When pure O_2 ambient is utilized for oxidation in the Ba-incorporation method, thicker cap-SiO_2 over 30 nm is needed. In order to achieve both the thin cap-SiO_2 layer and high mobility, it would be effective to reduce the annealing temperature, its time, and oxygen concentration during oxidation. Depositing a thick BaO_2 layer may provide BaO-rich silicate at the MOS interface. However, this can induce poly-crystallization.

At 100% of oxygen concentration during oxidation, 3 nm-thick BaO_2 and 30 nm-thick cap-SiO_2 layers are suitable to improve MOS interface properties.

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Chapter 3

High-temperature characteristics of SiC MOSFETs with interfacial Ba-silicate layer

3.1 Introduction

The development of SiC MOSFETs with high-temperature reliability has been progressed. In 1991, Davis et al. of North Carolina State University reported an enhancement-mode MOSFET utilizing 6H-SiC and poly-Si gate; it operated up to 650°C [1]. The good drain-current saturation was obtained at a temperature in the range of 25°C to 400°C. At 650°C, the slight leakage current flowed when applying a high drain-source voltage (V_{DS}). In 2014, Ghani et al. of General Electric [2] reported that using the N-incorporation method and poly-Si gate, the 4H-SiC MOSFETs provided stable operation at a temperature in the range of −193 to 500°C. Moreover, they demonstrated a ring oscillator and an amplifier built of the MOSFETs. These integrated circuits exhibited long-time stability for more than 100 hours at 500°C.

In our research group, Kuroki et al. reported high-temperature operation of 4H-SiC MOSFET with thin thermal-SiO_2 up to 450°C [3]. Thus, at least, an operational temperature of a developed MOSFET needs to be over 450°C. In the previous chapter, it is shown that for the Ba-incorporation method, the roles of SiO_2/BaO_2 layers and a clue to improve SiC MOS interface. Based on these results, I fabricated n-channel MOSFETs with a different cap-SiO_2 thickness and evaluated their high-temperature characteristics.

3.2 Experimental procedure

A fabrication process is shown in Fig. 3.1. Lateral n-channel MOSFETs were fabricated on p-type 4H-SiC (0001) Si-face epilayer (4° off-axis) with the acceptor concentration of 6×10^{17} cm^{-3}. The channel length (L) and width (W) were designed by the ion-implantation regions and the gate-metal width. Source/drain (S/D) regions were formed by arsenic ion implantation at a temperature of 500°C. Subsequently, the substrate covered with a diamond-like carbon film was annealed for impurity activation at 1800°C in Ar atmosphere. The donor concentration and the S/D junction depth (x_j) were 5×10^{19} cm^{-3} and 130 nm.

After a wet cleaning process, a layered gate dielectric with an interfacial Ba-silicate layer was formed by the following process. Firstly, 3 nm of thin BaO_2 layer was deposited on the 4H-SiC substrate by the RF sputtering method. Subsequently, 30 nm or 40 nm of thick SiO_2 layer was deposited on BaO_2/4H-SiC by the RF sputtering method. Both depositions were carried out in the same vacuum chamber at room temperature. The sample was oxidized in dry-oxygen ambient at 950°C in a quartz tube furnace, forming an interfacial Ba-silicate layer at MOS interface.

As the gate metal, 1 wt% Si-doped Al was deposited on the gate-dielectric using DC-sputtering. The reaction of pure aluminum with SiO_2 can be significant at temperatures on the order of 500°C [4]. However, Si-doped Al can be expected to reduce dissolution and transport of Al into an SiO_2 layer even at a high temperature of 500°C [5, 6].

- Surface cleaning
- BaO_2 sputter deposition (3 nm)
- SiO_2 sputter deposition (30 or 40 nm)
- Oxidation (in O_2 gas, 950°C, 1hr)
- Deposition of Ni/Nb bilayer (100 nm)
- Silicidation (in N_2 gas, 900°C, 5min)
- Gate metal deposition (1 wt% Si-doped Al, 200 nm)
- Deposition of interlayer insulator (NSG, 500 nm)
- Formation of pad electrode (1 wt% Si-doped Al, 600 nm)

Formation of layered-gate dielectric

Fig. 3.1. Fabrication process of SiC MOSFETs with the Ba-incorporation.

S/D ohmic contacts were formed by depositing a Ni/Nb bilayer of 100 nm, followed by annealing at 900°C. For passivation, a non-doped silicate glass (NSG) interlayer of 500 nm was deposited on the sample by using atmospheric pressure chemical vapor deposition (APCVD). After contact-via patterning, 1 wt% Si-doped Al was deposited and patterned as the pad electrodes. Figure 3.2 shows a schematic layout of the fabricated MOSFET.

Electrical characterization at high temperatures from 27°C to 500°C was carried out by direct wafer probing system in KTH Royal Institute of Technology, Sweden, as shown in Fig. 3.3.

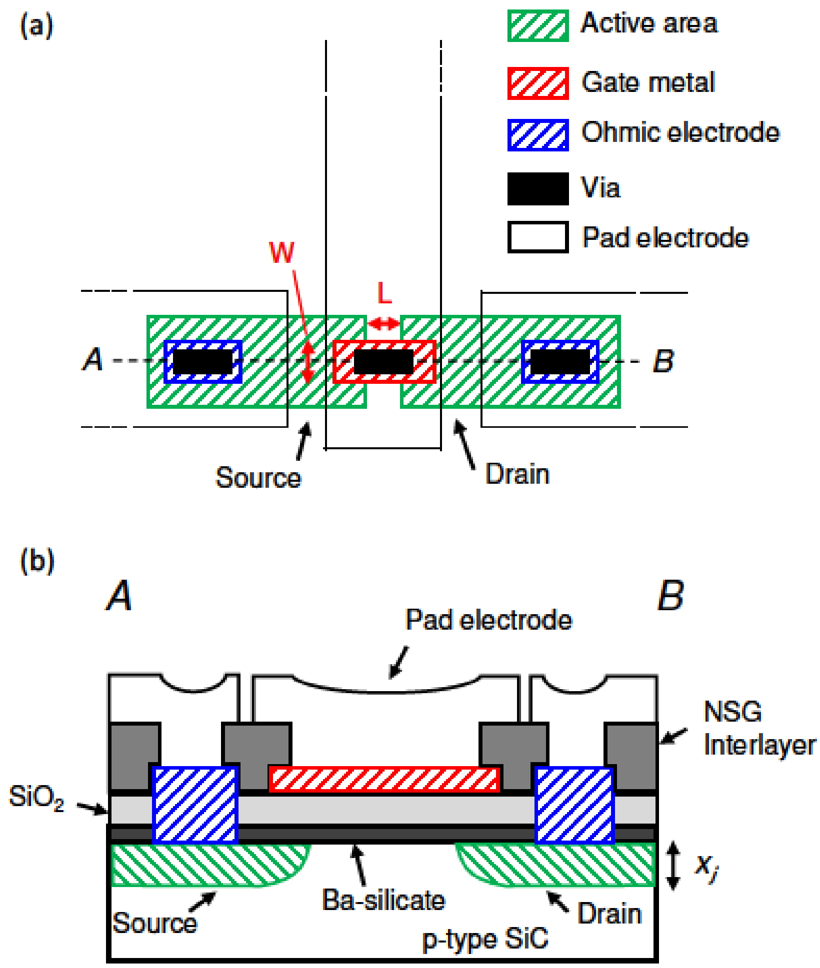

Fig. 3.2. Schematic layout of fabricated MOSFET: (a) top view and (b) cross-section along the *A*–*B* line (from the source to drain region).

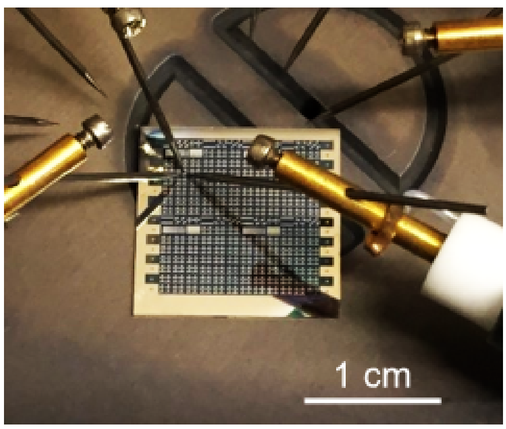

Fig. 3.3. Photograph of the MOSFETs on SiC chip during measuring high temperature characteristics.

3.3 Results and discussion

3.3.1 Influences of cap-SiO_2 thickness on high-temperature characteristics

Figure 3.4(a), (b) show drain current versus drain-source voltage (I_D–V_{DS}) characteristics at measurement temperatures (T) of 27°C and 500°C; the cap-SiO_2 thickness ($d_{cap\text{-}SiO2}$) was 30 nm. The device dimensions were L = 5 µm, and W = 50 µm. The MOSFET showed the clear characteristics with linear and saturation regions even at 500°C. Moreover, drain characteristics for $d_{cap\text{-}SiO2}$ = 40 nm are shown in Fig. 3.5. As well as $d_{cap\text{-}SiO2}$ = 30 nm, typical drain characteristics were obtained.

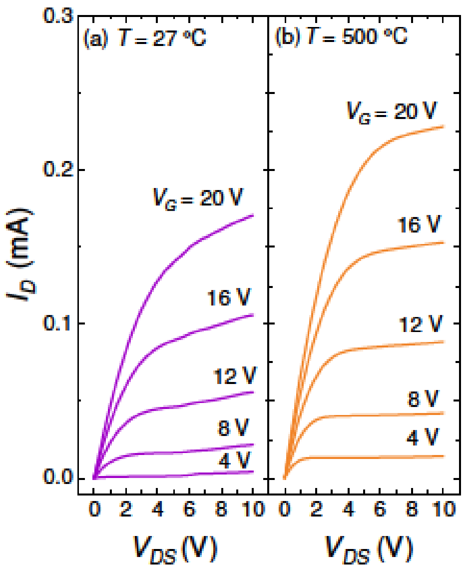

Fig. 3.4. I_D–V_{DS} curves for $d_{cap\text{-}SiO2}$ = 30 nm at temperature of (a) 27°C and (b) 500°C.

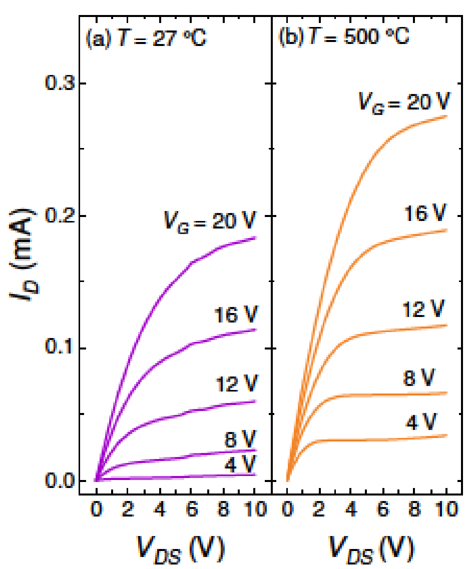

Fig. 3.5. I_D–V_{DS} curves for $d_{cap\text{-}SiO2}$ = 40 nm at temperature of (a) 27°C and (b) 500°C.

Figure 3.6(a), (b) shows drain current versus gate voltage (I_D–V_G) characteristics in a temperature range of 27–500°C for $d_{cap\text{-}SiO2}$ = 30 nm and 40 nm. In both cases, 10 nA of the off-leakage current flowed above 400°C, and the leakage current increased with the increasing measurement temperature. The insets in Fig. 3.6(a), (b) show the hysteresis of I_D at 500°C. The threshold voltage shifts (ΔV_{th}) with the clockwise direction were +3.1 V and +1.9 V, respectively. A positive threshold voltage shift is derived from electron injection, not mobile ion drift [7].

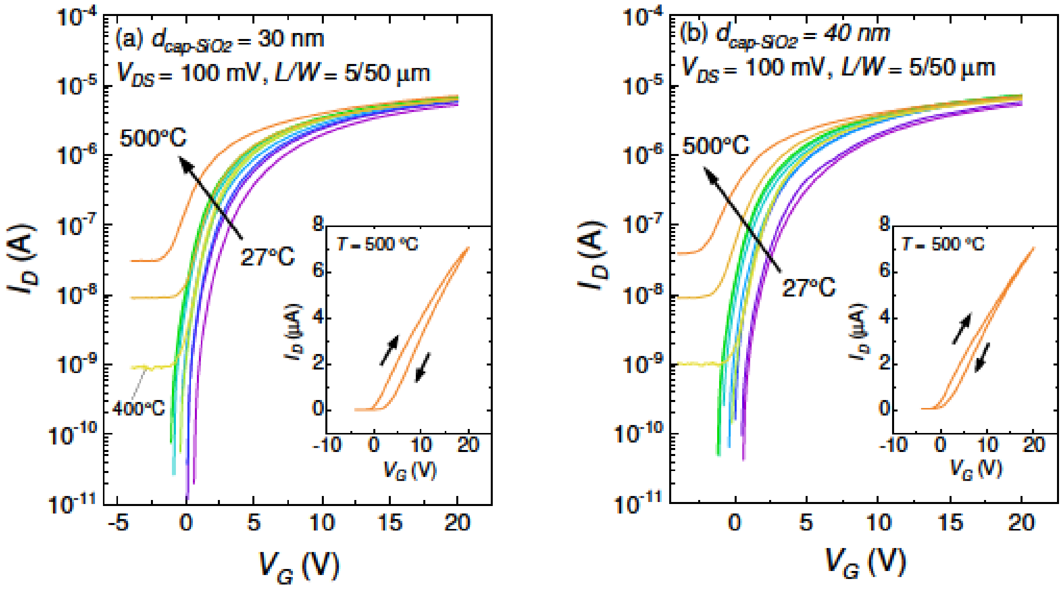

Fig. 3.6. I_D–V_{DS} curves for (a) $d_{cap\text{-}SiO2}$ = 30 nm and (b) $d_{cap\text{-}SiO2}$ = 40 nm at temperature range of 27–500°C. The insets show bidirectional drain current curves at 500°C.

Figure 3.7 shows field-effect mobilities (μ_{FE}) with different cap-SiO_2 thickness at two temperatures of 27°C and 500°C. μ_{FE} is given by

$$\mu_{FE} = \frac{L}{WC_{ox}V_{DS}}\frac{dI_D}{dV_G}, (5.1)$$

where C_{ox} is the gate-oxide capacitance per unit area and V_G is the gate voltage. At 27°C, each peak mobility was 9.0 and 10 $cm^2V^{-1}s^{-1}$; the thicker cap-SiO_2 layer resulted in higher mobility. The result supports the idea that a thick cap-SiO_2 layer forms BaO-rich silicate, thereby enhances channel mobility, written in Chapter 2. Both channel mobilities increased at 500°C.

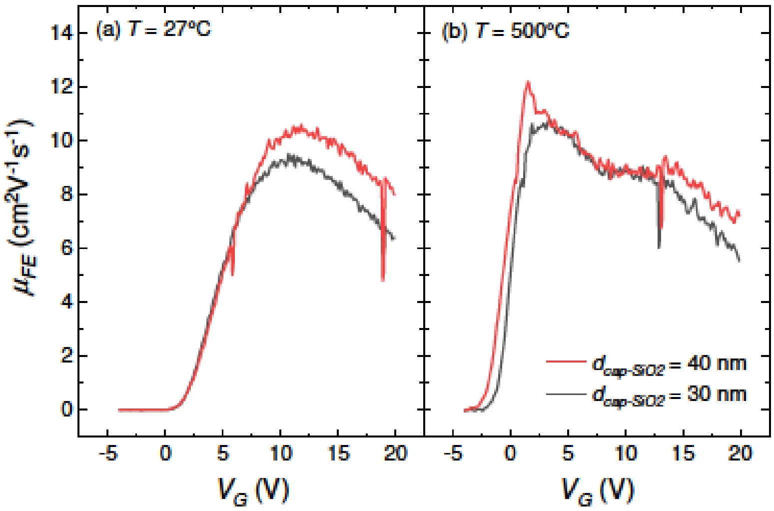

Fig. 3.7. Field-effect mobilities with different cap-SiO2 thickness at two temperatures of (a) T = 27°C and (b) T = 500°C. Channel length and width were 5 µm and 50 µm. The drain-source voltage was 100 mV.

Figure 3.8 and 3.9 show temperature dependencies of μ_{FE} and threshold voltage (V_{th}) for $d_{cap\text{-}SiO2}$ = 30 nm and 40 nm. V_{th} was determined by linear extrapolation. For $d_{cap\text{-}SiO2}$ = 30 nm, the mobility slightly increased in proportion to $T^{0.05}$. V_{th} decreased with a rate of −7.0 mV/°C. Note that V_{th} increased at a temperature of over 350°C. This trend also emerged for $d_{cap\text{-}SiO2}$ = 40 nm. In the case of 40 nm, the V_{th} decreased with a rate of −8.5 mV/°C; over 350°C, V_{th} increased. Turn-around of V_{th} suggests that electron injection into slow traps like near-interface traps (NITs) in a gate dielectric [8].

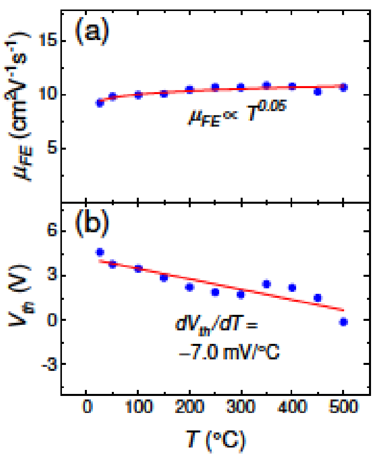

Fig. 3.8. Temperature dependencies of (a) μ_{FE} and (b) V_{th} for $d_{cap\text{-}SiO2}$ = 30 nm.

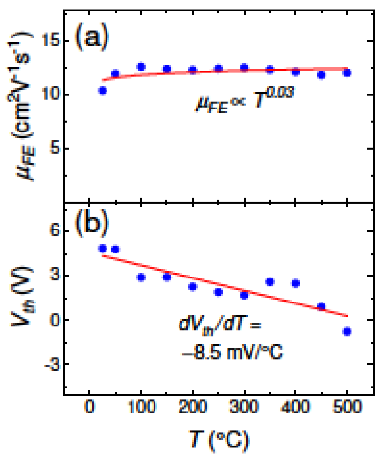

Fig. 3.9. Temperature dependencies of (a) μ_{FE} and (b) V_{th} for $d_{cap\text{-}SiO2}$ = 40 nm.

The density of trapped electrons was estimated from the hysteresis of I_D–V_G curve. All MOSFETs exhibit a threshold voltage shift (ΔV_{th}) with the clockwise direction in the range of 27–500°C. A trapped-electron density (ΔN_{te}) is simply given by

$$\Delta N_{te} = C_{ox}\Delta V_{th}/q. \quad (5.2)$$

ΔV_{th} and ΔN_{te} as a function of T are shown in Fig. 3.10. There is a peak of ΔV_{th} at 100°C in the both samples; corresponding ΔN_{te} values were 3×10^{11} cm^{-2} and 7×10^{11} cm^{-2}. Moreover, at 150°C, threshold voltage shifts decreased. That is, interfacial Ba-silicate layers have slow traps at an energy level above the conduction band of SiC, and these states were filled by electron injection with thermal energy at 100°C. With increasing temperature, ΔV_{th} increased again. For $d_{cap\text{-}SiO2}$ = 30 nm, ΔN_{te} exhibited a maximum value of 8×10^{11} cm^{-2} at 450°C. Whereas ΔN_{te} for $d_{cap\text{-}SiO2}$ = 40 nm had 7×10^{11} cm^{-2} of ΔN_{te}. That is, the Ba-silicate layer with 40 nm of cap-SiO_2 had smaller slow trap density at high temperatures.

A clockwise hysteresis of I_D indicates that electron injection, not mobile ion drift. That is, the interfacial Ba-silicate structures are stable even at 500°C. Previously, Lichtenwalner et al. reported that the threshold voltage of the MOSFET with Ba was stable up to 175°C by bias-temperature stress test. They expected that the thermodynamically stable Ba-compound resulted in the durable MOS interface without mobile ion [9]. As shown in Fig. 2.10, Chapter 2, interfacial Ba-silicate had Ba atom with a binding energy of 780.6 eV. This binding energy is higher than that of the metallic Ba (779.5–780.2 eV) [10, 11]. That is, the incorporated Ba atom is strongly bonded to the non-bridging oxygen in the silicate structure [12]. This difference would stabilize high-temperature characteristics even at 500°C.

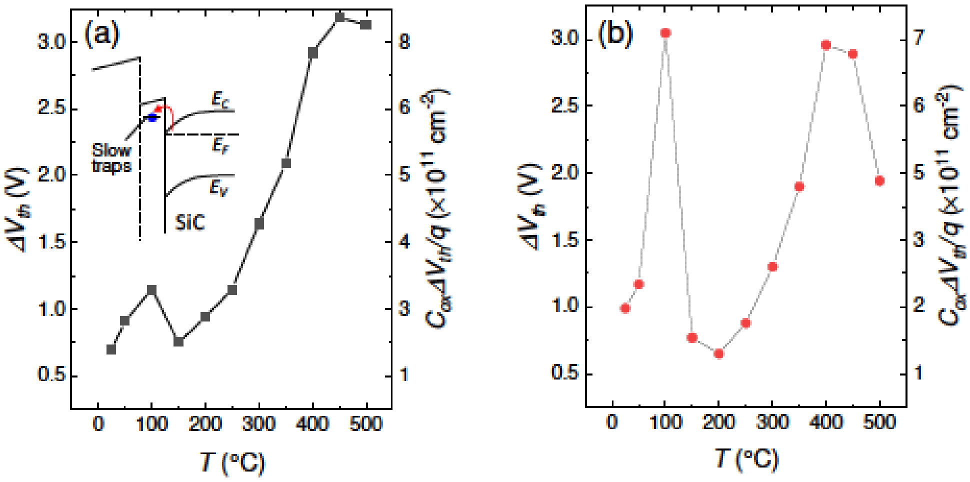

Fig. 3.10. Temperature dependencies of ΔV_{th} and ΔN_{te} for (a) $d_{cap\text{-}SiO2}$ = 30 nm and (b) 40 nm. The inset shows energy band diagram with slow traps.

3.3.2 Influences of high-temperature measurement on SiC MOSFETs

After measuring electrical characteristics up to 500°C, the SiC MOSFETs were cooled to room temperature. I_D/I_G–V_G characteristics of the cooled MOSFET were then measured at T = 27°C, shown in Fig. 3.11. The thickness of cap-SiO_2 was 40 nm. After cooling, the subthreshold swing was not changed. It indicates that the MOS interface was not damaged due to the electron injections during the measurements. The positive ΔV_{th} was 220 mV, and the calculated ΔN_{te} was 5.0×10^{10} cm^{-2}. Thus, the injected electrons at T = 500°C almost removed. In the term of I_G, the leakage current of the cooled MOSFET was slightly larger than that of the as-fabricated MOSFET. These results imply that the density of slow traps in the gate dielectric slightly increased due to electron injection during the measurement.

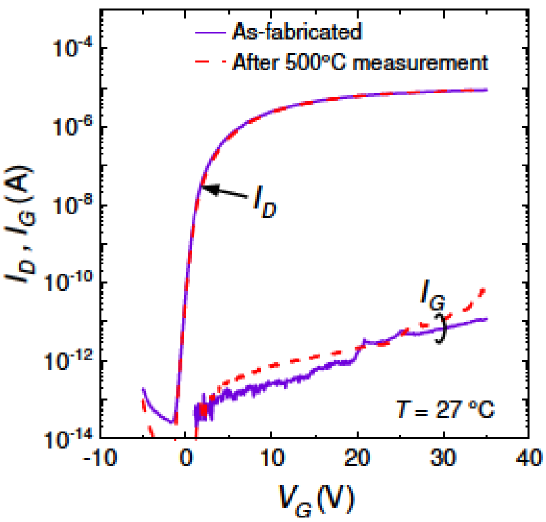

Fig. 3.11. I_D–V_{DS} curves before and after 500°C measurement at a measurement temperature of 27°C. (L/W = 5/50 µm, V_{DS} = 100 mV, $d_{cap\text{-}SiO2}$ = 40 nm)

Figure 3.12(a), (b) display top-view micrographs of the SiC MOSFET before and after 500°C measurement. Some voids with a diameter of 5–8 µm were seen on Al pad-electrodes of SiC MOSFETs after 500°C measurement. Moreover, the Al pad with the voids peeled off by pricking probe needle, shown in Fig 3.12(c). The peel-off of the Al pad indicates the reduction of adhesion to NSG interlayer dielectric by heating. In most cases, the pad electrode for gate metal was taken off, and other pad electrodes remained on the interlayer dielectric.

Tanimoto et al. reported the impact of high temperatures on Al electrode in Ref. [6]. They showed the creation of Al_2O_3 voids around an interlayer dielectric as a result of a chemical reaction between Al and Si, after 12 hours of storage at 500°C. There is a possibility that voids on Al pads, shown in Fig. 3.11 (b), are originated by Al_2O_3 void.

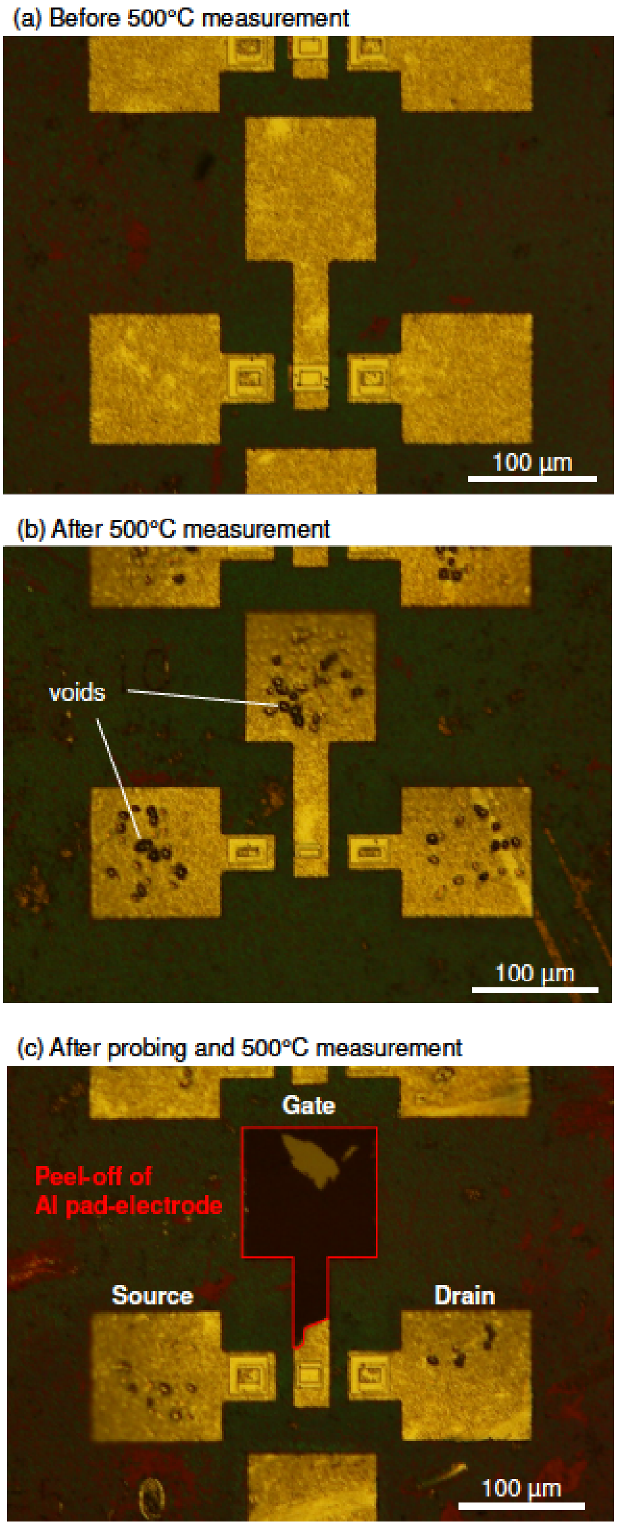

Fig. 3.12. Top-view micrographs of SiC MOSFETs (a) before and (b) after 500°C measurement and (c) after probing.

3.3.3 Thermally grown SiO_2 and Ba-incorporated SiO_2

In this subsection, a MOSFET with incorporated Ba is compared with previously fabricated-MOSFET. The former MOSFET had a layered gate dielectric with $d_{cap\text{-}SiO2}$ = 40 nm, expressed as Ba-incorporated SiO_2; the latter one had thermally grown SiO_2, expressed as Dry SiO_2. This SiO_2 film was grown at 1150°C in dry-oxygen ambient, and the thickness was 20 nm. The detail fabrication process was reported in Ref. 3. Both MOSFET have the same acceptor concentration of 6×10^{17} cm^{-3} on the channel region.

Figure 3.13 shows the temperature dependence of μ_{FE}. Channel length and width were 5 and 50 µm, respectively. For the Ba-incorporated SiO_2, the field-effect mobility was approximately 12 $cm^{-2}V^{-1}s^{-1}$ in the range of 50–500°C, slightly increased in proportion to $T^{0.03}$. Whereas, using Dry SiO_2 as gate-oxide, the mobility dramatically increased in proportion to $T^{1.3}$. The mobility of the Ba-incorporated SiO_2 was more stable than that of Dry SiO_2. As shown in Fig. 2.7, Chapter 2, Dry SiO_2 resulted in high interface trap density of 3×10^{12} $cm^{-2}eV^{-1}$ near the conduction band edge. This high defect states induce Coulomb scattering of the channel carries, thereby producing an increase in μ_{FE} with increasing temperature. The difference in the proportions of the two MOSFETs implies that the Ba-incorporated SiO_2 has significantly lower interface state density.

Figure 3.14 shows a dependence on the temperature of threshold voltages. For Ba-incorporated SiO_2, V_{th} of the MOSFET decreased with a rate of –8.5 mV/°C. Whereas, V_{th} for Dry SiO_2 decreased with a rate of –4.3 mV/°C. The V_{th} stability of Dry SiO_2 is higher than that of Ba-incorporated SiO_2. It is influenced by high C_{ox}. The total thickness of the Ba-incorporated SiO_2 is 93 nm and 4.7 times thicker. The thick gate-dielectric degrades the temperature dependence of V_{th} [7].

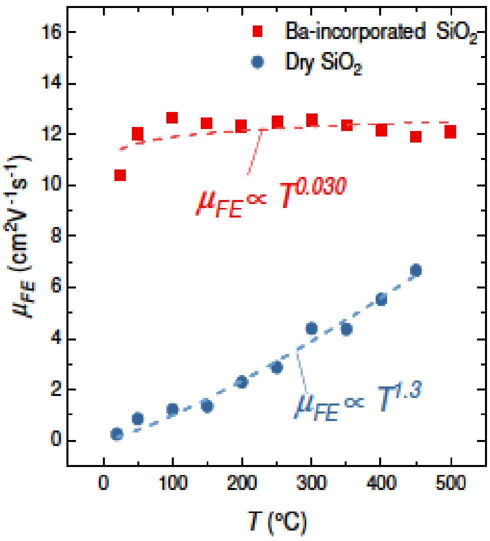

Fig. 3.13. Field-effect mobilities with Ba-incorporated SiO_2 and DrySiO_2 as a function of temperature.

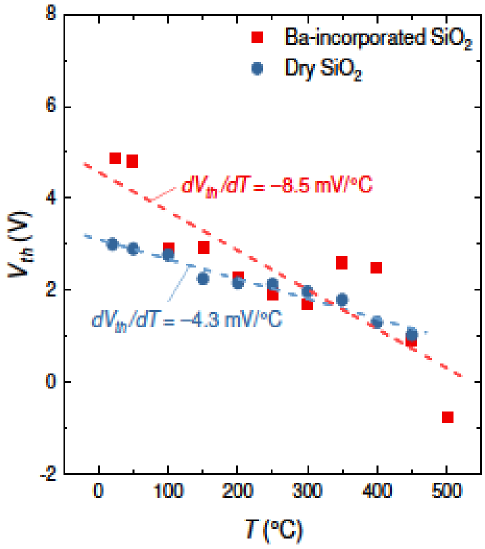

Fig. 3.14. Threshold voltages with Ba-incorporated SiO_2 and DrySiO_2 as a function of temperature.

3.4 Conclusions

In this chapter, high-temperature characteristics of three SiC MOSFETs with two different cap-SiO_2 thickness and Dry SiO_2 were shown and discussed.

As expected in Chapter 2, the thicker cap-SiO_2 layer resulted in 10 $cm^2V^{-1}s^{-1}$ of higher channel mobility. Although the Ba-incorporated MOSFET could operate even at high-temperatures up to 500°C, the gate dielectrics with interfacial Ba-silicate layer had slow traps, which induced the turnaround of V_{th} at temperatures over 350°C. Ba-silicate layer with thicker cap-SiO_2 of 40 nm trapped 7×10^{11} cm^{-2} of electrons at 400°C.

In comparison with Dry SiO_2, the Ba-incorporated SiC MOSFET with $d_{cap\text{-}SiO2}$ = 40 nm exhibited more stable mobility with temperature thanks to lower interface state density. Whereas, the threshold voltage shift was larger than that of Dry SiO_2, due to thick gate-dielectric.

In the term of interface properties, 3 nm-thick BaO_2 layer and thick cap-SiO_2 more than 40 nm are suitable. In the next work, we need to find a method or a fabrication condition to stabilize threshold voltage at high temperatures over 300°C.

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Chapter 4

Radiation effects of SiC MOSFETs with interfacial Ba-silicate layer

4.1 Introduction

The radiation response of a MOS device is susceptible to the gate metal, oxide thickness, and the passivation technique [1–4]. In the case of conventional Si-MOSFETs, the Si-H bonds at the SiO_2/Si interface are broken by trapping the holes generated by gamma-ray irradiation, resulting in the degradation of channel mobility [3]. In SiC MOS devices, the nitrogen incorporation into MOS interface reduces TID tolerance [5, 6]. In 2006, Dixit et al. of Vanderbilt University compared radiation responses of nitrided and non-nitrided SiO_2/4H-SiC capacitors; significantly higher oxide-trapped charge density was observed in the nitrided sample [5]. In 2009, Arora et al. reported that nitrided gate oxide on 3C-SiC increased oxide-trapped positive charge. They revealed the relationship between the nitrogen density and the oxide-trapped charge density [6]. This relationship is also reported by Rozen et al. [7]. The current N-incorporation method requires high-temperature annealing over 1100°C, and it has not been optimized for radiation-hardened electronics [8].

A radiation response of P-incorporated oxide was also reported. Vivona et al. showed the Gate oxide annealed in $POCl_3$ resulted in larger flat band voltage shift in comparison with the N-incorporated oxide [9]. In summary, the method for acquiring the both high TID hardness and high mobility has not reported yet. In this chapter, it is evaluated that the radiation response of Ba-incorporated gate dielectric using MOSFET structure.

4.2 Experimental procedure

4.2.1 Device fabrication

Although fabrication process of SiC MOSFET is already written in Chapter 3, it is rewritten again here. N-channel MOSFETs with a Ba-silicate interface layer were fabricated on 4° off-axis 4H-SiC (0001) substrate with an epitaxial p-type SiC layer. The MOSFETs were designed without an isolation region, as shown in Fig. 4.1(a). The acceptor concentration (N_A) of the epitaxial layer was 6×10^{17} cm^{-3}, and the impurity was aluminum. Source/drain (S/D) regions were formed by As-ion implantation at the temperature of 500°C, followed by high-temperature activation at 1800°C. The channel length and width were designed by the ion-implantation regions and the gate-metal width, respectively. After a wet cleaning process, a layered gate dielectric with a Ba-silicate interface layer (called Ba-incorporated SiO_2) was formed by the following process. Firstly, a barium peroxide (BaO_2) layer of 3 nm was deposited on the 4H-SiC substrate by the RF sputtering method. Subsequently, silicon dioxide (SiO_2) of 40 nm was also deposited on BaO_2/4H-SiC by the RF sputtering method. Both depositions were carried out in the same vacuum chamber at room temperature. The sample was oxidized in dry-oxygen ambient at 950°C in a quartz tube furnace. After oxidation, the gate oxide thickness increased to 93 nm, and Ba-silicate was formed at the SiO_2/SiC interface. Aluminum gate metals and Ni/Nb ohmic contact materials were deposited by the sputtering method. Silicidation with SiC was carried out at 900°C. For passivation, a non-doped silicate glass (NSG) interlayer of 500 nm was deposited on the ohmic electrodes and the gate metals by using atmospheric pressure chemical vapor deposition (APCVD). After contact-via patterning, aluminum was deposited and patterned as wires. Figure 4.1(b) shows a schematic cross-section of the fabricated MOSFETs.

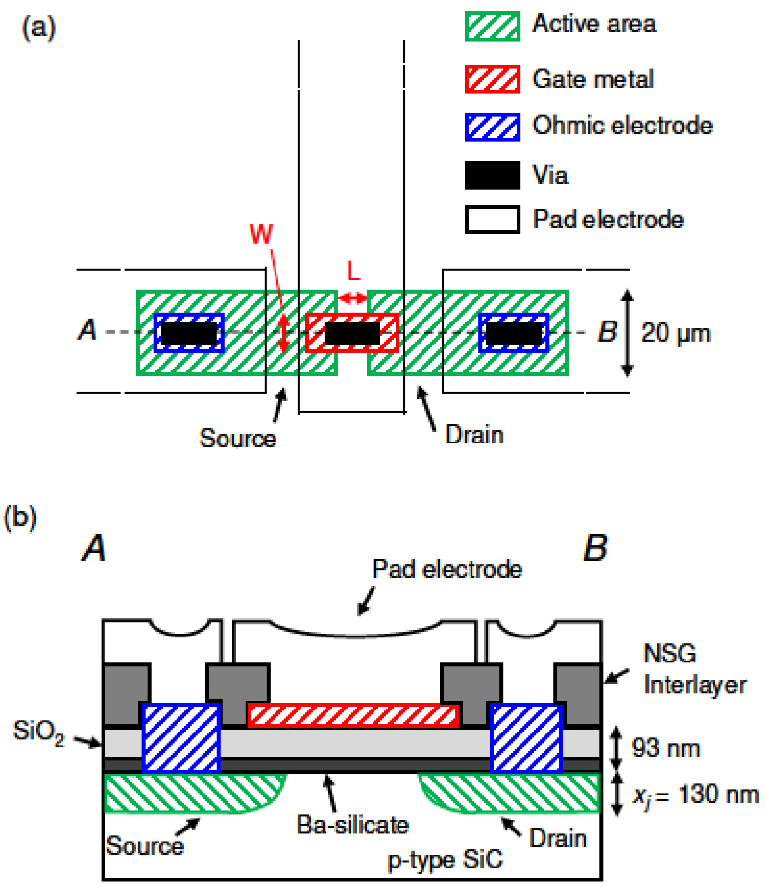


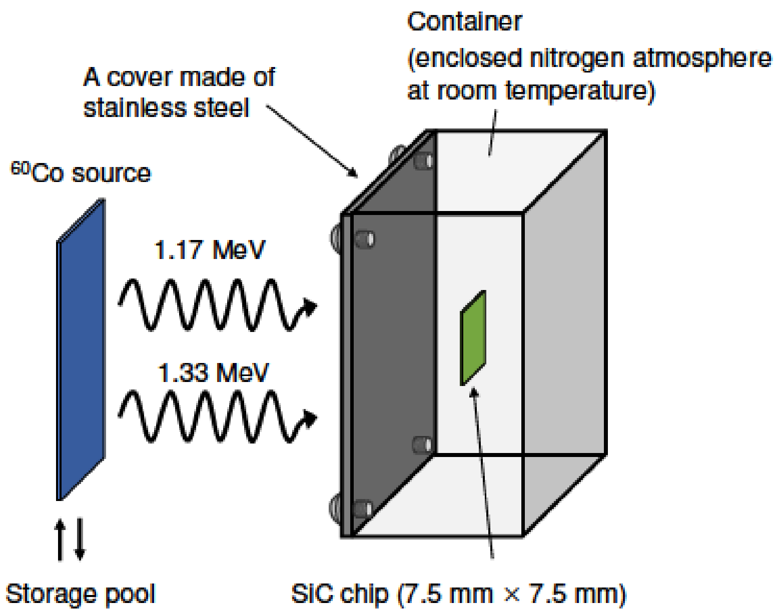
Fig. 4.1. (Repeat) Schematic layout of fabricated MOSFET: (a) top view and (b) cross-section along the *A*–*B* line (from the source to drain region).

4.2.2 Gamma-ray irradiation

Gamma-ray radiation on the MOSFETs was carried out at a cobalt-60 irradiation facility in Japan; the Takasaki Advanced Radiation Research Institute, National Institutes for Quantum and Radiological Science and Technology (QST). Figure 4.2 shows the irradiation setup. SiC chip with MOSFETs put in a container made of stainless steel, and the whole container was received gamma-rays. Nitrogen gas was enclosed in the container to prevent oxidation. The MOSFETs were irradiated with a gamma-ray dose rate of 10 kGy/h at room temperature. The total gamma-ray dose reached up to 850 kGy. During the irradiation, the substrate with the MOSFETs was grounded and no bias was applied to all electrodes.

The electrical characteristics were measured at room temperature prior to irradiation and after step-stress irradiations up to 850 kGy. In this chapter, the gamma-ray dose is expressed as an equivalent dose of SiO_2.

(a)



(b)

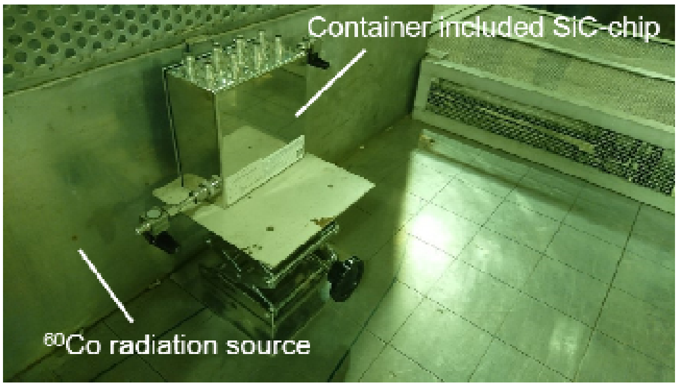


Fig. 4.2. (a) Schematic and (b) photograph of the irradiation setup.

4.3 Results and discussion

4.3.1 Midgap-subthreshold technique

Before showing experimental results, the midgap-subthreshold technique proposed by McWhorter et al. is explained here [10]. Radiation-induced threshold voltage shift (ΔV_{th}) is affected by both negative and positive components: interface traps (ΔV_{it}) and oxide-trapped charges (ΔV_{ox}). The midgap-subthreshold technique can separate ΔV_{th} into the contributions of ΔV_{it} and ΔV_{ox}.

The midgap-subthreshold technique performs applied as per the following steps [10–12]. The schematic of this technique is shown in Fig. 4.3. Firstly, the midgap current I_{mg} is calculated with the formula:

$$I_{mg} = \sqrt{2}\mu(W/L)(qN_A L_B/\beta)(n_i/N_A)^2 \exp(\beta\psi_s)\,(\beta\psi_s)^{-1/2}, \quad (4.1)$$

where q, μ, n_i, Ψ_S are the elementary charge, the channel mobility, the intrinsic carrier concentration, and the band bending at the SiC surface, respectively. In this study, the field-effect mobility (μ_{FE}) was used as the channel mobility. β is reciprocal thermal energy as given by q/kT. The Debye length is given by $L_B = [\varepsilon_{SiC}/(\beta q N_A)]^{1/2}$, where ε_{SiC} is the dielectric constant of SiC. I_{mg} is derived as the drain current when ψ_s corresponds to the midgap condition, $\psi_B = (kT/q)\ln(N_A/n_i)$.

Using the calculated I_{mg}, the midgap voltage (V_{mg}) is determined with the extrapolation of the I_D–V_G curve. When $\psi_s = \psi_B$, the interface traps in the upper half of the bandgap become neutral, and thus the interface traps do not contribute to the threshold voltage shift. A stretch-out voltage (V_{so}) is defined as

$$\Delta V_{so} = V_{th} - V_{mg}. \quad (4.2)$$

Sweeping the gate voltage from V_{mg} to V_{th} fills the interface traps in the upper half of the bandgap with electrons. As a result, the subthreshold curve is stretched with the variation of V_{so}, which is denoted as ΔV_{so}. If the device suffers from irradiation, ΔV_{it} is expressed by

$$\Delta V_{it} = \Delta V_{so} = V_{so,post} - V_{so,pre}, \quad (4.3)$$

where “post” and “pre” denote after and before irradiation. Since the interface traps at V_{mg} do not contribute any voltage shift, a threshold voltage shift at V_{mg} is caused only by oxide-trapped charges according to

$$\Delta V_{ox} = \Delta V_{mg} = V_{mg,post} - V_{mg,pre}. \quad (4.4)$$

The radiation-induced interface trap density (ΔN_{it}) and oxide-trapped charge density (ΔN_{ox}) are given by

$$\Delta N_{it} = C_{ox}|\Delta V_{it}|/q, (4.5)$$

$$\Delta N_{ox} = C_{ox}|\Delta V_{ox}|/q. (4.6)$$

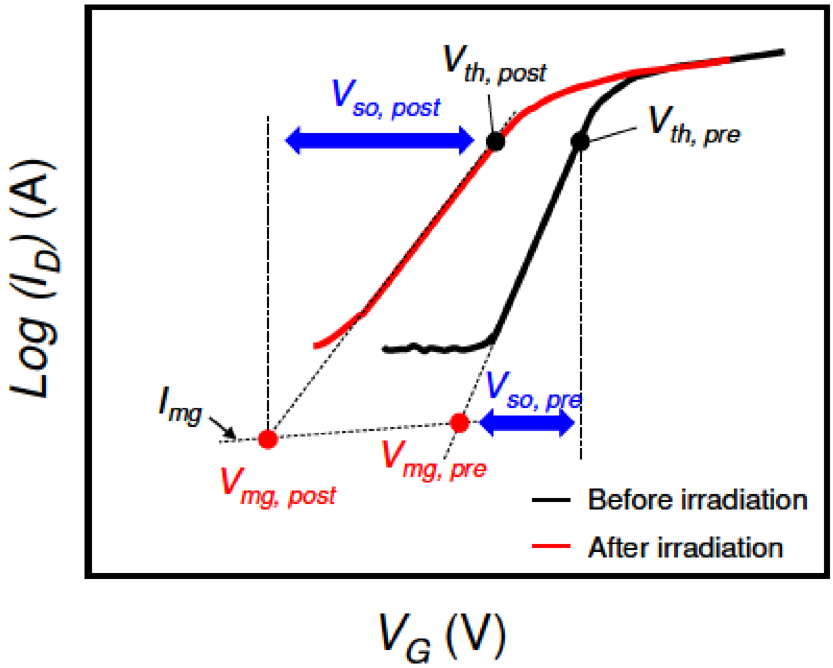


Fig. 4.3. Schematic of the midgap-subthreshold technique. "post" and "pre" denote after and before irradiation.

4.3.2 Degradation of I_D–V_G characteristics due to TID effect

Figure 4.4(a) shows I_D–V_G curves of the MOSFET from 0 kGy to 850 kGy. The channel length and width were 10 and 10 µm, and V_{DS} was set to 100 mV. The off-leakage current increased with the increasing total dose, and the on/off ratio decreased to 10^4 at 600 kGy. After irradiation of 850 kGy, the drain current decreased at a voltage of over 25 V. This reduction was induced by the gate-leakage current. Before irradiation, the threshold voltage (V_{th}) was 9.0 V by linear extrapolation of the I_D–V_G curve on a linear scale [11]. V_{th} shifted toward the lower V_G by increasing the total dose, and it became 2.3 V at 600 kGy. Above 600 kGy, a slight positive shift was observed. These trends indicate that interface traps and oxide-trapped charges are generated in the MOSFET by irradiation [13].

The total dose dependence of ΔV_{th}, ΔV_{it}, and ΔV_{ox} for the MOSFET is shown in Fig. 4.4(b). The values of ΔV_{it} and ΔV_{ox} shifted to the positive and negative voltage side by irradiation. These results indicate that gamma-rays generate negatively charged interface traps and positive charges in the gate dielectric.

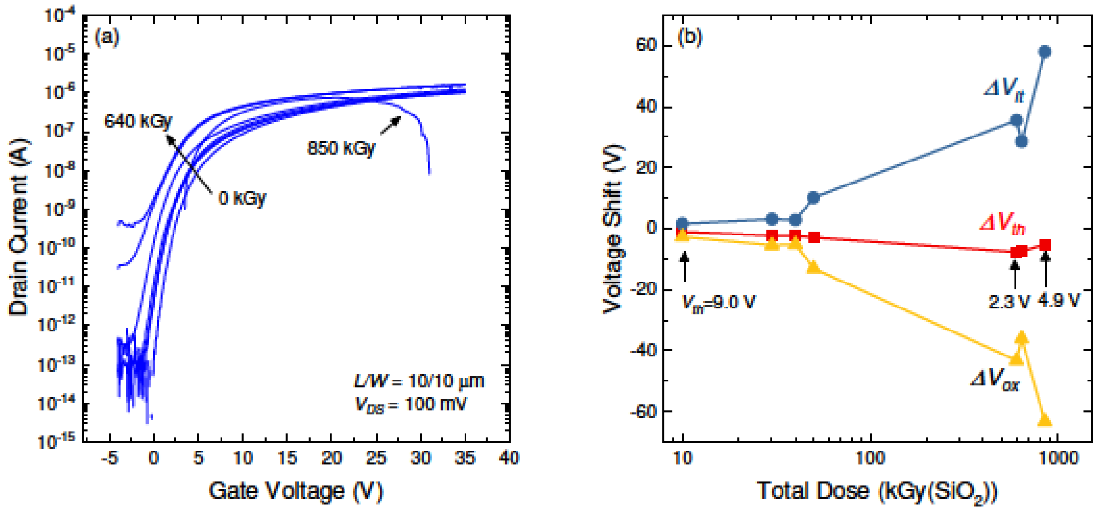


Fig. 4.4. (a) I_D–V_G curves for the Ba-incorporated MOSFET before and after irradiation up to 850 kGy (L/W = 10/10 µm, V_{DS} = 100 mV). (b) dependencies of ΔV_{th}, ΔV_{it}, and ΔV_{ox} on total dose for MOSFET.

The total dose dependence of ΔN_{it} for the Ba-incorporated SiO_2 is shown in Fig. 4.5(a). The values of ΔN_{it} increased with a total dose with an exponent of 2/3. For comparison, it is also shown that the dependence for another 4H-SiC MOSFET with thermal grown SiO_2, expressed as Dry SiO_2. This SiO_2 was formed by thermal oxidation in dry-oxygen ambient at 1150°C, and the thickness was 20 nm. The detail fabrication process was reported in Ref. 14. For the Dry SiO_2, the power-law dependence was an exponent of 2/3. The two gate oxides exhibit no difference in the power-law dependence. However, ΔN_{it} for the Ba-incorporated SiO_2 was higher than that for the Dry SiO_2. Figure 4.5(b) shows the total dose dependences of ΔN_{ox} for the Ba-incorporated SiO_2 and the Dry SiO_2. Both ΔN_{ox} increased with a total dose with an exponent of 2/3. As with ΔN_{it}, ΔN_{ox} for the Ba-incorporated SiO_2 was higher than that for the Dry SiO_2. These results clearly indicate that the Ba-incorporated SiO_2 has less radiation hardness than the Dry SiO_2.

Note that thicknesses of the Ba-incorporated SiO_2 and the Dry SiO_2 are different. The values of ΔN_{it}, ΔN_{ox} are affected by gate-oxide thickness. Thus, it can not be concluded that *interfacial Ba-silicate* reduces TID tolerance. To calibrate for the effects of gate-oxide thickness on radiation responses, dimensionless parameters of generated defects are calculated below. The interface trap generation efficiency (f_{it}) and the oxide charge trapping efficiency f_{ox} are estimated using following formulas [15]:

$$f_{it} = \frac{-\Delta V_{so}\varepsilon_0\varepsilon_s}{q\kappa_g f_y f_{de} {t_{ox}}^2 D}, (4.7)$$

$$f_{ox} = \frac{-\Delta V_{mg}\varepsilon_0\varepsilon_s}{q\kappa_g f_y f_{de} {t_{ox}}^2 D}, (4.8)$$

where ε_0 and ε_s are the vacuum permittivity and the relative permittivity of gate oxide; κ_g is the number of electron-hole pairs generated in gate-oxide; f_y is the probability that electron-hole pairs escaping initial recombination processes; f_{de} is the dose enhancement factor; t_{ox} is the oxide thickness and D is the adsorbed dose. The interfacial Ba-silicate layer accounts for only 2% of the whole Ba-incorporated SiO_2, and the greater layer consists of SiO_2. Moreover, ε_s of the Ba-incorporated SiO_2 was 3.8, closing to that of SiO_2 [16]. This relative permittivity was estimated from high frequency C–V curve.
Therefore, κ_g of SiO_2 (8.1×10^{14} cm^{-3}Gy^{-1}) is substituted to Eq. (4.7) and (4.8) for the both cases. f_y is estimated by numerical formula [17]:

$$f_y = \frac{1}{\frac{0.27}{E_{ox}+0.084}+1}, (4.9)$$

where E_{ox} is the applied oxide electric field during irradiation; E_{ox} = 0 MV/cm. f_{de} is 1 in the case of Co-60 gamma-ray [1].

The values of f_{it} and f_{ox} are shown in Table 4.1. f_{it} and f_{ox} of the Ba-incorporated SiO_2 are slightly smaller than that of the Dry SiO_2, indicating that the interfacial Ba-silicate layer is less prone to damage. That is, the interfacial Ba-silicate is essentially rugged than the Dry SiO_2. The great ΔN_{it} and ΔN_{ox} for the Ba-incorporated SiO_2 are strongly influenced of gate-oxide thickness.

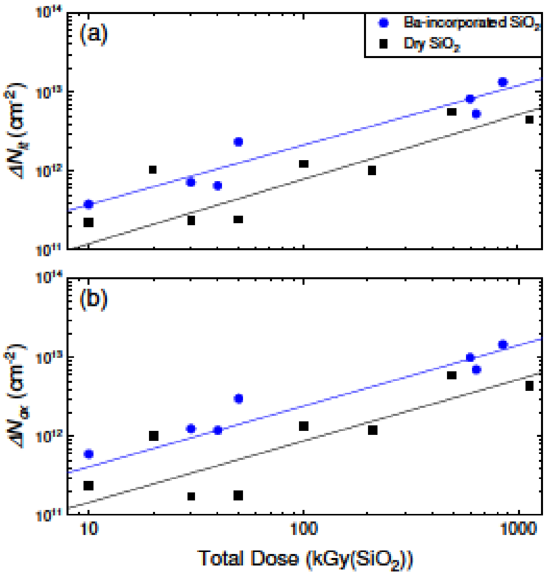


Fig. 4.5. Total dose dependencies of (a) ΔN_{it} and (b) ΔN_{ox} for the Ba-incorporated SiO_2. The vales for the Dry SiO_2 are also shown for comparison.

Table 4.1. Interface trap generation efficiency (f_{it}) and net oxide charge trapped efficiency (f_{ox}).

	t_{ox} (nm)	D (kGy)	ΔV_{it} (V)	ΔV_{ox} (V)	f_{it} (%)	f_{ox} (%)
Ba-incorporated SiO_2	93	850	58	–63	0.88	0.96
Dry SiO_2	20	1130	4.2	4.0	1.0	1.0

Figure 4.6(a) shows μ_{FE} versus V_G (μ_{FE}–V_G) curves before and after irradiation at two radiation doses. Although the gamma-ray generated the interface traps at the MOS interface, above 600 kGy, the field effect mobility increased from 12 to 18 cm^2/Vs. To clarify the relationship between the mobility and the interface trap density, the dependence of the mobility on ΔN_{it} is shown in Fig. 4.6(b). The mobility is normalized by the initial value at non-irradiation (μ_0). In ΔN_{it} below 4×10^{12} cm^{-2}, the normalized mobility was almost the same. However, the Ba-incorporated MOSFET exhibited an increase of the normalized mobility in ΔN_{it} above 7×10^{12} cm^{-2}. In the dissertation, this phenomenon is called radiation-induced mobility enhancement effect, and the origin and the mechanism will be discussed in the next chapter detail.

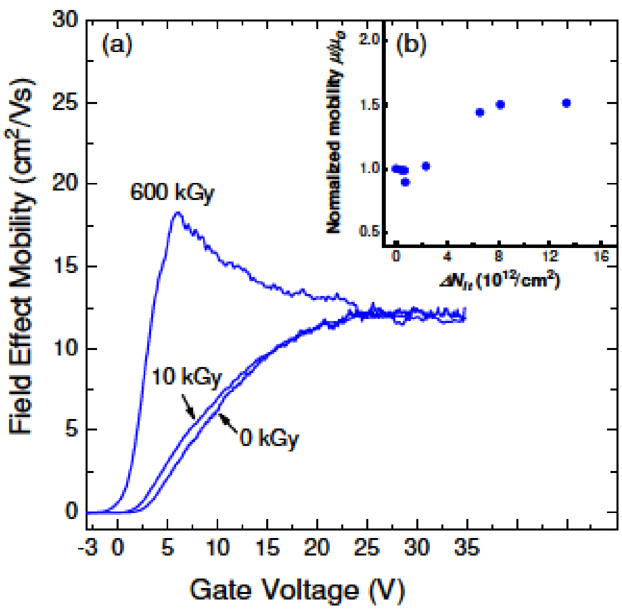


Fig. 4.6. (a) Field effect mobility of the MOSFET before and after irradiation at two radiation doses. (b) Relationship between the normalized mobility and ΔN_{it}, for the Ba-incorporated SiO_2.

4.3.3 Leakage current on I_D–V_{DS} characteristics

Figure 4.7(a), (b) show I_D–V_{DS} characteristics of the same MOSFET before and after irradiation. The non-irradiated MOSFET exhibited typical output characteristics with linear and saturation regions. After gamma-ray irradiation, the drain current increased overall. The increase in the drain current is attributed to a V_{th} decreasing and radiation-induced mobility enhancement effect. The irradiated MOSFET showed a clear linear region. However, the drain current on the saturation region suddenly increased at V_{DS} over 8V.

The threshold V_{DS}, which presents the sudden rise of I_D, is defined by the second derivative of I_D ($\partial^2 I_D/\partial V_G^2$), shown in Fig. 4.7(c). The threshold V_{DS} was 9 V except for V_G = 0V. Moreover, we define ΔI_D, which is the difference in drain current between V_{DS} = 8 V and V_{DS} = 10 V. The ΔI_D monotonically increased from 0.1 μA to 3 μA with increasing V_G, shown in Fig. 4.7(d). Thus, the ΔI_D is affected by V_G.

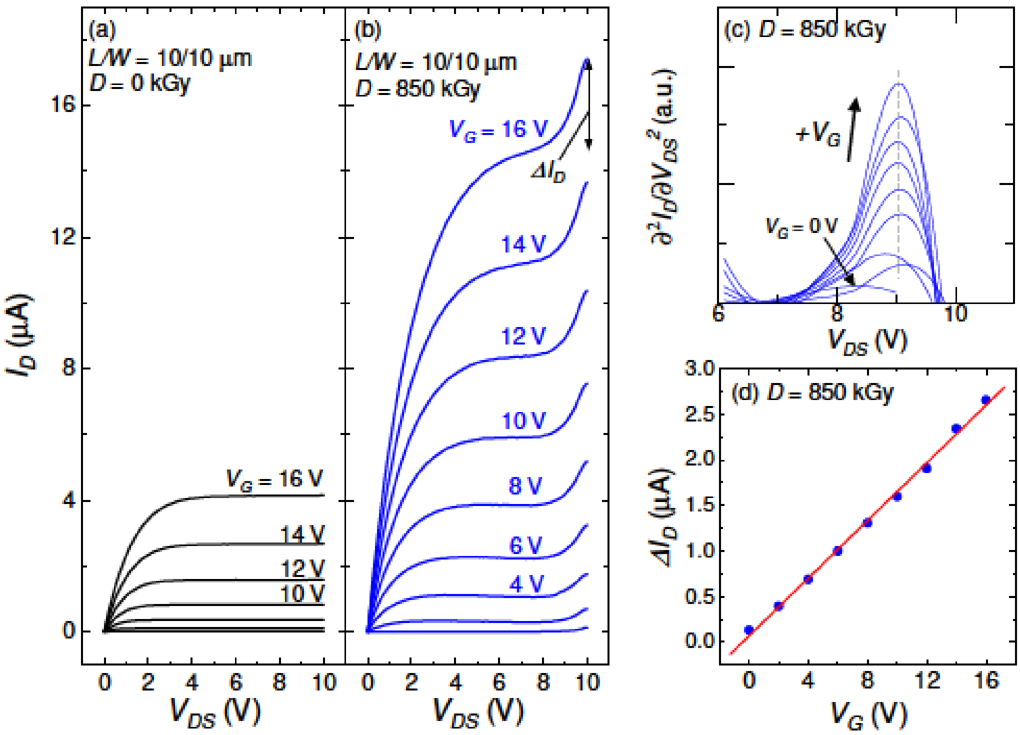


Fig. 4.7. I_D–V_{DS} curves for (a) non-irradiated MOSFET and (b) irradiated MOSFET. (c) $\partial^2 I_D/\partial V_G^2$ plot for the irradiated MOSFET. (d) ΔI_D versus V_G characteristic. Channel length and width are 10 μm and μm, respectively.

Here, the horizontal axis of Fig. 4.7(b) is converted from V_{DS} to drain-to-gate voltage (V_{DG}). This drain characteristic of the irradiated device is shown in Fig. 4.8. The threshold V_{DG} is defined as the same as the threshold V_{DS}. It was reduced from 9 V at V_G = 0 V with increasing V_G, reaching –7 V at V_G = 16 V. That is, this phenomenon occurs at positive and negative V_{DG}. Thus, the sudden increase emerges in both the accumulation and depletion conditions of the drain region overlapped with the gate metal. In order to confirm a condition of the drain region, the gate-to-drain capacitance (C_{GD}) was measured. Figure 4.9(a) shows the circuit for the C_{GD} measurement. The gate electrode and the drain region were connected to the high and low terminals, and the source region was grounded. Moreover, SiC substrate was electrically floated to prevent forming the inversion layer. Figure 4.9(b) shows a cross-sectional schematic of the MOSFET during the C_{GD} measurement. The obtained C_{GD}–V_{DG} curve is shown in Fig. 4.9(c). The measurement frequency was 10 kHz. C_{GD} increased with decreasing V_{DG} below V_{DG} = 6V, indicating accumulation of the drain region. Thus, the sudden increase of I_D at V_G = 20 V occurred when accumulated in the drain region. This result indicates that the sudden increase of I_D flowed for both the accumulation or the depletion of the drain region.

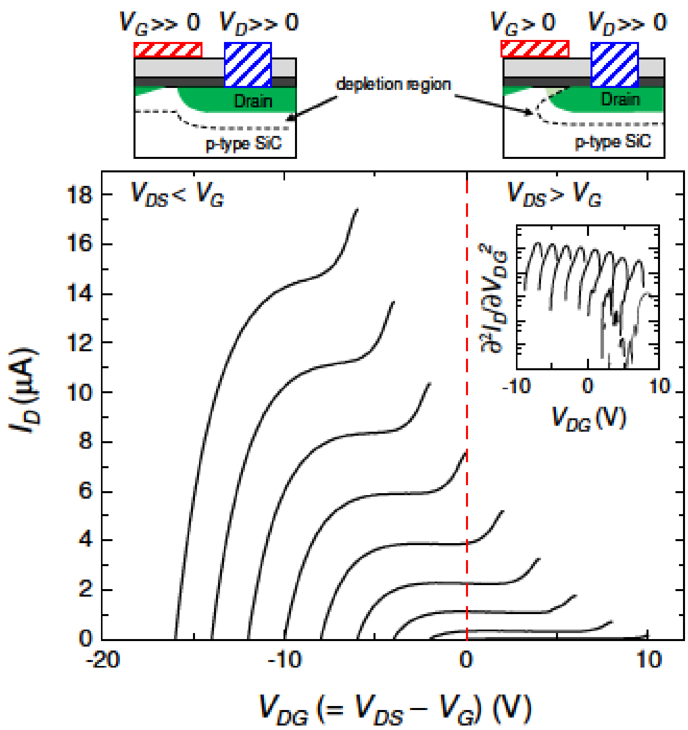


Fig. 4.8. I_D–V_{DG} curves for irradiated MOSFET. The inset shows $\partial^2 I_D/\partial V_{DG}^2$ characteristics.

Figure 4.10(a) shows the gate leakage current (I_G) characteristics. The lower V_{DS} region below V_{DS} = −6 V had a slight positive leakage current (I_G < +0.2 pA). The negative leakage current flowed at the voltage above V_{DS} = 8V. Moreover, the negative substrate current simultaneously flowed, shown in Fig.4.10(b). These currents are due to hole injections into the gate-oxide and the SiC substrate. That is, the sudden rise of I_D is accompanied by the hole injections. Therefore, the sudden rise of I_D is expected to derive from the generation of electron-hole pairs.

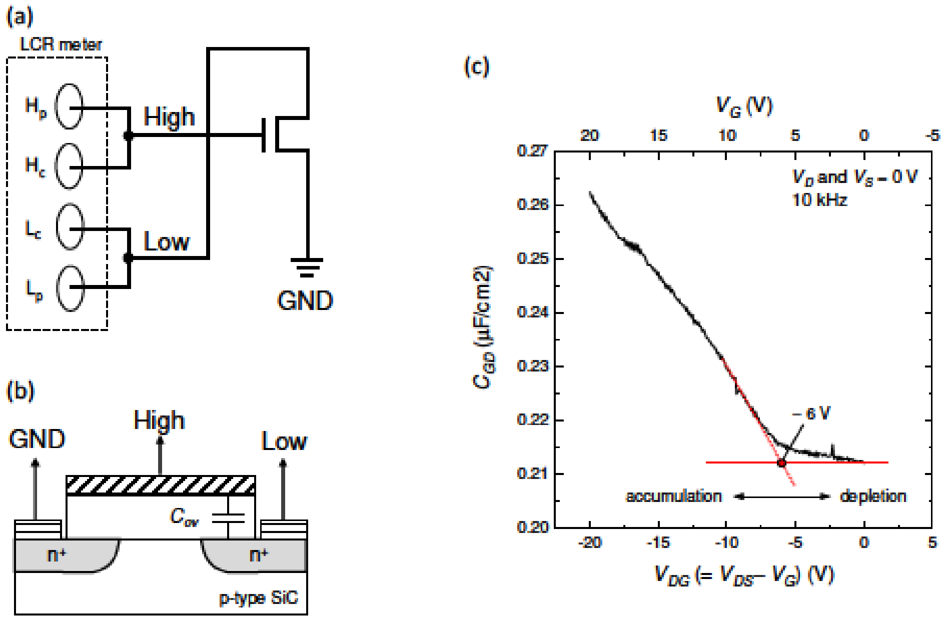


Fig. 4.9. Schematic for the C_{GD} measurement: (a) circuit and (b) cross-section. (c) C_{GD}–V_{DG} curves for irradiated MOSFET. C_{ov} is overlap capacitance.

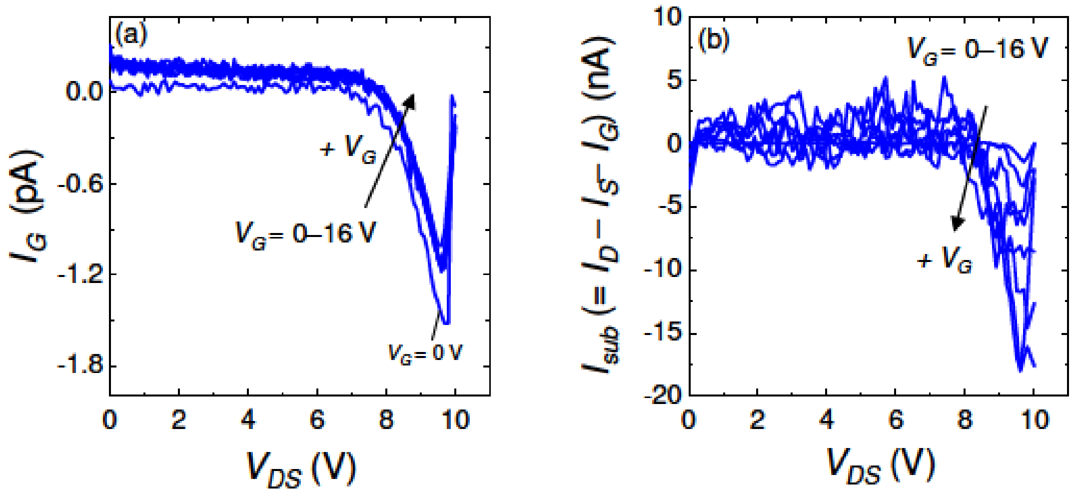


Fig. 4.10. (a) Gate leakage current and (b) substrate current characteristics after γ-ray exposure of 850 kGy.

The sudden increase of I_D on the saturation region resembles a gate-induced drain leakage (GIDL) current [18, 19]. This leakage current is caused by both the increasing V_{DS} and decreasing V_G. The GIDL current arises from band-to-band tunneling which occurs in the deep depletion layer underlying the overlap region of gate-to-drain. That is, it is caused by applying positive V_{DG}. Moreover, GIDL current is accompanied by generation of electron-hole pairs; the electrons move to the drain electrode; the holes are injected into gate-oxide and substrate electrode. Furthermore, interface traps increase GIDL current. Hori et al. reported the emerging GIDL current in low V_{DG} region after hot-carrier stressing. This is because generation of electron-hole pairs by band-to-defect tunneling via interface traps at MOS interface when the deep depletion region forms in the drain region [19], shown in Fig. 4.11. Since gamma-ray irradiation damages a gate-oxide and its interface due to TID effect, GIDL current seems to be most likely the origin of the sudden increase in I_D on saturation region. However, this mechanism inadequate explains the sudden rise of I_D which occurs in the accumulation condition of the drain region.

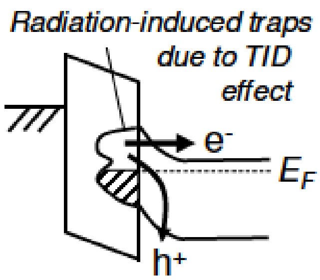


Fig. 4.11. Schematic diagram of band-to-defect tunneling via radiation-induced interface trap due to TID effect.

There is a possibility that electron-hole pairs are generated by the tunneling of the valence band electrons into the conduction band via deep defect states in the space-charge region at the drain-substrate junction, shown in Fig. 4.12. Incident gamma-rays produce secondary electrons, and then these electrons cause the displacement damage on a semiconductor device as a result of the interaction with the host atoms [20]. Onoda et al. reported that the displacement damages by gamma-ray irradiation created the generation-recombination centers in the bandgap of 6H-SiC at the dose of 960 kGy (SiC) [21]. The sudden rise of I_D would be drain-to-substrate leakage current; it is induced by the displacement damages due to gamma-rays. The photon energy mass energy-absorption coefficients for Si, O, and Ba are almost equal in the energy range of ^{60}Co source [22]. Hence, the incorporated-Ba does not enhance the secondary electron due to gamma-ray. Figure 4.13 shows simulated energy band diagrams for the drain-substrate junction, with and without applying the threshold V_{DS}. The energy band diagrams were calculated by the abrupt depletion layer approximation and the full-depletion approximation. The depletion region becomes thin to 6 μm by applying the threshold V_{DS} of 9 V.

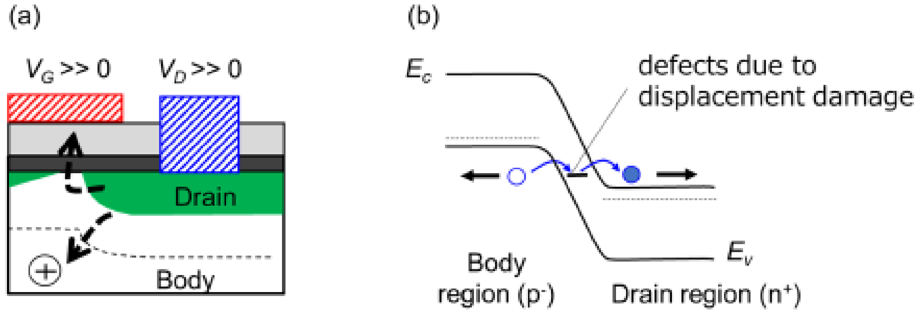


Fig. 4.12. (a) device cross-section near drain region and (b) energy band diagram for trap-assisted band-to-band tunneling via defects due to displacement damage.

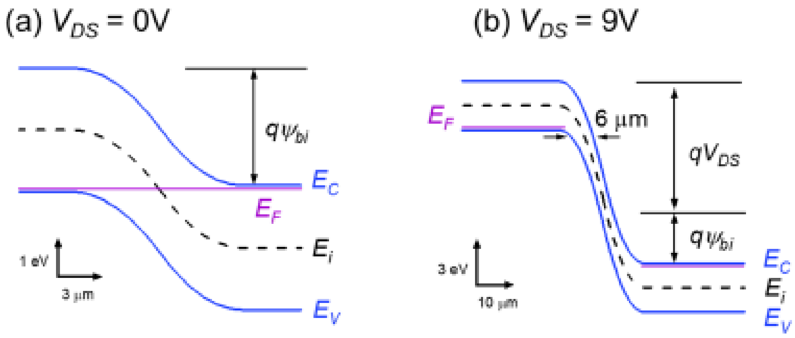


Fig. 4.13. Simulated energy band diagrams for (a) V_{DS} = 0V and (b) V_{DS} = 9 V. Ψ_{bi} is built-in potential. (N_A = 4.6×10^{17} cm^{-3}, N_D = 5.0×10^{17} cm^{-3}), n_i = 5.0×10^{-9} cm^{-3}, T = 300 K, the activation ratio of implanted impurity was set to 1%)

4.3.4 Impact of bidirectional sweep, light illumination, and high temperature on irradiated MOSFETs

In order to confirm the presence of the trap-assisted band-to-band via the defects in the drain-substrate junction, three experiments were performed. Figure 4.14 shows bidirectional I_D/I_{sub}–V_{DS} characteristics of the irradiated SiC MOSFET up to 850 kGy. An anti-clockwise hysteresis of I_D appeared in the voltage range of 4–10 V. For the forward sweep, the sudden increase of I_D emerged around V_{DS} = 8 V; simultaneously, hole current flowed into the SiC substrate. For the backward sweep, humps of I_D were un-obviously seen around V_{DS} = 8 V. Also, positive substrate current flowed around V_{DS} = 8 V. The positive I_{sub} suggests that the holes injected by the forward sweep come back to the drain region. The absolute maximum value of I_{sub} for the backward sweep was lower than that for the forward sweep. That is, the injected holes were incompletely removed. It is a reason that the anti-clockwise hysteresis appears.

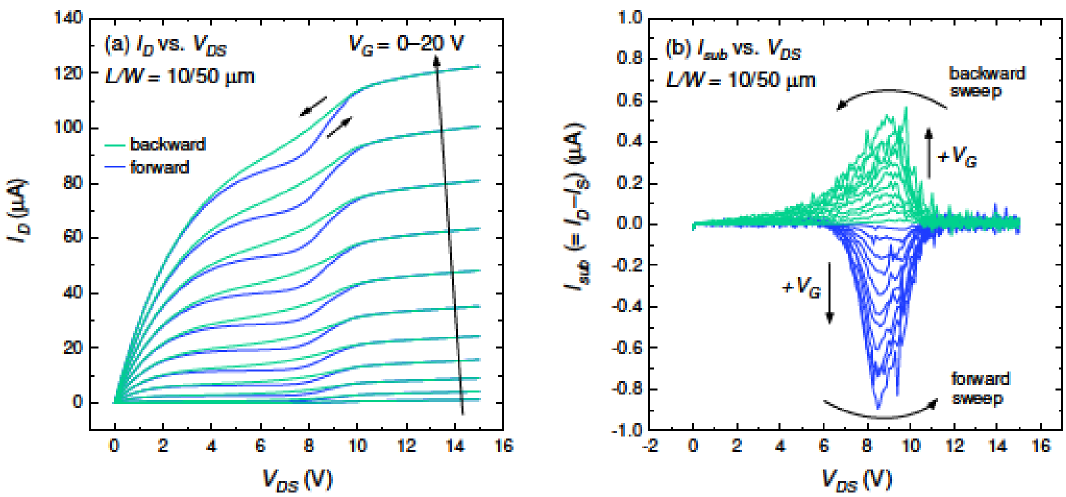


Fig. 4.14. Bidirectional (a) I_D and (b) I_{sub} versus V_{DS} characteristics of the SiC MOSFET after irradiation to 850 kGy. Channel length and width were 10 and 50 μm, respectively.

Figure 4.15(a), (b) shows bidirectional I_D–V_{DS} curves and I_D–V_G curves with and without light illumination of white light. A fluorescent lamp was used as the light source; the illuminance was set to 6 klux. The sudden increase of I_D on the saturation region arose around V_{DS} = 8 V in both conditions, and threshold V_{DS} was not changed by the light illumination. However, when I_D–V_{DS} characteristics were measured while the light illumination, the drain current was saturated around V_{DS} = 11 V. Figure 4.16 (a), (b) show substrate current characteristics with and without the light illumination. The absolute maximum value increased from 0.4 μA to 0.9 μA by the illumination. This result suggests that hole injection into the SiC substrate is enhanced by the light illumination. There is a possibility that the drain-substrate junction adsorbs the incident white light and more electron-hole pairs are generated.

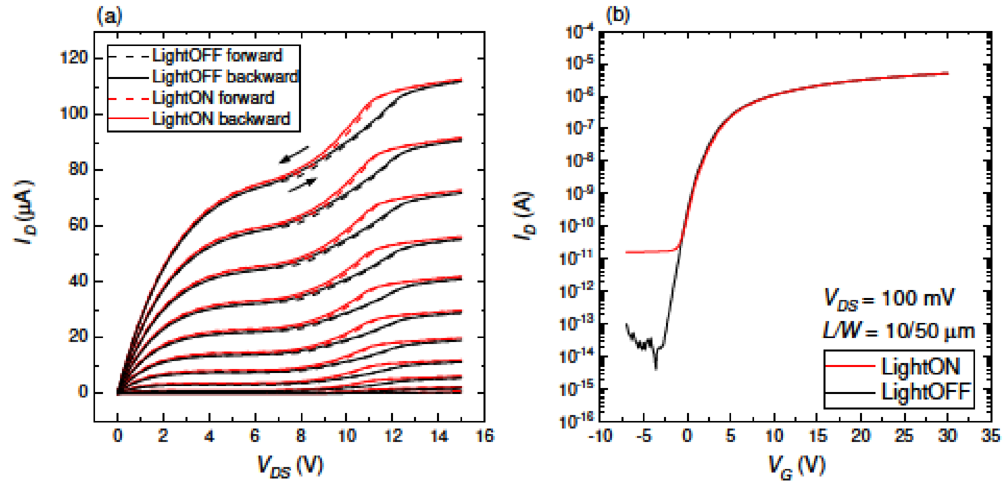


Fig. 4.15. (a) Bidirectional I_D–V_{DS} and (b) I_D–V_G characteristics of the gamma-ray irradiated SiC MOSFET, before and after light illumination. Channel length and width were 10 and 50 μm, respectively. In I_D–V_{DS}, V_G was swept from 0 V to 20 V.

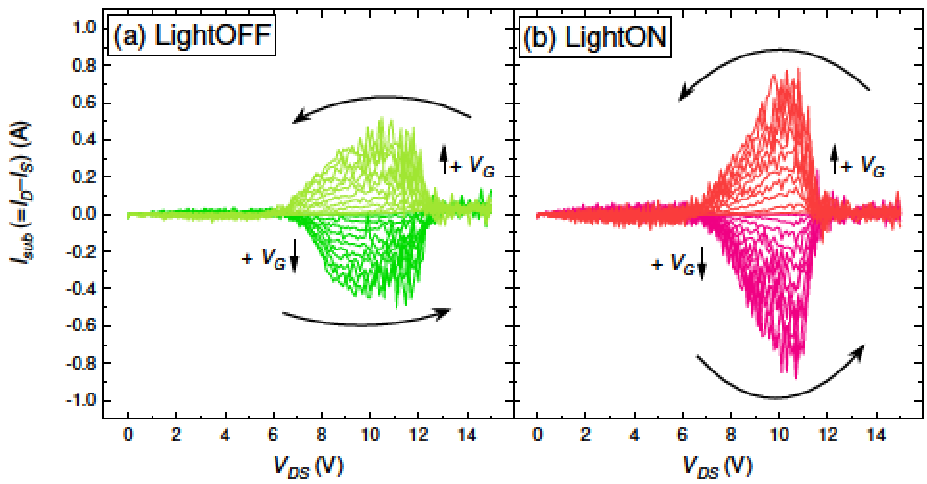


Fig. 4.16. I_{sub}–V_{DS} characteristics of (a) the non-illuminated SiC MOSFET and (b) the illuminated MOSFET. Channel length and width were 10 and 50 μm, respectively. V_G was swept from 0 V to 20 V.

Figure 4.17(a), (b) show I_D/I_{sub}–V_{DS} characteristics in a temperature range of 21–200°C. The applied gate voltage was fixed at 20 V. At 21°C, the drain current was saturated around 11 V. As increasing temperature, the saturation voltage increased from 11 V to 13 V, a hump of drain current became unclearly. The absolute value of the hole current decreased from 0.3 μA to 0.05 μA. Figure 4.17 (c), (d) show the second derivative of I_D and I_{sub}. Threshed V_{DS} increased from 8V to 10 V with increasing temperature. The negative peak voltage in $\partial^2 I_{sub}/\partial V_G^2$ plot also increased from 6 V to 8 V. The peak voltage of $\partial^2 I_{sub}/\partial V_G^2$ was below the threshold V_{DS} with regardless of temperature.

The built-in potential (ψ_{bi}) at drain-substrate junction decreases from 3.1 V to 2.8 V with increasing temperature. Assuming a step junction, the electric field at the pn junction is given by [23]

$$E_{pn} = \sqrt{\frac{2qN_A N_D(V_{DS} + \psi_{bi})}{\varepsilon_{SiC}(N_A + N_D)}}. \quad (4.10)$$

I postulated that N_A, N_D, and ε_{SiC} are constant values in the temperature range of 21–200°C. When a V_{DS} is applied, the electric field decreases owing to the increase in temperature. Thus, the increase in temperature is considered to reduce the negative I_{sub}. However, the difference in the threshold V_{DS} was much higher than the difference in ψ_{bi}. Therefore, other factors should be introduced to explain sufficiently the temperature dependencies of I_D/I_{sub}–V_{DS} characteristics. In general, as direct tunneling is independent of temperature [16], the variation in the threshold V_{DS} supports the trap-assisted band-to-band tunneling via the radiation-induced defects, as shown in Fig. 4. 12(b).

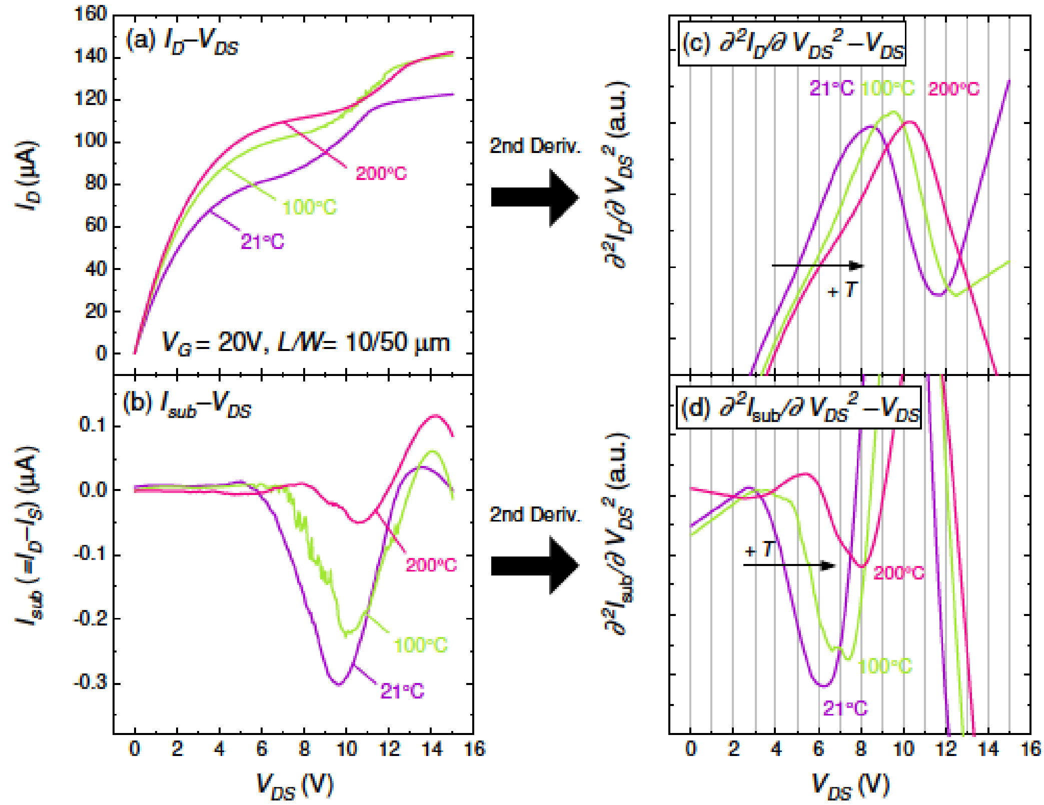


Fig. 4.17. Temperature dependencies of (a) I_D and (b) I_{sub} versus V_{DS} characteristics for the irradiated MOSFET. Gate voltage was 20 V. (c) $\partial^2 I_D/\partial V_G^2$ and (c) $\partial^2 I_{sub}/\partial V_G^2$ plots.

4.4 Conclusions

In this chapter, radiation responses of the Ba-incorporated MOSFET are shown.

The TID effect on the MOSFETs by I_D–V_G characteristics was evaluated. ΔN_{it} and ΔN_{ox} for the Ba-incorporated SiO_2 were higher than that for the Dry SiO_2. This result clearly indicates that the Ba-incorporated SiO_2, which consists of the thick layered gate dielectric, has less radiation hardness than the thin Dry SiO_2. However, this trend is affected by oxide thickness. After correcting the contribution of oxide thickness, for the Ba-incorporated SiO_2, the interface trap generation efficiency (f_{it}) and the oxide charge trapping efficiency (f_{ox}) were slightly smaller than that of the Dry SiO_2, indicating that the interfacial Ba-silicate layer is less prone to damage. That is, the interfacial Ba-silicate is essentially rugged than the Dry SiO_2.

The output characteristics of the irradiated SiC MOSFET are also discussed. The irradiated MOSFET exhibited the drain characteristics with a typical linear region and the sudden rise of I_D on the saturation region. The sudden rise of I_D was accompanied by hole injections into the gate-oxide and the substrate. It is concluded that the sudden rise of I_D results from the electron-hole pairs by electron tunneling via defects at the drain-substrate junction. The defect states are expected to be induced by the displacement damage due to gamma-ray irradiation, and the drain-substrate leakage current is independent of the introduction of the interfacial Ba-silicate layer. The sudden increase of I_D was affected by the accumulation of the holes, the light illumination, and the measurement temperature. These results support the idea of trap-assisted band-band tunneling via defects generated by gamma-ray irradiation. Since the increase in I_D depends on the injected hole into the SiC body region, the sudden rise of I_D is expected to originate from the kink effect.

In conclusion, the layered SiO_2/Ba-silicate dielectric can enhance TID tolerance. However, thinning the dielectric is required. I attempted to reduce the thickness by reducing the oxygen concentration during oxidation, based on the idea written in Chapter 2. 12 nm of Ba-incorporated SiO_2 was realized; this gate-dielectric resulted in 13 $cm^2V^{-1}s^{-1}$. These results are summarized in Ref. 24.

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Chapter 5

Radiation-induced mobility enhancement effect

5.1 Introduction

In the previous chapter, radiation effects on the SiC MOSFETs were discussed. Gamma-ray irradiation above 600 kGy (SiO_2) induced an anomalous mobility enhancement effect, which was accompanied by an increase in interface trap density. In this dissertation, this phenomenon is called radiation-induced mobility enhancement. The mechanism and the origin of this effect are discussed in this chapter.

There are some reports on mobility enhancement of SiC MOSFETs by gamma-ray irradiation. Lee et al. reported that the hole mobility in 6H-SiC p-channel MOSFET was improved by the reduction of scattering and capture of holes with built-up positive trapped charges [1]. Further, Hishiki et al. reported that the channel mobility in 6H-SiC NMOSFET increased by reduction of the interface trap density above 1 MGy [2]. However, these mobility enhancement mechanisms are inadequate to explain the radiation-induced mobility enhancement effect. The reasons are that reduction of interface traps is not observed in the irradiated Ba-introduced MOSFET; moreover, its carrier type is n-type. Thus, there is unreasonable that built-up positive trapped charges reduce scattering and capture of electrons.

There are some reports of the mobility enhancement accompanied by an increase in interface traps. A relationship between field-effect-mobility of irradiated MOSFETs and its total dose is summarized in Fig. 5.1 [3–8]. It includes data of 6H-SiC MOSFETs. In fact, the radiation-induced mobility enhancement effect accompanies by an increase in interface traps has been observed on the sample which has either nitrogen or barium at the MOS interface. There is a possibility that the incorporation of other elements (e.g. B or P) into MOS interface also leads to the anomalous mobility enhancement. Therefore, the mechanism must be elucidated. If this phenomenon is understood and it thereby becomes controllable, the radiation-induced mobility enhancement effect may be an advantage against the high-temperature oxidation method and so on [9].

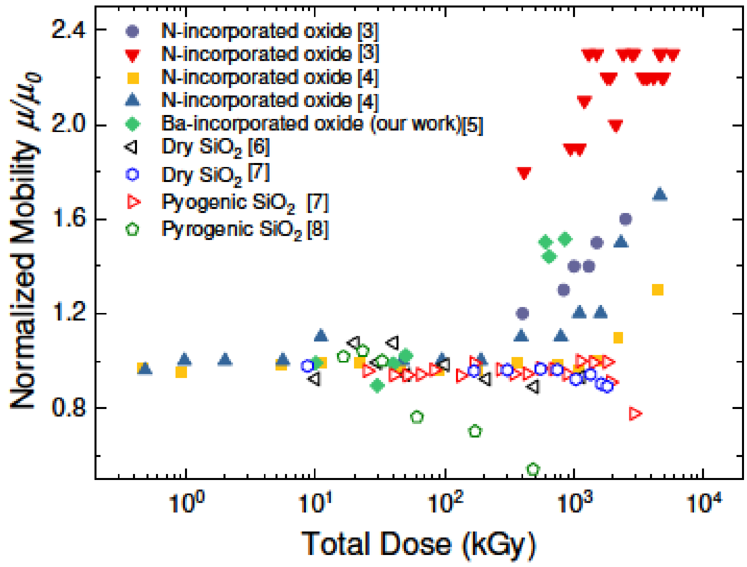

Fig. 5.1. Total dose dependence of field effect mobilities for 4H-SiC and 6H-SiC MOSFETs.

5.2 Results and discussion

In this section, it is shown that various electrical characteristics of the irradiated SiC MOSFETs. In the previous chapter, since describing the fabrication process of measured SiC MOSFETs, the process is not described in this chapter.

5.2.1 Bias-temperature stress test

Above 600 kGy, the μ_{FE}–V_G curves showed a sharp peak around V_G = 6 V, as shown in 4.6(a), Chapter 4. This sharp peak and the negative threshold voltage shift resemble the curve of the MOSFET whose oxide is contaminated with sodium ions [10]. Tuttle et al. reported that after applying a positive bias-temperature stress (BTS) test of +15 V at 175°C, the Na-contaminated MOSFET showed an extremely high mobility of 211 $cm^2 V^{-1}s^{-1}$ with a sharp peak structure and a negative threshold voltage shift. They concluded the high mobility is strongly correlated with the presence of Na ions at the SiO_2/SiC interface. Therefore, I considered that the irradiated MOSFET also included Ba-ions at the gate-oxide/SiC interface as well as the Na-contaminated MOSFET. To evaluate this hypothesis, positive and negative BTS tests were performed to the irradiated MOSFET up to 850 kGy as per the following procedure, shown in Fig. 5.2.

The applied oxide electric field was +1 MV/cm or −1 MV/cm. Firstly, the irradiated MOSFET was heated to 200°C, and then the electric field of +1 MV/cm was applied for the sample to drift the Ba-ions toward the gate-dielectric/SiC interface direction. The MOSFET was then cooled to room temperature under the electric field. Finally, the I_D–V_G curve was measured at room temperature. After the positive BTS test, the procedure was repeated with the same MOSFET with a reverse bias of −1 MV/cm.

Figure 5.3(a), (c) show V_{th} and μ_{FE} variations in a cumulative stress time by applying the positive electric field. After applying the positive BTS, the NMOSFET showed a positive threshold voltage shift of 3.5 V due to electron injection from the SiC surface [11]. The stressed mobility fluctuated around 15 cm^2 V^{-1}s^{-1}, and the mobility enhancement effect, like the Na-contaminated MOSFET, was not observed. Subsequently, the same NMOSFET was applied with the negative electric field, as shown in Fig. 5.3(b), (d). The threshold voltage decreased to 3 V as the cumulative stress time increased; the threshold voltage was close to the initial threshold voltage of 2.6 V before the positive BTS. Thus, this voltage shift is mainly caused by removal of the injected electron. Note that the threshold voltage was incompletely recovered. The residual threshold voltage shift of 0.4 V would be due to hole injection.

Unlike Na-contaminated MOSFETs, the irradiated MOSFET exhibited no mobile ion drift under the BTS tests. That is, the irradiated MOSFET did not contain a number of Ba-ions sufficient to detect ion-drift. It is concluded that the mechanism of radiation-induced mobility enhancement is different from the mobility enhancement mechanism of the Na-contaminated MOSFET.

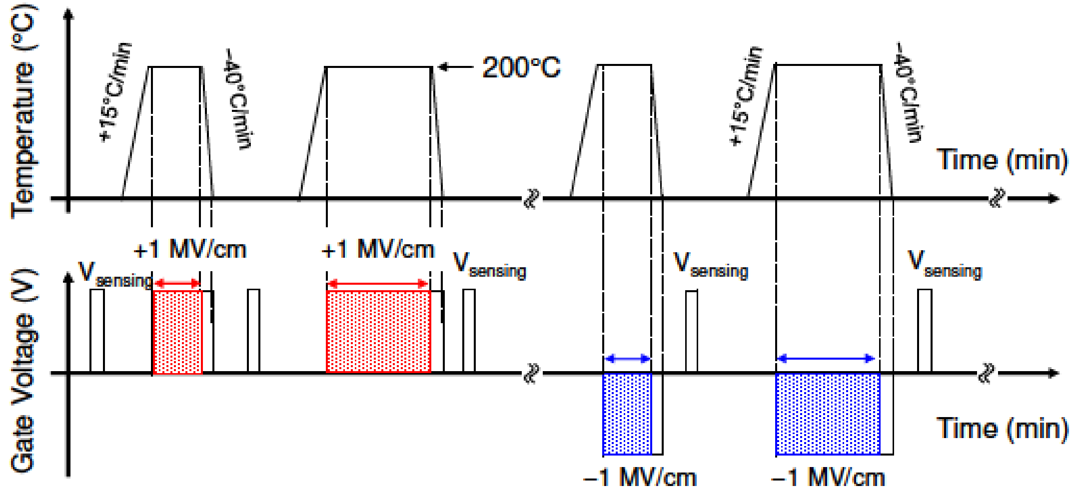

Fig. 5.2. Schematic of positive and negative bias-temperature stress (BTS) tests.

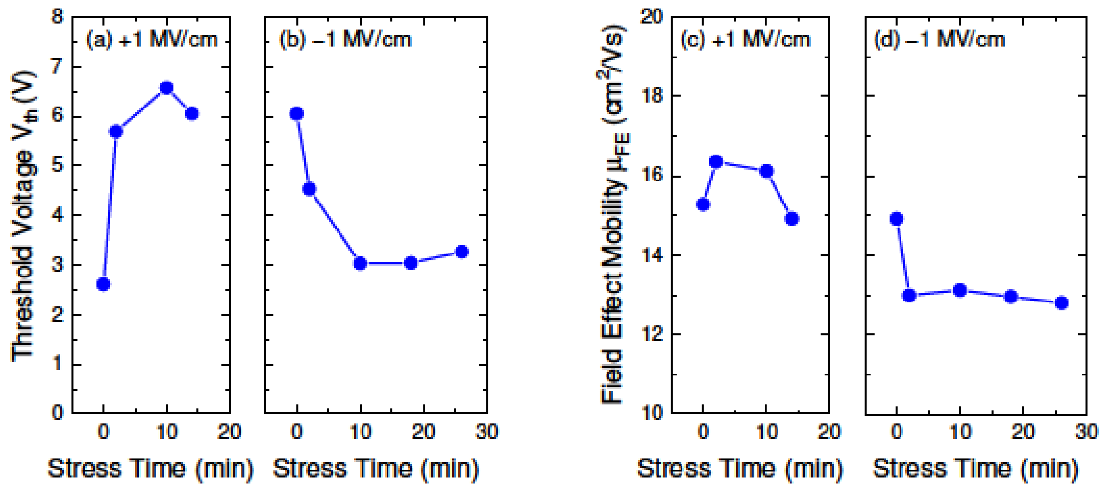

Fig. 5.3. Bias-temperature stress tests with bipolarity biases on the irradiated-NMOSFET: V_{th} variation of (a) + 1MV/cm, (b) −1 MV/cm, and μ_{FE} variation of (a) + 1MV/cm, (b) −1 MV/cm. The channel length and width were 10 μm and 10 μm, respectively.

5.2.2 Temperature dependence of mobility

After gamma-ray irradiation, the temperature dependence of μ_{FE} is also changed. Figure 5.4 shows the temperature dependencies for non-irradiated and irradiated MOSFET. The radiation dose was 850 kGy. A non-irradiated MOSFET with L/W = 5/50 µm showed channel mobility was proportional to $T^{0.4}$. On the other hand, the irradiated MOSFET of L/W = 10/10 µm showed a different dependence. The mobility increased from 17 cm^2 V^{-1}s^{-1} to 19 cm^{2}V^{-1}s^{-1} in the range of 300–350 K, and the mobility decreased in proportion to $T^{-0.6}$ above 350 K.

Note that radiation responses are affected by post-radiation-annealing [12, 13]. The holes trapped in the SiO_2 of a MOS device are not truly permanently trapped. A fraction of trapped hole is compensated by electron tunneling and thermal annealing over time from milliseconds to years. Thus, there is a possibility that by the measurement at high temperatures, the radiation effects are partially recovered.

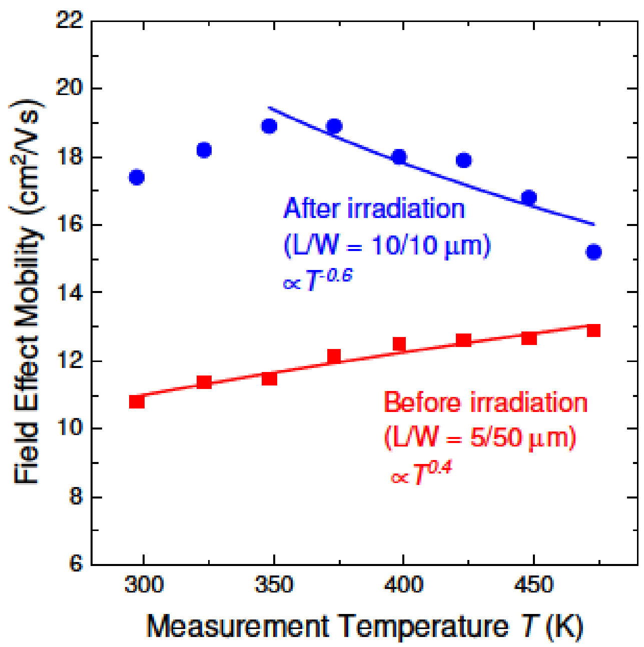

Fig. 5.4. Temperature dependencies of channel mobility of non-irradiated MOSFET at L/W = 5/50 µm, and irradiated MOSFET at L/W = 10/10 µm.

5.2.3 Estimation of effective mobility

Effective mobility (μ_{eff}) is evaluated in this subsection. Evaluation of effective mobility requires a mobile charge density (Q_n), which is generally determined by the split C–V method [14]. However, this procedure can not apply to the irradiated SiC MOSFETs. The reason is that gamma-ray damages gate-oxide and MOS interface due to the TID effect, thereby causing a much frequency dispersion on C–V curve. If Q_n of the irradiated sample is measured by the split C–V method, it includes the contribution of interface traps, leading to overestimate Q_n. In this work, μ_{eff} and Q_n are approximated by

$$\mu_{eff} = \frac{g_d L}{W Q_n}, (5.1)$$

$$Q_n = C_{ox}(V_G - V_{th}), (5.2)$$

where g_d is the drain conductance [14]. Figure 5.5 shows the effective mobility before and after irradiation. Irradiated MOSFETs exhibited higher mobility than that of the non-irradiated MOSFETs.

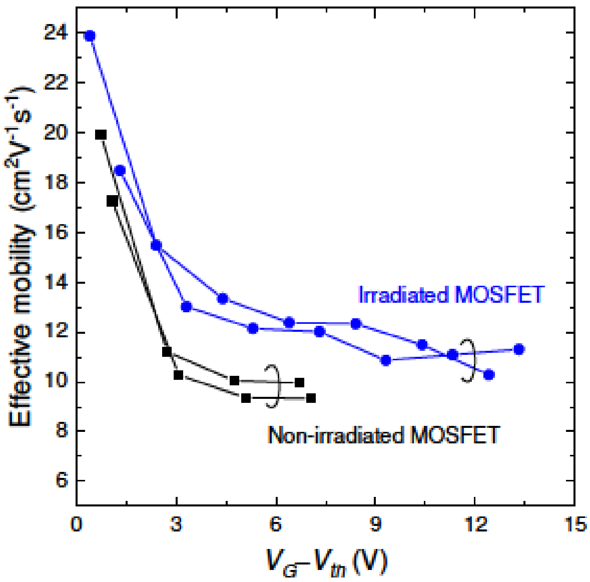

Fig. 5.5. Effective mobilities of the non-irradiated and irradiated SiC MOSFETs. (D = 850 kGy (SiO_2), L/W = 10/10 μm)

5.2.4 Radiation-induced narrow channel effect (RINCE)

Figure 5.6 shows the μ_{FE}–V_G curves for a narrow channel width (10 µm) and a wide channel width (50 µm) in the MOSFET before and after irradiation. The radiation dose was 850 kGy. For the narrow channel, the mobility was enhanced from 12 $cm^2 V^{-1}s^{-1}$ to 17 $cm^2 V^{-1}s^{-1}$, and the μ_{FE}–V_G curve had a sharp peak around $V_G = 6$ V. On the other hand, for the wide channel, the mobility was slightly degraded. Moreover, no sharp peak was observed.

The channel width dependencies of V_{th}, μ_{FE}, and I_G are summarized in Fig. 5.7 before and after irradiation to 850 kGy. Before irradiation, V_{th} and μ_{FE} increased with the narrowing channel width. These trends are caused by a high series resistance such as a drift resistance and an ohmic contact resistance [14, 15]. For example, at $W = 50$ µm, the MOSFET's series resistance accounted for 26% of its total resistance. As a result, a high voltage dropped across the series resistance, and V_{th} and μ_{FE} were modified with a difference of effective V_{DS}. After irradiation, the threshold voltage shifted to the negative direction due to radiation-induced oxide-trapped charges. The channel width dependence of V_{th} shift is typically called radiation-induced narrower channel effect (RINCE) in Si-MOS devices. The threshold voltage shift, as defined as $|V_{th,\,post} - V_{th,\,pre}|$, increased with the narrowing channel width, where 'post' and 'pre' denote after and before irradiation. The effective positive-charge density (ΔN_{eff}) is given by

$$\Delta N_{eff} = \frac{C_{ox}}{q}\left|V_{th,post} - V_{th,pre}\right|. \quad (5.3)$$

The narrowing channel enhanced ΔN_{eff}, which increased from 1.1×10^{12} cm^{-2} to 1.6×10^{12} cm^{-2}. Note that ΔN_{eff} is expressed by $\Delta N_{eff} = \Delta N_{it} + \Delta N_{ox}$, and then the increase of ΔN_{eff} indicates channel narrowing enhances the relative oxide-trapped charge density against the interface trap density.

Similarly, the narrower channel tends to increase μ_{FE} after irradiation. Although the narrow channel MOSFET of $W = 10$ µm showed a wide variation of μ_{FE}, it resulted in the highest mobility of 18 $cm^2V^{-1}s^{-1}$. At only $W = 50$ µm, the μ_{FE} was below that of the non-irradiated sample. These results indicate that the narrower channel enhances radiation responses such as the threshold voltage shift and the increasing mobility.

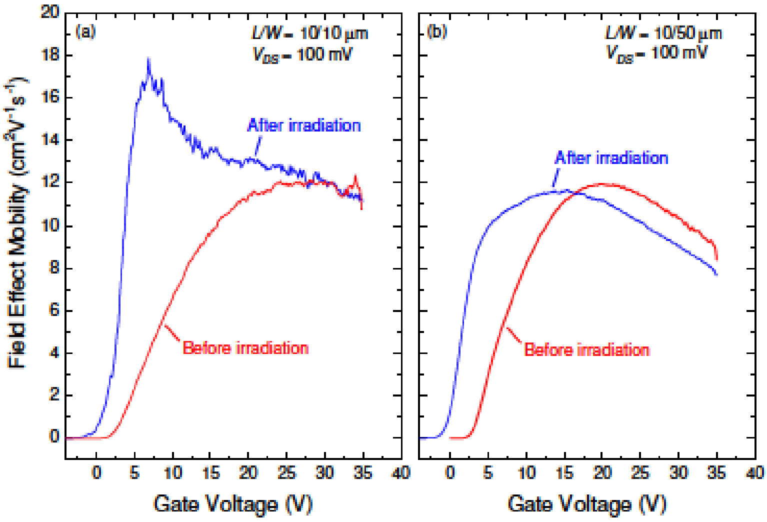

Fig. 5.6. Field effect mobility of NMOSFETs with (a) W = 10 µm and (b) W = 50 µm before and after irradiation. Both channel lengths were 10 µm.

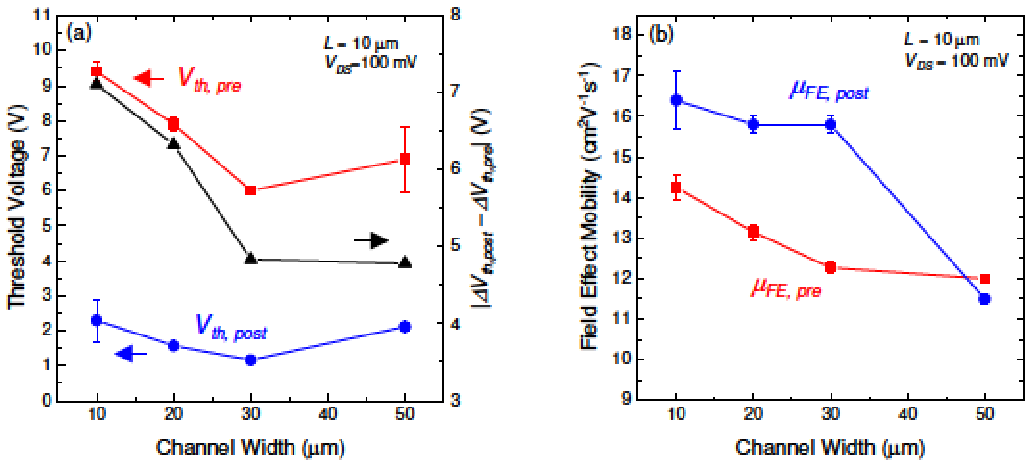

Fig. 5.7. (a) Threshold voltage shift, (b) field effect mobility at V_{th} on the MOSFETs as a function of the channel width.

5.2.5 Analysis using gate-to-channel conductance (G_{GC})

5.2.5.1 Relationship between channel width and G_{GC}

In order to clarify the origin of RINCE, a gate-to-channel conductance, G_{GC}, was measured. G_{GC}–V_G characteristic of a MOSFET was measured using an Agilent 4284A LCR meter and an Agilent 4294A impedance analyzer. Figure 5.8(a) shows the circuit for the G_{GC} measurement [14, 16]. The small-signal AC amplitude was set to 100 mV. The high terminal was connected to the gate electrode; S/D regions were connected to the low terminal, and SiC substrate was grounded. Figure 5.8(b) shows a cross-sectional schematic of the MOSFET during the G_{gc} measurement.

Here, V_{inv} is defined as the gate voltage corresponding to a SiC surface potential of $2\psi_B$ [17]. It is important to note that the SiC surface potential, corresponding to V_{th} determined by the linear extrapolation, is generally greater than the $2\psi_B$ value [14,17]. V_{inv} is determined by the following procedure [17, 18]. Firstly, the ideal subthreshold current was obtained at the surface potential of $2\psi_B$, where ψ_B is the Fermi potential with respect to midgap. The ideal subthreshold current is expressed with the formula [19]:

$$I_D = \mu \frac{W}{L} \sqrt{\frac{q\epsilon_{SiC} N_A}{2\psi_B}} \left(\frac{n_i}{N_A}\right)^2 \left(\frac{kT}{T}\right)^2 \exp\left(\frac{q\psi_B}{kT}\right) \left(1 - \exp\left(-\frac{qV_{DS}}{kT}\right)\right), \quad (5.4)$$

where k, T, q, n_i are the Boltzmann constant, the absolute temperature, the elementary charge, and the intrinsic carrier density. And ε_{SiC} denotes the dielectric constant of SiC. The field-effect mobility was used as channel mobility. Finally, V_{inv} is defined as the V_G corresponding to the calculated inversion current on measured I_D–V_G characteristic.

Figure 5.9 shows I_D/G_{GC} versus V_G characteristics of the irradiated MOSFETs with W = 10 µm and W = 50 µm. The measurement frequency was 100 kHz. The V_{inv} for W = 10 µm was −1.7 V. And this narrower channel transistor exhibited a single G_{GC} peak at V_G = −5.1 V. The gate voltage at the peak is lower than the V_{inv}. Whereas, the wider channel transistor of W = 50 µm showed markedly different G_{GC} characteristic. The V_{inv} of W = 50 µm was 5.5 V. The wider channel exhibited three G_{GC} peaks. Each peak located at −0.96 V, 3.4 V, and 6.6 V, labeled as $D_{it,1}$, $D_{it,2}$, and $D_{it,3}$. Interestingly, the gate voltage corresponding $D_{it,3}$ was larger than the V_{inv}. It indicates that the wider channel has interface traps at the energy level near the conduction band bottom (E_c). The traps at the energy level near E_c is called as the shallow traps. After forming the inversion layer on channel region, induced electrons communicate with the shallow traps. It is considered that the mobility degradation in the wider channel transistor results from the shallow traps.

Interface trap density was estimated by the single-frequency approximation technique proposed by Hill et al. [20]. The method requires G_{GC}–V_G curve at a high-frequency. The value of D_{it} is expressed by the following equation:

$$D_{it} = \frac{2\left(\frac{G_{m,max}}{\omega}\right)}{qS}\left(\left(\frac{G_{m,max}}{\omega C_{ox}}\right)^2 + \left(1 - \frac{C_{mc}}{C_{ox}}\right)^2\right)^{-1}, (5.5)$$

where $G_{m,max}$ is the maximum conductance and C_{mc} is its corresponding capacitance. S and ω are the device area and the signal frequency in rad/sec, respectively. C_{ox} is gate oxide capacitance. The D_{it} estimation was performed at 100 kHz. The surface potential was estimated with ideal subthreshold current as with the V_{inv} determination procedure. Estimated D_{it} values of the irradiated MOSFETs are shown in Table 5.1. The shallow trap density for W = 50 μm was 1×10^{12} $\mathrm{cm^{-2}eV^{-1}}$.

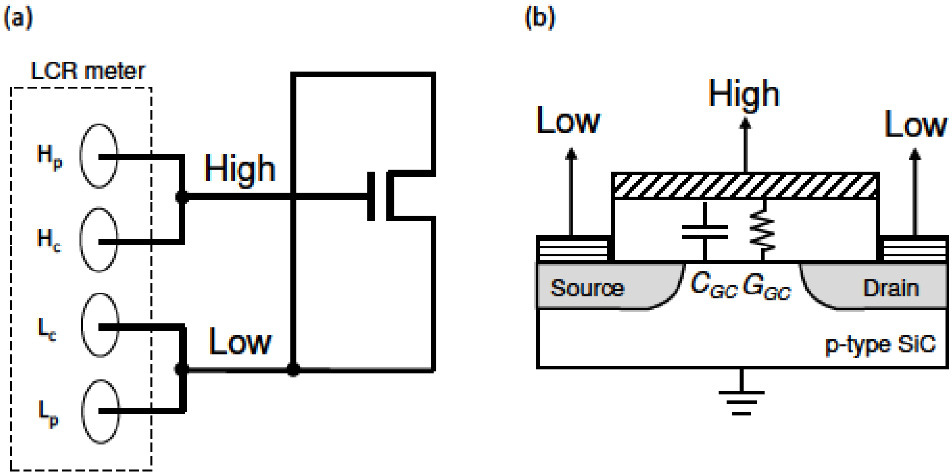

Fig. 5.8. Schematic for G_{GC} measurement: (a) circuit and (b) cross-section. C_{GC} denotes gate-to-channel capacitance.

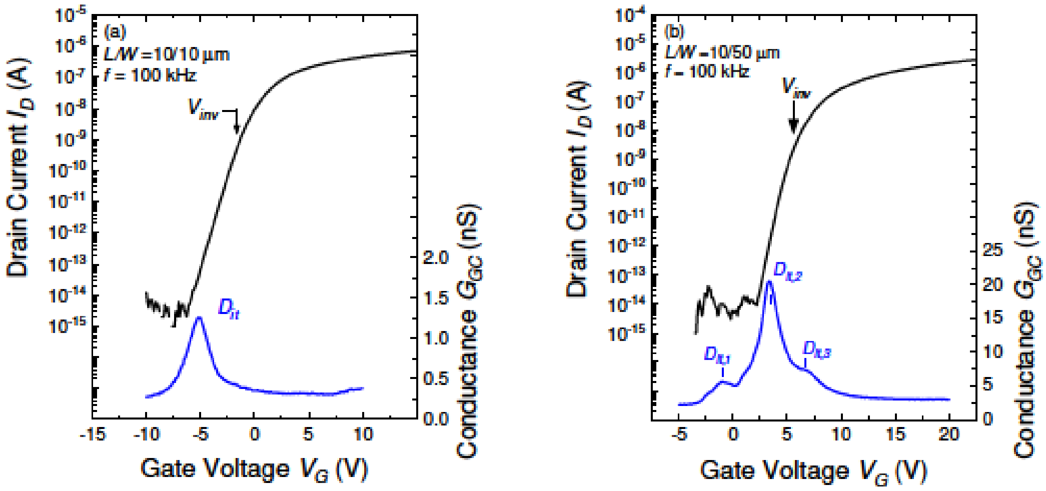

Fig. 5.9. I_D/G_{GC}–V_G characteristics of the irradiated MOSFETs with different channel width:(a) $W = 10$ μm and (b) $W = 50$ μm. Channel length was 10 μm. V_{inv} is the gate voltage corresponding to a SiC surface potential of $2\psi_B$.

Table 5.1. Estimated interface trap density of the irradiated MOSFETs with different channel width.

Channel width W **(μm)**	**Interface trap density** D_{it} **(cm^{-2}eV^{-1})**	**Energy level** E-E_c **(eV)**
10	8×10^{11}	0.35
	1×10^{10}	0.71
50	3×10^{11}	0.30
	1×10^{12}	—

5.2.5.2 Influence of partial recovery on G_{GC}

As mentioned in subsection 5.2.2, radiation effects in gate-dielectric are not permanent. The irradiated MOSFET with W = 10 μm was recovered by electron injection at a temperature of 200°C for 40 min. The electron injection performed by applying an oxide electric field of + 1 MV/cm.

Figure 5.10 shows field-effect mobility after the recovery process. After the recovery process, the mobility decreased to 16 cm^{-2}V^{-1}s^{-1}, which was still higher than the initial mobility before irradiation. G_{GC}/I_D–V_G characteristic of the recovered MOSFET is shown in Fig. 5.11. This figure includes the drain characteristics before and after irradiation. V_{inv} increased from 0.4 V to 7.6 V by electron injection. This voltage shift suggests the neutralization of oxide-trapped positive charge. The initial V_{inv} before irradiation was 2.5 V. V_{inv} of the recovered MOSFET was larger than the initial value, still remaining radiation-induced interface traps. Electron injection at 200°C is insufficient to cure interfacial defects; recovering is incomplete.

For G_{GC} curve received the recovery process, there are two G_{GC} peaks at gate voltages of −0.5 V and 6.4 V. Each peak is labeled as $D_{it,1}$ and $D_{it,2}$. Interestingly, the $D_{it,1}$ appeared on out of the subthreshold region of measured I_D–V_G curve.

At first, $D_{it,1}$ is predicted to result from the traps at gate-dielectric/SiC interface on the overlap regions. Chen et al. reported that radiation-induced interface traps were nonuniformly distributed spatially; the trap densities on S/D regions were different from that of channel region [21]. It is speculated that there are two spatially separated interface-traps, which are located on the channel region and overlap region; each interface states are filled by a different gate voltage. In order to reveal the presence of interface traps on overlap regions, the gate-to-drain conductance (G_{GD}) was measured. However, there was no peak on the obtained G_{GD}–V_G characteristic. Therefore, it is concluded that the $D_{it,1}$ corresponds to interface traps at gate-dielectric/SiC interface on the channel region, not overlap region.

Interface trap density was estimated using Eq. (5.5), shown in Table 5.2. The recovered MOS interface had two kinds of interface states at the different energy levels in the bandgap. $D_{it,1}$ and $D_{it,2}$ correspond to interface traps of 3×10^{11} cm^{-2}eV^{-1} and 2×10^{12} cm^{-2}eV^{-1}, respectively. Moreover, $D_{it,2}$ was located at the energy level of E–E_c = 0.18 eV. This shallow state near E_c did not appear on the G_{GC}–V_G characteristic before the recovery process, shown in Fig. 5.9(a). It is concluded that the recovery process induces high shallow-trap density.

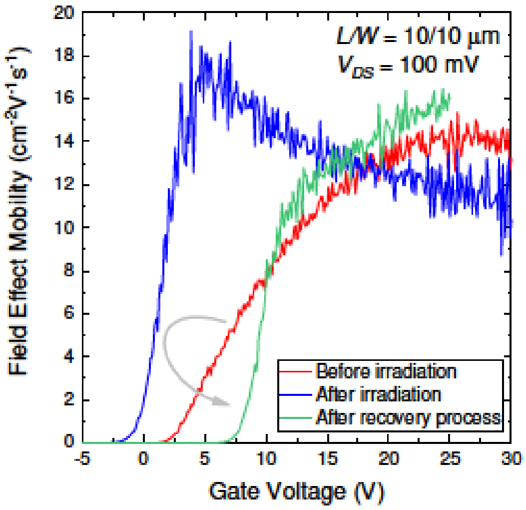

Fig. 5.10. Variation of field effect mobility by gamma-ray irradiation and the recovery process.

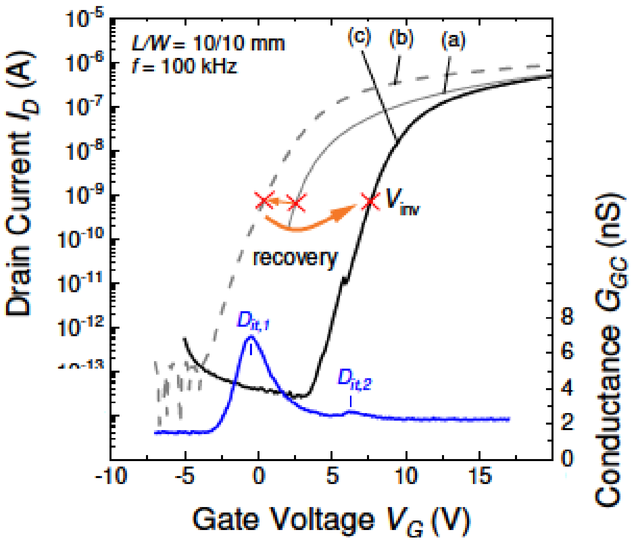

Fig. 5.11. G_{GC}–V_G characteristic of the partially recovered MOSFET. And I_D–V_G characteristics (a) before irradiation, (b) after irradiation, and (c) after recovering.

Table 5.2. Estimated interface trap density of the recovered MOSFET.

Interface trap	Interface trap density D_{it} (cm^{-2}eV^{-1})	Energy level E-E_c (eV)
Deep trap	3×10^{11}	0.54
Shallow trap	2×10^{12}	0.18

5.2.6 Proposal for the mechanism of Radiation-induced mobility enhancement effect

Applying the recovery process reduced channel mobility and induced the shallow traps. Shallow trap state is expected to have large capture cross-section, and then its state highly influences on channel mobility [14]. Thus, the mobility reduction is due to shallow traps. Not only after recovering, but also the wide channel MOSFET of $W = 50$ µm had the shallow traps. This wide channel MOSFET did not exhibit radiation-induced mobility effect. It is speculated that the shallow trap cancels out the radiation-induced mobility enhancement effect in the wide channel MOSFET.

Shallow traps near E_c play a key role in occurrence of the radiation-induced mobility enhancement effect. Shallow traps were observed in samples with less oxide-trapped charge density. The wide channel MOSFET of $W = 50$ µm had less ΔN_{eff}, and the recovery process reduced oxide-trapped positive charges. It is expected that the relationship between shallow traps and oxide-trapped charges. In other words, oxide-trapped charges relate to the occurrence of the radiation-induced mobility enhancement effect. Reduction of oxide-trapped charge by the recovery process (electron injection at a high-temperature) is a reasonable result. Here, the channel dependence of oxide-trapped charge density is discussed below.

The channel width dependence of V_{th} shift, shown in Fig. 5.7(a), is typically called radiation-induced narrower channel effect (RINCE) in Si-MOS devices. The cause of RINCE has been explained by mainly two models; one is that a source—channel potential barrier drops by build-up of positive charges on shallow trench isolation (STI) around the transistor [22]. In this study, the fabricated MOSFET has no isolation layer like STI, moreover, the simple change of the potential barrier insufficiently explains the mobility enhancement effect. Another model is that mechanical stress in MOSFETs enhances the amount of radiation-induced positive charge [23]. It is well known that electrode-induced mechanical stress modifies radiation response [24, 25]. A gate electrode introduces mechanical stress into a gate oxide, and this strength depends on the metal's thickness and the electrode-width [26]. In other words, a thick and/or narrow gate electrode introduces more mechanical stress on the gate oxide. For example, in Si-MOSFETs, the shorter channel induced more oxide-trapped charges [27, 28]. As shown in Fig. 5.7(a), the narrower channel in the SiC MOSFETs also implies the presence of more oxide-trapped charges. Moreover, the channel width was controlled by Al gate-metal width. Therefore, the mechanical stress is predicted to induce both

RINCE and the radiation-induced mobility enhancement effect.

The mechanical stress dependence of radiation sensitivity is explained by the bond strain gradient (BSG) model [29]. Based on the BSG model, holes created by radiation break strained Si-O-Si bonds leading to the formation of oxygen vacancy (E′-center) [30]. These oxygen vacancies act as the oxide-trapped positive charges [31]. Also, there is a strain gradient of the bond in SiO_2/Si interface, and the magnitude of the gradient modifies propagation of E′-center into the interface. And hence, the electrode-induced mechanical stress or an extra stress is able to control radiation response such as the number of the oxygen vacancies. For example, the MOS capacitors with fluorinated gate-oxide were more resistant to X-ray irradiation, and the gate-size dependence was suppressed [32]. Electrode-induced mechanical stress is greater near the edge of the electrode and falls off hyperbolically away from the edge [25]. And thus, when the gate electrode is narrowed, not only more stress strength, the relative stress-distribution also increases. Therefore, the decrease in the channel-width would enhance the formation of oxygen vacancies and cause RINCE in the Ba-incorporated MOSFET. This schematic diagram is shown in Fig. 5.11(a).

The mobility enhancement effect may be attributed to the oxygen vacancies enhanced by the electrode-induced mechanical stress. Radiation or hole injection creates oxygen vacancies in gate-oxide, leading to transformation of the interfacial structure [30-37]. In Chapter 2, it is shown that the interfacial Ba-silicate structure changes electrical characteristics for the Ba-incorporated MOS device. Propagated holes break the interfacial Ba-silicate structure, and this modification of the interfacial structure may cause the mobility enhancement effect. Figure 5.11(b) shows the equivalent circuit of irradiated NMOSFET, includes three transistors (Central and Edge devices) in parallel. When the edge devices become dominant with the stress and radiation, the obvious enhancement is observed on the electrical characteristics. Dycus et al. reported that the Ba-incorporation reduced the interfacial mechanical stress, and then this strain reduction at the SiO_2/SiC interface improved the field effect mobility on 4H-SiC MOSFET [38]. Based on their proposed idea, the strained Ba-silicate layer is transformed into a more relaxed structure by gamma-ray irradiation. As a result, the mobility is more improved.

After irradiation, the mobility at W = 50 μm decreased, and its ΔN_{eff} became the lower value. Based on the postulation mentioned above, the reason can be explained as below: the wider channel weakens the stress strength. Moreover, the strained layer is localized around the gate-metal's edge. As a result, the created oxygen vacancy and the modified layer are also localized; the degradation of the mobility becomes dominant rather than the mobility enhancement effect.

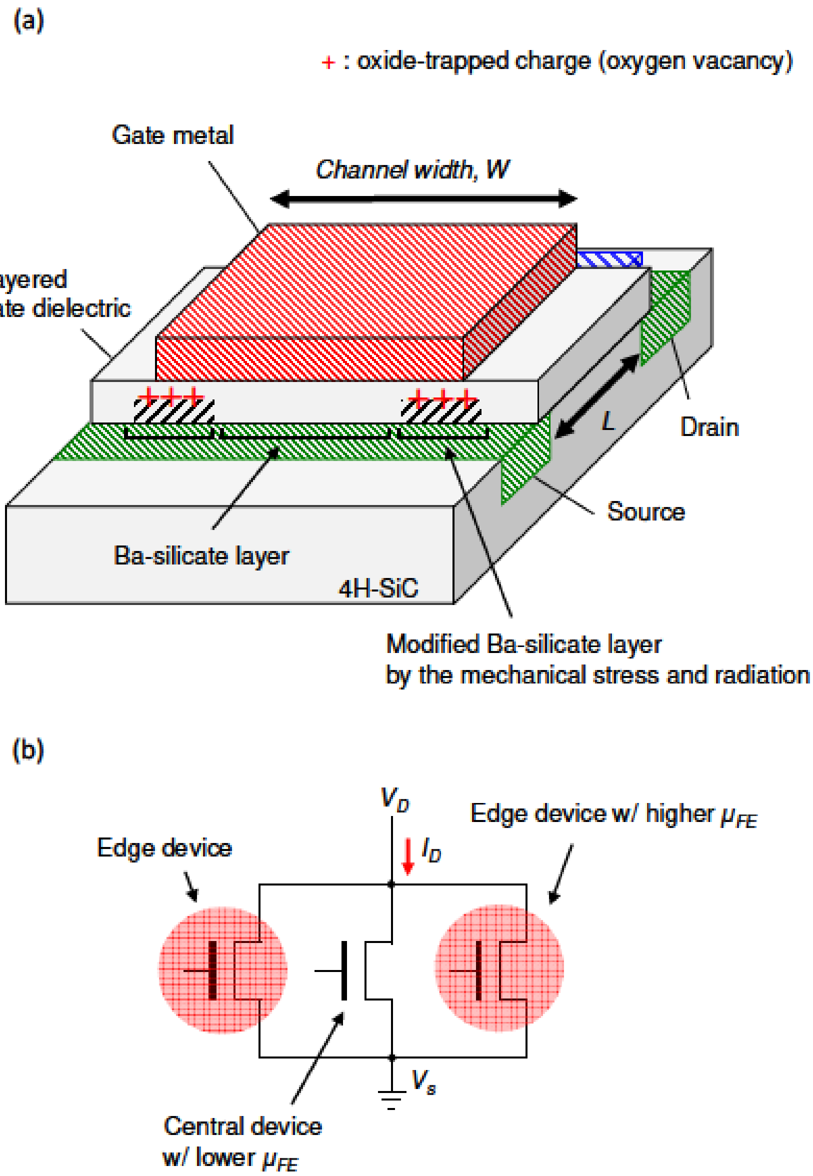

Fig. 5.11. (a) Schematic diagram of distribution of the modified layer for Ba-incorporated MOSFET. (b) The equivalent circuit for the irradiated MOSFET.

5.3 Conclusions

In this chapter, the radiation-induced mobility enhancement effect is characterized by some electrical characteristics.

The Na-contaminated SiC MOSFET was reported to show extremely high mobility owing to the presence of Na ion. It was considered that the irradiated SiC MOSFET also included Ba ions at the gate dielectric/SiC interface, and then BTS test performed to detect the Ba ions. Unlike the Na-contaminated MOSFET, the irradiated MOSFETs have no mobile ion. Thus, the mobility enhancement effect is not caused by interfacial mobile ions.

The enhanced mobility and threshold voltage shift depend on channel width. It is found that the wide channel MOSFET does not exhibit the radiation-induced mobility enhancement effect. This wide device has less the oxide-trapped charges and exhibited the shallow trap state at energy level near E_c. After electron injection at a high temperature, the narrow channel MOSFET also exhibited reduction of oxide-trapped charges and the shallow traps. It is speculated that the shallow trap cancels out the radiation-induced mobility enhancement effect. That is, shallow traps play a key role in occurrence of the radiation-induced mobility enhancement effect. Shallow traps were observed in samples with less oxide-trapped charge density.

The following mechanism is proposed; radiation and electrode-induced mechanical stress induce much oxide-trapped charges in the gate-dielectric around the edges of gate electrode. These oxide-trapped charges modify the interfacial Ba-silicate layer and form high mobility transistors at the edges.

Although the mechanism is insufficiently understood, the results of the both RINCE and the radiation-induced mobility enhancement are useful for designing devices with radiation hardness. Because the logic circuits are designed with varying channel width to optimize circuit design. A designer is able to control radiation sensitivity with not only gate-oxide thickness, but also the channel width. Most MOSFETs are degraded by radiation, the mobility degradation provides lower drive-current. The mobility enhancement effect may be able to compensate for this reduction, leading to more stable operation.

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Chapter 6

Conclusions

The objective of this study is the development of SiC MOSFETs with high-mobility and hardness in the harsh environments. Obtained results are summarized for each chapter.

Chapter 1 shows research background and purpose. High effectiveness of 4H-SiC as semiconductor substrate is described in order to achieve the decommissioning of nuclear power plants.

In Chapter 2, it is shown that the impacts of different thickness of cap-SiO_2/BaO_2 layers on structural and interfacial properties of layered gate-dielectrics. SiO_2 cap layer plays two important roles in the formation of Ba-silicate; one is to ensure that Ba-silicate remains intact at the MOS interface even after oxidation. SiO_2 capping helps localize Ba-silicate at the MOS interface. Another role is to control the stoichiometry of interfacial silicate. A thicker cap-SiO_2 layer resulted in a more BaO-rich silicate structure and reduction of the interface trap density.

For the BaO_2 layer, a thick BaO_2 layer over 6 nm induces poly-crystallization of Ba-silicate. The poly-crystallized Ba-silicate loses the ability to improve the MOS interface. The non-crystallized BaO-rich silicate layer is conducted to be necessary for improving the 4H-SiC MOS interface properties.

In Chapter 3, high-temperature characteristics of SiC MOSFETs with the interfacial Ba-silicate layer are shown. The Ba-incorporated MOSFET operated even at high-temperatures up to 500°C. And the channel mobility is independent of measurement temperature thanks to low interface trap density owing to Ba.

Chapter 4 shows the radiation responses of Ba-incorporated MOSFET. Radiation-induced interface traps and oxide-trapped charges were higher than those obtained for the Dry SiO_2. This result indicates the Ba-incorporated SiO_2 with a thick gate-dielectric layer has less the TID hardness than the thin Dry SiO_2. However, this result is strongly affected by gate-oxide thickness. After correcting the contribution of gate oxide thickness, for the Ba-incorporated SiO_2, the interface trap generation efficiency and the oxide charge trapping efficiency were slightly smaller than those of the Dry SiO_2. That is, the interfacial Ba-silicate layer is robust to radiation.

Moreover, the output characteristics of the irradiated MOSFET are discussed. The irradiated MOSFET exhibited the drain characteristics with the sudden rise of I_D on the saturation region. The sudden rise of I_D is concluded to result from the electron-hole pairs created by electron tunneling via defects at the drain-substrate junction. The defects are expected to be induced by the displacement damage due to gamma-ray irradiation.

In Chapter 5, the radiation-induced mobility enhancement effect is discussed. For the Ba-incorporated MOSFET, gamma-ray irradiation above 600 kGy (SiO_2) induces an anomalous mobility enhancement, which is accompanied by an increase in interface trap density. Based on some electrical characterizations, the following mechanism is proposed; radiation and electrode-induced mechanical stress induce much oxide-trapped charges in the gate-dielectric layer around the edges of gate electrode. These oxide-trapped charges modify the interfacial Ba-silicate layer and form high mobility transistors at the edges.

In summary, the Ba-incorporated MOSFET operated after stressing by two extreme environments, high-temperature up to 500°C and high radiation of 850 kGy (SiO_2). Therefore, the Ba-incorporated gate-dielectric shows high potential as a gate insulator for the harsh environment electronics.

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Kosuke Muraoka

March 6th, 2020

Appendixes

A List of symbols

Symbol	Description
C	Capacitance
C_{FB}	Flat-band capacitance
C_{GD}	Gate-to-drain capacitance
C_{it}	Interface trap capacitance
C_m	Measured capacitance
C_{mc}	Capacitance corresponding to $G_{m,\,max}$
C_{ox}	Gate-oxide capacitance
C_p	Equivalent parallel capacitance
C_s	Semiconductor capacitance
$d_{cap\text{-}SiO2}$	Thickness of cap-SiO_2 layer
$d_{silicate}$	Thickness of interfacial silicate layer
D	Adsorbed dose
D_{it}	Interface trap density
E	Energy
E_c	Energy level of conduction band bottom
E_d	Threshold displacement energy
$E_{e\text{-}h}$	Electron-hole pair creation energy
E_g	Bandgap of semiconductor or oxide
E_i	Intrinsic Fermi level
E_k	Kinetic energy
E_{ox}	Oxide electric field

Symbol	Description
E_t	Energy level of interface traps
f_{de}	Dose enhancement factor
f_{it}	Interface trap generation efficiency due to radiation
f_{ox}	Oxide charge trapping efficiency due to radiation
f_y	Probability that electron-hole pairs escaping initial recombination
g_d	Drain conductance
G_{GC}	Gate-to-channel conductance
G_m	Measured conductance
$G_{m,\ max}$	Maximum measured conductance
G_p	Equivalent parallel conductance
I_D	Drain current
I_G	Gate (leakage) current
I_{mg}	Midgap current
I_{sub}	Substrate current
k	Dielectric constant
k	Boltzmann constant
L	Channel length
L_B	Debye length
n	Carrier density
n_i	Intrinsic carrier density
N_A	Acceptor impurity concentration
N_c	Effective density of states in conduction band
N_D	Donor impurity concentration
N_{eff}	Effective positive-charge density
N_p	Initial number of electron-hole pairs owing to incident particle
N_v	Effective density of states in valence band

Symbol	Description
q	Elementary charge, = 1.6×10^{-19} C
q_{xy}	Horizontal scattering vector
q_y	Vertical scattering vector
Q_n	Mobile charge density
T	Temperature
$T_{intrinsic}$	Temperature at switching from the saturation region to the intrinsic region
T_j	Junction temperature
V	Voltage
V_{DG}	Drain-to-gate voltage
V_{DS}	Drain-source voltage
V_{inv}	Gate voltage corresponding to the surface potential of $2\Psi_B$
V_{mg}	Midgap voltage
V_s	Normalized surface potential to kT/q
V_{so}	Stretch-out voltage
V_{th}	Threshold voltage
W	Channel width
x_j	Source/drain junction depth
β	Reciprocal thermal energy to q/kT
ΔN_{it}	Radiation-induced interface trap density
ΔN_{ox}	Radiation-induced oxide-trapped charge density
ΔN_{te}	Trapped-electron density in oxide
ΔV_{it}	Threshold voltage shift due to interface traps
ΔV_{mg}	Shift in midgap voltage
ΔV_{ox}	Threshold voltage shift due to oxide-trapped charges
ΔV_{so}	Shift in stretch-out voltage
ΔV_{th}	Threshold voltage shift

Symbol	Description
ε_0	Permittivity of vacuum
ε_i	Relative permittivity of insulator
ε_{SiC}	Permittivity of silicon carbide
θ	Angle
κ_g	Number of electron-hole pairs generated in oxide
μ	Channel mobility
μ_0	Normalized channel mobility
μ_{eff}	Effective mobility
μ_{FE}	Field effect mobility
$\rho_{silicate}$	Electron density of interfacial silicate layer
σ_s	Surface potential fluctuation
τ_n	Time constant for electron
ψ_{bi}	Built-in potential at equilibrium
ψ_B	Fermi level from intrinsic Fermi level, $\lvert E_F - E_i \rvert / q$
ψ_s	Surface potential with respect to bulk
ω	Angular frequency

B List of acronyms/abbreviations

Acronym/Abbreviation	Description
2D-XRD	Two-dimensional X-ray diffraction
APCVD	Atmospheric pressure chemical vapor deposition
BSG model	Bond strain gradient model
BTS test	Bias-temperature stress test
DDD effect	Displacement damage dose effect
GIDL current	Gate-induced drain leakage current
HAXPES	Hard X-ray photoelectron spectroscopy
JFET	Junction field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
NASA	National aeronautics and space administration
NITs	Near-interface traps
NSG	Non-doped silicate glass
QST	National Institutes for Quantum and Radiological Science and Technology
RINCE	Radiation-induced narrow channel effect
S/D regions	Source/drain regions
SEEs	Single event effects
SiC	Silicon Carbide
SIMS	Secondary ion mass spectrometry
TID effect	Total ionizing dose effect
TMR	Triple modular redundancy
TOA	Take-off angle of photoelectrons
XRR	X-ray reflectivity

C List of publications

Papers and presentations related to this doctoral dissertation are shown as follows:

-Published papers

First author

1. Enhanced-Oxidation and Interface Modification on 4H-SiC(0001) Substrate Using Alkaline Earth Metal
   Kosuke Muraoka, Hiroshi Sezaki, Seiji Ishikawa, Tomonori Maeda, Tadashi Sato, Takamaro Kikkawa, and Shin-Ichiro Kuroki
   Materials Science Forum **897**, 348-351 (2017).

2. Correlation between Field Effect Mobility and Accumulation Conductance at 4H-SiC MOS Interface with Barium
   Kosuke Muraoka, Seiji Ishikawa, Hiroshi Sezaki, Tomonori Maeda, and Shin-Ichiro Kuroki
   Materials Science Forum **924**, 477-481 (2018).

3. Characterization of Ba-Introduced Thin Gate Oxide on 4H-SiC
   Kosuke Muraoka, Seiji Ishikawa, Hiroshi Sezaki, Tomonori Maeda, and Shin-Ichiro Kuroki
   Materials Science Forum **963**, 451-455 (2019).

4. Gamma-ray irradiation-induced mobility enhancement of 4H-SiC NMOSFETs with a Ba-silicate interface layer
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"4H-SiC MOS キャパシタにおける SiC 表面の CF_4 エッチングの効果"、
公益社団法人　第 64 回　応用物理学会春季学術講演会、16a-P5-7、パシフィコ横浜、2018 年 3 月：ポスター講演

D List of awards

1. 平成28年度広島大学先端物質科学研究科半導体集積科学専攻エクセレント・スチューデント・スカラシップ

2. 平成29年度広島大学先端物質科学研究科半導体集積科学専攻エクセレント・スチューデント・スカラシップ

3. 平成30年度広島大学先端物質科学研究科半導体集積科学専攻エクセレント・スチューデント・スカラシップ

4. 日本原子力研究開発機構　Student Poster Award　（2018年11月27日）

5. The 3rd International Symposium on Biomedical Engineering, Young Researchers Poster Award（2018年11月9日）

6. 応用物理学会中国四国支部学術講演会 発表奨励賞 (2018年11月4日）