Carrier Mobility Modeling of Organic MOSFETs for Circuit Design and Application to Organic Photovoltaics

(回路設計及び有機太陽電池への応用に向けた有機 MOSFET の

キャリア移動度モデリング)

March 2019

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Abstract

In recent years, devices using organic semiconductor materials attract much attention because organic devices enable new product applications that could not be realized with conventional semiconductor materials. The major application areas are transistors for circuit, Organic Photovoltaic (OPV), Organic Electroluminescence (EL). Features of organic devices are low-cost simple process by printing technology, flexibility, large area, and diversity of materials and functions. More and more researches that anticipate the future of organic electronics are being carried out actively in the world. However, there are many issues to be solved to enter the market and compete with conventional products. This research is motivated by such a situation and aims to find new applications of organic devices that can be accepted even in disadvantaged areas in the world such as non-electrified areas.

Firstly, OPV is focused to investigate the potential of OPV in the solar product market. Renewable energy has been introduced aggressively in the world and solar energy is widely used not only in developed countries but also developing countries due to the easiness of installing and its unlimited resource from the sun. At the end of 2017, cumulative introduction amount of solar power reached around 400 million kilowatt and became larger than that of nuclear power. In the countries of Asia, Africa and Latin America, there are still many non-electrified areas that are not connected to the power grid, and standalone small-scale solar home systems are utilized in such areas. This proves that solar power has the high convenience and versatility even in non-electrified areas. In this research, focusing on this small-scale solar home system, it is investigated whether OPV products match people's lives and needs in non-electrified areas. The obtained result tells that OPV is preferred to use as a private solar home system (PSHS). At the same time, technical issues of OPV and influences on their culture and society are highlighted. Possible solutions/approaches for those issues are discussed.

This research approaches to the lowness of energy conversion efficiency from a view point of circuit

application. To make best use of organic material properties, it is important to integrate functions as much as possible on a sheet by flexible devices, which is conceptualized by NEDO (New Energy and Industrial Technology Development Organization) as flexible multi-functions device. In general, solar cells are connected in series and in parallel and balanced to keep sufficient voltage and current since generation voltage of the cell is determined by the magnitude of the photoelectric effect and current of the cell is dependent on cell area. Even for organic solar cell with low conversion efficiency, it is effective to increase the size of the panel and/or boost the voltage by a converter circuit. If the boost circuit can be configured with organic devices, organic solar cells and organic circuit can be formed on a flexible sheet together. Dickson charge pump DC-DC boost circuit is feasible for organic-based circuit because it can reduce the number of complicated passive elements such as inductors. However, there has been no standardized organic device model to design organic-based circuits. Therefore, the first priority in this research is to develop organic device model for circuit design. Compact device model for circuit design has been developed based on silicon material properties and device physics, and reliable device models are used in the circuit simulation or even in the system level simulation. It is known that organic devices have unique conduction mechanism and current characteristics different from silicon devices. This indicates that organic semiconductor properties and conduction mechanism must be described properly in the model to reproduce the device characteristics. Although some conduction mechanisms of organic semiconductor have been proposed as a carrier mobility model, all of these haven't been implemented in a complete device model. In other words, Compact organic device model: HiSIM-Organic that the author has engaged is the only one complete model that has decryptions of organic device physics.

This thesis consists of 7 chapters as follows. Chapter 1 overviews the history of inorganic and organic semiconductor and their developments. Three major electronic products; Transistor and circuit, EL, and PV are explained to compare features of inorganic and organic products. This clarifies the advantage of organic products and helps to consider new application areas. Chapter 2 includes a study on new product application of OPV in non-electrified areas carried with the support of

"TAOYAKA program". This chapter starts with an outline of the global energy situation and the roles played by renewable energy, and continues to the needs survey conducted in the non-electrified villages in India. A possible solution is presented from a viewpoint of circuit application toward low energy conversion efficiency of OPV that was reconfirmed in the survey. Specifically, the suggested solution is to design DC-DC boost converter with organic devices and integrate into OPV sheet. Chapter 3 is to explain device physics of organic MOSFETs (OFETs). Both silicon MOSFETs and OFETs are explained to identify common and different points properly. Chapter 4 explains important techniques for OFETs fabrication and shows the process that the author had followed. The latter part describes the measurement method and the result to understand device characteristics that is particular to OFETs. Chapter 5 is focused on device modeling of OFETs. Basic concept of compact device model for circuit simulation: HiSIM is explained at first. HiSIM has been developed based on silicon MOSFET properties, therefore, the features of carrier transport in organic semiconductor has to be considered and described as a carrier mobility model. The process of describing the carrier transport of OFETs is shown step by step. Thereafter, temperature dependence is analyzed because device temperature is one of the most important parameters that determine device performance. Although OFETs show different temperature dependence from Si MOSFETs, it is sufficiently reproduced by developed model. It is discussed that OFETs have fast degradation phenomena which may deserve to be considered in the model. Chapter 6 is for operation verification of organic-based circuit. DC-DC boost converter (introduced in chapter 2) needs ring oscillator to be operated by pulse signal. Accordingly, oscillation frequency of measured and simulated data are compared to verify whether accurate prediction by developed model is available or not. Simulated frequency is close to the measured data, which indicates the developed model is reliable to be applied to the circuit simulation. At last, Chapter 7 summarizes this research.

Chapter List

Chapter 1
Introduction

1-1: Overviews of Organic and Inorganic Electronics

Semiconductor products are overflowing in the modern society. Several billions of semiconductor elements are buried in the hardware of the handheld units such as smartphone or tablet and make many complicated functions available now. Enormous number of transistors work as a switch under the display of TV and PC to deliver beautiful pictures to our eyes. Downsizing, light weighting, and multi-functionalization have been accelerated by "integration of semiconductor", and it is said that the paradigm shift of the human modern lifestyle was surely carried by the development of the semiconductor technology. Interestingly, the development of this semiconductor technology follows to sail up the periodic table from the fourth period of the IV genus to the third period and continues shifting to the second period. The change from discovery of Germanium (Ge: the IV genus, the fourth period) to Silicon (Si: the IV genus, the third period) happened from the viewpoint of stability and manageability of Si. The Si semiconductor brought big innovation for electronics and information industry and accomplished remarkable growth after the 1950s, and now the market size reaches to 412,221 million dollars in 2017 with an ongoing growth [1, 2]. As well as Si and Ge, the variety of semiconducting materials shows an expanse to compound semiconductors such as GaAs and GaN that are often taken up as a direct transition type and carbon located in the IV genus of the second period, namely, the semiconductor material is now on the stage of wide diversification. It is expected that the carbon causes a new paradigm shift again. As for carbon, the properties of matter change dramatically by only a slight difference of combination between carbons. In other words, carbon is the versatile material that it can be the materials with super strength such as diamond and graphene but also the plastic-formed soft materials. High performance power devices such as silicon-carbide (SiC) attract attentions in the power electronics field, in addition, the diamond transistor which has

super high breaking voltage and heat resistance has been reported [3]. On the other hand, the conductivity was found also in the organic molecular materials including carbon by the transportation of electrons (or holes) through π-bonds, which indicates carbon is the core material to carry organic electronics [4]. In this way, the electronic materials are widely used from inorganic semiconductors to an organic semiconductors, and it is anticipated that the product application suitable for each materials will be designed in the future. This chapter firstly touches about the history of inorganic as well as that of organic semiconductor and continues to the product examples made of organic semiconductors. After that, the purpose of this study and the prospective result are shown.

1-1-1: History of inorganic electronics

Semiconductor* was discovered in 19th century and the first transistor was invented in 1940s'. The origin of transistor was from the success of transatlantic wireless communication by G. Marconi*. During the wireless communication, current has to be detected to extract the information from received signal. Ores such as selenium and silicon were used as a point-contact-type signal detector. The performance of such detector was unstable and vulnerable to noise. Meanwhile, vacuum tubes appeared. The concept of vacuum tubes used the idea of light bulbs. However, vacuum tubes also had some issues for the operation. The heater necessary for the operation of vacuum tubes had bad durability and was easily burned out, and the heat from the tubes caused high temperature of the room. Moreover, it was not good at operating with high frequency because vacuum tubes need long time to discharge electrons between electrodes. In 1935, R. Ohl in Bell laboratory investigated the micro property of current flowing inside the ores, and selected Si as more stable and conductive material [2]. Afterwards, J. Scaff and W. H. Brattain observed in the process of refinement that an area which has boron impurities can be p type (charge carrier is hole) and an area which has phosphorous impurities can be n type (charge carrier is electron). Also they measured that the interface between these two different types shows rectifying effect, which would be established as a "pn junction". In 1947, the first point-contact-type Ge transistor based on the mechanism of schottky

junction was invented. This transistor showed an amplifying function to a certain extent, but was still unstable and too sensitive to the position of contact point. Shockley investigated the reason of such instability based on quantum mechanics and revealed that schottky junction can be replaced with pn junction. This assisted the birth of a pn junction based transistor. After that, Czochralski (CZ) method for single crystalline silicon by G. Teal and Planer method for transistor fabrication had been adapted and finally reached to the concept of transistor integrated circuit. The major dominant point of planer type transistor was to be able to use oxide layer as an insulator. D. Kahng and M. M. Atalla conducted an experiment that they applied voltage to the electrodes deposited at the surface of thermally oxidized p-type silicon, and found that electrons are accumulated at the interface and controllable by the voltage value. The result indicated that there is less dangling bond at the interface of silicon and oxide silicon, this led to the realization of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) which is one of the most popular type of transistor [3]. The performance of transistors such as switching speed, device size, breakdown voltage, reliability, device lifetime and many other elements have been drastically improved. The number of transistor integrated in IC chip have been increased according to Moore's law with device miniaturization in particular after 1970s. The number of transistor integrated in a chip was around 2000 in 1971, but now it have increased to hundreds of millions. The size of single transistor reaches less than 10 nm level technology [4, 5].

Scientific field called as semiconductor physics/semiconductor device physics have been developed in parallel that semiconductor industry has accomplished successful development. To reach higher performance of transistors, various aspects have been studied including quantum mechanics, material physics, interfacial control, fabrication method, and evaluation/measurement technique, which means that the device physics reaches extremely high level in particular to silicon based devices. Thus, the properties of silicon and related materials were revealed and a band conduction theory was established as well. Also, a lot of experimental data gave empirical equations and analytical equations that can represent the device properties mathematically. The progress of device physics and computing technology gave a birth of Technology Computer Aided Design (TCAD). TCAD is a general

name on semiconductor device process simulation and operation simulation. While device fabrication takes at least several weeks originally, it becomes possible by TCAD simulation to make a virtual device and even to calculate the electric characteristics instantly. Measurement has advantage to extract current, voltage and/or capacitance as an output data, however, it is difficult or time-taking to have detailed properties inside of the device. TCAD simulation can calculate and reproduce inside potential distribution and carrier behaviors by solving equations iteratively, which accelerates device optimization. Many electronics venders started to use TCAD since 1970s to reduce the time and cost for trial manufacturing and boost to develop for higher performance devices. Currently, Sentaurus Device Simulator and Process Simulator from Synopsys [6] and ATHENA and ATLAS from Silvaco are the major TCAD software [7].

An indispensable tool for circuit integration is a circuit simulator. Circuit simulator can predict circuit operation efficiently and is used in logic circuits constituting IC chips as well as power electronics circuit. In 1973, SPICE (Simulation Program with Integrated Circuit Emphasis) [8] capable of simulating electronic circuits was developed at the University of California, Berkeley and carried innovation in analog circuit design. The source code of SPICE is basically open to the public, and many EDA (Electronic Design Automation) vendors have developed original simulation software based on SPICE. Device models are commonly used in these circuit simulators to reproduce each circuit elements. Device models are also applied to active elements such as transistors and diodes which exhibit nonlinear electrical characteristics as well as passive elements such as resistance, capacitance and inductance. More efficient circuit/device design can be performed by combining with device simulators. The device model is described in detail in Chapter 5.

1-1-2: History of organic electronics

Conductivity of organic solids was already discovered in the first half of the 19th century, but the term “organic semiconductor” was still not applied to it. The discovery of organic semiconductor was derived from the study of carbon. Iguchi and Samejima et al. expected the transportation of π

electrons in polycyclic aromatic compounds and measured their conductivity. For the experiment, it was important to measure the minute current and secure the purity of the sample. This is because inorganic semiconductor is positively doped with impurities in order to activate its conductivity, but impurities in organic materials often interfere with the transportation of electrons and holes. The first organic semiconductor was reported as "The electrical conductivity of graphite and carbon black has been attributed to their molecular structures which are made of network planes of the conjugated double bonds of carbon atoms with the pai-electrons." by H. Akamatu and H. Inokuchi in 1950 [9]. After this, they continued to research on conductivity of organic materials [10] and they started to call it as "organic semiconductor" [11].

In 1986, A. Tsumura et al. reported organic-based field effect transistor [12] as the first case. The carrier mobility* in those years was valued around 10^{-5} cm^2/Vs that is totally insufficient to compete with inorganic materials. However, a large number of research on organic semiconductors were conducted because it was expected that organic semiconductor can realize new device concepts with flexibility and printability that are impossible for inorganic solid materials. Performance of organic transistors has been improved due to the continuous invention of organic materials and fabrication methods. Figure 1-1 shows the growth of carrier mobility [13]. A recent reported value reaches 40 cm2/Vs [14] that is over the mobility of amorphous silicon and poly silicon.

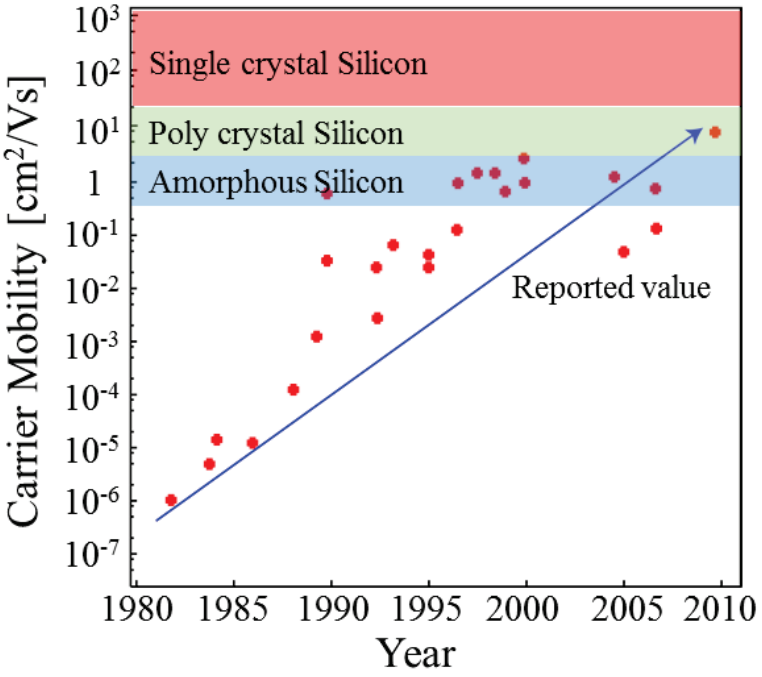


Fig. 1-1: Reported carrier mobility value of organic semiconductor. [13]

Although organic semiconductor devices are still not industrialized presently, those remarkable improvements and developments have been continued and will continue to motivate organic electronics to enter the market.

1-1-3: Organic semiconductor devices

Organic semiconductor can offer new applications with use of organic material properties such as flexibility, light-weight, large scalability, transparency and etc. Figure 1-2 shows several products that are already commercialized or under development [13, 15-21]. It has been discussed for a long time that printing and roll-to-roll process technique can reduce the manufacturing cost and realize mass production of organic devices, which gives price competitiveness. However, the current price of these products in the market is still expensive compared to conventional ones. It is expected that more and more marketing researches and product designs focused on the market penetration of the organic devices will be carried out in near future.

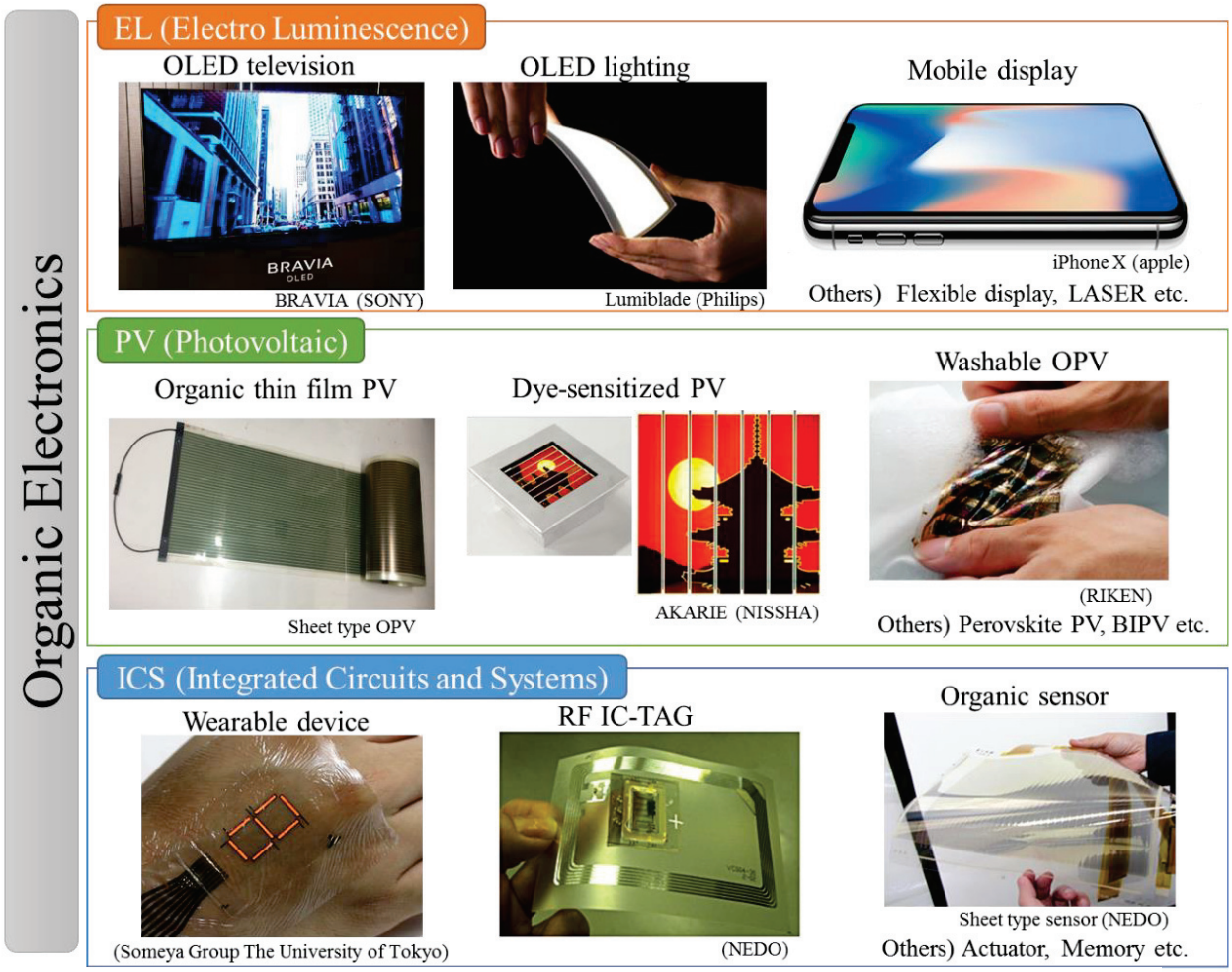


Fig. 1-2: The product examples of organic electronics with three categories; Electro Luminescence, Photovoltaic, and Integrated Circuits and System. [15-21]

Organic Transistor

As mentioned in 1-1-1, transistor has been driving the development of inorganic semiconductor. The word “transistor” is often used in a broad sense. Since the structure and material change significantly depending on the application, it can be divided into many classifications. For example, it can be classified according to the type of carrier to be used. Bipolar transistors have pnp junction or npn junction structure and use two types of carriers (electron and hole) and unipolar transistors use only one type (electron or hole). IGBT (Insulated Gate Bipolar Transistor), which is often used as a power device, is the device that efficiently incorporates the bipolar transistor and unipolar (field effect) transistor in the body [4]. When classifying by crystallinity, there are single crystal,

polycrystalline, and amorphous, the performance and the application greatly change depending on the crystallinity. Size, operation speed and voltage of transistors are also widely diversified. Classification of transistors by operation speed and voltage is summarized briefly in Fig. 1-3 [4].

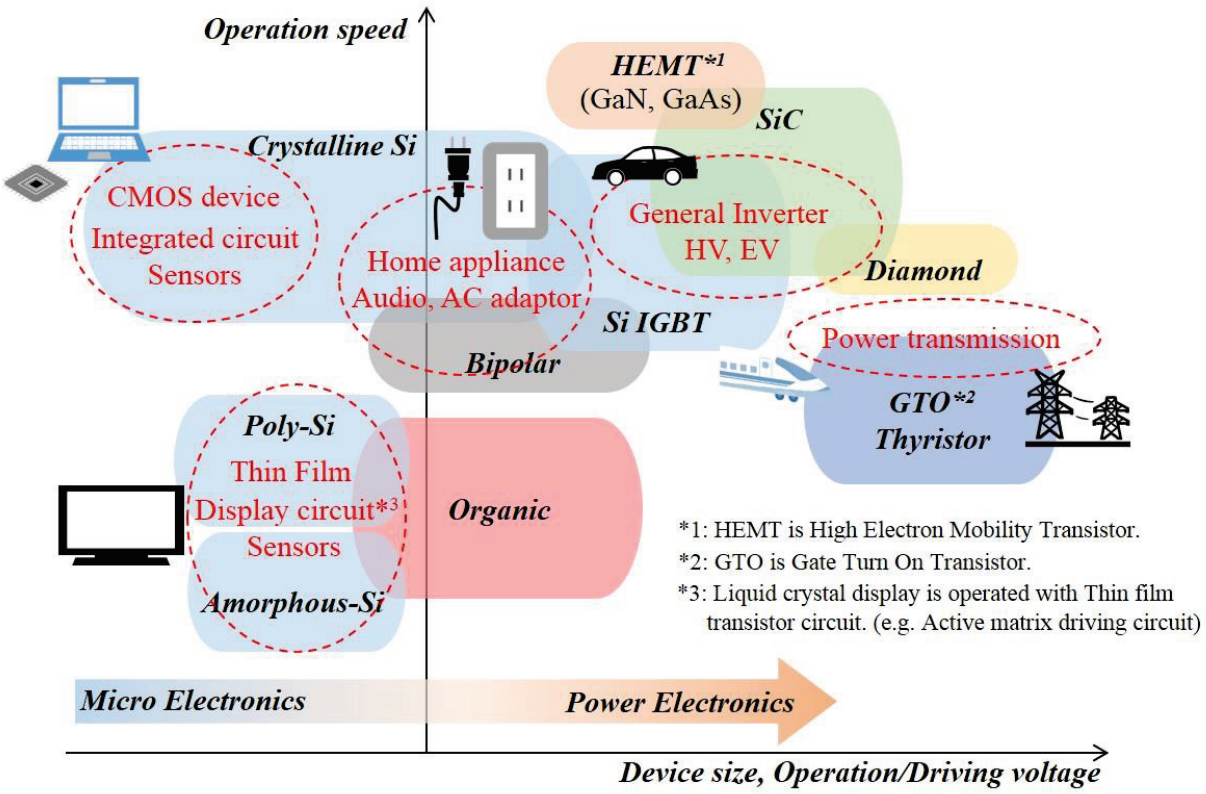


Fig. 1-3: Classification of transistors by operation speed and voltage with some practical applications. [4]

Applicable domain of organic device is similar to that of multi-crystalline silicon device (polysilicon, amorphous silicon, and etc.) since they have almost same value of carrier mobility (see Fig. 1-3). However, it is impossible to simply replace multi-crystalline silicon devices by organic devices since there are some difficulties to be solved for the implementation. One of such difficulties is device's durability. Regardless of the materials, transistor is degraded by aging, and the aging speed can be accelerated by temperature elevation. Likewise, degradation of organic transistors is accelerated by heat, but it occurs even at a relatively low temperature [23-25]. In addition, while the heat resisting temperature of silicon is about 180 °C, organic semiconductors are caused thermal transition and splitting of crystals even at about 100 ° C, and may not function as a device in some cases. The origin of device degradation is not only the aging. When semiconductors are exposed at the air, they can be

oxidized or react with moisture in the air, that interferes with conductivity [25]. Another important issue is that the voltage required for driving the organic devices is higher than that of the inorganic devices[3]. This is because the carrier conduction mechanism is different between inorganic and organic transistors even they have similar structure. In other words, since the inherent carrier mobility of organic semiconductors is low, the voltage necessary to flow the current inevitably increases.

The operation principle of both transistors is described below. Figure 1-4 shows an overhead view of a typical inorganic MOSFET. In this structure, a pn junction is intentionally formed between p-type semiconductor of the substrate and n-type semiconductor of the source and the drain portion. No current flows between the source and the drain due to the rectifying action under the zero voltage condition. When voltage is applied to the gate, a strong electric field is generated in the oxide film and the semiconductor layer, electrons which are minority carriers of the p-type substrate are attracted and n-type inversion layer is formed right under the oxide film. This inversion layer (strong inversion layer) is called a channel. Electrons mainly flow from source to drain though the channel.

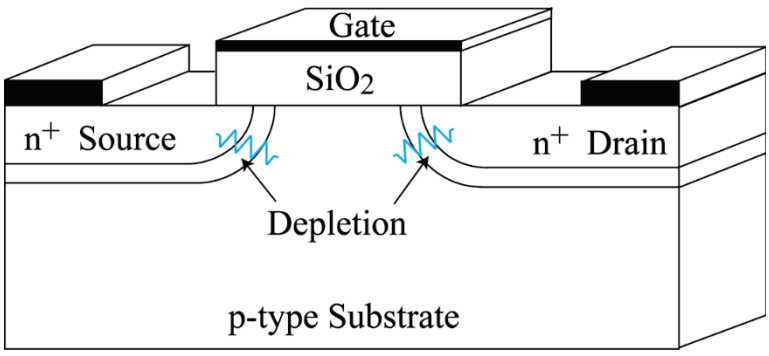


Fig. 1-4: Overhead view of a typical inorganic MOSFET.

On the other hand, the operation principle of organic transistors is different from inorganic ones. Here, description will be given by taking as an example a charge injection type organic field effect transistor which the most practical as an organic transistor. Organic transistors, organic field effect transistors, organic MOSFETs and organic thin film transistors (OTFTs) are collectively called as

OFETs. Figure 1-5 shows an overhead view of a bottom gate top contact type OFET. In the case of OFETs, transistor materials are not directly formed using substrate materials like planar type FET. Therefore, the substrate material can be glass or plastic. Furthermore, intentional doping of impurities is not performed, so that a p-type and n-type region is not formed in the semiconductor layer. Therefore, there is no pn junction for cutting off the current in the bulk portion. Instead, the current is blocked by the charge injection barrier between the source/drain electrode and the organic semiconductor. Research on reduction of contact resistance and improvement of conductivity by impurity doping to the organic semiconductor layer is also being conducted [3, 26, 27]. Conduction type of OFET is determined by the combination of a semiconductor and an electrode material. When no voltage is applied, charge injection into the organic semiconductor from the electrode does not occur and no current flows between source and drain. When voltage is applied to the gate, electric charge starts to be injected from the source or drain electrode. Injected charges are induced to the insulator by the electric field and the channel is formed.

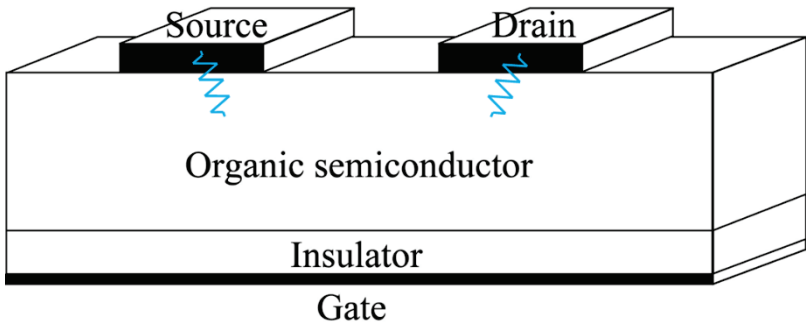


Fig. 1-5: Overhead view of a bottom gate top contact type OFET.

Remarkable point is that even the operation principle is different from each, the fundamental of current characteristics as a transistor never change. The necessary conditions for constructing a transistor are as follows;

- ✓ Free carriers can be induced in the channel area with practical range of gate voltage.
- ✓ The density of induced carriers is larger enough than intrinsic carrier density at thermal equilibrium condition.

- ✓ Induced carriers by gate voltage can be controlled (driven) by voltage from source to drain.
- ✓ Energy bandgap is around 2.0 eV (preferable value for a channel material)

If these requirements are satisfied, the channel material of the transistor can be anything in fact. Most of the organic substances are considered to be electrically insulators, but most of the organic substances, particularly those having absorption in the visible light region, have the lowest unoccupied molecular orbital (LUMO) and the highest occupied molecular orbital (HOMO) equivalent to the band gap is around 2.0 eV. Among such organic semiconductors, materials having relatively high carrier mobility are used for the channel material. Therefore, even in the case of OFETs, as long as the carrier number is controlled by the gate voltage and the carriers are accelerated by the source-drain voltage, general expressions for the OFET motion essentially or apparently can be regarded as the same of inorganic MOSFETs [28]. Since these operation principles are essentially important for understanding OFET, further explanation is described in Chapter 3.

Organic Electroluminescence

Organic electroluminescence (EL) is a general name for devices that utilize a converting system from electrical energy to optical energy. The most famous EL element is Light Emitting Diode (LED) which is commonly used for point lighting sources. Organic semiconductor can be used as the light emitting layer in LED device, named as Organic LED (OLED) to distinguish from conventional LED. Inorganic EL has a different light emitting mechanism. Figure 1-6 summarizes EL devices and light emitting mechanisms for each [29, 30].

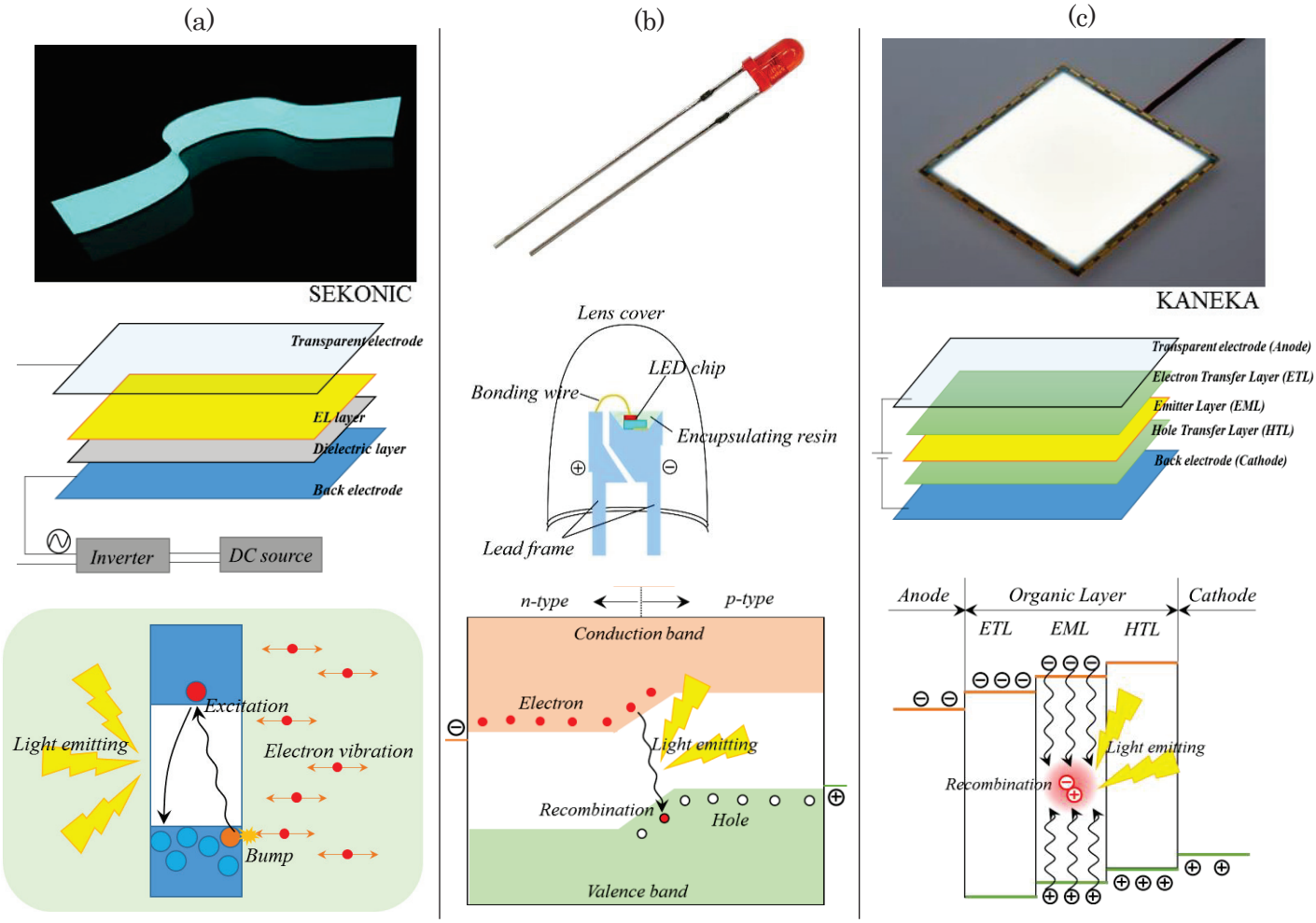


Fig. 1-6: Electroluminescence devices and its light emitting mechanisms by three types; (a) Inorganic EL, (b) LED, and (c) OLED. [29, 30]

Andre Bernanose, a father of OLED, discovered electroluminescence phenomena in organic materials in the early 1950s. In addition, Bridgman method [31] for formation of single crystalline organic semiconductor was reported at the same period. These two discoveries are the beginning of organic EL. In 1987, Tang and Van reported an innovative OLED device which has a thin organic semiconductor layer (around 100nm) with amorphous condition, can emit the light under 10V, and has a stable cathode material (alloy: Mg and Ag). After this, the conceptualization of organic display using OLEDs became so active, which led to aggressive commercialization of smartphone display and OLED TV. The benefit of using OLED is that they can reduce the backlight and liquid crystal layer

or plasma discharge layer, resulting in decrease of thickness and weight in the display application. The thinnest OLED TV reaches under 5mm and the weight of 65 inches display is around 8 kg while liquid crystal TV with same size weighs over 20 kg [3]. By using organic materials, it is possible to produce thin and large-area light emitting layer with low cost. OLED TV display can be thin and flexible if the circuit for driving is composed accordingly.

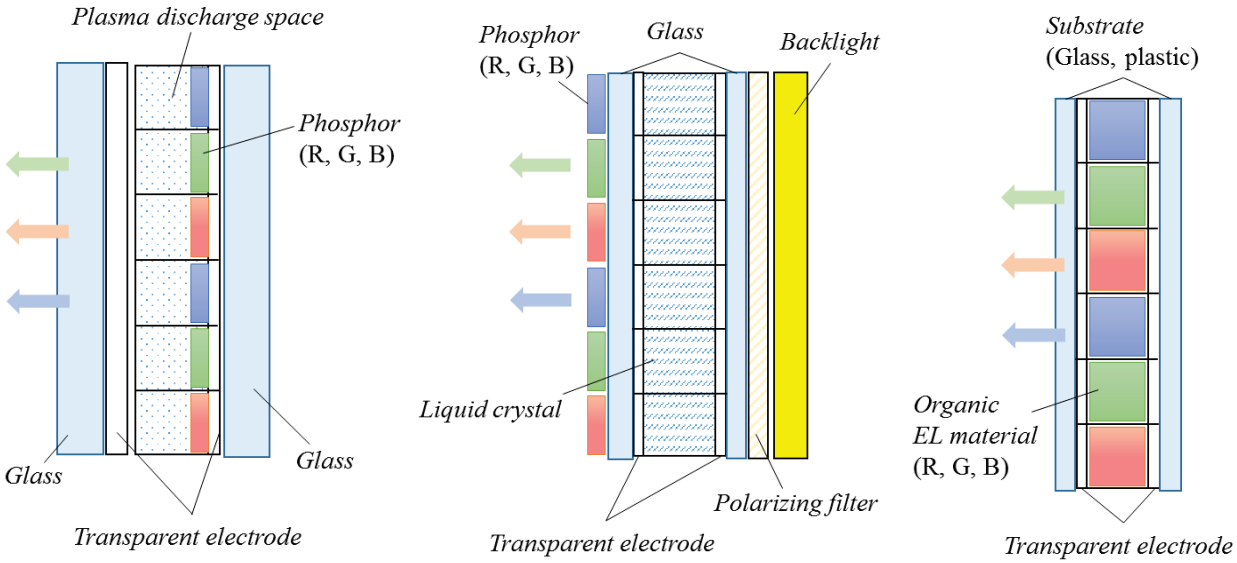


Fig. 1-7: Mechanisms of Display in (a) Plasma TV, (b) Liquid Crystal TV, and (c) OLED TV.

As another possible product with OLED, light source application has been discussed since J. Kido et al. [32] reported white light emitting organic electroluminescent devices in 1994. LED and OLED have similar light emitting mechanism at the point of carrier injection type. Even though LED has a superb potential as a point light source, is disadvantageous as a surface light source, therefore, they need to reproduce the surface light source by multiple LED lines. On the other hand, OLED takes advantage in use of surface lighting. When used as lighting, there are evaluation items such as brightness and efficiency, lifetime, response, average color rendering property and so on [33]. Each evaluation is summarized in Table 1-1.

Table 1-1: Evaluation items for lighting source

	Luminous efficiency (under 1,000cd/m2)	Lifetime (LT70)*1	Response	CRP*2
Fluorescent	～110 lm/W	12000 hrs	Via a discharge tube	84
LED	～190 lm/W	40000 hrs	Instantaneous	80
OLED	～40 lm/W	50000 hrs	Instantaneous	86
Max efficient	683 lm/W	*3	Instantaneous	100 (= Natural Light)

*1: LT70 represents a lifetime that the luminance decreases down to 70% of initial performance. LT50 and LT80 are also used to represent products' lifetime.

*2: Color Rendering Property. This value is used to indicate how the light is near to natural light. CRP=100 corresponds to natural light.

*3: There was a tradeoff relation between luminance and lifetime in OLED. Lifetime was inversely proportional to 1.2 ~ 2 power of luminance. Multi Photon Emission (MPE) type solved this issue.

Besides, there are evaluation items such as heat resistance and temperature dependency. The heat resistance of the OLED depends mainly on the heat resistance of the organic material. It is said that the temperature which the stable shape can be maintained as a thin film is approximately 100 ° C to 150 ° C or so. When OLED is used for lighting or displaying, a heat dissipation protection system is required so that errors due to high temperature never occur. In addition, as a tendency of the temperature dependence, response and luminous efficiency of OLED hardly decrease at a low temperature of about -30 ° C. However, at high temperatures, although response and luminous efficiency do not change, they have a negative influence on the lifetime. For example, it has been reported that the lifetime characteristic at 85 ° C is less than half of the lifetime at 25 ° C [10]. When using only for lighting, the device temperature doesn't rise so much, but if it is used for a long time or becomes a large area, the device temperature definitely rise during driving. LED lighting that has a well-balanced in these items and has a rich designability is desired.

1-2: Purpose and outcome of the research

The major purpose of this research is to make it clear that organic devices have a good potential to be applied into the society. The first activity with a focus on OPV proved that the products can be competitive to the conventional ones as long as they are designed with a best use of organic device features. However, it was also proven that OPV have many issues to be solved, especially its low conversion efficiency. One possible solution for such issues is to compensate them by using circuit application. If any boost circuit or other useful circuit can be designed by organic devices, multiple functions can be combined on a flexible sheet by low-cost simple process with a printing technology. This motivates the organic device modeling to design organic-based circuit.

Excellent device model can accurately predict device and circuit operation, it can drastically reduce the time, labor and material cost of product development, so it is indispensable for designing products with electronic circuits. However, there has been no practical device model for designing circuits based on organic semiconductors. For this reason, it was necessary to substitute a conventional device model with a physical quantity such as carrier mobility for organic-based circuit design and/or prototype a single transistor for mobility measurement. With such a method, it is difficult to cope with changes in the practical environment including changes in materials and temperature. Also, unlike inorganic semiconductors, the mobility of organic semiconductors is low because carriers conduct by hopping between molecules and between crystal grains, but the electric characteristics cannot be reproduced simply by reducing the mobility. By constructing a model based on the electrical characteristics of organic semiconductors, it is possible to drastically reduce the time required for product design, and it will become a successful step forward for the future practical application of organic products. Therefore, the top priority of this research is to develop the compact model: HiSIM-Organic [34, 35] for organic devices with analyzing the electrical characteristics of organic semiconductors and constructing the mobility model based on device physics. Fortunately, a lot of research has been done on the conduction mechanism of organic semiconductors [3], and the elucidation has been made. How to describe those mechanisms as a compact model is an important task. The factors to be considered

in organic device model are temperature dependence and trapping effect since these influence on the device performance. The developed device model is verified by comparing with measured value of devices and circuits.

Chapter 2

Organic Photovoltaic

This work addresses the quality of life in non-electrified villages and challenged to find new applications of PSHS with considering features of organic PV. Their preferences' on PSHS are analyzed in our survey and the result is reflected on the product design.

2-1: World energy situation

Energy consumption of the world never stops to grow up due to the population grows and increasing demands for technologies. Population without electricity is mainly distributed in Developing Asia and Africa that has large population grows rate (see Fig. 2-1). While the electrification rate is increasing year by year, disadvantaged areas like poor, remote, mountainous, and disaster prone areas are still remained to have difficulty accessing to the electricity grid. According to the World Energy Outlook 2015 [1], 22% of the people in developing countries still don't receive electricity supply from power grid.

Renewable energy such as solar energy is one of the viable way to supply electricity to humans for securing minimum quality of life. It has been proven that solar power can take a critical responsibility in the energy sector through all of the past activities regarding rural electrification [1-6]. Several developing countries in south Asia and Africa are approaching the energy issue by encouraging solar power with off-grid as well as on-grid application [4]. Fortunately, those areas have some advantages to use solar power in a sense of irradiance level and spacious land. Some of the remoted place have been already electrified with mini- or micro-solar grid, and more and more households in non-electrified areas start to use Private Solar Home System (PSHS) [4, 5]. PSHS consists of solar panel (~1kW), battery, charge controller, and lighting equipment. There are various capacity sizes depending on users' demand. In developed countries, PSHS is used as a supplementary power, that is, the houses have connection to both national power grid and PSHS. In order to cover all electricity

in a house, the capacity of PSHS should be basically more than 1.0kW. In contrast, the houses in disadvantaged areas have small capacity of PSHS which is standalone and under 200W in general. Such type of PSHS is aggressively spreading to non-electrified villages [4, 5, 6].

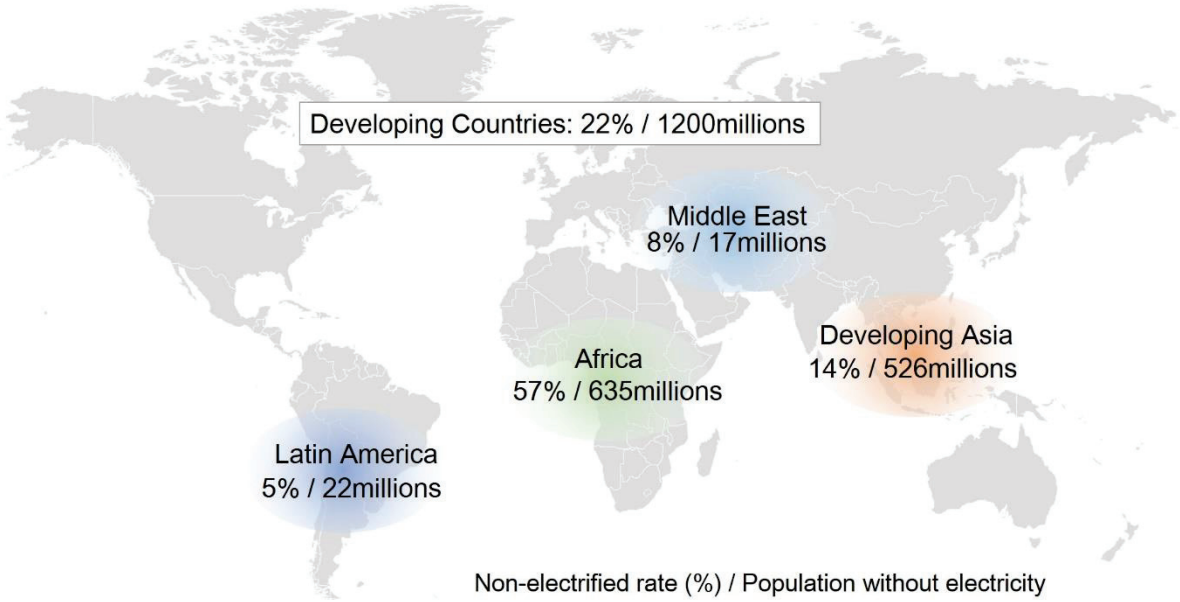


Fig. 2-1: World map with non-electrified rate and population living without electricity grid.

2-2: Motivation of OPV technology

2-2-1: Overview of photovoltaic technology

There are various PV cell technologies in the market using different types of materials. PV cell technologies are usually classified into three generations that are depending on the basic material and the level of commercialization [7, 8]. First-generation PV uses the wafer-based crystalline silicon cells. Single-crystalline silicon cell and multi-crystalline silicon cell are the most popular products in the solar market. Second-generation PV is based on thin-film PV technologies such as amorphous silicon, micromorph silicon (micro crystalline plus amorphous Si), Cadmium-Telluride (CdTe), Copper-Indium-Selenide (CIS) and Copper-Indium-Gallium-Diselenide (CIGS). Third-generation PV indicates future generation of PV technologies that are still under demonstration or have not been widely commercialized yet. There are some emerging technologies such as quantum dots, dye-sensitized cells, organic cells, perovskite cells and thermoelectric devices hold great promise for the future. Table 2-1 summarizes categories of solar cell by materials [9, 10].

Table 2-1: Categories of solar cell by materials with commercialization status.

Category		Features	Conversion efficiency in Module	Commercialization (present status)	Bendability
Silicon	Single crystal	High efficiency and reliability. Comparatively expensive due to use of high purified Si.	~20%	◎	△
	Multi crystal	Lower cost than single crystal one. The most commercialized solar panel.	~15%	◎	△
	Amorphous	More lower cost than multi crystal one, but efficiency is still under 10%.	~9%	○	○
	Micromorph	Tandem structure of amorphous Si and multi crystal Si. Expensive due to difficulty of process.	~18%	△	○
Compound	CIS	Based of Copper, Indium, Selenium. Low cost and efficiency is comparatively high.	~12%	○	△
	CIGS	CIS plus Gallium.	~13%	○	△
	CdTe	Based of Cadmium and Tellurium. Popular in Europa and America.	~11%	○	△
	GaAs	Based of Gallium and Arsenic. High efficiency but very expensive. Mainly Used in satellites.	~25%	△	△
Organic	Organic Thin film	Applicable for Roll-to Roll process with low fabrication cost.	~13% (cell)	△	◎
	Dye-sensitized	High designability (color and shape). Low fabrication cost with ease.	~11% (cell)	△	◎
	Perovskite	Organic-Inorganic hybrid material. Applicable for Roll-to-Roll process.	~18% (cell)	△	○
Quantum dots		High potential of efficiency. Scaling-up of cell is main obstacle.	~19% (cell)	△	△

2-2-2: OPV prospect

Different types of solar PV have both strengths and weaknesses respectively. Today first-generation PV is dominant for the market with their low costs and the best commercially available efficiency. They are relatively matured with a wide range of well-established manufacturers. Although very significant cost reductions occurred in recent years, the costs of basic materials are relatively high and it is not clear whether further cost reductions will be sufficient to achieve full economic competitiveness in the wholesale power generation market in areas with modest solar resources. According to Energy Technology Perspectives [11, 12], it is estimated that thin films including OPV will be competitive at the PV market in the future as shown in Fig. 2-2.

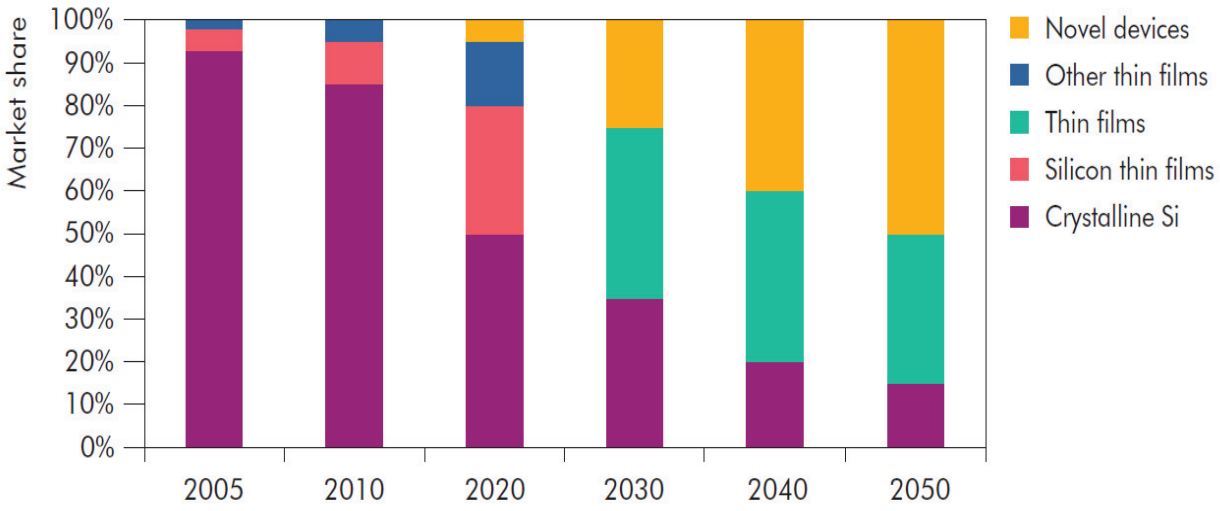


Fig. 2-2: Solar technology perspectives in the future PV market. [11, 12]

Compared to conventional PV module, efficiency is not high and duration is considerably shorter than that of Si PV. Although there are such obstacles, a large number of study are still being conducted because of some attractive points of OPV as follows;

(1) Flexibility and lightweight - This is an ideal feature for mobile application. OPV can be fabricated on a plastic film, therefore, the product is bendable and rollable with frameless and glassless concept. This positive feature can reduce a limitation of installation cost and place.

(2) High designability - OPV can be colored and/or transparent in a certain extent. Colorfulness encourages interior application and transparency enables to be installed on the windows of buildings.

(3) High scalability - Since OPV has lower generation efficiency, it is necessary to be large to keep the same output. It is possible to enlarge single cell further more than Si crystalline cell.

(4) Performance retention in weak irradiance condition - It is unavoidable to be decreased performance in cloudy and rainy condition. However, OPV can work even in such condition due to its weak dependence on irradiance unlike conventional PV.

(5) Environmental friendly technology - Although solar power is recognized as an environmental friendly technology only when they are generating power, strictly speaking, PV emits CO_2 in production and disposal stage. OPV production can use low-temperature process and standard printing technology, which means CO_2 emission / Watt can be smaller than conventional PV.

In addition to OPV's high performance retention in bad weather as mentioned above, OPV doesn't have a limitation of installation place. Solar panel is basically installed horizontally (0°~30°) on land or rooftop facing south. But due to recent expanding demand of energy, it has been started to install vertically facing not only south but others. Conventional Si crystalline solar PV has strong dependence on angular toward light, however, OPV (Dye-sensitized PV: DSC) has less dependence on irradiance angular. Figure 2-3 compares irradiance (light intensity) dependence and angular dependence reported by Fujikura[13, 14].

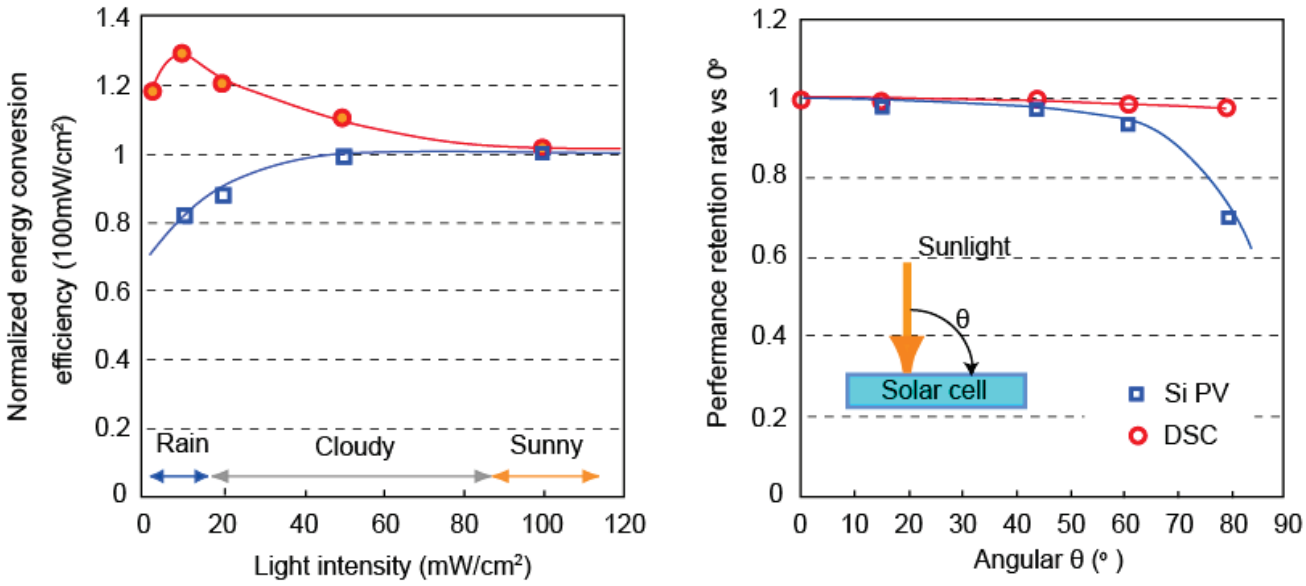
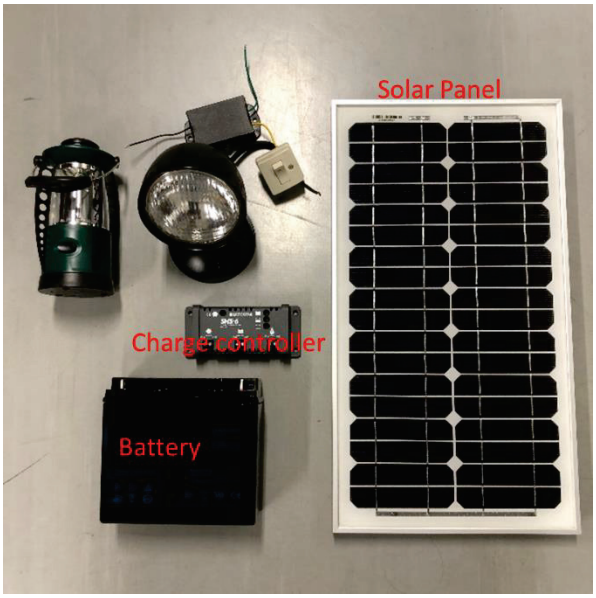


Fig. 2-3: OPV Performance retention in weak illuminance and angular dependence. [13, 14]

These advantages expand the application range. But expected uses are basically limited such as building surfaces, windows, curved body of vehicles etc [15-17]. Our survey was arranged to explore the other adaptable applications and users, ultimately, to investigate whether these features match people's needs or not in the non-electrified areas.

2-2-3: Solar Home System in non-electrified area in India

India government is now promoting domestic electrification with not only on-grid but also off-grid technology like solar home. Each state in India has each energy development agency, which encourage the self-sufficient power supply. They provide solar home system to the local people who don't have electricity grid connection to secure the necessary light for their daily life. Basically, a solar home system consists of: solar Panel (5W, 10W, 20W~), Battery (12V), and Charge Controller as input components and LED light (2~3), Mobile Charger (1~2), Small Fan (1) etc. as output components. Picture 2-1 displays a typical type of solar home system kit for small application



Picture 2-1: Solar Home System Kit for private use (PSHS).

In the conventional solar home system, solar panel is installed on the roof with fixing frame, output load is connected to Control BOX. The Control BOX has a battery and a charge controller, which control the charge to charge a battery or transfer to the output component. In this case, the electricity is not converted from DC to AC, that is, all products have to be DC operation type.

This solar home system had greatly improved the quality of life of the people living in disadvantaged area especially at night [4]. Before the installation of solar home system, children had been forced to do homework of read text with feeble candle fire or kerosene lump. And mothers had been forced to cook in the dark kitchen. The solar home system changed such incogitable situations. However, there still exist issues, for example, financial difficulty, maintenance & repair (aftercare), security problem (theft). The price of solar home system is gradually decrease, but it is concerned that using only the same materials will face a limit of price decline [8].

2-3: Field work for exploring new applications in non-electrified areas

Electricity is one of the vital technology for modern people, however, there are still more than 1200 millions people living without electricity in the world. Solar power can light up the darkness and improve the Quality of Life in non-electrified areas with use of PV technology. Presently PV market is getting diversified thanks to aggressive research on new materials and novel concepts. OPV was invented a few decades ago and gave us an impact. But organic PV hasn't been industrialized yet even though it has unique features such as flexibility, light-weight and designability. Remained issues are low generation efficiency and short duration but these have been improved by progressive studies on materials and packaging technique [9, 10]. Partition of each PV technology in the market is also important task, in other words, it is necessary to point out the targeting consumers. This work dare to focus on application in not urban areas but disadvantaged areas with considering features of OPV. Consumers' preferences are investigated on small-size solar-home-system in non-electrified area with positive expectation for further OPV development. The survey is conducted following the methodology of Conjoint Analysis which is widely adapted in marketing field. Through the survey, we got interesting response from villagers and their opinions were reflected on our product design with use of OPV based on the concept of reverse innovation.

2-3-1: Methodology of Conjoint Analysis

Conjoint analysis is one of the effective methods in marketing to measure use's preference, forecast demand and develop product design [18, 19]. We applied the choice-based conjoint experiment to estimate the preference of respondents on electricity use and product design of organic PSHS. In a choice-based conjoint experiment, respondents are usually asked to choose predetermined combinations of attributes & levels that are referred to as profiles. All of the attributes & levels are taken into consideration of technical feasibility be-cause this survey contains future functions of organic PSHS which is not existing as of now.

Sampling frame of the survey is shown in Fig. 2-4. Households were selected from 11 villages that are randomly selected from village list of Barnawapara forest range in Balodabazar district.

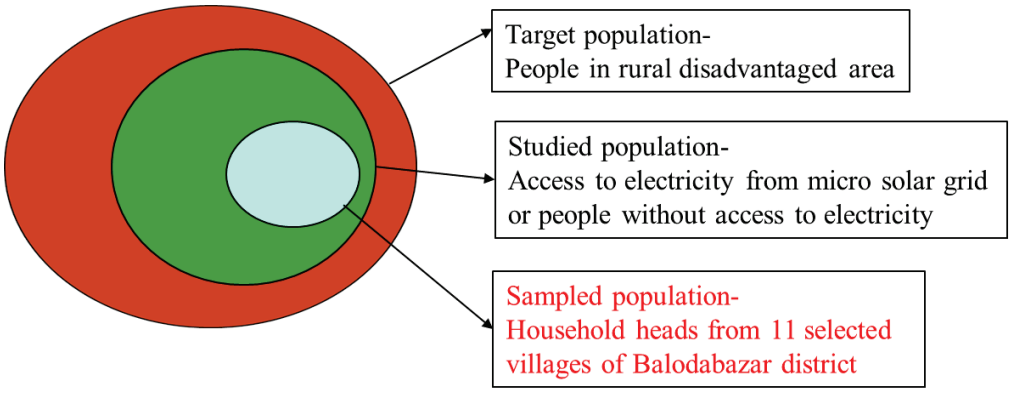


Fig. 2-4: Sampling frame; target population, studied population and sampled population.

2-3-2: Target Area and Population

India is presently world's sixth largest economy and fifth large energy consumer in the world [20, 21]. Although India has 18% of the world's population, uses only 6% of the world's primary energy. Around 30% of the total population have no access or limited access to the electricity. People who living in urban area can easily access to the electricity, on the other hand, people living in remote or mountainous area have very less accessibility to the electricity grid, this huge gap causes such strange numbers. Indian government is intensifying the use of renewable energy to solve the inequality of energy supply [21, 22]. Chhattisgarh state, India is one of the leading player in the field of off-grid PV applications [23], rural electrification rate was only 37% in 1994, 62% in 2005, and drastically increased to 85% in 2012 [20, 24, 25].

The survey was conducted in Balodabazar district, Chhattisgarh, India. Target villages are mainly located in Barnawapara forest range, therefore, this can be a case study of remote, forest, flat-land and less-electrified area. Location of the survey is depicted in Fig. 2-5, and some indicators are summarized in table 2-2. There are several reasons that we consider for selection of the village such as:

- Disadvantaged region in terms of geographical condition, income opportunities.
- No connection to power grid. There is huge government subsidy that support to poor households to be electrified through micro solar grid. Some villages have been already electrified by micro solar grid, villagers know PV technology in some extent.
- Demand for electricity is expanding due to electric appliances and telecommunication tools, while villagers still have problem to use electricity especially in rainy season.
- There is initiative and implementation policy taken by Chhattisgarh Renewable Energy Development Agency (CREDA). They can provide some supporters to communicate with local people.

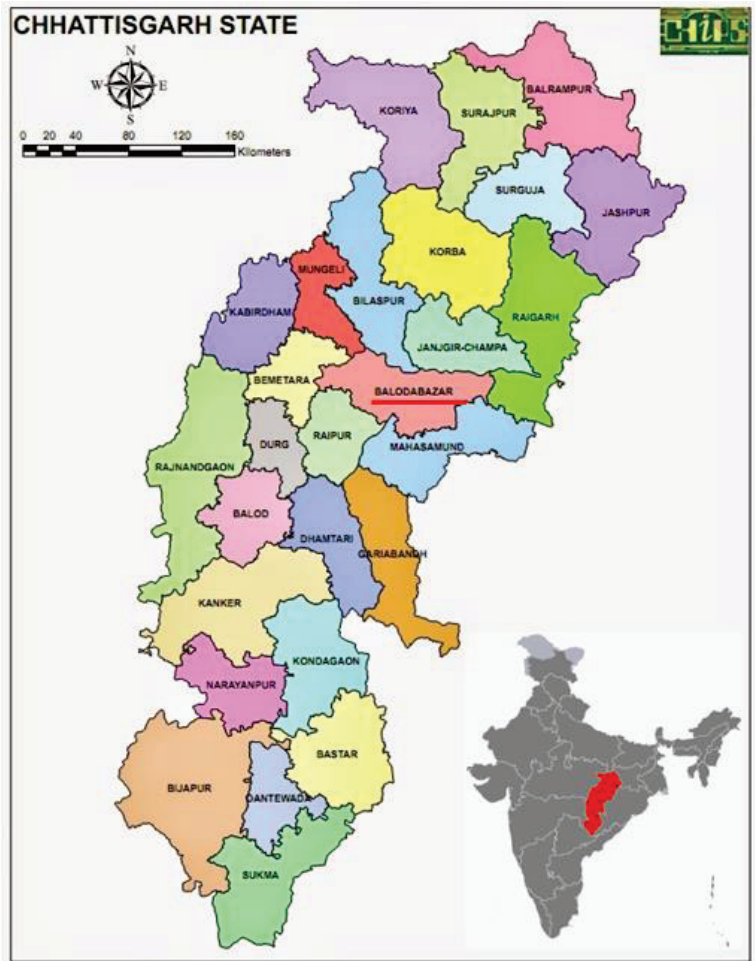


Fig. 2-5: Location of the survey; Balodabazar district, Chhattisgarh state, India [25].

Table 2-2: Chhattisgarh indicators at a glance.

Particulars (year)		
No. of Districts (2017)	27	
No. of total villages (2017)	20,126	
Total Population (2017)	29 million	
Literacy rate (2012)	71 %	
Poverty rate (2012)	Urban	24 %
	Rural	45 %
Electrification (2012)	Urban	92 %
	Rural	85 %
Access to drinking water (2012)	Urban	62 %
	Rural	17 %

2-3-3: Data Collection in the villages

We conducted a pilot survey before the main survey in order to justify the attributes and levels and understand the real situation clearly. What we learned from the pilot survey is that;

- All of the respondents know PV regardless of age, but have never seen organic PV. Features of organic PV could be attractive for villagers by explaining new functions such as flexibility and designability, but it's hard for them to imagine organic PV products and compare with conventional ones. Some treatment like illustration of system design or appearance can help them visually [26].
- Their decisions are quite consistent that they care about system price at first, and lifetime at second, which is common response as a consumer [27, 28]. These two must be included in the attributes, but the levels must not be unrealistic and differentiated so much.
- As for the other attributes, subdividing the levels doesn't work well. Complexity of levels may decrease the reliability of their responses. For instance, if we set many levels of chargeability in cloudy weather as 5%, 10%, 15% …, their choice making become difficult and long process [29]. Importance is making simple to understand even for villagers (like Yes (30%) / No (0%)).

Observations of their house from inside and outside taught us that the roof of their house is just a

pile of cray roof tiles on wooden frames. And at the entrance, there are shading eaves which is made of wooden frames and straws as shown in Fig. 2-6. Plus, they are using such structures inside the house as well, which are looked like a tent. Basically their houses are linked to neighboring houses as shown in Fig. 2-6. One block has several families (these families are relatives in principle), and they have a space in the block. This space is basically used for drying laundry clothes, storage, livestock, and sometime for family party, marriage, festival and so on. These situations gave us an idea for shading eave application and tent application. Sheet type solar panel is further better than conventional one because their roof structures are not enough concrete to fix heavy solar panel.

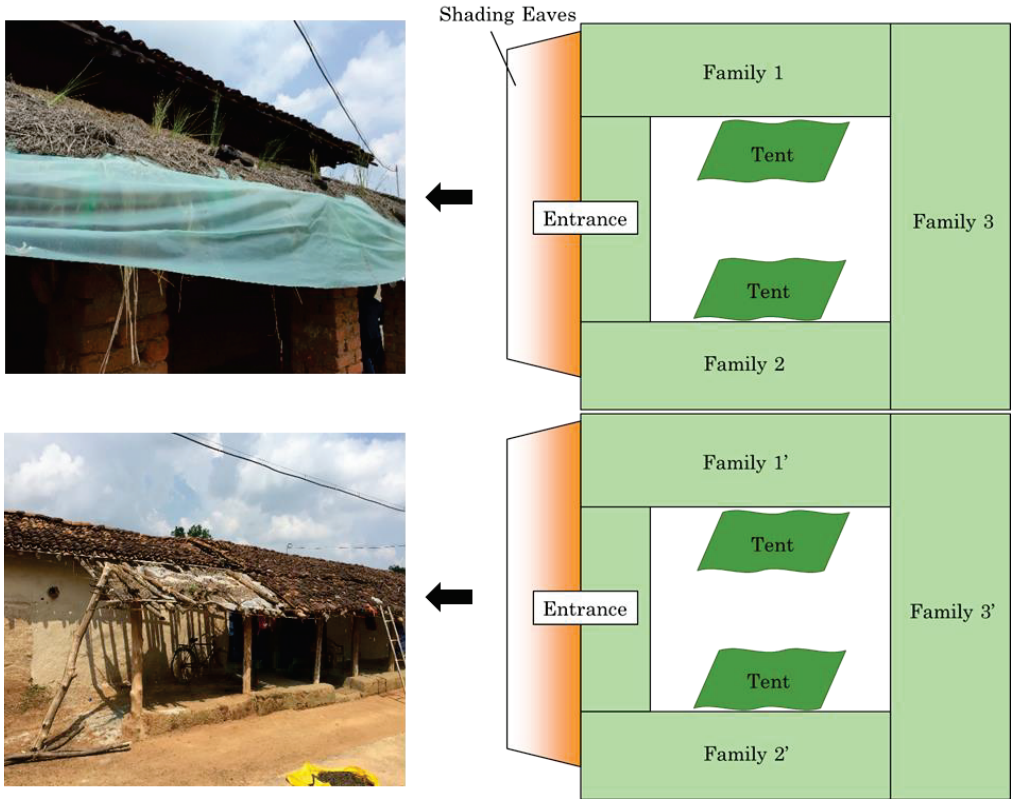


Fig. 2-6: Shading eaves in the village (left) and schematic structure of neighboring houses (right).

One another inspiration from pilot survey is water-related function. Needless to say, they have no water supply piped in each household, they have to go to water pump and bring almost every day (see Pic. 2-2). This water is used for drinking and cooking [30]. They have problems for other water use like toilet, washing, bathing, and etc.

Picture 2-2: Water pump with women (left) and children and pumped water (right).

Focusing on a sanitation problem of their life, we came up with a water harvesting function by flexible solar panel. Curving shape of organic solar panel can be used for harvesting rain water, and harvested water will be stored in a tank falling through a connected hose. These new ideas were depicted in illustrations as shown in Fig. 2-7 to make them easy to understand the concept of OPV product.

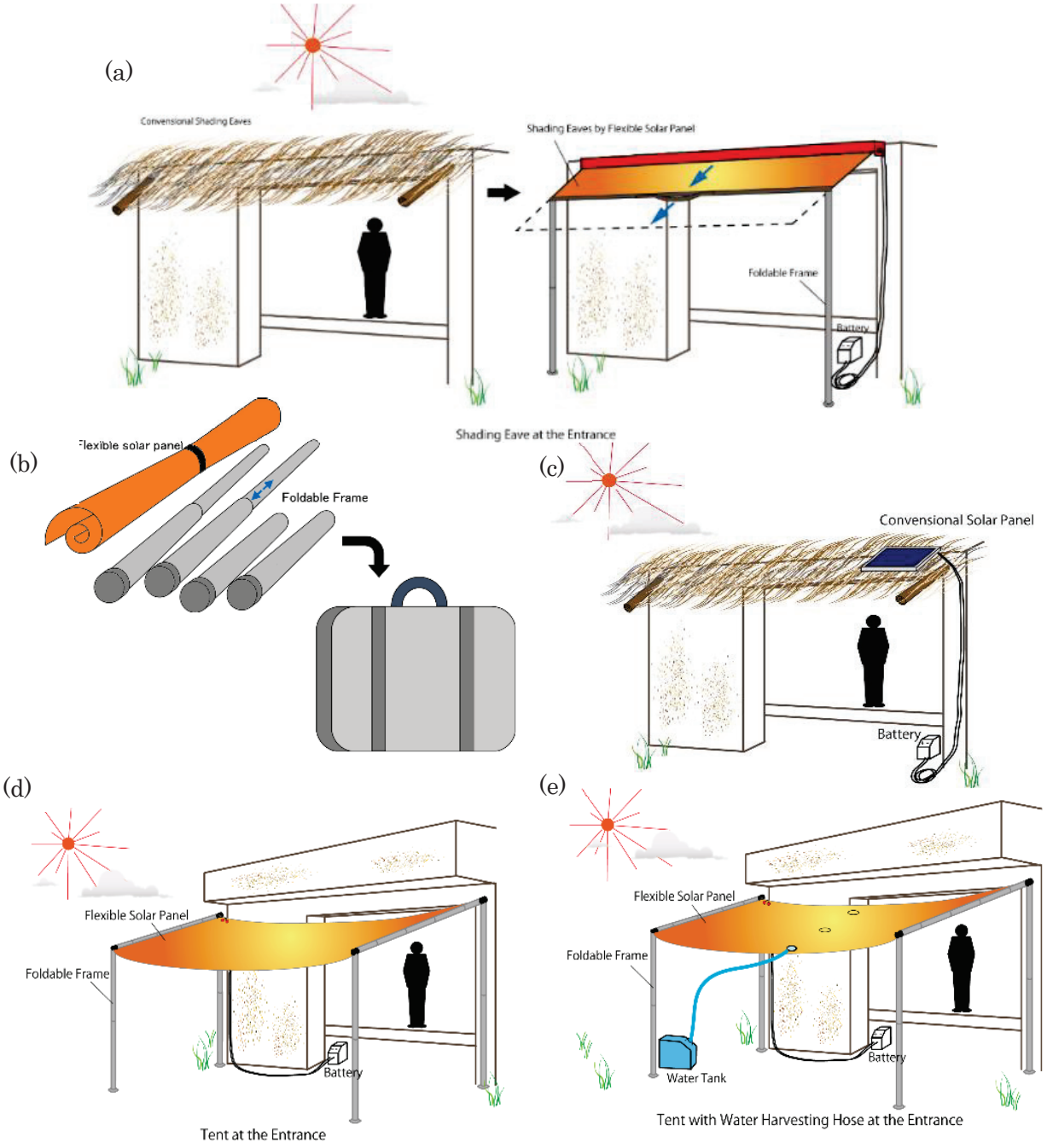


Fig. 2-7: Illustrations used in the main survey; (a) shading eave application, (b) concept of foldable frame and flexible solar panel, (c) conventional solar panel, (d) tent application, and (e) tent application with water harvesting system.

Based on all observations in pilot survey, attributes and levels for the main survey were customized (summarized in table 2-3). All of the choice sets are randomly selected from the combinations of levels. Villagers made a ranking from 3 choice sets including status quo. Here, the status quo is the set of level 1 in each attribute.

Table 2-3: List of Attributes and Levels for new PSHS design in the main survey.

Attributes	**Levels**	
System design of panel and battery	Level 1	Separated, fixed panel and heavy battery (30kg)
	Level 2	Combined, panel and light battery (totally 5kg)
Panel size and feature	Level 1	Hard and conventional (Top glass and aluminum frame)
	Level 2	Flexible panel, good for shading eave extended from roof (10 feet2)
	Level 3	Flexible panel & foldable frame, good for tent (30 feet2)
	Level 4	Flexible panel & foldable frame, good for tent (30 feet2) plus rain water harvesting
Translucency	Level 1	100% cut (such as black sheet)
	Level 2	50% cut (such as sun glasses)
Chargeability in cloudy weather	Level 1	No (0 % of sunny day)
	Level 2	Yes (30% of sunny day)
Lifetime	Level 1	5 years
	Level 2	10 years
	Level 3	15 years
Price (one time payment)	Level 1	10000 Rupees (100 USD)
	Level 2	20000 Rupees (200 USD)
	Level 3	40000 Rupees (400 USD)
Print design on the panel surface	Level 1	Nothing
	Level 2	Hindi symbol
	Level 3	Family picture

2-3-4: Result analysis

In the main survey, we were able to take 220 interviews to heads of household on the following intervention and procedure:

a. Treatment group: Enumerators explain the functions of PV includes conventional PV and organic PV. The feature of flexible, foldable, use as tent and rain water harvesting facility are shown by illustrations before the interview. A total number of respondents is 109, detailed number of respondents is shown in table 2-4.

Table 2-4: Village breakdown by number of respondents (Treatment group)

Name of Village	No. of respondents
Bar	12
Dond 1	32
Dond 2	17
Loridkhar	16
Mohda	18
Gudagarh	14
Total	109

b. Control group: Enumerators interview villagers without any illustrations to explain the functions of organic PV as well as conventional PV. A total number of respondents is 111, detailed number of respondents is shown in table 2-5.

Table 2-5: Village breakdown by number of respondents (Control group)

Name of Village	No. of respondents
Amgaon	10
Dheba	27
Dhebi khar	23
Kauhabahra	16
Dond 2	12
Rawan	23
Total	116

Comparison of the two groups can reveal an impact of visual information, simultaneously, relation of their understanding toward organic PV and choice making can be analyzed.

Collected data was converted to average marginal component effect [31, 32], through equation (1).

$$y_{itj} = \beta_0 + \sum_{l=1}^{7} \sum_{d=2}^{Dl} \beta_{ld} \times a_{itjld} + u_{itj}. \quad (1)$$

Where, a_{itjld} = dummy variable (for the l–level of an attribute l of a policy j in task t of a respondent i), Dl = number of level of an attributes, β_{ld} = coefficient, u_{itj} = error terms, and $y_{itj} \in \{0, 1\}$ = a choice indicator variable. Their preferences are digitized into two choice probabilities; internal choice probability and external choice probability. Internal choice probability-policy is preferred to the alternative policy. It compares ranking between two proposed choice profile, wherein if ranking 1 is assigned to an alternative with the higher ranking, and 0 otherwise, irrespective of the ranking of the status quo. External choice probability-policy is preferred to the status quo. It compares the ranking between the status quo and other two alternatives. If 1 is assigned to any choice set, then it reveals a higher ranking than that of the status quo, and 0 otherwise. We can say that if the ranking of the status quo is the highest or lowest, both two alternative choice sets assign 0 or 1. Numerated results of treatment group are shown in Fig. 2-8, and that of control group is shown in Fig. 2-9.

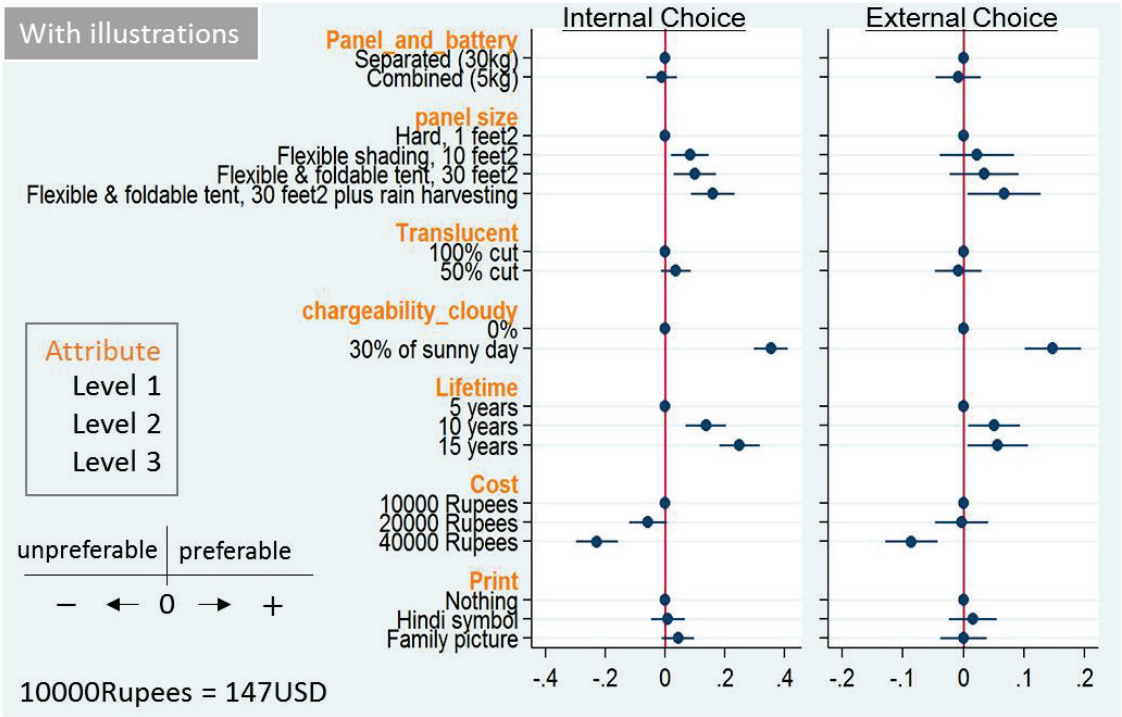


Fig. 2-8: Choice probability (result of treatment group).

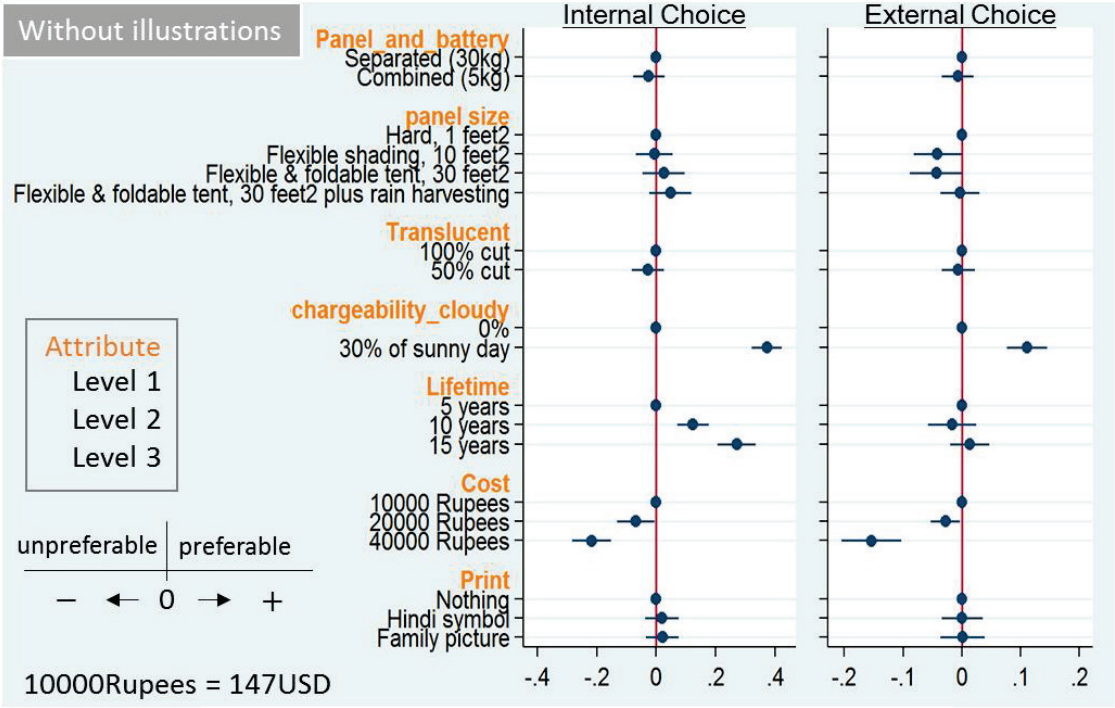


Fig. 2-9: Choice probability (result of control group).

These results indicate that;

- There is no significant difference between internal and external choice probability, tendencies of their choice are similar in both choice probabilities.
- Their choices are consistent on cost and lifetime; cheaper and longer lifetime are always preferred.
- Chargeability in cloudy weather has considerable impact. An impact level of 0% to 30% and that of 30% to 60% aren't same, but higher tolerance against weak irradiation is obviously preferred.
- Regarding panel size, we got drastic difference between treatment group and control group, flexible panel for shading eaves, foldable tent and tent plus water harvesting system are liked by treatment group. This results from the illustration impact and the enhancement of understanding level.
- Other attributes (system design of panel and battery, translucency, print design on the panel surface) don't have strong impact on their choices.

The evidences we obtained are reflected back to product design. The most preferred product design is PSHS with flexible panel & foldable frame, good for tent (50pW, 30 ft^2) plus rain water harvesting function (depicted in Fig. 2-10(a)). Although it is nonsense to estimate the total cost because OPV still haven't been industrialized and other parts need original design, we dared to estimate the present cost and weight. Estimated cost is 1,580USD + battery and estimated weight is 15.9 kg + battery (shown in Fig 2-10(b)). OPV has to be large because of low energy density (approx. 17pW/10ft^2), but this demerit could be a merit by applying it to rollable sheet.

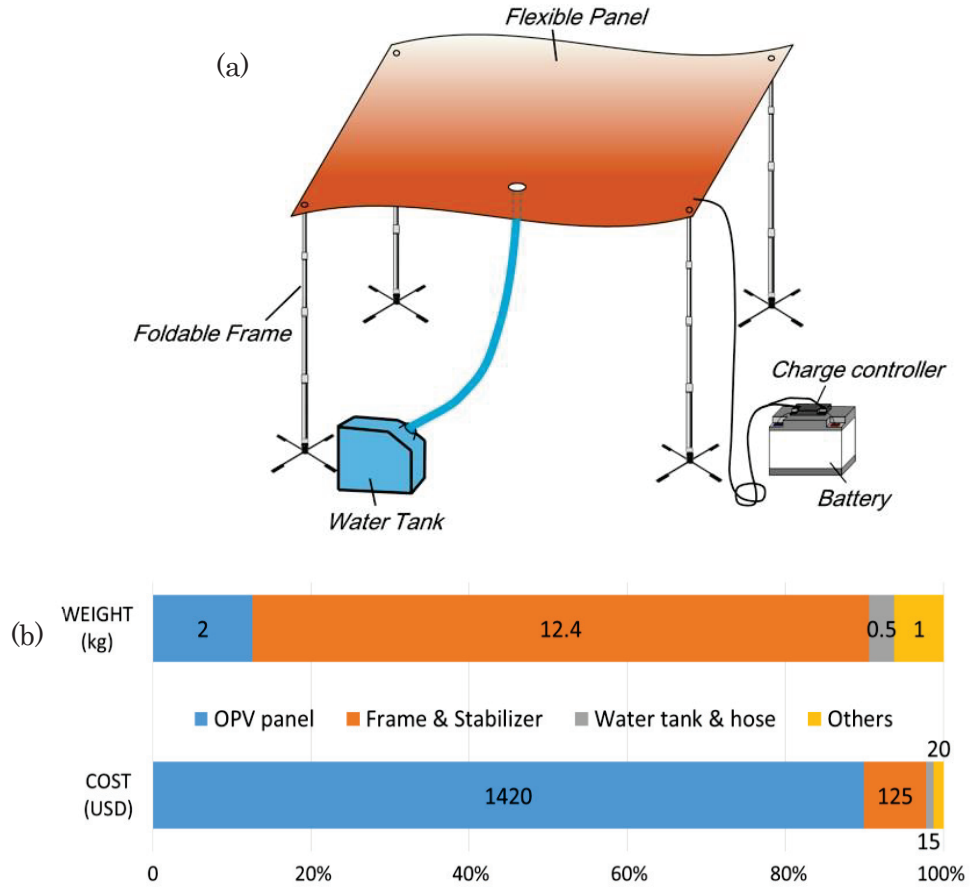


Fig. 2-10: (a) Proposed PSHS; tent application with rollable sheet OPV, foldable frames and rain water harvesting function, and (b) Estimated cost and weight breakdown without battery

Technical challenges of OPV for the tent application are;

(1) Tradeoff between the robustness of panel and thinness for flexibility with passivation film.

(2) Degradation of power generation by repetition of folding/rolling and aging of panel in use as a carriable PV.

(3) Inevitable influences of external factors on the cell in practical use environment such as temperature, humidity and irradiance.

(4) Power conversion efficiency improvement to maximize the usable time to charge the battery (to keep a charging voltage condition).

Since OPV is comparatively light, thin, and flexible, they don't have physical restrictions for installment. However, the surface of PV can be heated up to 60 ^{o}C in the outdoor use, that is, it is necessary to expand the range of usable temperature especially in elevated temperature range. Molecular design to optimize the optical absorption may promote outdoor applications as well as indoor ones.

Once a new technology is introduced in a village, there must have various impacts affecting their culture and society. Measuring those impacts is not easy and requiring long term monitoring. Nevertheless, it's still worth considering various aspects of quality of life. Table 2-6 describes some of quality of life index and possible impacts by desired PSHS referring to quality of life index [33, 34].

Table 2-6. Quality of life index and possible impacts by designed PSHS

Index	Impact (very good: ◎, good: ○, no impact: =, bad:△)
Health (life-expectancy, disease, injury etc.)	(○) There is less number of toilet, bathroom and washing place. New product could solve their water and sanitary problems through water harvesting system with a water purifier.
Employment and working condition	(○) Their working place is basically in farming land. They have to work under strong sunlight especially in summer season. Tent type solar system can give some shading for them if it is portable and lightweight. Thus, working place can be improved. New product may create new materials flow, which can also increase the chance of employment.
Satisfaction of Leisure	(=) An effective way to promote a leisure aspect is to design more artistic surface of the panel since they use many tents or curtains to decollate the place in festivals or parties. Colorful or highly designed flexible panels with organic PV can get people's preference.
Satisfaction of income and consumption	(=) Solar water pump can help their agricultural work and increase their income, but the new product with organic is not good at operating such system which requires large capacity of energy (1kW~).
House and living condition	(◎) Water harvesting system can remove their burden to pump-up water from a well and to wash clothes at dirty ponds. Harvested water can be used for their livestock too. Tent type application is available even in front of or inside of the house for shading.
Educational situation	(○) Lighting for study or homework will be available by the product. Also they can easily see and touch the real product, that is, they understand how it is operated. Their curiosity about these technology will work positive for the future.
Quality of family relation	(=) Lighting at night or dinner time probably can make happier family relation.
Quality of community life	(○) Social trust in the villages is quite high and there is very less number of trouble in the community. Even if some portable products is installed in front of the house, robberies never happen. Also tent type or shading eaves type can provide spaces for taking a rest and communication with neighbors.
Equality and freedom of social class	(△) As far as we observed, we didn't see any inequality of social class. Their trust with each other are so strong that they are willing to help neighbors in all villages. However, although it is not a matter of social class, there exists a gap of income even in the same village. In our survey, possession rate of PSHS is 37.4%, which might be from difference of income. If they start to introduce new products, the possession gap possibly increases.

2-4: Motivation to organic circuit design and application

OPV conversion efficiency have grown in recent year (shown in Fig. 2-11) and reached to 10% level. However, the growth of conversion efficiency starts being saturated and there is less hope to overcome the conversion efficiency of conventional PV. A possible way for OPV to enter the PV market is innovate the applications that use the maximum advantage of OPV features. As observed in our survey, flexibility, designability, light-weight (portability) can get users' preference. But this is just a case when OPV and conventional PV have the same performance level. Simply, only replacing the conventional solar panels with organic solar panel is nonsense and unattractive.

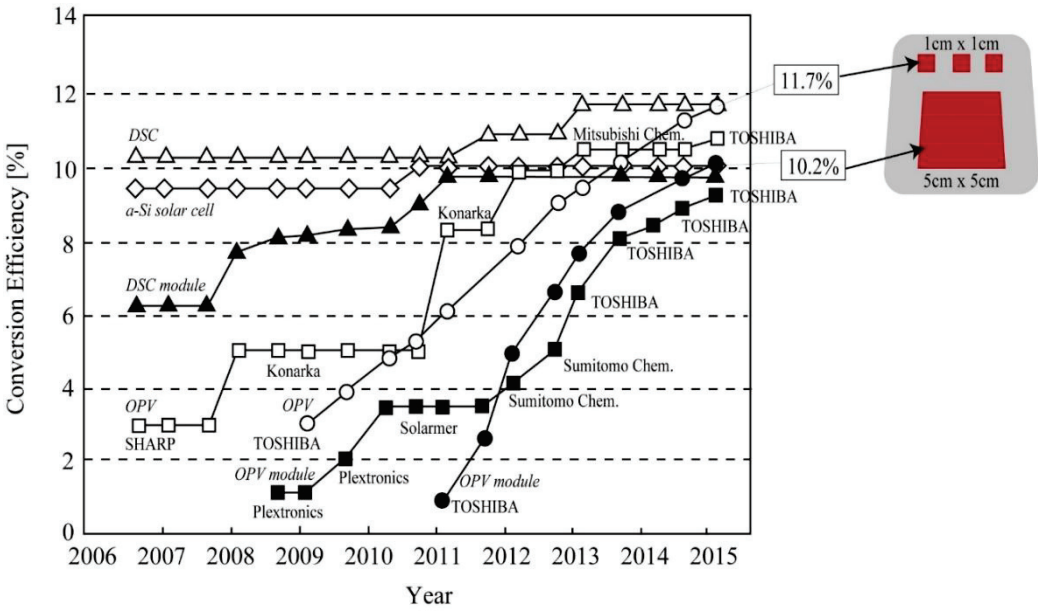


Fig. 2-11: Conversion efficiency growth of thin film PV [35].

To make the best use of organic material property, it is important to integrate functions on a sheet by flexible devices as much as possible, which is conceptualized by NEDO (New Energy and Industrial Technology Development Organization) [14] as flexible multi-functions device. In general, solar cells are connected in series and in parallel and balanced to keep sufficient voltage and current since generation voltage of the cell is determined by the magnitude of the photoelectric effect and current of the cell is dependent on cell area. Even for organic solar cell with low conversion efficiency, it is effective to increase the size of the panel and/or boost the voltage by a converter circuit. If the boost

circuit can be configured with organic devices, organic solar cells and organic circuit can be formed on a flexible sheet together as conceptually depicted in Fig. 2-12. It can be said as “system on a sheet”.

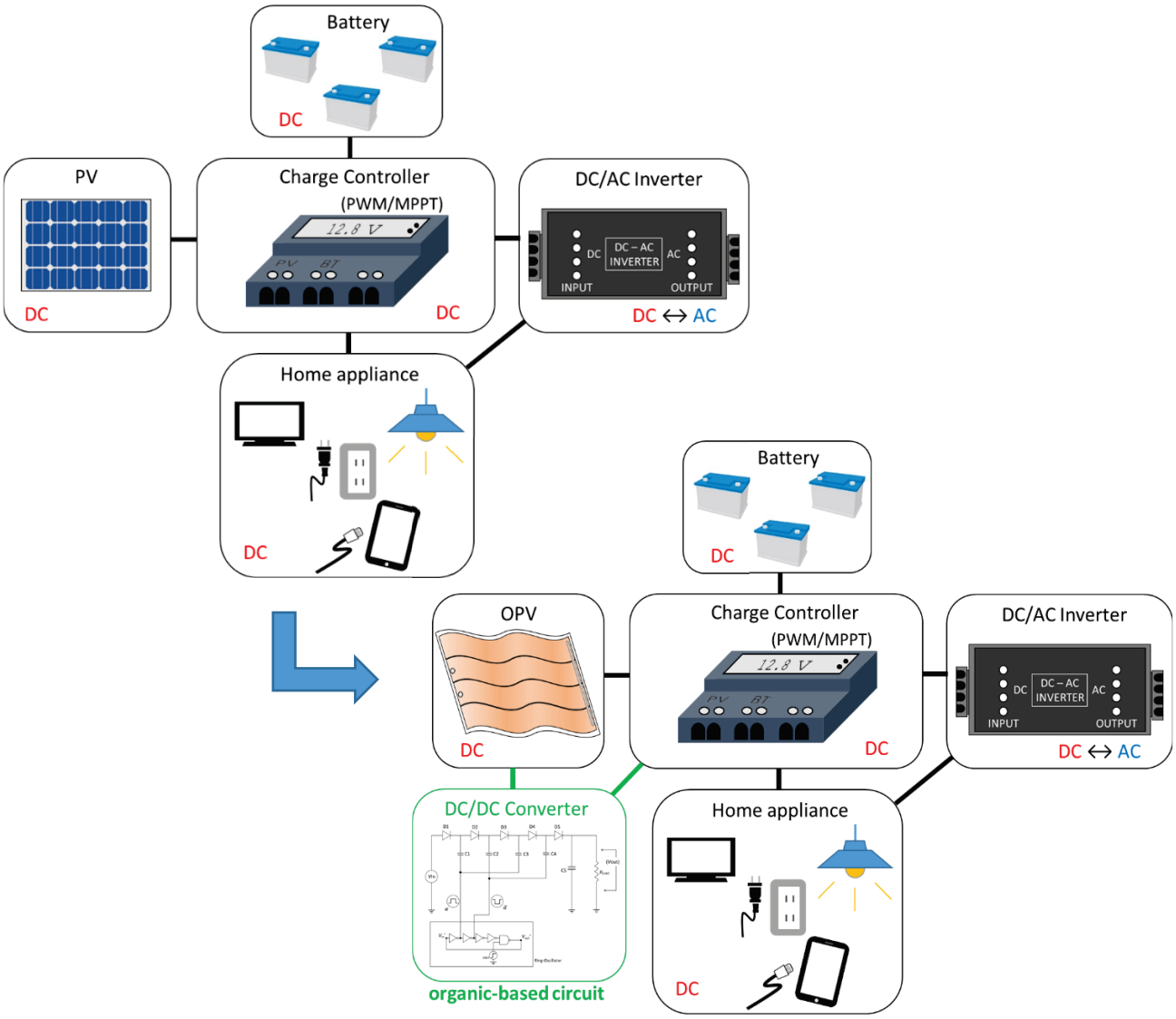


Fig. 2-12: Concept of circuit-assisted use of OPV for PSHS.

There are many types of converters that utilized in power electronics. But applicable converter with organic based circuit is limited because most of power conversion circuit uses high speed switching which is not suitable for organic devices. A possible organic converter circuit is Dickson charge pump (DCP) DC-DC boost circuit [36]. DCP circuit is feasible for organic-based circuit because it can reduce the number of complicated passive elements such as inductors. For driving the pumping system in DCP, clock design is necessary. Two clock phase α and $\bar{\alpha}$ is used to pump up charges at each stage.

One of the ways to generate a square-wave clock signal is using a ring-oscillator. Ring oscillator consists of NOT gates. The NOT gate includes positive and negative type transistor, which is called CMOS inverter. Fig. 2-13 shows circuit diagram of 5-stage DCP circuit connected to 5-stage ring oscillator as a signal generator. Device modeling and analysis of OFETs in chapter 3 to 6 are all for simulating this signal generating ring oscillator.

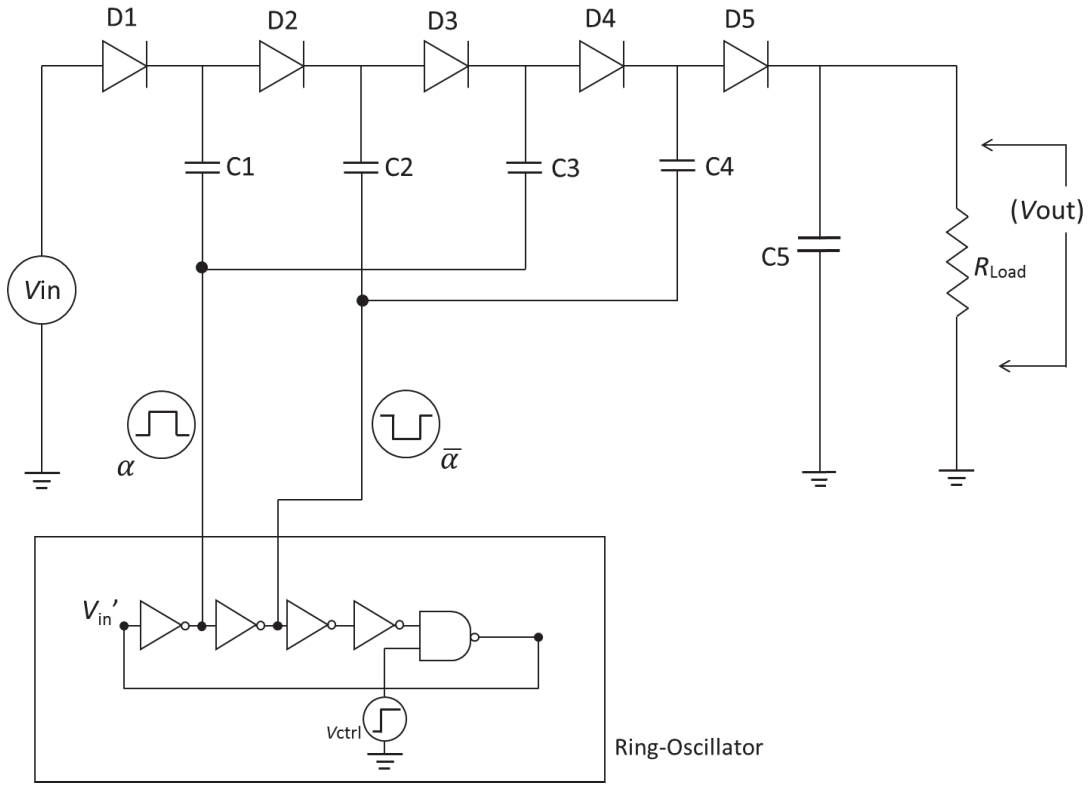


Fig. 2-13: Circuit diagram of Dickson charge pump DC-DC converter connected with ring-oscillator works as wave form generator.

Chapter 3

Device Physics of OFETs

3-1: MOS (Metal-Oxide-Semiconductor)

3-1-1: MOS structure

MOS (Metal-Oxide-Semiconductor) structure is, as literary, a junction structure of Metal layer, Oxide layer and Semiconductor layer shown in Fig. 3-1(a). MOS structure is called in circuitry as MOS diode or MOS capacitor as shown in Fig3-1(b). MOS is the most important structure to drive MOSFET. Performance of MOSFET is quite dependent on the junction between semiconductor and insulator, therefore, silicon MOS consists silicon as a semiconductor, oxide silicon (SiO_2) as an insulator, and doped silicon or conductive material as a metal to realize promising junctions.

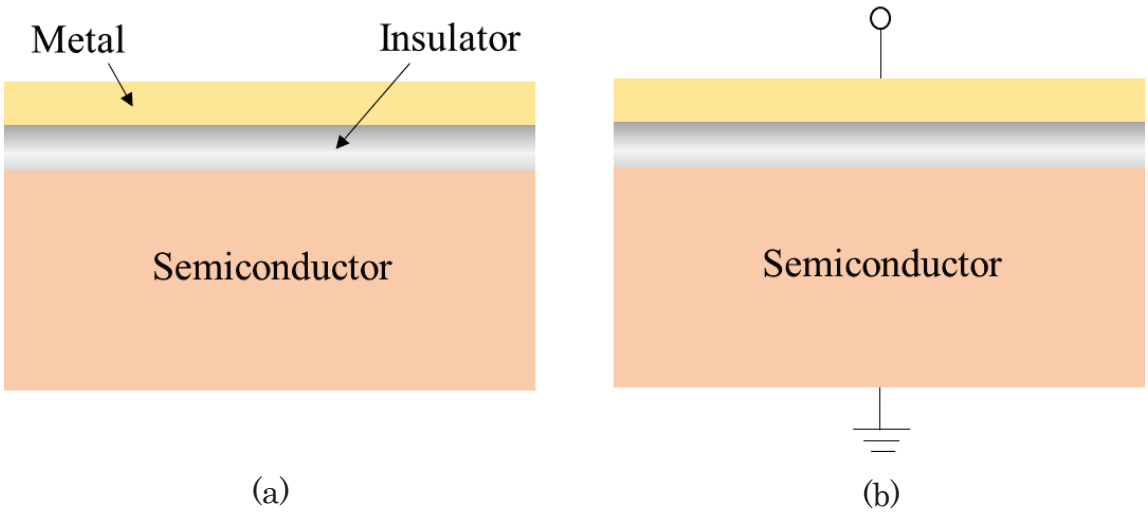


Fig. 3-1: (a) MOS structure and (b) MOS diode.

Here considers a case of applying voltage to MOS diode (p-type silicon MOS). When a voltage $V_1 =$ 0V, silicon bulk and surface is kept as p-type and the capacitance C_0 of this MOS diode is calculated as $C_0 \propto 1/d_1$, where d_1 is the thickness of insulator depicted in Fig. 3-2 (a) and (d).

Once a voltage V_2 is applied to the electrode, holes near the surface of p-type semiconductor are driven out and depletion layer d_2 is appeared just below the insulator as shown in Fig. 3-2 (b) and (e). Since the depletion layer has a high resistance, it can be regarded as a part of insulating area

qualitatively. Assuming the permittivity of silicon and insulator are similar (differ in real), the capacitance C_1 in this case is written as $C_1 \propto 1/(d_1 + d_2)$.

Applying larger voltage V_3 ($>V_2$), minority carriers intrinsically existing in p-type semiconductor are induced at the thin area just under the gate metal as shown in Fig. 3-2 (c). This area is called inversion because electrical p-type semiconductor is partially inversed to n-type. In the inversion condition, the capacitance becomes C0 because the distance between gate metal and inversion is d1 as shown in Fig. 3-2 (f).

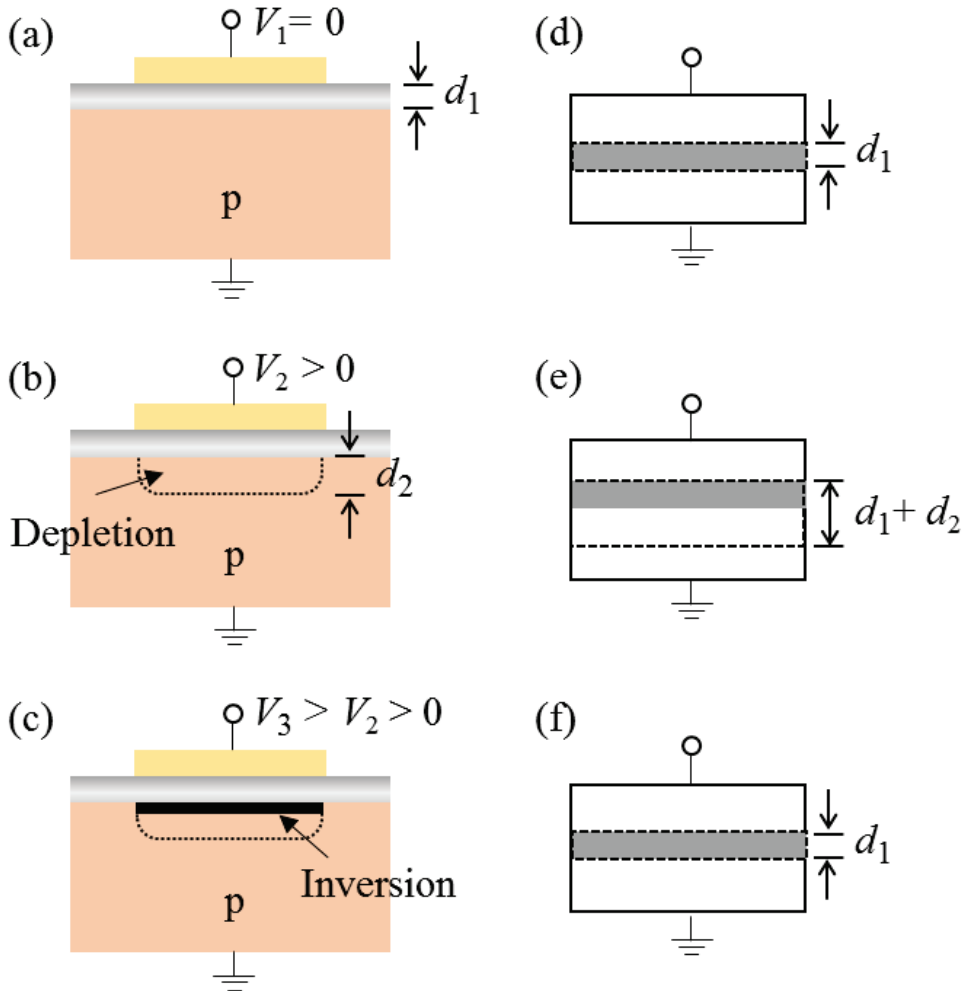


Fig. 3-2: Depletion and inversion condition of MOS capacitor.

Similar phenomena occurs in n-type semiconductor when the applied voltage is negative. That is, the minority carrier: hole is induced at the surface and forms p-type inversion in the high voltage condition.

3-1-2: MOS operation mode

In order to make it easy to understand the behavior when voltage is applied to the MOS structure, here considers an ideal MOS structure (p-type semiconductor) without three effects of work function difference, residual charge and mirror effect.

First, when a negative voltage V_1 is applied to the metal side, a difference of qV_1 occurs between metal and semiconductor at the Fermi level, and the band diagram becomes as shown in Fig. 3-3 (a). On the semiconductor surface, the valence band energy E_V approaches the Fermi level E_F, and the hole density becomes higher in the surface layer than that in the bulk. As shown in Fig. 3-3 (a), holes are induced on the surface by electrostatic induction. This condition is called accumulation.

Next, when a positive voltage is applied to the metal side, the energy band diagram is opposite to the case of accumulation as shown in Fig. 3-3 (b). When the positive voltage V_2 is not so large, the bending of the band is small, and on the semiconductor surface, due to the positive voltage applied to the surface, holes are driven out of the surface as shown in Fig. 3-3 (b). That is, a depletion layer is generated. This condition is called depletion.

Furthermore, when a larger positive voltage V_3 ($>V_2$) is applied to the metal side, the conduction band edge energy E_C approaches the Fermi level E_F very closely as shown in Fig. 3-3 (c) on the surface where the depletion layer is formed, Conduction electrons are induced on the semiconductor surface, and the surface region is inverted to n-type. This region is an inversion layer, and this condition is simply referred to inversion.

As described above, in the MOS structure, three states of accumulation, depletion, and inversion appear depending on the applied voltage to the surface. That is, in the MOS structure, by changing the electric field, not only the resistivity of the semiconductor surface but also even the conduction type can be changed, the conduction characteristics of the surface can be largely changed. These phenomena are substantially dependent on the dopant materials and its density.

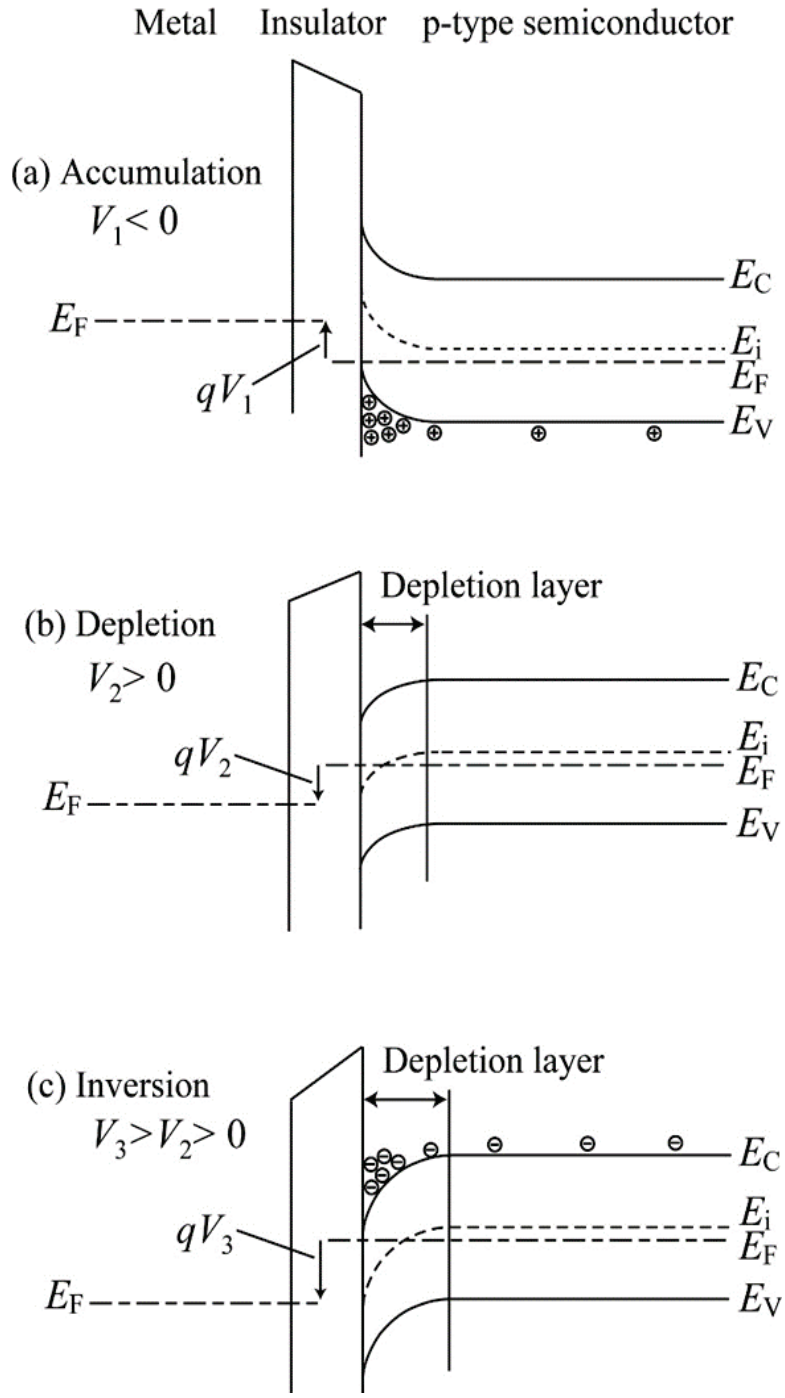


Fig. 3-3: Energy band diagram of MOS structure in three conditions: (a) Accumulation, (b) Depletion, and (c) Inversion.

The relationship between the depletion layer generated by applying gate voltage V_g, the potential $\varphi(x)$ within the width W_D (depletion layer width) and the surface potential $\varphi_s(x)$ in the case of the p-type semiconductor is explained below.

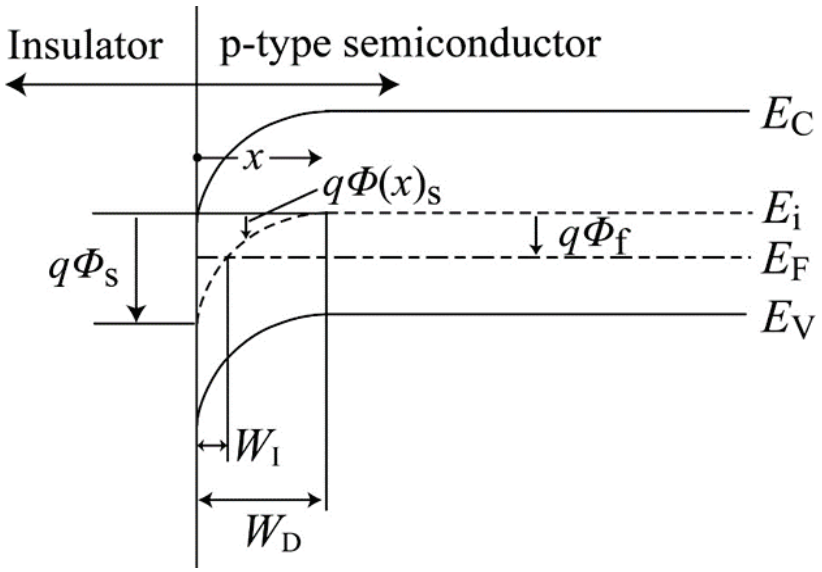


Fig. 3-4: Relation of surface potential, depletion width, and inversion width in the energy band diagram of MOS structure.

The potential $\varphi(x)$ in the depletion layer shown in Fig. 3-4 can be obtained by the following Poisson equation;

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_{si}} . \tag{3-1}$$

Here, ρ (x) is calculated by using hole density p, conduction electron density n, donor density N_d, and acceptor density N_a as;

$$\rho(x) = q\left(N_d - N_a + p - n\right). \tag{3-2}$$

Under no inversion condition,

$$N_d = p = n = 0 \tag{3-3}$$

is completed in the depletion layer. Equation (3-1) simplified as;

$$\rho(x) = -qN_a . \tag{3-4}$$

Since the value of the potential $\varphi(x)$ and its change rate $d\varphi(x)/dx$ are also zero at the depletion layer edge ($x = W_D$) as the boundary condition,

$$\phi(W_D) = 0, \left.\frac{d\phi(x)}{dx}\right|_{x=W_D} = 0 \tag{3-5}$$

is obtained. Using equation (3-4) and (3-5) in (3-1), φ(x) becomes;

$$\phi(x) = \frac{qN_a}{2\varepsilon_{si}}\left(W_D^2 - 2xW_D + x^2\right) = \frac{qN_a}{2\varepsilon_{si}}W_D^2\left(1 - \frac{x}{W_D}\right)^2. \tag{3-6}$$

From Fig 3-4, since the potential at x = 0 is the surface potential, φ_s is calculated as;

$$\phi_s = \frac{qN_a}{2\varepsilon_{si}}W_D^2. \tag{3-7}$$

Electric field E(x) is calculated as;

$$E(x) = -\frac{d\phi}{dx} = \frac{2\phi_s}{W_D}\left(1 - \frac{x}{W_D}\right). \tag{3-8}$$

Electric charge per unit area in depletion layer is written as;

$$Q_{dep} = -qN_aW_D. \tag{3-9}$$

Using a permittivity in oxide: ε_{ox}, an electric field at semiconductor surface: E_{Si}, electric field in oxide: E_{ox}, and Gaussian law,

$$\varepsilon_{ox}E_{ox} = \varepsilon_{si}E_{si} = -Q_{dep} \tag{3-10}$$

is obtained. Therefore, the potential in oxide layer φ(x) becomes;

$$\phi(x) = \frac{Q_{dep}}{\varepsilon_{ox}}x + c. \tag{3-11}$$

As the boundary condition, the potential at x=0 is φ_s. Thereby, φ(x) is obtained as;

$$\phi(x) = \frac{Q_{dep}}{\varepsilon_{si}}x + \phi_s. \tag{3-12}$$

Suppose the oxide thickness is t_{ox}, the potential at x=-t_{ox} is equal to V_G. Therefore, the relation of V_G, φ_s and Q_{dep} becomes

$$V_G = \phi_s - \frac{t_{ox}}{\varepsilon_{ox}} Q_{dep} = \phi_s - \frac{Q_{dep}}{C_{ox}} . \tag{3-13}$$

Here C_{ox} represents the capacitance of the oxide layer, written as;

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} . \tag{3-14}$$

When a larger gate voltage is applied to the MOS diode, an inversion layer is formed at the semiconductor surface as shown in Fig. 3-4, and the gate voltage V_G for just inverting the surface condition ($\varphi_s = 2\varphi_F$) is defined as the threshold voltage V_{th}.

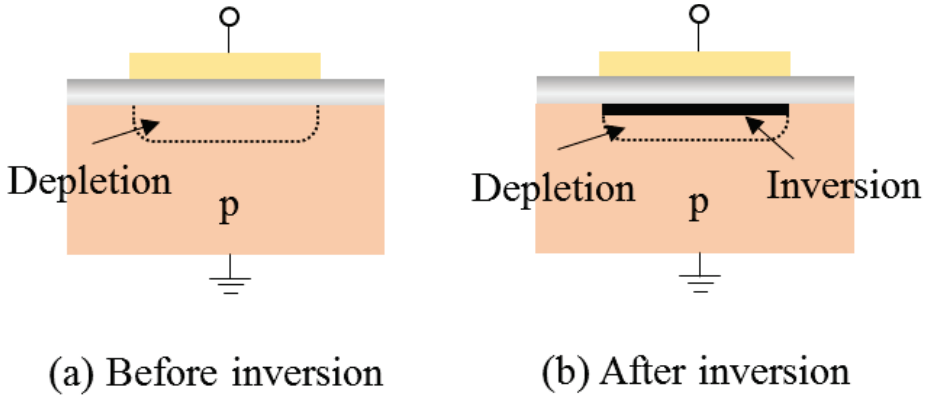


Fig. 3-4: Difference of before and after the inversion forming.

In the ideal MOS structure, the gate voltage V_G is written as;

$$V_G = \phi_s - \frac{Q_{dep}}{C_{ox}} . \tag{3-15}$$

For the real MOS structure, it needs to consider the flat band voltage V_{FB}. Then the gate voltage V_G is corrected as;

$$V_G = \phi_s + V_{FB} - \frac{Q_{dep}}{C_{ox}} . \tag{3-16}$$

In order to cause inversion, it is necessary that the surface potential φ_s is equal to twice the Fermi potential φ_F. After the inversion occurs, depletion width W_D becomes maximum value W_{Dmax} written as;

$$W_{\mathrm{Dmax}} = \sqrt{\frac{2\varepsilon_{\mathrm{si}}\phi_{\mathrm{s}}}{qN_{\mathrm{a}}}} = \sqrt{\frac{2\varepsilon_{\mathrm{si}}\left(2\phi_{\mathrm{f}}\right)}{qN_{\mathrm{a}}}} \,. \tag{3-17}$$

Substituting this W_{Dmax} to equation (3-9), electric charge density per unit in depletion layer Q_{dep} becomes

$$Q_{\mathrm{dep}} = -\sqrt{2\varepsilon_{\mathrm{si}} qN_{\mathrm{a}}\left(2\phi_{\mathrm{f}}\right)} \,. \tag{3-18}$$

Using above values, threshold voltage Vth can be calculated. When the inversion just starts, the relation $\varphi_{\mathrm{s}}=2\varphi_{\mathrm{f}}$ is satisfied. Substituting this relation $\varphi_{\mathrm{s}}=2\varphi_{\mathrm{f}}$ and equation (3-18) to equation (3-16), the gate voltage VG is written as;

$$V_{\mathrm{G}} = V_{\mathrm{th}} = 2\phi_{\mathrm{f}} + V_{\mathrm{FB}} + \frac{\sqrt{2\varepsilon_{\mathrm{si}} qN_{\mathrm{a}}\left(2\phi_{\mathrm{f}}\right)}}{C_{\mathrm{ox}}} \,. \tag{3-19}$$

If the substrate of the MOS is n-type semiconductor, electric charge density in depletion layer Q_{dep} is written as;

$$Q_{\mathrm{dep}} = qN_{\mathrm{d}}W_{\mathrm{D}} \,. \tag{3-20}$$

Therefore, threshold voltage Vth in the case of n-type substrate becomes

$$V_{\mathrm{th}} = -2\left|\phi_{\mathrm{f}}\right| + V_{\mathrm{FB}} - \frac{\sqrt{2\varepsilon_{\mathrm{si}} qN_{\mathrm{d}}\left|2\phi_{\mathrm{f}}\right|}}{C_{\mathrm{ox}}} \,. \tag{3-21}$$

In this case, in order to clarify the inversion with negative voltage, the Fermi potential is often given an absolute value symbol. As is apparent from the equations (3-19) and (3-21), the first term corresponds to the inversion layer and is the surface potential for strong inversion condition, the third term is the component corresponding to the depletion layer .

3-2: Operation principles of MOSFETs

3-2-1: MOSFET structure

A MOS transistor is generally called as field-effect transistor (MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor) because the device is operated by the action of electric field. This is currently the most important and popular passive element among LSI [1, 2. 3]. The structure of n-type MOSFET is shown in Fig. 3-5.

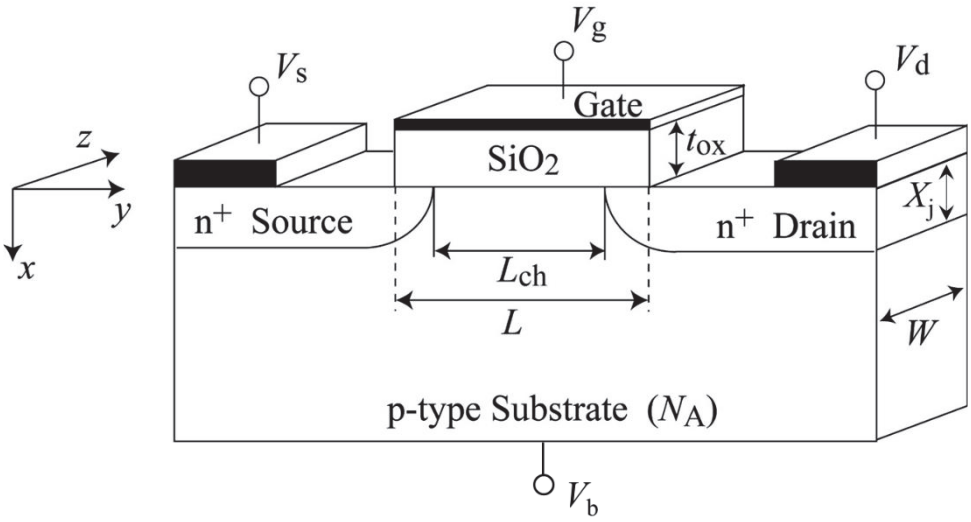


Fig. 3-5: Schematic structure of n-type MOSFET.

The MOSFET consists of a thin oxide film (SiO_2: thickness t_{ox}) on a semiconductor substrate, and a conductive layer called the gate electrode is on the oxide film. The p-type doped substrate is bonded to the bulk electrode. Also, the two regions heavily n-type doped with depth X_j are called source and drain. This is formed on both sides of the gate in the substrate. The region between the source and drain junctions is called the channel region. It has length L and width W. The mask length L_{mask} and mask width W_{mask} are different from L and W due to process variations. When a positive voltage is applied to the gate of the MOSFET, an n-type inversion layer is formed as described in the MOS structure. At this time, when a voltage is applied between the source and the drain, a current flows through the channel region. Since the magnitude of this current is determined by the number of electrons (holes for the case of p-type) induced by the gate voltage, the characteristics of the transistor are mainly controlled by the gate voltage. Also, MOSFETs have n+ source and drain regions unlike

MOS diodes. Therefore, the electrons forming the channel are supplied from the n+ region of the source and the drain. L_{ch} represents the length between the edge of source and drain region that is slightly different from L. MOSFETs are designed to have an overlap region intentionally under the gate to make it easy to form the channel.

3-2-2: Operation conditions

MOSFETs have three major operation regions; Cut off region, Linear region, and Saturation region. These three operation regions are explained below.

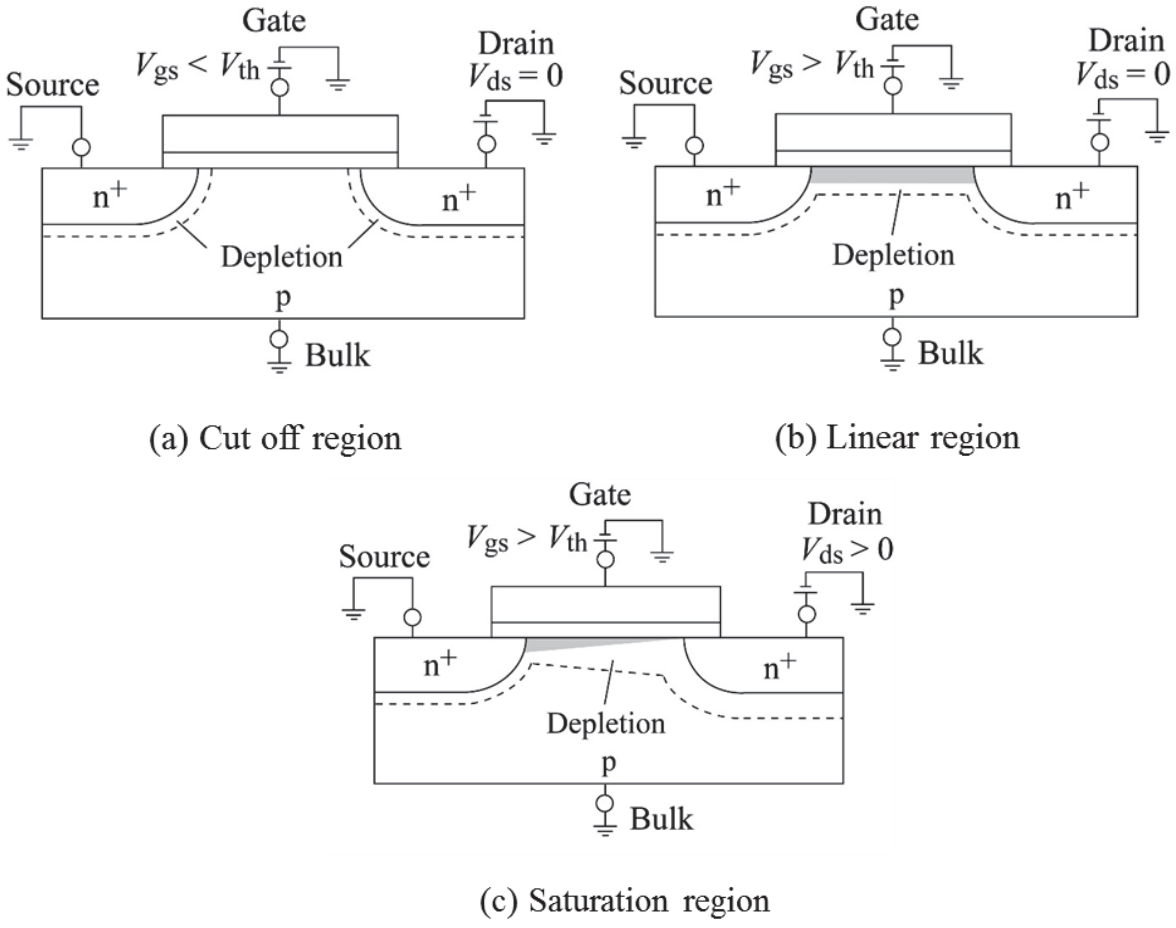


Fig. 3-6: Operation conditions of n-type MOSFET; (a) cut off region, (b) linear region, and (c) saturation region.

- Cut off region

If the voltage from source to gate (V_{gs}) is lower than the threshold voltage (V_{th}), the substrate just below the gate remains p-type as shown in Fig. 3-6 (a), and the source and drain are separated by the

reverse biased pn junction. Therefore, even if the voltage from source to drain (V_{ds}) is applied, the drain current (I_{ds}) doesn't flow. This operation region is called cut off region, and when considered as a switch, it's in the off state. However, even if the V_{gs} is lower than V_{th}, the substrate surface can be slightly inverted, the channel conductance becomes high and I_{ds} flows slightly. This state is a weak inversion state, that is, the case where the surface potential φ_s is between the Fermi potential φ_f and $2\varphi_f$. Since this region is below V_{th}, it is called sub-threshold (subthreshold) region. The current at this state is called subthreshold current or leak current.

- Linear region

When V_{gs} is equal to or higher than V_{th}, electrons are induced on the surface of the p-type silicon substrate with the gate oxide film interposed between as shown in Fig. 3-6 (b). Then the source and drain are connected by the inversion layer. That is, MOSFET is turned on. As a result, when a voltage is applied between the source and drain, induced carriers felt the electric field and are driven. Since carriers drift quickly in proportion to V_{ds}, I_{ds} increases in proportion to V_{ds}, hence this operating region is called linear region. Also, in this linear region the channel can be regarded as a resistance. At this state, in the inversion layer, electric field E_x (vertical to the channel) is larger than electric field E_y (parallel to the channel).

- Saturation region

As V_{gs} is fixed from the linear region and V_{ds} is further increased, V_{ds} becomes a reverse bias at the drain end as shown in Fig. 3-6 (c). Therefore, at the drain end of the substrate surface, a depletion region appears and the depletion width increases. Therefore, the inversion layer disappears at the drain end. This phenomenon is called pinch-off. At this pinch-off point, E_y is larger than E_x. As a result, most of V_{ds} is consumed between the edge of the channel and the drain end, and a large electric field is applied to this region. Therefore, electrons that flowed into pinch-off region are accelerated by the electric field, drift quickly and reach the drain. Even if V_{ds} is further increased from this state,

the electron concentration at the drain end doesn't change but only the depletion width increases. For this reason, the drain current has a constant value independent of V_{ds}. From such characteristics, this operation region is called saturation region. However, actual MOSFETs don't show complete saturation. In practice, I_{ds} gently increases with increasing V_{ds} and has drain conductance. Although it is saturated with respect to V_{ds}, the electron concentration in the channel can be controlled by V_{gs}. Therefore, even in saturation region, I_{ds} can be controlled by V_{gs}.

3-2-3: Current – Voltage characteristics (*IV* characteristics) of MOSFETs

Three operation regions explained in chapter 3-2-2 can be described in the *IV* characteristics of MOSFETs. Figure 3-7 (a) shows a typical I_{ds} - V_{ds} characteristics of MOSFETs. This I_{ds}-V_{ds} characteristics include linear region in which I_{ds} increases substantially in proportion to V_{ds}, saturation region where I_{ds} is determined by V_{gs}, saturation region which doesn't depend on drain voltage, and Cut off region where I_{ds} doesn't flow because V_{gs} is lower than V_{th}.

To obtain V_{th} from *IV* characteristics, I_{ds}-V_{gs} characteristics is useful. Figure 3-7 (b) shows a typical I_{ds}-V_{gs} characteristics of MOSFETs. There are multiple methods to extract Vth form Ids-Vgs such as constant current method, GME (gm extapolation) method and etc. A dominant current in subthreshold region is a diffusion current and that in inversion region is a drift current. The slope value $S=dV_{gs}/d(\log I_{ds})$ of subthreshold region ia used to indicate the switching property of MOSFETs. Theoretical limit value is 60mV/dec. for silicon MOSFETs and smaller value is more preferable for switching.

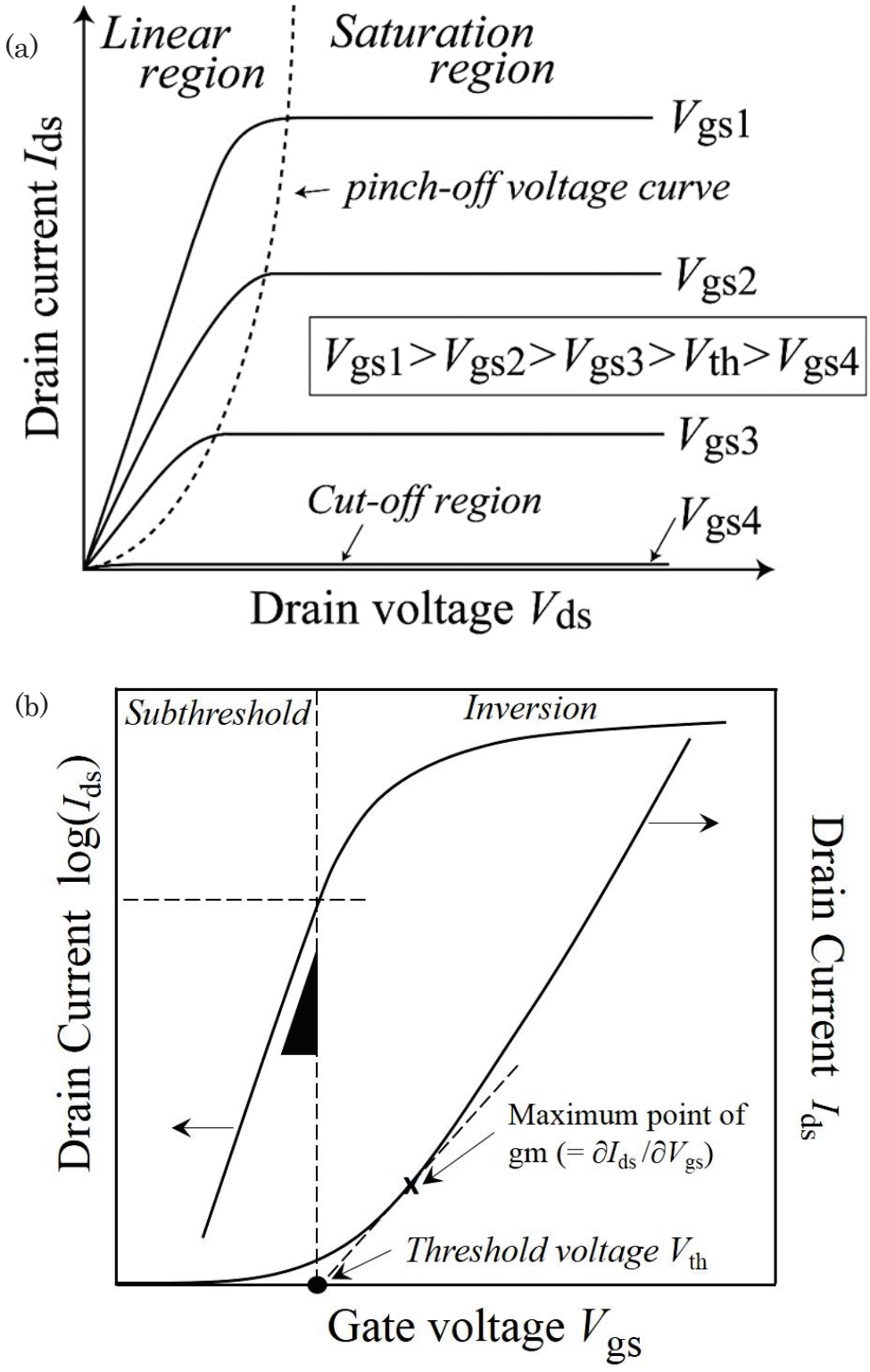


Fig. 3-7: Typical *IV* characteristics of MOSFETs: (a) I_{ds}- V_{ds} characteristics and (b) I_{ds}- V_{gs} characteristics.

Current equation expressing the operation of MOSFETs is deriven from here.

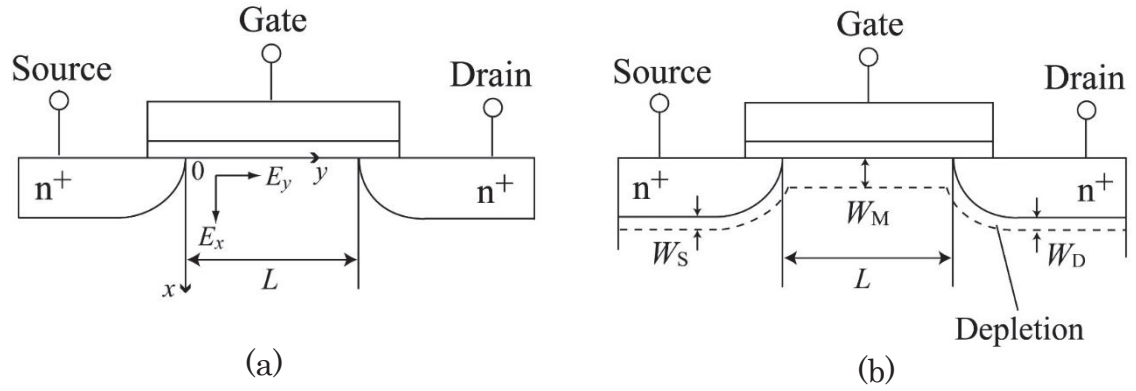


Fig. 3-8: Coordinates for characteristic analysis of MOSFETs; (a) x: vertical direction along the depth, y: horizontal direction along the channel, (b) depletion width.

As shown in Fig. 3-8 (a), the x axis is taken in the depth direction, the y axis is taken in the direction parallel to the channel, and the contact point on the surface of the source region and the channel region is taken as the origin. Also, let the electric field in the x direction dependent on the gate voltage be E_x, and the electric field in the y direction dependent on the drain electric field be E_y. Here, the structure under the gate is assumed to be an ideal MOS structure, and the mobility and the impurity concentration of the channel region are also fixed. Also assume that $E_x >> E_y$ (the electric field by the gate voltage is dominant). Consider Ex only for potential analysis. This assumption is true only when a condition;

$$L \gg W_S + W_D \tag{3-22}$$

is true, where L is the channel length, and W_S and W_D are the depletion widths of source and drain junction. When equation (3-22) is not satisfied, a short channel effect occurs, and the electric field E_y also influences the characteristics of MOSFETs. When equation (3-22) is satisfied, using the potential $\varphi(x)$, Poisson equation is written as;

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon_{si}}(N_d - N_a + p_p - n_p)\,. \tag{3-23}$$

This equation can be transformed to

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon_{si}}\{p_{p0}(e^{-q\phi(x)/k_BT} - 1) - n_p(e^{q\phi(x)-V_D)/k_BT} - 1)\}, \tag{3-24}$$

Where q is element charge, k_B is boltzman constant, T is temperature, N_d is donor density, N_a is acceptor density, p_p is hole density in p-type semiconductor, and n_p is electron density in n-type semicondutor. Here the value of n_p is influenced by the drain voltage V_{ds} and becomes

$$n_p = n_{p0}e^{q(\phi(x)-V_{ds})/k_BT}. \tag{3-25}$$

Here n_{p0} represets the initial vaule of electron density at equilibilium state. The reason of this change is that the energy band at drain side is bended by V_{ds} as shown in Fig. 3-9. Here the equation expressing the relation of Fermi level and potential;

$$E_i - E_F = q(\phi_f - \phi(x)) \tag{3-26}$$

needs to be changed to

$$E_i - E_F = q\{\phi_f + V_{ds} - \phi(x)\}. \tag{3-27}$$

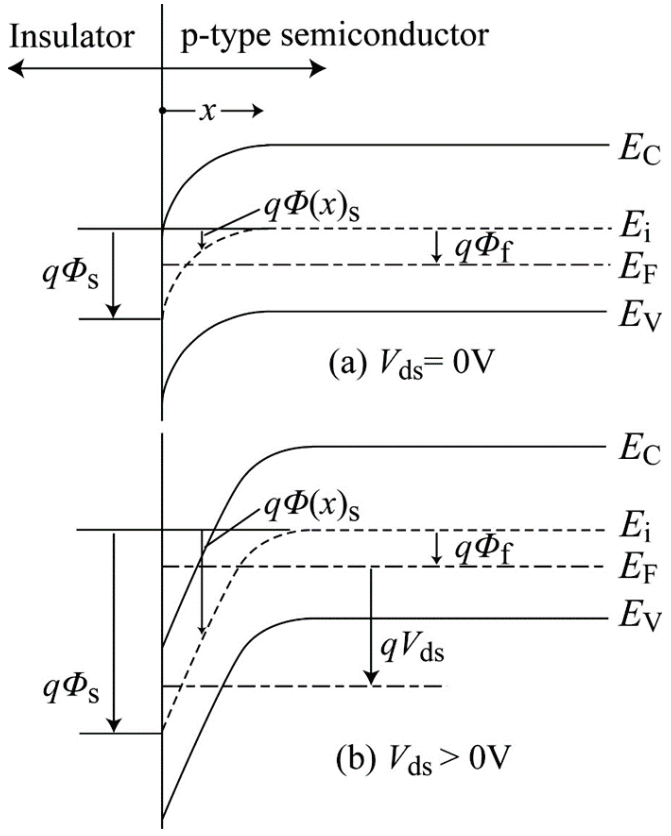


Fig. 3-9: Energy band diagram at the insulator and the p-type semiconductor;

Therefore, n_p is transformed as;

$$n_p = n_i e^{(E_F - E_i)/k_B T} = n_i e^{-q\phi f/k_B T} e^{q(\phi(x)-V_{ds})/k_B T} = n_{p0} e^{q(\phi(x)-V_{ds})/k_B T} . \quad (3\text{-}28)$$

Then the electric field E_x becomes

$$E_x = -\frac{\partial \phi(x)}{\partial x} = \pm \frac{\sqrt{2} k_B T}{q L_D} \cdot F\left(\frac{q}{k_B T} \phi(x), V_{ds}, \frac{n_{p0}}{p_{p0}} \right). \quad (3\text{-}29)$$

With Gaussian theory, The toal electric charge per unit area on the surface of the semiconductor (Q_S) is given by the electric field on the surface of the silicon crystal (E_S) as;

$$Q_s = -\varepsilon_{si} E_s = \mp \frac{\sqrt{2} \varepsilon_{si} k_B T}{q L_D} \cdot F\left(\frac{q}{k_B T} \phi(s), V_{ds}, \frac{n_{p0}}{p_{p0}} \right), \quad (3\text{-}30)$$

$$L_D = \sqrt{\frac{k_B T \varepsilon_{si}}{p_{p0} q^2}} , \quad (3\text{-}31)$$

where L_D is the debay length of holes. Function F is written as;

$$F\left(\frac{q}{k_B T} \phi(x), V_{ds}, \frac{n_{p0}}{p_{p0}} \right) = \left\{ \begin{array}{l} e^{-\frac{q}{k_B T}\phi(x)} + \frac{q}{k_B T}\phi(x) - 1 \\ + \frac{n_{p0}}{p_{p0}} e^{-\frac{q}{k_B T}V_{ds}} (e^{\frac{q}{k_B T}\phi(x)} - \frac{q}{k_B T}\phi(x) e^{\frac{q}{k_B T}V_{ds}} - 1) \end{array} \right\}^{\frac{1}{2}} . \quad (3\text{-}32)$$

Equation (3-30) is a general equation for the total charge Q_S. Since the total charge Q_S is the sum of the charge Q_B due to the depletion layer and the charge Q_I due to the inversion layer in the state where the inversion layer is generated. Therefore, Q_B is written as;

$$Q_s = Q_I + Q_B . \quad (3\text{-}33)$$

The depletion charge QB considering the depletion width in under the gate W_M is written as;

$$Q_B = -qN_a W_M = -\sqrt{2\varepsilon_{si} q N_a (V_{ds} + 2\phi_f)} . \quad (3\text{-}34)$$

This Q_B includes the influence of V_{ds}.

In the ideal MOS structure (V_{FB} = 0V), the relation of Q_s and V_{gs} is written as;

$$Q_S = C_0(\phi_S - V_G). \tag{3-35}$$

From equation (3-33) and (3-34), Q_I is written as;

$$Q_I = C_0(\phi_S - V_G) - Q_B = -(V_G - \phi_S)C_0 + \sqrt{2\varepsilon_{si}qN_a(V_D + 2\phi_f)}. \tag{3-36}$$

Suppose V(y) is the component affected by V_{ds} at an arbitrary point under the gate, considering that $\varphi_s = 2\varphi_f$ in the invertion condition, the surface potential at an arbitrary point under the gate is;

$$\phi_S(y) = 2\phi_f + V(y). \tag{3-37}$$

Consecuently, equation (3-36) is transformed to

$$Q_I(y) = -\{V_G - V(y) - 2\phi_f\}C_0 + \sqrt{2\varepsilon_{si}qN_a(V(y) + 2\phi_f)}. \tag{3-38}$$

Assuming that there is no influence of the depletion, equation (3-38) is approximated (gradual channel approximation) as;

$$Q_I(y) = -\left\{V_{gs} - V(y) - 2\phi_f - \frac{\sqrt{2\varepsilon_{si}qN_a(2\phi_f)}}{C_0}\right\}C_0. \tag{3-39}$$

When V_{FB} = 0V, from equation (3-19), equation (3-39) is transformed to;

$$Q_I(y) = -(V_{gs} - V(y) - V_{th})C_0. \tag{3-40}$$

Suppose a voltage drop by the drain current I_{ds} is ∂V, the channel resistance is written as;

$$R = -\frac{L}{W\mu_n Q_I(y)}, \tag{3-41}$$

then, ∂V becomes

$$\partial V = I_{ds}\partial R = -\frac{I_{ds}}{W\mu_n Q_I(y)}\partial y, \tag{3-42}$$

Where μ_n is an electron mobility. Therefore, the drain voltage Ids is written as;

$$I_{ds} = -W\mu_n Q_I(y)\frac{\partial V}{\partial y} = W\mu_n Q_I(y)E_y. \tag{3-43}$$

Here W represents the channel width. Equation (3-43) is transformed to

$$I_{ds}\partial y = -W\mu_n Q_I(y)\partial V \,. \tag{3-44}$$

Using equation (3-40) and integrating Q_I from the source end (y=0, V=0) to the drain edge (y=L, V=V_{ds}),

$$I_{ds}\int_0^L \partial y = W\mu_n C_0\left\{(V_{gs}-2\phi_f-\frac{V_{ds}}{2})V_{ds}-\frac{2}{3}\frac{\sqrt{2\varepsilon_{si}qN_a}}{C_0}[(V_{ds}+2\phi_f)^{\frac{3}{2}}-(2\phi_f)^{\frac{3}{2}}]\right\}. \tag{3-45}$$

This equation is simplified with some approximations as;

$$\begin{aligned} I_{ds}\int_0^L \partial y &= W\mu_n C_0\int_0^{V_D}(V_{gs}-V(y)-V_{th})\partial V \\ &= W\mu_n C_0\left\{(V_{gs}-V_{th})V_{ds}-\frac{1}{2}{V_{ds}}^2\right\}. \end{aligned} \tag{3-46}$$

After all, the current equation;

$$I_{ds}=\frac{W\mu_n C_0}{L}\left\{(V_{gs}-V_{th})V_{ds}-\frac{1}{2}{V_{ds}}^2\right\}. \tag{3-47}$$

is obtained. This equation is called gradual channel approximation formula. Since it is assumed that the inversion layer always occurs, it is not absolutely accurate in the weak inversion region ($\varphi_f < \varphi_s < 2\varphi_f$). However, as a whole this is a fairly accurate approximation.

Above equation can be explained by another way as follows. In general, setting that the carrier density is n, the speed of carriers is v, and the cross-section area of the current path is S, the current is written as $I = nqvS$. In the case of MOSFETs, when the carrier mobility is μ and the electric field between source and drain is E, the carrier velocity v is written as $v=\mu E$. When the channel width is W and the channel depth is d, the drain current I_{ds} is written as;

$$I_{ds} = nq\mu EWd = \mu Q_c WE\,, \tag{3-48}$$

Where $Q_c = nqd$, is the charge density in the channel per a unit area. On the other hand, the gate charge Q_G is the product of the voltage applied to the gate oxide V_{ox} and the gate oxide capacitance C_{ox}. Also Q_G is the sum of Q_c and the depletion charge density Q_B. Then,

$$Q_G = C_{ox}\cdot V_{ox} = Q_C + Q_B \tag{3-49}$$

is satisfied. Suppose the potential at the channel is φ_c, $V_{ox} = V_{gs} - \varphi_c$. Therefore,

$$Q_c = C_{ox} \cdot V_{ox} - Q_d = C_{ox}(V_{gs} - V_{th} - \phi_c). \tag{3-50}$$

Now assuming that the potential of the channel is the average value $\varphi_c = V_{ds} / 2$ between source and drain, and the electric field of the channel is $E = V_{ds} / L$, I_{ds} is written as;

$$I_{ds} = \mu Q_c W E = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds}. \tag{3-51}$$

When V_{ds} is much smaller than $V_{gs} - V_{th}$,

$$I_{ds} = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})V_{ds}. \tag{3-52}$$

This equation represents the current of linear region because I_{ds} is proportional to V_{ds}. When V_{ds} increased and satisfies $V_{ds} \geq V_{gs} - V_{th}$, the current is saturated. Then,

$$I_{ds} = \frac{\mu C_{ox}}{2} \frac{W}{L}(V_{gs} - V_{th})^2. \tag{3-53}$$

Although the above current equation (3-47), (3-51), (3-52), (5-53) uses many approximations, an error may occur but it is useful for understanding the current-voltage characteristics of MOSFETs.

3-2-4: Capacitance – Voltage characteristics (*CV* characteristics) of MOSFETs

There are measurements that can obtain device parameters other than *IV* characteristics. Capacitance-Voltage (*CV*) characteristic can extract MOS oxide thickness and oxide layer capacitance C_{ox} and can estimate the threshold voltage. Figure 3-7 shows *CV* characteristics of an ideal MOS diode. When a negative voltage is applied to the metal electrode, it is in the accumulation state. That is, the capacitance value becomes equal to C_{ox} irrelevant to the voltage. The reason why the capacitance value decreases around 0 V is that series capacitances are generated due to the accumulated charge. Next, when the voltage becomes positive, the diode becomes depleted, and the capacity of the depletion layer enters in series, so the total capacitance decreases. Further, when the bias voltage is increased, the capacitance becomes minimum, and when the inversion layer is formed on the surface, it increases again and becomes C_{ox}. This is the case of low frequency that the rate of generation and recombination of minority carriers can follow the change of the alternating signal. A voltage at the point of intersection of the minimum capacitance value and the extrapolation of CV curve in the depletion region becomes the threshold voltage.

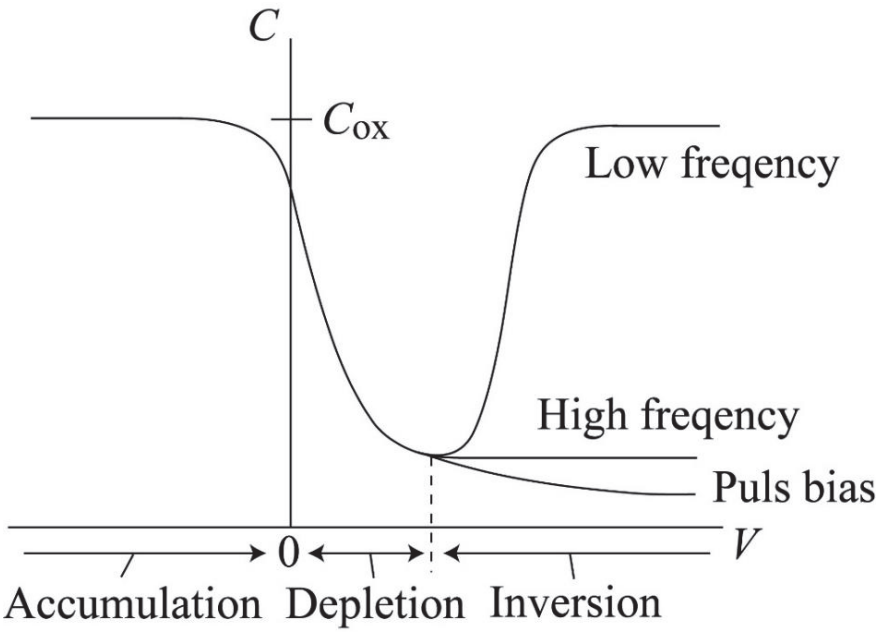


Fig. 3-10: Capacitance – Voltage (*CV*) characteristics.

Since the carrier can't follow the change of AC signal at high frequency, the end of the depletion layer expands and contracts due to the AC voltage, and the MOS capacitance C_{ox} becomes the series capacitance of the depletion layer. However, in the inversion state, the thickness of depletion layer scarcely changes, so the MOS capacitance has a constant value. In the case of MOSFETs, electrons immediately flow from the adjacent source region, the capacitance value increases even at high frequencies. When a pulse bias is applied, the depletion layer widely spreads, so the capacitance decreases. This state is called deep depletion. In the case of a general MOS diode, that is, when there is a difference of work function between a metal and a semiconductor, and when there is a fixed charge in the insulator, the entire *CV* characteristic moves in parallel. When there is a fixed charge in the insulator, the capacitance curve in the depletion region becomes gentle, and the frequency characteristic also differs from the ideal one. Also, if there is a leakage current in the insulator, the inversion charge doesn't stay, so *CV* curve shows deep depletion characteristics even when DC signal is applied [1, 3].

3-2-5: Carrier mobility of inorganic semiconductors

As described above, MOSFETs accumulate carriers with a vertical electric field caused by the gate voltage and accelerate carriers with a lateral electric field caused by the drain voltage. When a MOSFET is in the ON state, the channel part can be seen as a kind of resistance. The concept of capturing this resistance as a conductivity in reverse is a carrier mobility. Although carrier mobility is handled as a constant in the current equation explained in Chapter 3-2-3, actual carrier mobility is altered because carriers in the channel of MOSFET are scattered by the electric field, therefore, it will not be constant. Here, the meaning of carrier mobility in MOSFETs and its scattering mechanism are explained.

An electron mobility of substance is physically defined as;

$$\mu = \frac{q}{m}\tau \,, \tag{3-54}$$

where, q is element charge, m is effective mass, and τ is average relaxation time. However, this mobility is seldom used in discussing the carrier mobility of semiconductor devices. In semiconductor engineering, carrier mobility μ is defined by the following equation;

$$\frac{1}{\rho} = qn\mu \,, \tag{3-55}$$

where, ρ is resistivity, q is element charge of the carrier, and n is carrier density. That is, the carrier mobility which means the resistivity of the channel portion, is an important parameter for determining the electrical characteristics of semiconductors. This carrier mobility is determined by several scattering mechanisms. In crystalline silicon, there are phonon scattering, coulomb scattering and surface roughness scattering. Naming the mobility considering phonon scattering, coulomb scattering and surface roughness scattering as μ_{PH}, μ_{CB},and μ_{SR} respectively, the total carrier mobilityμ_0 is written following Matthiessen's law as;

$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} \,. \tag{3-56}$$

Matthiessen's law is applicable only when the factors independently occur from each.

- Phonon sccattering

Phonon scattering is based on an irregular potential change occurring in the crystal due to the lattice thermal vibration. The magnitude of scattering increases by temperature T. Figure 3-11 depicts a mechanism of phonon scattering schematically. According to a simple theory, the mean free path l is proportional to T^{-1}. On the other hand, the thermal velocity v_{th} is proportional to $T^{1/2}$. Therefore, the mean free time τ is proportional to $T^{-3/2}$ since $l=\tau v$. The mean free time is equal to the average relaxation time $<\tau>$, so $\mu=q<\tau>/m$ is satisfied. Then the mobility μ_{PH} in only the case when this scattering mechanism is dominant is given by the following equation;

$$\mu_{PH} \propto T^{-\frac{3}{2}}. \tag{3-57}$$

Using the effective electric field in the vertical direction E_{eff} caused by the gate voltage, μ_{PH} is expressed by the following equation;

$$\mu_{PH} \propto E_{eff}^{-0.3}. \tag{3-58}$$

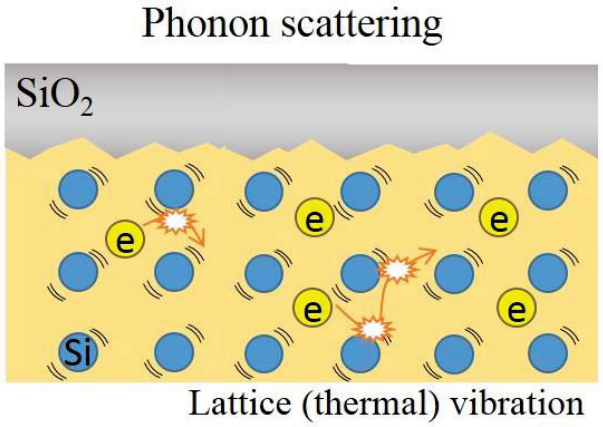


Fig. 3-11: Schematic mechanism of phonon scattering by lattice thermal vibration.

➢ Coulomb scattering

Scattering due to ionized impurities is called coulomb scattering. This is based on the phenomenon that the trajectory is bent by the coulomb force (Rutherford scattering) when carriers pass near the ionized impurity. Figure 3-12 depicts a mechanism of coulomb scattering schematically. As the carrier slowly passes through the vicinity of the ions, the impulse increases and the trajectory is greatly bent. In other words, l (mean free path) becomes shorter as v_{th} (thermal velocity) becomes smaller and impurity density becomes larger. Coulomb force acts on all substances, but it is much smaller than the electric field applied to the channel part. Therefore, coulomb scattering appears in the low electric field region. According to a simple calculation, l is proportional to v_{th}^4 / N. Therefore, the mobility in only the case when this scattering mechanism is dominant is

$$\mu_{CB} \propto T^{\frac{3}{2}} / N . \tag{3-59}$$

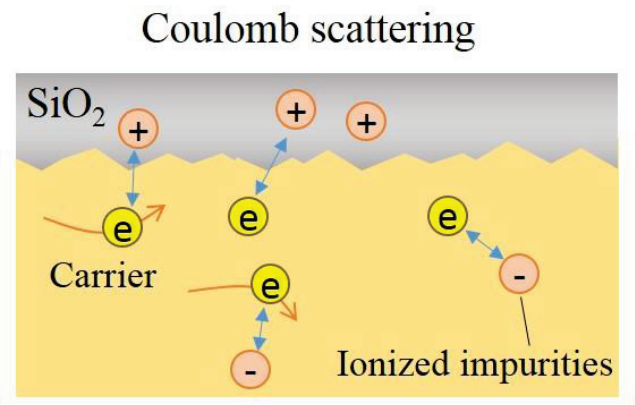


Fig. 3-12: Schematic mechanism of coulomb scattering by ionized impurities.

➢ Surface roughness scattering

Carriers passing through the channel are strongly attracted to the oxide end due to a strong electric field by the gate voltage. However, the interface between silicon and gate oxide is not smooth in atomic scale. Moreover, the conducting carriers don't always proceed in the horizontal direction. Therefore, as shown in Fig. 3-13, carriers are scattered by the rough surface. This is called surface roughness scattering. This effect becomes particularly important in the strong inversion condition. This

scattering mechanism relates to the distance to the carrier from the interface. The closer the distance is, the stronger the scattering due to the surface roughness becomes. Using the effective electric field in the vertical direction E_{eff}, it can be expressed by the following equation;

$$\mu_{\mathrm{SR}} \propto E_{\mathrm{eff}}^{-2}. \tag{3-60}$$

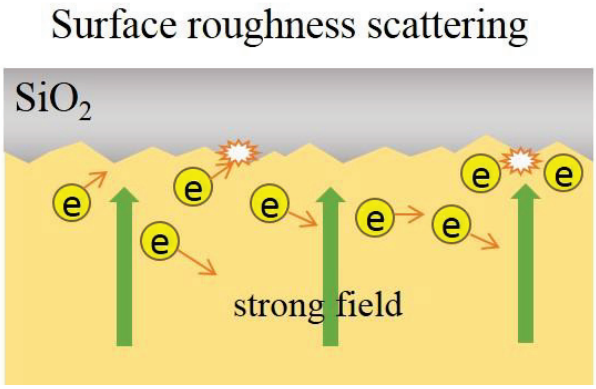


Fig. 3-13: Schematic mechanism of surface roughness scattering near the oxide.

As shown in equation (3-57) ~ (3-60), the effective electric field E_{eff} is important for the calculation of carrier mobility. E_{eff} is calculated by a following equation;

$$E_{\mathrm{eff}} = \frac{1}{\varepsilon_{\mathrm{si}}}\left(\gamma \cdot Q_{\mathrm{D}} + \eta \cdot Q_{\mathrm{I}}\right), \tag{3-61}$$

Where γ and η is 1.0 and 0.5 respectively for silicon MOSFETs, Q_{D} is the depletion charge and Q_{I} is inversion charge. E_{eff} is actually almost the same value to the vertical electric field $E_{\perp}$ at just blow the gate insulator.

Moreover, it is known that carrier mobility has universality as a function of E_{eff} ($E_{\perp}$) which is almost proportional to the gate voltage [2, 4, 5] shown in Fig. 3-14. The universality can be observed under the low field condition in the lateral direction.

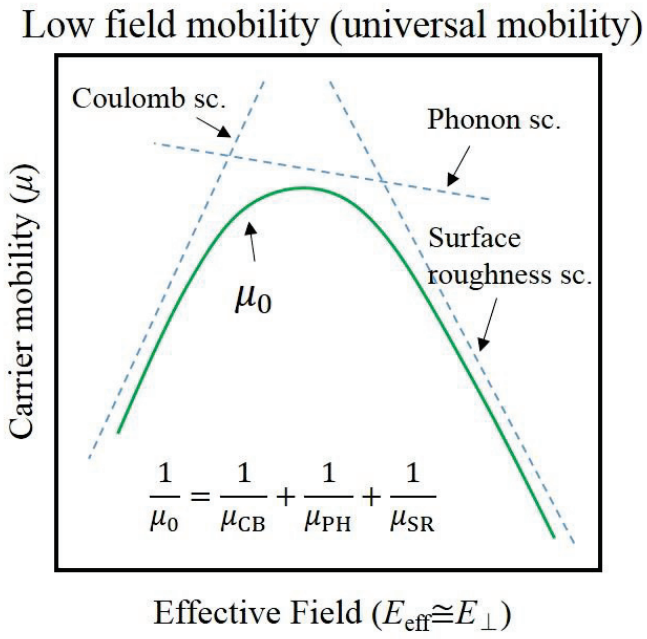


Fig. 3-14: Universality of carrier mobility.

3-3: Advanced Si devices

3-3-1: Micro electronics

Micrometer order devices including transistors are categorized into microelectronics. Since silicon has grown as a material for planar type MOSFETs, the transistor size has been steadily miniaturized and has been widely applied to processors and memories as large scale integration (LSI) devices. The demand for higher performance and multi-function of electronic products continues to increase, and the channel length of transistors now reaches nanometer order. While the aggressive miniaturization, MOSFETs have been suffering from the short-channel effects. Many possible improvements have been undertaken to continue further down-scaling of the MOSFET without the sacrifice of degradation of the high MOSFET-performance characteristics. The silicon-on-insulator (SOI) technology is one of such technologies, mitigating the achievement of above scaling goals [1-3]. The SOI technology has been extended to very thin layers for both SOI and buried oxide (BOX) in the silicon on thin BOX (SOTB)-MOSFET generation, which enables the strong threshold voltage (Vth) control by the back gate voltage [4, 5]. The Vth control is exploited to realize reliable low voltage applications [3, 4]. The SOTB structure is close to the ultimate double-gate structure enabling higher

circuit performance due to higher current and additionally smaller subthreshold swing. Figure 3-15 compares the structure of Si bulk-MOSFET and SOI-MOSFET. The performance changes by the thickness of SOI layer from partially-depleted (PD) to fully-depleted (FD). SOTB MOSFET is one of the extreme FD type SOI MOSFETs, have very thin BOX layer (approx. 10nm) and SOI layer (approx. 10nm). Figure 3-16 shows the controllability of threshold voltage in I_{ds}-V_{gs} characteristics.

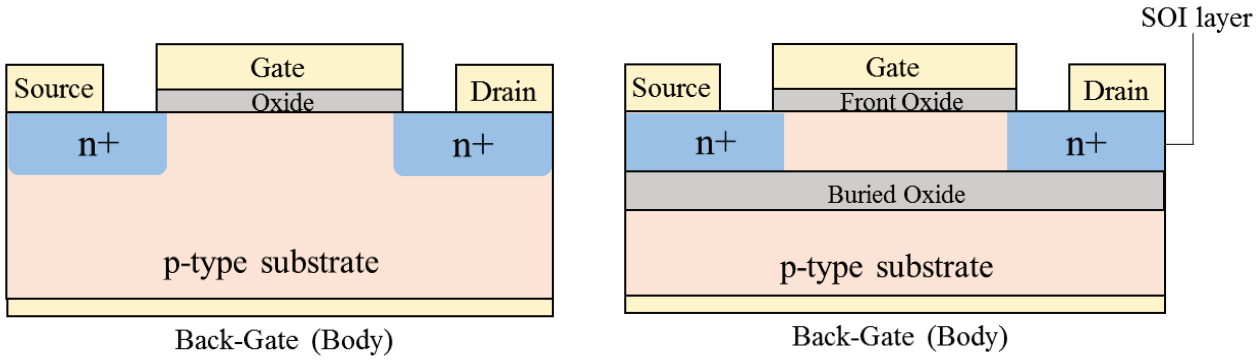


Fig. 3-15: Schematic structure of (a) Si bulk-MOSFET and (b) SOI-MOSFET.

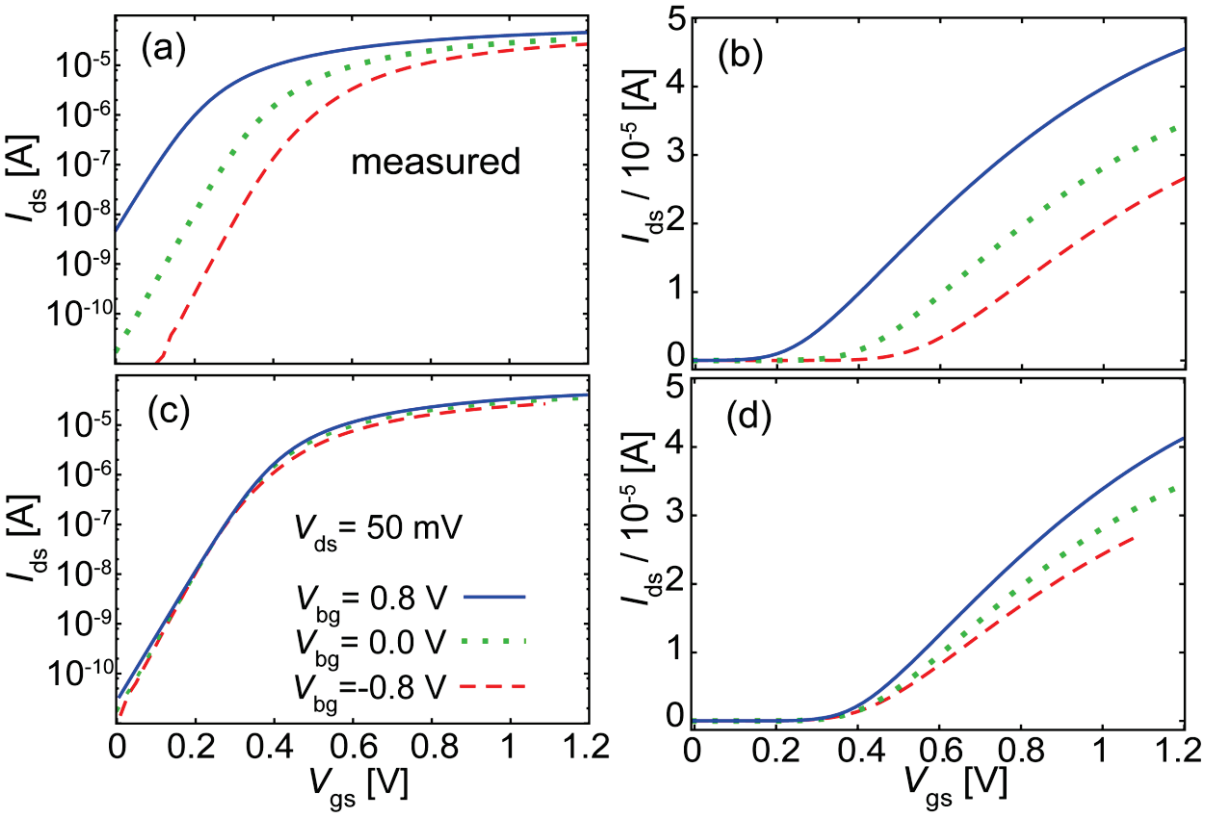


Fig. 3-16: Measured I_{ds}-V_{gs} characteristics of a SOTB-MOSFET with gate length 1 μm and gate width 0.5 μm as a function of the gate voltage V_{gs}: (a) half logarithmic, (b) linear, (c) the same plot as (a) but V_{th} shifted to the V_{bg}=0.0V value, and (d) the same plot as (b) with shifted V_{th} to the V_{bg}=0.0V value.

3-3-2: Power electronics

Power electronics is engineering that deals with technology related to power conversion and power opening / closing using power semiconductor devices. In a broader sense, power electronics is a general application system centered on power conversion and control. It differs significantly from the microelectronic device in terms of size and operating voltage range. As a representative technical example, power converter such as a forward converter (rectifier) for converting from AC to DC and an inverter for changing DC to AC are developed.

Silicon materials have also been used in power electronics devices. Since the band gap of silicon is 1.1 eV, physically the dielectric breakdown electric field is low. That is, silicon is not so suitable for a high breakdown voltage device in fact. However, by devising the structure, silicon can also be used for power electronics devices and circuits [1, 6]. For example, as shown in Fig. 3-16 (a), a trench type Si - MOSFET used as a power MOSFET has a structure in which current flows vertically from the source to the drain. By sandwiching an n- layer called as drift layer, the electric field applied inside the device is dispersed, making it possible to be used at high voltage application. In the IGBT shown in Fig. 3-16 (b), a parasitic bipolar transistor is formed inside the structure by using a substrate of an opposite type to that of a normal power MOSFET. The drain current of the MOSFET is included in the portion corresponding to the base current of the bipolar transistor, and the on/off of the switch can be controlled by the gate voltage of the MOSFET part. IGBTs have attracted much attention as a device that have low on-resistance and can be used under high power, and are used as inverters in power conversion elements in various fields. However, performance improvement of silicon is getting closer to the physical limit. For this reason, in recent years, device development using new materials such as SiC (silicon carbide) and GaN (gallium nitride) has been conducted, because those materials have physically better properties as a power semiconductor as shown in table 3-1 [7]. However, these new materials are difficult to manufacture and difficult to achieve stable quality, and there is a problem that they are high cost devices, so many problems still exist in practical application.

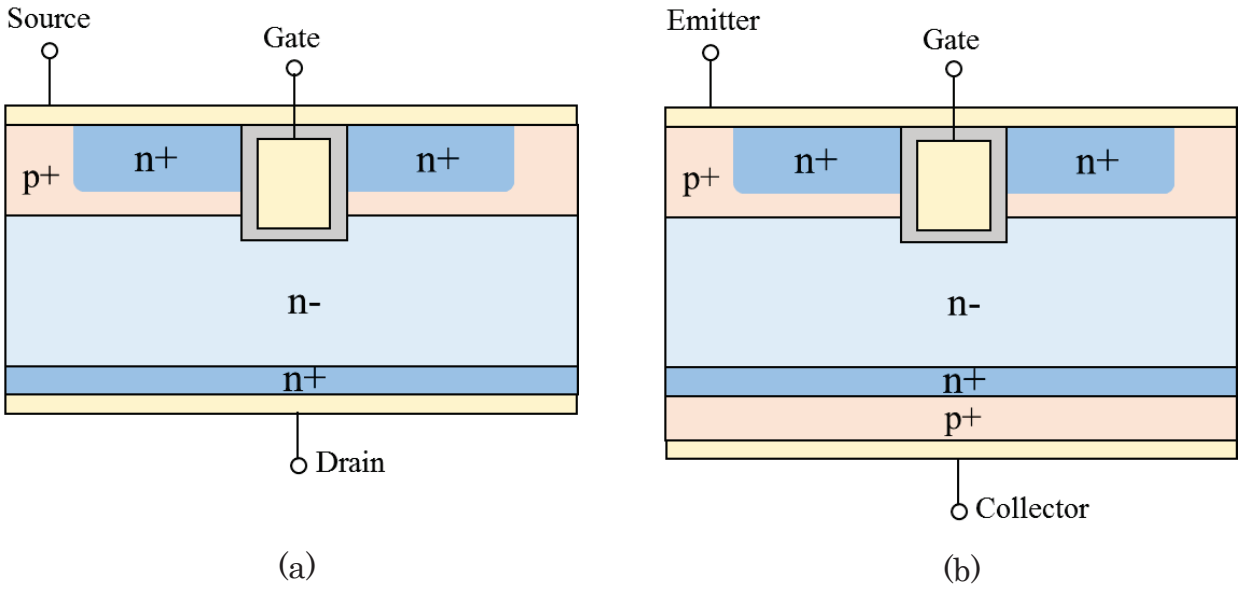


Fig. 3-16: Schematic structure of (a) Trench type power MOSFET and (b) power IGBT.

Table 3-1 : Semiconductor material property for power electronics. [7]

Property	Si	SiC	GaN
Bandgap (eV)	1.1	3.3	3.4
Electron Mobility (cm2/Vs)	1350	700	1500
Breakdown Electric Field (MV/cm)	0.3	3.0	3.3
BFOM ($\varepsilon\mu_e E_c^3$) *1	1	440	1130

*1: BFOM (Baliga figure of merit) is defined by $\varepsilon\mu_e E_c^3$. Here, ε is permittivity, μ_e is electron mobility, and E_c is breakdown electric field. BFOM is determined by physical constants and is an indicator of the marginal performance peculiar to the material of power device.

3-4: Physics of organic semiconductor

In inorganic semiconductors and organic semiconductors, the mobility greatly changes due to the material, structure, crystallinity, etc., and the conductivity also changes accordingly. In other words, investigating the conductivity of a material equals to examine the mobility of a substance, understanding the behavior of this carrier leads to understand the operation of the electronic device. This section explains the behavior of carriers in the organic semiconductors and the reason why organic materials can have a high conductivity.

3-4-1: π electron and conjugation

The definition of organic material is a substance (compound) composed of atoms such as hydrogen H, oxygen O, and nitrogen N, with carbon C as a main element. All electrically conductive organic materials have two important properties. The first is the presence of conjugated double bonds along the backbone. In conjugation, organic materials consist of alternate single and double bonds between the carbon atoms. This alternating structure can be observed in polyacetylene depicted in Fig. 3-17. The second property is that the organic materials must be doped, implying that electrons are removed by oxidation or introduced by reduction. These extra electrons or holes can move along the molecule to contribute the conductivity [8]. Organic materials for semiconducting application are not to be doped with “impurities” different from inorganic semiconductor application.

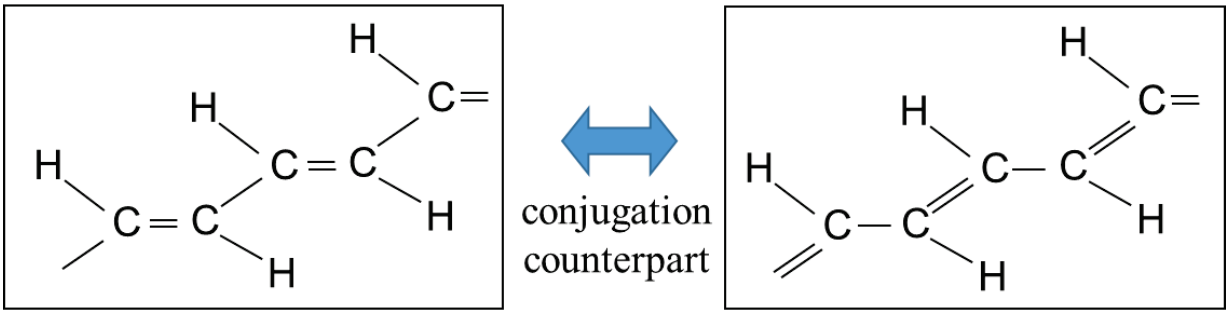


Fig. 3-17: Alternating structure of conjugated double bonds in polyacetylene.

In the conjugated double bond structure, the single bond is a sigma bond, and the double bond consists of a sigma bond and a pi bond. The strongest type of covalent bonds, require that both atoms

give an electron from each. Thus, the electrons forming the sigma bond are attracted to the two nuclei and are localized. Pi bonds are a direct sharing of electrons between the two atoms. Pi bonds are weaker than sigma bonds because their orbitals are further away from the positively changed nucleus. Normally, the electrons forming a pi bond are localized. However, in conductive organic materials, pi orbitals of the neighboring double bonds overlap due to the conjugated structure as depicted in Fig. 3-18. This overlapping results in weakly localized or delocalized pi electrons that can move from one bond to another or move along the entire molecule. Therefore, delocalization, accomplished by the continuous overlapping pi orbitals of the conjugated backbone, makes the conduction of charge carriers along the polymeric chains possible [8, 9]. Such conjugated structure enables the carrier transportation between molecules (intramolecular transportation) as well.

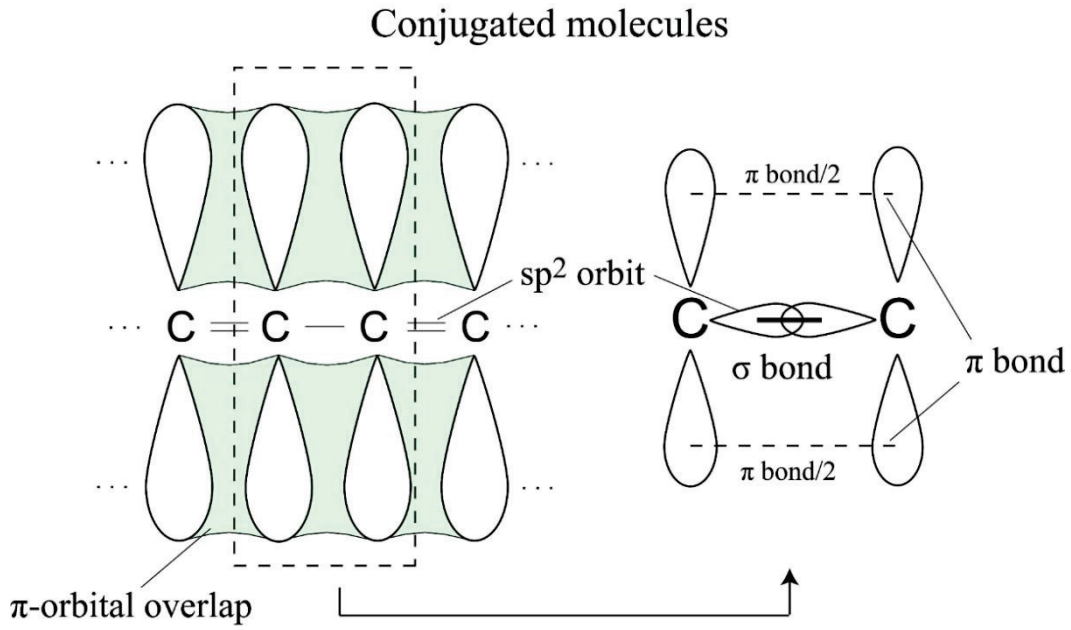


Fig. 3-18: Conjugated bond structure of an organic molecule.

An example of other molecules having a conjugated system is benzene. Aromatic molecules such as benzene are substances showing excellent conductivity as semiconductors. Figure 3-19 shows the localized π orbit before the bond formation and the delocalized π orbit after the bond formation. Benzene's delocalized π orbits become like clouds due to their overlap and are called electron clouds.

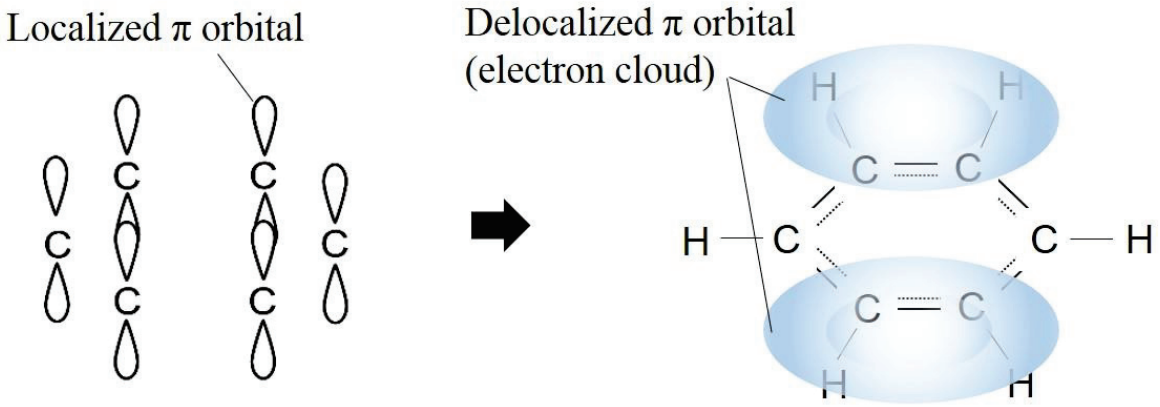


Fig. 3-19: Delocalized pi orbital forming of Benzene.

Highly conjugated organic materials can work as semiconductors because of their strong pi orbital overlap. When an electron is added or a hole is injected, the resultant charge becomes delocalized across the conjugated system. This injected charges act as carriers for current conduction through the molecules and the organic semiconductor thin film.

3-4-2: Band structure

The system of alternating double and single bonds in the conjugated backbone gives rise to a separation of bonding and anti-bonding states, resulting in the formation of a forbidden energy gap and a spatially delocalized band-like electronic structure, as illustrated in Fig. 3-20. The highest occupied molecular orbital (HOMO) consists of bonding states of the pi orbitals with filled electrons, and is analogous to the valence band in silicon. The lowest unoccupied molecular orbital (LUMO) consists of empty higher energy anti-bonding (pi*) orbitals, and is analogous to the conduction band. The energy difference between the HOMO and LUMO defines the band-gap energy (E_G). E_G depends on the chemical structure of the repeating unit, and generally decreases with the number of repeat units in the chain. E_G of conjugated organic semiconductors is typically in the energy range of 1-4 eV. This band-like structure, along with low electron mobility, is responsible for the semiconducting properties observed in conjugated organic materials.

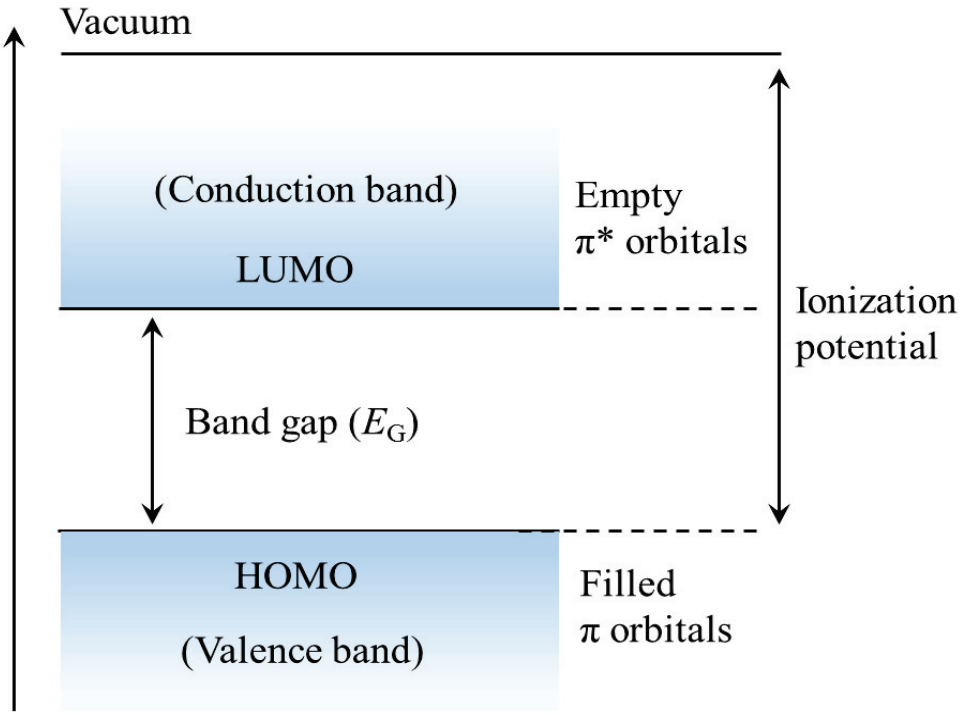


Fig. 3-20: Energy band diagram of organic semiconductors.

Due to the disordered nature of organic materials, the conduction mainly occurs via phonon-assisted hopping and polaron-assisted tunneling between localized states, which is in contrast to crystalline semiconductors such as silicon where conduction occurs in the energy band through delocalized states. Most conductive organic materials in the neutral state are wide bandgap semiconductors and exhibit very low conductivities.

The horizontal axis of the band structure diagram in the semiconductor represents the wave number k per unit length and is the proportionality constant for the phase of the coefficient of the wave function in each atom. However, since quantum mechanics treats electrons as a wave, the velocity of the wave that has the wave number k is expressed by equation (3-62) using energy E.

$$v(k) = \frac{1}{n}\left(\frac{\partial E}{\partial k}\right). \tag{3-62}$$

Considering an infinitely long carbon chain, k can be positive and negative corresponding to electrons moving in opposite directions at velocity $v(k)$. Since the number of 2pz electrons in the n sp^2 carbon chains is n, and two electrons are entered at each level, the π band is clogged with electrons 1/2 from the bottom, and the remaining 1/2 will be empty. That is, if there is a certain number of electrons, the

same number of electrons of -k exist. When n is large, the interval between the levels becomes extremely small. Even if the occupancy ratio of the level slightly changes to the positive/negative level of k, the energy hardly changes. In that case, it is possible to change the occupancy ration of the level with only a little external actions. When the interval between the levels is large, since the energy changes greatly by merely transferring one electron, the corresponding energy is required to change the occupation ratio. When an electric field is applied in a direction along the carbon chain in a state where the level interval is extremely small, electrons are accelerated directly by the electric field, the electrons having k0 in the +x direction become large k with time. Electrons having a wavenumber in the -x direction are decelerated by the reverse electric field. If there is no friction, electrons are accelerated even in a weak electric field, but in reality, electrons are scattered, feel frictions and reach the terminal speed due to the influence of atoms' thermal vibration and interaction between electrons. However, as the electric field causes bias of the velocity distribution, the current corresponding to the electric field flows. Such electric conduction is called band conduction and has high mobility. It is necessary that the gap between occupied level and unoccupied level is infinitely small for the condition of current flow with a small electric field (this is a necessary condition for Ohm's law). When the number of electrons becomes two per an atom, the level for making a band is filled up. Then, in order to change the occupation ratio of the level to the positive/negative of k, electrons have to be transferred to the band consisting of other levels, and a large energy is required to ship from a band to another band. This system occurs in insulators or weak conductive materials. Under the condition that considered solid substance is a well crystallized material, the behavior of electrons can be dealt as a wave over long distance. But in the case of organic materials, this condition is not always satisfied. Figure 3-21 conceptually shows the difference in band structure between inorganic semiconductors and organic semiconductors [10]. This indicates that the crystallinity of organic semiconductor in MOSFETs has to be high as much as possible.

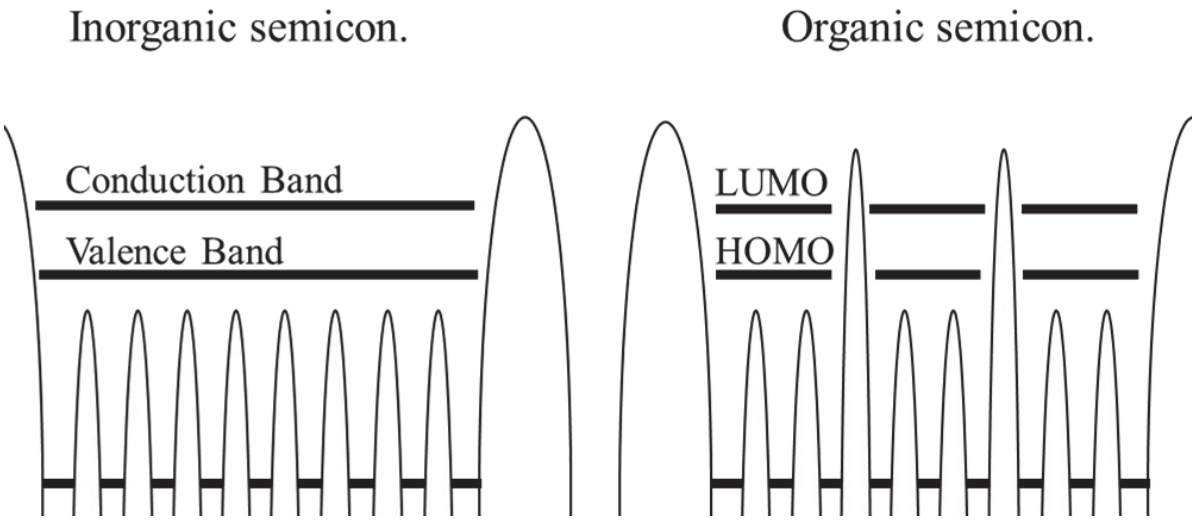


Fig. 3-21: Band structure of inorganic semiconductor and organic semiconductors. [10]

3-4-3: Conduction theory in organic semiconductor

- Hopping conduction [10]

Although atoms and molecules are regularly composed within the grains in organic semiconductors, the important is a molecular level sequence. In general, an organic semiconductor layer used for transistors is often amorphous in which molecules are clustered. It is obvious from the organic EL made of amorphous that the current flows even in such a case. Electrons behave as electric charges localized in molecules, not waves spreading the entire solid. That is, molecules containing electrons become negative ions, and molecules containing holes become positive ions. These ions transfer charges to the next molecule and convert them to ions, and they return charges to neutral molecules by themselves. The electric conduction caused by such a mechanism is called hopping conduction. In organic semiconductors, it can be happened that charges are not localized in a single molecule, but an electric charge is shared by several molecules. However, theoretical handling in such a case has not yet been formulated.

Here considers the transfer of charges between adjacent molecules. If the potential barrier between molecules is very high and the charge moves via tunneling, handling by Marcus theory [11, 12] is often used for the probability of jumping. This incorporates that the local structure such as the molecule itself and the distance to surrounding molecules changes due to the charge being entered into the molecule. As a simple model, it is known that a repulsion occurs between atoms when they become negative ions, and molecules become larger than neutral molecules. Charge transfer can also be regarded as a movement of charges accompanied by a structural change of molecules, and a complex of this charge and local structural changes are also called polaron because of the similarity with a polaron seen in ionic solids.

In Figure 3-22, the vertical axis (y axis) is Energy. The horizontal axis (x axis) is the change in the local structure accompanying electron transfer, which is called reaction coordinates. ΔG^* refers to activation free energy. Let s1 be the size of molecule1 and s2 be the size of molecule2 and let x = s2 - s1 be the corresponding coordinates. Let the magnitude of the negative ion be larger by α than the

neutral molecule. The relationship between reaction coordinates and free energy is not easy, but in Marcus theory, it is approximated by a harmonic oscillator. That is, the parabola corresponding to the beginning state (A-M) is depicted at the left side, the parabola at the right side corresponding to the final state (M-A) gives the minimum value by following equations;

At the beginning state (A-M): $y = (\lambda / a2)(x+a)^2$.

At the final state (M-A): $y = (\lambda / a2)(x-a)^2 + \Delta$.

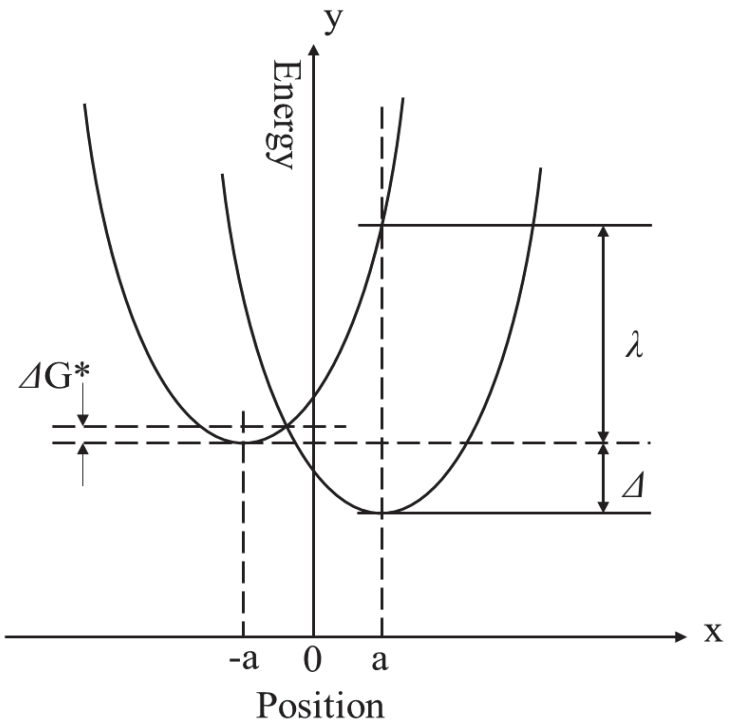


Fig. 3-22: Energy diagram of electron transfer reaction by Marcus theory. [11, 12]

Here, the energies of the final state and the beginning state are different because this takes a common example in which energy difference exists between neighboring molecules due to the differences in molecules and environment. The intersection point is obtained from the graph, and the difference between the y coordinate and the minimum value of the parabola gives the activation energy. The value of λ can be quantum chemically calculated by exchanging the charge number while maintaining the structure of the neutral molecule and the anion. The value of Δ can also be calculated by finding a re-stable structure.

The Marcus theory is used to explain the speed of electric charge transfer occurring in the

photosynthetic system. In the case of organic semiconductors, many cases are applied also for the estimation of carrier mobility, but the estimation is used based on the following assumptions;

(i) The intermolecular potential barrier to jumping electrons is high, and electric charge transfer occurs due to the tunnel effect (transfer integration is small).

(ii) The energy (λ) related to the local structural change accompanying charge transfer is large.

That is, Marcus theory is effective in the case of amorphous or multi crystalline organic semiconductors with low mobility, in which the effect of the band can be neglected.

- Bassler theory [8, 11]

When conduction occurs due to charge hopping between adjacent molecules, it is necessary to consider the description of macro parameters such as carrier mobility. Organic semiconductor molecule consists of various parts; atoms, covalent bonds and functional groups have some charge and internal bias. As a result, the coulomb potential sensed by the electrons in the adjacent molecule is modulated, and the electron state changes from the isolated molecule state. In the case of amorphous, since the structure is cluttered, a difference occurs in the surrounding environment. Consequently, the energy level is slightly different in each molecule.

On the other hand, the probability of jumping/hopping between molecules also varies depending on the distance of relevant molecules and the variation in molecular orientation. Bässler has proposed a method of estimating various properties by computer simulation, by introducing the variation magnitude as a material parameter describing the property of amorphous, assuming that the variation in energy level follows a normal distribution (Gaussian distribution). This model can explain electric field dependence of mobility (ie deviation from Ohm's law) well and is still widely used presently. A calculator is necessary to practically use Bässler theory, but when the mobility is extremely low, it can be handled analytically. Ideally the current follows Child's law proportional to $(\text{voltage})^2 / (\text{distance})^3$. This theory is interpreted to Gaussian Disorder Model (GDM) as a carrier mobility model.

3-4-4: Summary of the difference between organic and inorganic semiconductor

In organic semiconductors, it is not necessary to control carriers by intentionally and actively adding a dopant even it's common in inorganic semiconductors. The remarkable difference between inorganic semiconductors and organic semiconductors lies in the dielectric constant and the effective mass. This effective mass is a quantity representing the inertia when the electron moves in response to the external field, and can be obtained by approximating the E-k curve of band structure to a parabola that free electrons have, and expressed by equation (3-62).

$$\frac{1}{m^*} = \frac{1}{h^2}\left(\frac{\partial^2 E}{\partial k^2}\right). \tag{3-62}$$

In the case of materials that have an amorphous composition or a strong polaron effect, the effective mass becomes very large. For example, considering Si, the permittivity ε is 11.7 and the effective mass is about 0.2 m_0 (m_0 is a rest mass of an electron). On the other hand, for most organic semiconductors, ε is less than 4, and the effective mass is larger than 1.

The major difference appears at the activation energy of carriers when it's doped. The feature of inorganic semiconductors such as Si is that if silicon is doped with a group 15 element such as phosphorous (P), it becomes n type, if doped with a group 13 element such as boron (B), it becomes p-type, and the carrier concentration can be modified in proportion to the doping concentration. This is because the permittivity of Si is high and the effective mass is small. For example, when P is doped in Si, P uses 4 valence electrons for covalent bonding with Si, but one extra electron is attracted around P nucleus because the nuclear charge of P is one more than Si. This structure is similar to a hydrogen atom with one electron attracted around a hydrogen nucleus.

However, while hydrogen atoms are existing in vacuum, P is buried in Si, the permittivity ε and the electron masses m* are introduced. Since the ionization energy is smaller than the thermal energy at room temperature ($k_B T$ = 26meV), it is quantitatively ionized at room temperature. The ionized electrons can enter the conduction band of Si and move freely. For this reason, it is a great advantage of inorganic semiconductors such as Si that it is possible to quantitatively form carrier density by

doping amount. In organic semiconductors, ε is small and m* is large, so the ionization energy is about 200 meV which is much larger than the thermal energy at room temperature. In this case, even if a dopant (such as an ionizable atom) is added, it is expected that the carrier will not be free and will be trapped. Therefore, at present, organic semiconductors are not used with active doping and are used as intrinsic semiconductors for FETs and etc. [9]. However, although such impurity doping is not conducted for organic materials, an effective doping method has been investigated to increase electrical conductivity. The conductivity of a conjugated organic material can be modified by chemical doping or electrochemical doping, where oxidation and reduction are used to make p-type (electron removal) and n-type (electron addition) doping respectively [9, 11]. These doping processes provide mobile charge carriers that move in the electric field, giving rise to electrical conductivity. Conductive organic materials are doped by oxidation that is comparatively easy, therefore, p-type conductive organic materials a with hole conduction are more common.

3-5: Operation Principles of OFETs

One of the obstacles of OFETs is the junction of organic semiconductor and gate, source and drain electrodes. Here will be an explanation of the junction barrier at the interface. In organic transistors, doping is not usually performed, so it is no exaggeration to say that blocking and operation of transistors is performed by injection of carriers from the electrodes. When the doping is not performed, materials must be selected so as to reduce the injection barrier with a consideration of the work function difference between the electrode material and the organic material. This section contains electric characteristics such as I_{ds}-V_{ds} and I_{ds}-V_{gs} by 2-dimensional (2D) device simulation.

3-5-1: OFETs structure

It is well known that inorganic semiconductors such as Si perform band conduction by allowing majority carriers in the excited state to propagate freely in the conduction band, but in the case of organic semiconductors, most of them are polycrystalline or amorphous crystals where it is difficult

for carriers to move in the same energy level band like the conduction band. Carriers in organic semiconductors need to move between discrete levels. Therefore, the conduction mechanism is complicated and the carrier mobility is much lower than that of inorganic semiconductors.

Figure 3-23 (a) and (b) show schematic diagrams of device structures that are most well-used among OFETs. For a comparison, the structure of n-type Si MOSFETs is shown in Fig. 3-23 (c).

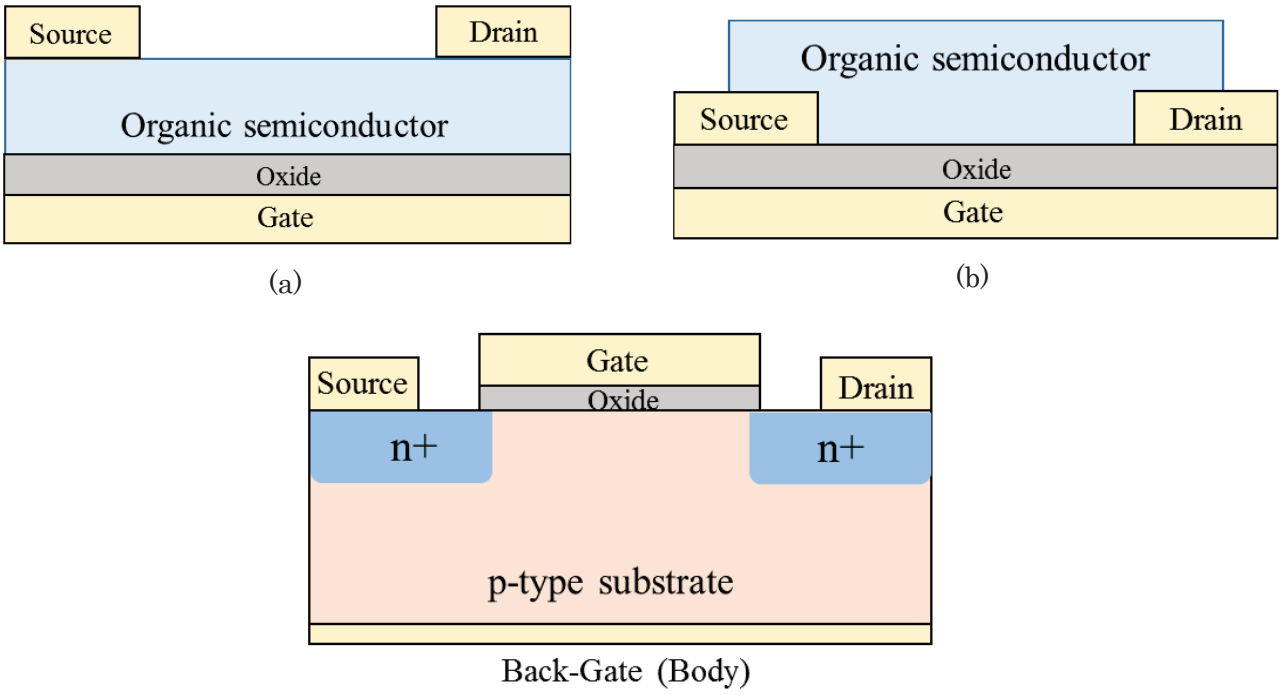


Fig. 3-23: Schematic structure of MOSFETs: (a) Bottom gate top contact type OFETs, (b) Bottom gate bottom contact type OFETs, and (c) n-type Si MOSFETs.

Generally, in the case of inorganic MOSFETs such as Si MOSFETs, p-type or n-type doping is performed intentionally and locally in the semiconductor layer, which guarantees the operation of MOSFETs. For example, in the structure shown in Fig. 3-23 (c), the entire semiconductor is weakly doped by p-type while the vicinity of the electrode is n-type. Therefore, in a state where no gate voltage is applied, since the pn junction is formed between the two electrodes, no current flows between source and drain, which means the MOSFET in an off state. When a gate voltage is applied and electrons are accumulated, the channel can be opened and the MOSFET is turned on. Such an operation mode is called normally-off. If the channel is intentionally doped, a state is formed in which a channel is

initially formed between source and drain. The channel is turned off by applying a reverse gate voltage. Such an operation mode is called normally-on. In this way, in inorganic semiconductors, since substitutional doping is often established, a transistor structure is formed on the basis of doping, and the operating characteristics of the transistor are tuned by doping. On the other hand, in organic semiconductors, general doping techniques used for inorganic semiconductors have not been carried out much. So organic transistors are often used without doping to organic semiconductors. Nevertheless, it operates with sufficient reliability as the current characteristic. It is necessary to make full use of the simplicity of the organic transistor which does not necessarily need doping, but in order to further improve the performance and to improve the controllability of the operating characteristics, other type of doping techniques should be applied to increase the number of carriers in organic semiconductors and not to degrade crystallinity [12-14].

It is reported that the structure shown in Fig. 3-23 (a) has higher performance than the structure shown in (b). This is due to the difference in crystallinity of the portion to be the channel of the organic semiconductor. In the structure of (a), crystallinity of the interface portion is improved by forming an organic semiconductor on the oxide that is accomplished a chemical treatment. In the structure (b), since the source and drain electrodes are formed first, the crystallinity in the vicinity of this electrode deteriorates. As a result, the current hardly flows. In addition, in the structure (a), a new energy level is created on the organic semiconductor side at the stage of forming the electrode, and the contact resistance is reduced, hence, the switching performance is also high.

3-5-2: Selection of device materials

In order to utilize organic semiconductors as an active layer of FETs, selection of an organic material, an electrode material, and an insulating film material is an important process determines device characteristics. Initially, in organic transistors, active doping process which is essential for inorganic transistors is not performed, so it is no exaggeration to say that blocking and operation of transistors is performed by carrier injection from the electrodes. In addition, when doping is not

performed, materials must be selected so as to reduce the injection barrier of carriers in consideration of the work function difference between the electrode material and the organic material. Fig. 3-24 shows the energy band diagram of the organic semiconductor device.

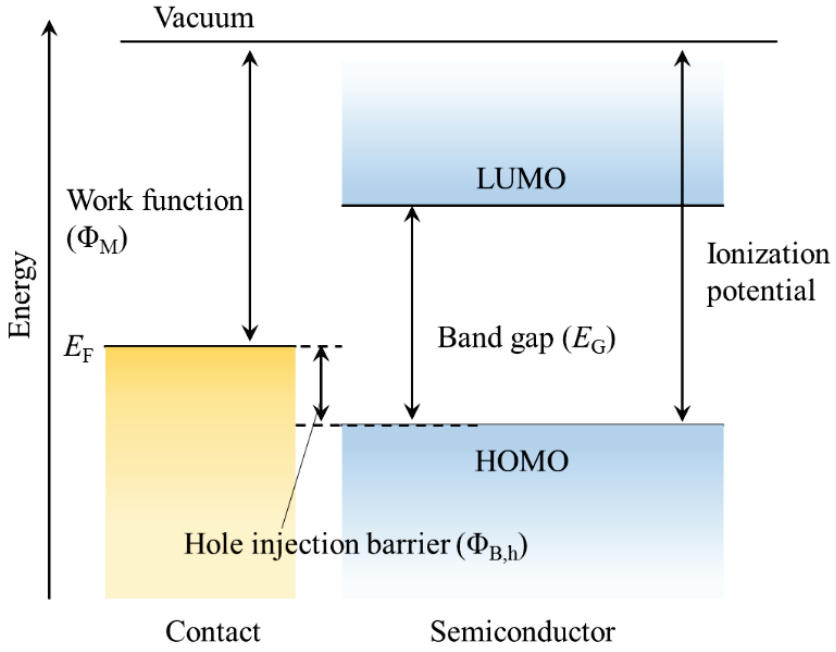


Fig. 3-24: Energy band diagram of a semiconductor and a contact electrode.

Here, the energy level of the organic semiconductor is represented by HOMO level (lower end) and LUMO level (upper end). When the Fermi energy of the electrode is close to the HOMO of the organic semiconductor, holes as carriers are easily injected, and p-type characteristics are observed. Similarly, in the case where it is close to LUMO, electrons are easily injected, and n-type characteristics can be expected. It was reported that pentacene, which operates p-type with respect to the gold electrode, exhibits an action called bipolarity that can inject both electrons and holes when a calcium electrode with a small work function is used as the electrodes [15]. Besides, C60 (fullerene) which operates n-type with respect to the gold electrode changes the work function when the surface of the gold electrode is modified with organic molecules, and p-type operation is also observed [9, 16].

As illustrated in Fig. 3-23, the functional device layers are the semiconductor, the gate dielectric (oxide/insulator), and the electrodes. Figure 3-25 depicts the key interaction mechanisms between various device layers. There are two additional material layers that require consideration for OFETs

fabrication: the substrate and the encapsulation. The substrate gives a platform for materials deposition. In case of organic devices, there is an application-driven aspiration toward flexible substrates. Encapsulation provides protection passivation for the functional device layers, which is particularly important for organic devices due to the sensitivity of organic materials to the environment. Table 3-2 summarizes device materials that is frequently used in OFETs [18].

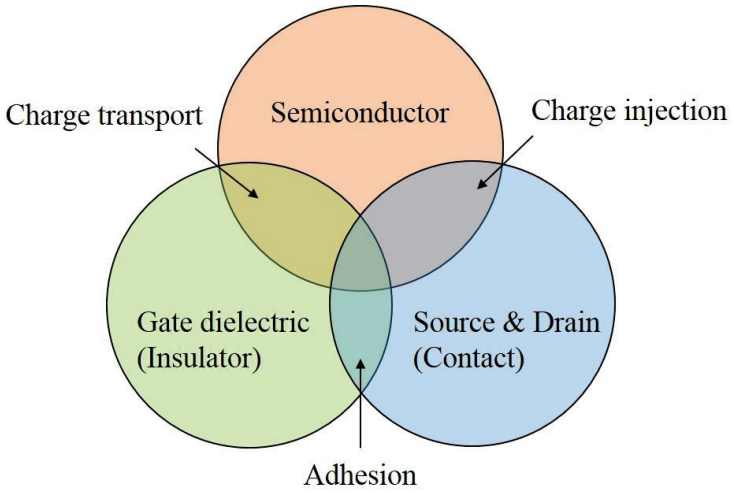


Fig. 3-22: Interaction between the three key device layers in OFETs. [18]

Table 3-2: Device materials in each layers frequently used in OFETs.

OFET device layers	Material choices
Dielectric (Insulator)	Thermal silicon dioxide (SiO_2) PECVD silicon nitride (SiN_x) PECVD silicon oxide (SiO_x) ALD aluminum oxide (Al_2O_3) etc.
Electrodes	Source / Drain contact: Au, Cr, etc. Gate electrode: Mo, Al, Au, etc.

	Ag	Al	Au	Cu	Cr	Mo	Ni	Pd	Pt	Ti	ITO
Φ_M	4.26	4.28	5.1	4.65	4.5	4.6	5.15	5.12	5.65	4.33	4.8-5.2

Substrate	Silicon wafer Glass wafer Steel foil Plastic substrate: Kapton, polyethylene naphtalate (PEN), Poly ethylene terephthalate (PET) , etc.
Encapsulation	Parylene Photoresist PECVD silicon nitride etc.

* Semiconductor materials used in OFETs are mentioned in table 3-3.

3-5-3: Current – Voltage characteristics (*IV* characteristics) of OFETs

It is known that OFETs have similar functions to inorganic MOSFETs that carrier number is controlled by the gate voltage and the carriers are accelerated by the source-drain voltage. Figure 3-26 shows hole-density distributions along the vertical direction of the organic device, as simulated with a 2-dimensional (2D) device simulator: ATLAS manufactured by SILVACO [18, 19]. Even though the gate oxide is relatively thick, the inversion charge is collected at the substrate surface showing the V_{gs} control of the carrier density as in conventional MOSFETs. Consequently, *IV* characteristics of OFETs (shown in Fig. 3-27) are very similar to conventional MOSFETs although the current amplitude is much small.

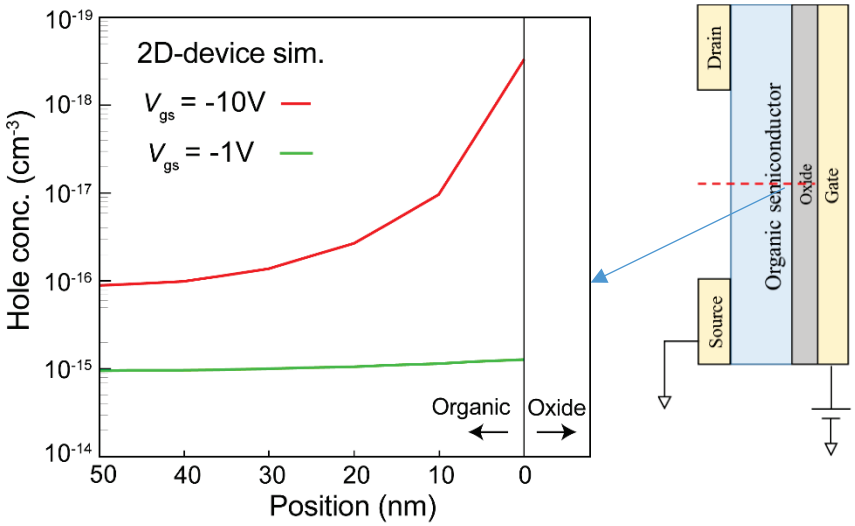


Fig. 3-26: Induced carrier (hole) density extracted across the depth of the organic MOSFET with a 2-dimensional device simulator (2D-device Sim.).

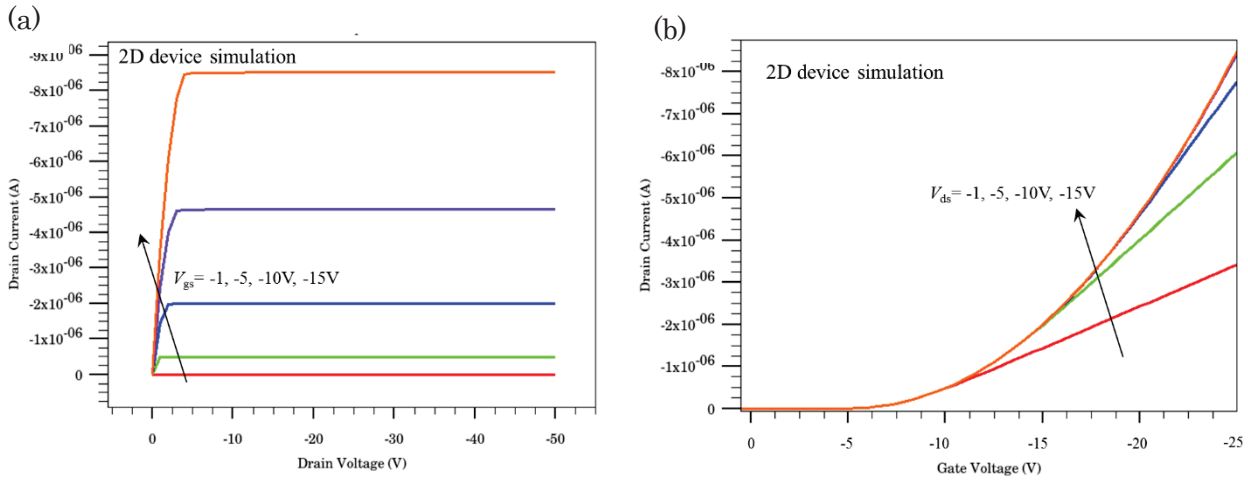


Fig. 3-27: IV characteristics of OFETs: (a) I_{ds}-V_{ds} and (b) I_{ds}-V_{gs} linear plot.

3-5-4: Small molecule OFETs

The active layer which is widely used in OFETs is a small molecule polycrystalline thin film such as pentacene. One of the reasons that many researches on organic transistors are actively being conducted is that, they realize transistor characteristics with extremely simple and inexpensive equipment compared to the common sense of inorganic semiconductor devices. Small molecule organic semiconductors form a closed shell structure as a basic unit of the electronic band structure. That results in, compared to polycrystalline thin films of inorganic semiconductors and amorphous devices, (a) there is less dangling bond, majority carriers are almost effectively accumulated and propagated, (b) the interface energy level at metal-semiconductor and dielectric-semiconductor is hardly generated. (c) Likewise, the in-gap level is relatively small also at the crystal grain boundary, and (d) the influences by the purity level of the raw material and impurities taken in the process are also relatively small. In addition to these merits, since it is possible to fabricate transistors even by room temperature depositions or the solution process (wet process) and by roll-to-roll process on a polymer film. It is expected to be able to produce large area circuits at low cost per area far more than conventional semiconductor technology.

Factors that interfere with currents in low molecular organic transistors are described separately as external limiting factors and internal limiting factors based on phenomena occurring in the fabrication process with taking pentacene as an example.

- External limitation factor

Hetero-oriented crystal grains observed in a film grown at comparatively low temperature have the major molecular axis parallel to the substrate surface. Such grains are insulated from the surrounding molecules oriented vertically to the substrate. This is because the continuity of the orbit is cut at the grain boundary. When such hetero-oriented crystal grains increase, the apparent mobility is decreased by 1/10 ~ 1/100. In organic transistors, "top contact type" in which a metal electrode is deposited from above the organic semiconductor layer to form the source and drain often shows higher

performance than "bottom contact type" in which the organic film is formed on the electrode. In the case of bottom contact type, the crystallinity tends to be poor at the end portion of electrodes. In addition, when the organic semiconductor is brought into soft contact with the metal, Schottky contact easily occurs and a large carrier injection barrier is generated. On the other hand, even in top contact type, apparent mobility reduction occurs due to electrode deposition. When depositing gold as the source and drain electrode, gold atoms at the sub-monolayer size also enter the channel portion. In this range, the carrier mobility of pentacene lowers. The injection barrier is lowered by gold deposition on the organic film causing a new in-gap level generation, which is a merit of top contact type. According to the ultraviolet photoelectron spectroscopy near the HOMO level, some new in-gap levels are formed at the shallower part of the sample in which gold entered with about 1/100 density, instead of deepening the HOMO level. This is considered to be due to the formation of a new level by a complex of a gold atom and a pentacene molecule. This level creates a new path of current in the longitudinal direction in the pentacene polycrystalline thin film and metallic electrical conduction is observed in these crystal grain boundary. A barrier of 0.23 eV has been confirmed for hole injection from gold Fermi level to pentacene HOMO level [20].

- Internal limitation factor

In the pentacene polycrystalline film, four-leaf or pyramid-like crystal grain grows, but even in side of the crystal grain, a carrier transport barrier exists also in a part without morphologically clear boundary. It is known that the growth process of pentacene crystal grains is formed by combining four leaves of four-leaf clover to form rhombic grains. Even if it seems to be morphologically smoothly fused, there is a domain boundary of the crystal. It was reported for the first time in the sample using oligothiophene that this tendency appears in OFETs having the small molecular polycrystalline film[9]. This is explained in "polycrystalline model" proposed for polycrystalline silicon and others.

Polycrystalline model considers that carriers thermally moving in crystal grains are limited by potential barriers caused by the concentration of traps at the grain boundary. In this model, the

mobility is modulated by the frequency of jumping the potential barrier by thermionic emission. Even in the polycrystalline model based on the diffusion theory, the mobility is proportional to the distance between the barriers (l), and is expressed by following equation;

$$\mu = \frac{ql}{2k_B T}\mu_h \cdot \sqrt{\frac{qN_A\Phi_b}{2\varepsilon_s}}\exp\left(-\frac{\Phi_b}{k_B T}\right). \tag{3-63}$$

Here, μ_h is the hole mobility in the crystal grain, N_A is the acceptor density, Φ_b is the barrier height, and ε_s is the dielectric constant of semiconductor. Although this mobility doesn't represent the channel mobility of transistors, but well reproduces the mobility between molecules and grains.

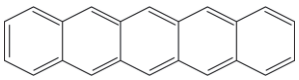
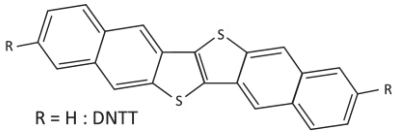
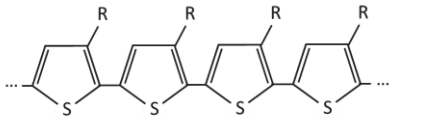
Carrier transport in a polycrystalline pentacene thin film can be explained by polycrystalline model based on diffusion theory without inconsistency. In the pentacene thin film on SiO_2, the potential fluctuation exists at the upper end of HOMO level which is responsible for carrier transport in p-type semiconducting. Potential fluctuation is also observed in the crystal grain. Among the potential fluctuations, the band edge fluctuation of about 30 meV is present in the peak to valley at the portion which is not influenced by the film surface shape. In most cases, the effective amplitude of the fluctuation is about 10 meV in average. This value is smaller than the band edge fluctuation that exists in amorphous silicon and is much smaller than the barrier height at the grain boundaries. It is considered that the mobility becomes smaller than that in single crystals because of trap/de-trap transport of percolation-like transport by such a fluctuation. In addition, since the movement speed of holes when crossing grain boundaries is only about 1/100 of that in the domain, the number of grain boundaries is much smaller by several orders than the total number of molecules in the path from source to drain, this specific mobility itself has little effect on macroscopic mobility. Together with band fluctuations within the domain, the mobility of holes single crystal grain can be expected to be about 10 to 20 cm^2 /Vs [21].

3-5-5: High molecule OFETs

When classifying organic transistors from the viewpoint of organic molecules, there are high molecular (polymer) materials as a relative to small molecular materials. Generally, as compared with small molecular materials, high molecular materials have high solubility in solvents and are regarded as materials that are easy to use in a solution (coating) process. Therefore, small molecular materials are deposited by vacuum vapor deposition (sublimation evaporation etc.), and high molecular materials can be used in an inkjet or a Roll - to - Roll process enabled by printing technologies.

Polymer materials have a drawback that the crystallinity is less than small molecular material and the mobility is also lowered. However, it has been found that aligning the orientation of polymers at the manufacturing process stage dramatically improves the carrier mobility [6], so developments of manufacturing process technology also flourishes in parallel with developments of new materials. Table 3-3 summarized the property of organic semiconductor materials used in OFETs [9, 17, 23].

Table 3-3: Properties, representative chemical structure, and carrier mobility of organic semiconductor materials used in OFETs with a comparison to silicon. [9, 17, 23]

Classes	Properties	Representative chemical structure	Carrier mobility (cm^2/Vs)
Small Molecules	Low molecular mass (20~40 carbon atoms) Size: ~1nm Polycrystalline or monocrystalline Vapor deposition Low process temperature (<150 °C)	Pentacene  Dinaphtho-Thieno-Thiophene (DNTT)  R = H : DNTT R = Ph : DPh-DNTT R = C_nH_{2n+1} : C_n-DNTT	<1 <10
High Molecules (Polymers)	Long molecular chains (made of repeating units of the monomer) High molecular mass (>50 carbon atoms) Size: ~10-1000nm Semi-crystalline or amorphous Solution process Low process temperature (<150 °C)	Regioregular poly (3-hexylthiophene) (P3HT)  R = $CH_2(CH_2)_4CH_3$	≦0.1
Silicon	Inorganic semiconductor High purity Impurity doping for conductivity High process temperature	Crystalline silicon Polycrystalline silicon Amorphous silicon (a-Si:H)	300-1000 50-100 ~1

Chapter 4

Fabrication and Measurement of OFETs

4-1: Overview of OFET fabrication technologies

To produce electronic devices, the existence of a trustworthy fabrication process is as critically important as the availability of high-performance materials. With regards to the OFET fabrication scheme, the device processing steps can be grouped into four categories: deposition, patterning, etching/ removal, and interface/surface modification [1-4].

- Deposition refers to depositing/coating a thin film of material onto the substrate. Relatively standard thin-film deposition techniques are used for the fabrication such as plasma enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD) for the gate dielectric layer, sputtering and thermal evaporation for the electrode layer (physical vapor deposition: PVD), spin-coating, of Inkjet printing (IJP) for the solution-processed organic semiconductor layer, and chemical vapor deposition (CVD) for the polymer passivation layer.
- Patterning refers to shaping or altering the existing shape of the deposited materials, or directly depositing materials onto a designed region to form a film with patterned structures. Three pattering approaches are generally employed: shadow mask, photolithography and IJP.
- Etching/removal refers to removing a material in designed regions from the wafer. Once an image is transferred from a mask to a wafer, one has to remove or etch material from designed regions to form the final device. Specially designed wet or dry etching processes enable to remove materials once the resist has been patterned. Organic layers are dry-etched with oxygen plasma (O_2 ashing) to avoid chemical/solvent interactions between wet-etchants and organic device layers. Source and Drain contacts are usually patterned by lift-off process.
- Interface/surface modification refers to functionalizing the device interfaces for performance enhancements. In OFETs and all the other transistor, the interfaces between the device layers

have an important role to realize transistor functions and to keep high performance. Interface modification has been a vital step for OFET fabrications so as to improve interfacial interaction and to control the quality of subsequently deposited organic layers. Modifications are typically done on the dielectric surface and contact interface prior to deposition of organic semiconductor layer, in the case bottom gate bottom contact structure.

Figure 4-1 shows the classification of thin film forming methods that can be used for organic semiconductors [4, 5]. Many conventionally used technologies are still applicable to OFETs fabrication. However, the IJT for transistor fabrication is a novel concept that encourages to proceed a mass production of organic devices.

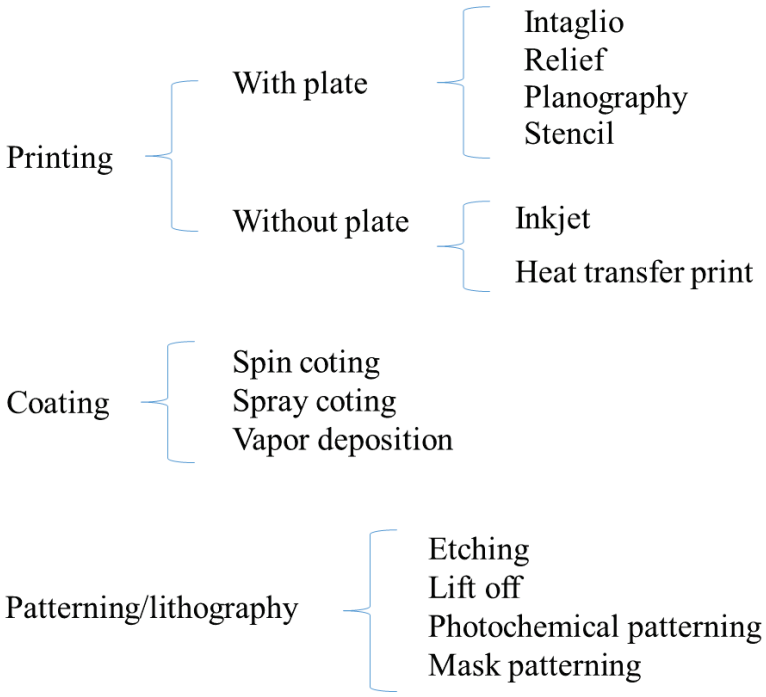


Fig. 4-1: Classification of organic thin film forming methods.

From here, important fabrication technologies: vacuum evaporation and solution-based deposition , patterning by photolithography, patterning by inkjet printing, and self-assembled monolayer (SAM) for a channel interface treatment are introduced. These are only some examples out of a vast amount of fabrication technologies, but are the essentials to maximize the performance of OFETs.

4-1-1: Vacuum evaporation and solution-based deposition

Small molecule organic semiconductors are typically deposited by vacuum evaporation, which consists of heating the material under reduced pressure. The process is conducted in a very high or ultra-high vacuum chamber. The organic material is put into a metal boat, which is heated by Joule heater system. Precursor conversion Target substrate is placed a few centimeters above the boat as shown in Fig 4-2 [7]. This technique is usually not applicable for high molecule organic materials, because they tend to decomposed by cracking at high temperature. For small molecule depositions, the substrate temperature is set 80 ~ 150 °C depending on the materials. The main advantages of vacuum evaporation are the easy control of the thickness and purity of the deposited film, and the ability to realize highly ordered films by monitoring the deposition speed and the substrate temperature. Microscale patterning can be accomplished with use of metal shadow masks. The major drawback is the need for sophisticated vacuuming system to keep the pressure pretty low, which is in contrast to the simplicity of spin coating and other solution-based process.

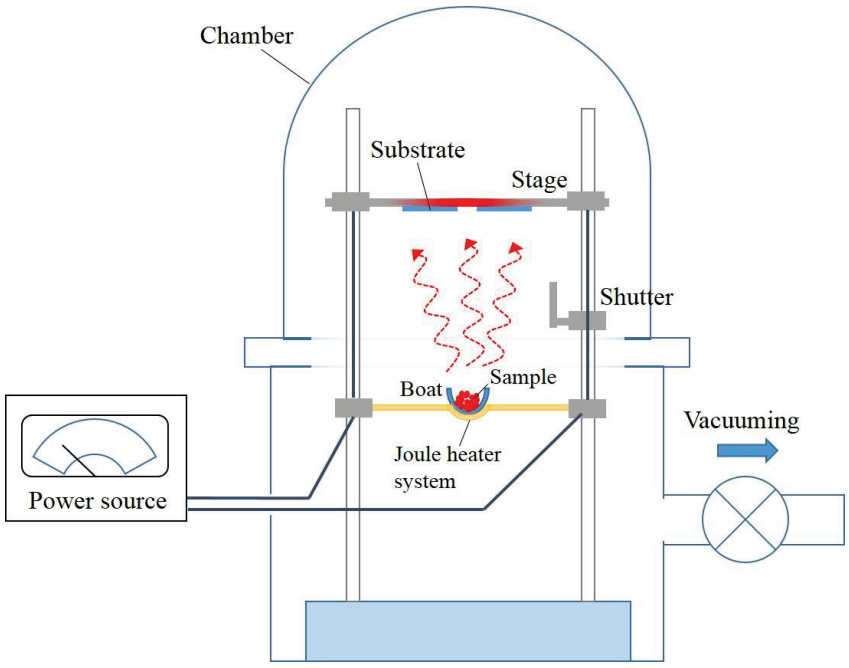


Fig. 4-2: Schematic of organic material deposition system in vacuum chamber.

Various techniques are available for processing soluble high molecular organic semiconductors films from the liquid phase including spin coating casting, spraying, printing, and soluble precursor

conversion. Spin coating is often used to realize a film due to its simplicity and effectiveness. If the conditions such as spin coating; spin speed, ramping rate, choice of solvent for the polymer solution, drying temperature and time are optimized, the film gets highly qualified with desired thickness and uniformity. However there are some negligible limitations of spin-coting. First is the lack of patterning capability. Second is that a large amount of compounds is required because most of the semiconductor solution is spun-out and wasted. Another is that the polycrystalline films are randomly ordered in a radial fashion from the center area since the solute materials rapidly crystallize. Such limitations could be the reason of a poor carrier mobility compared to the intrinsic mobility of organic semiconductors. One of the technology that overcomes such limitations is an edge-casting method, which uses slowly moving blade to coat polymers with a high crystallinity reaching a single crystalline level [7, 8].

4-1-2 Patterning by photolithography

Photolithography is a process utilized in micro level patterning to selectively remove parts of a thin film. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical (photoresist) on the substrate. A series of chemical treatments then engraves the exposure pattern onto the material underneath the photoresist. Fig. 4-3 depicts the photolithography process flow. It typically begins with coating the substrate with photoresist, whose properties can be modified by exposure to ultraviolet (UV) light. UV light is passed through a photomask that manipulates the phase and/or amplitude to achieve patterned exposure on the photoresist layer. The photomask can be in direct contact with or in proximity to the photosensitive material. Closer distance between the photomask and the material is more preferable to expose the pattern as originally designed. UV exposure lets the photoresists change with their chemical structure and solubility in a designed region. The development of photoresist removes the more soluble regions, leaving behind a patterned layer of photoresist on the substrate. This patterned photoresist acts as an etching mask for underlying film. Uncovered areas are removed by wet/dry etching process. After all, remained photoresist is

stripped and the image from the photomask is replicated on the substrate.

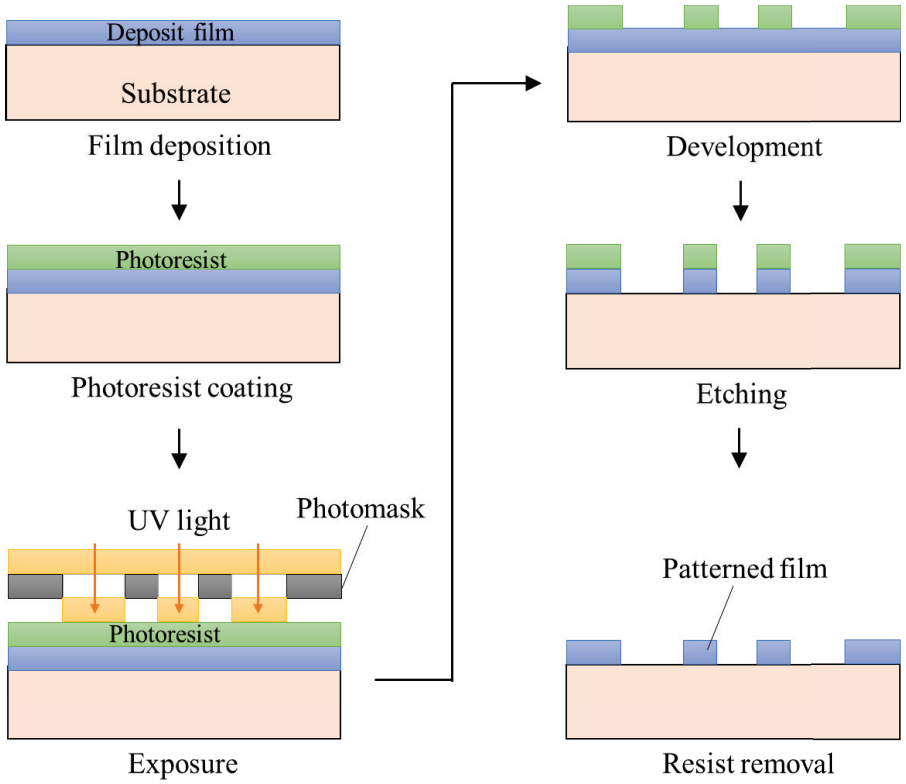


Fig. 4-3: Basic photolithography process flow for patterning a film on a substrate.

4-1-3 Patterning by inkjet printing

Conventionally, thin film formation processes using a vacuum chamber have been used for manufacturing semiconductor devices. As a substrate, silicon wafer or glass substrate are mainly used, and the movement to increase the size of the substrate is remarkable in order to realize cost reduction. Also, along with this, the amount of investment required for production facilities is also becoming enormous [8], a new production process that can lower the production cost even a little is desired. Inkjet printing (IJP) technology is gaining attentions since it is capable of forming a thin film in a large are, under atmospheric pressure, and with high speed. Regarding substrates, technology development using a flexible plastic sheet as a substrate instead of conventional wafers and glasses is underway. Along with other solution-based process, IJP can reduce fabrication costs and lead to large area, cost-effective roll-to-roll production (depicted in Fig. 4-4) of organic electronics [9, 10]. The advantages of IJP technology over the photolithography process for silicon devices including low

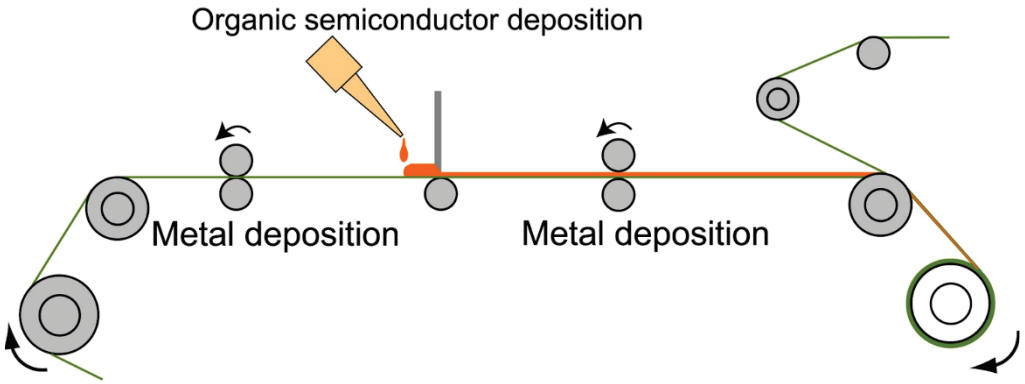


Fig. 4-4: Schematic of the roll-to-roll process method.

capital investment, large area capability, elimination of high-temperature and vacuum deposition processes, compatibility with flexible substrates, ease of customization, quick cycle and turnaround times, robustness, and an environmentally friendly production process [11]. Patterning images can be designed by software program, IJP presents a low-cost and convenient method to create prototype organic devices. Figure 4-5 illustrates the simplicity of the IJP fabrication process in comparison with the photolithography process. Printing combines deposition and patterning all in one step, results in reducing processing steps and material wastages [12].

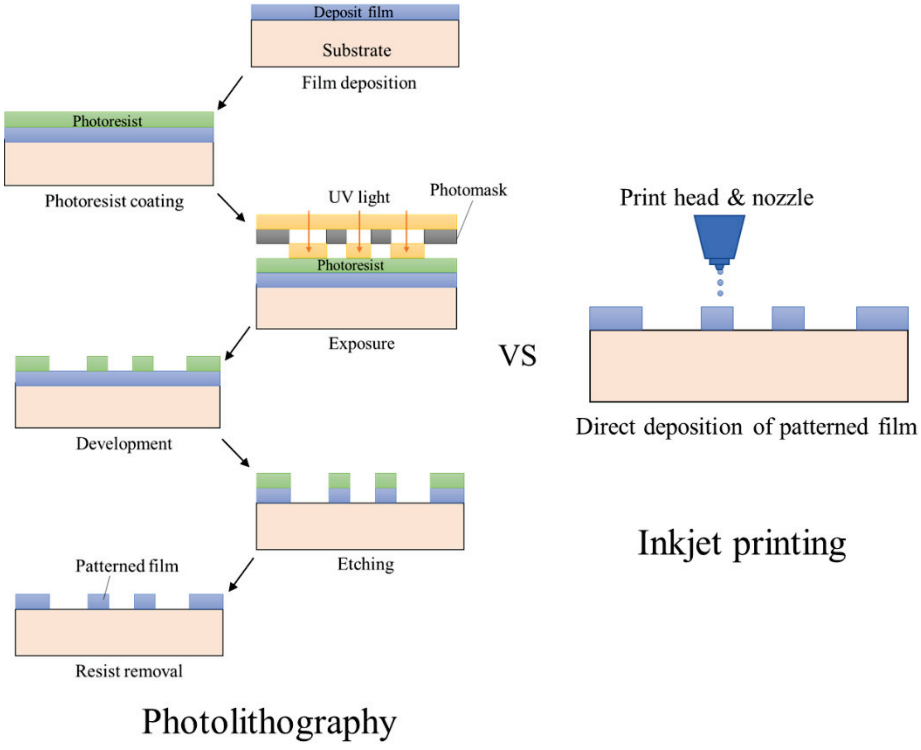


Fig. 4-5: Comparison of fabrication steps of photolithography and IJP.

Despite the many advantages mentioned above, there some challenges and limitations associated with IJP organic electronics material. Because the requirements of printing electronics functions are very different from those of printing visual images, the adaption of inkjet systems for processing organic devices will require careful consideration of many factors;

- ✓ Print-head performance (nozzle geometry, ink delivery, reliability, drive electronics)
- ✓ Solvent compatibility with polymer material and its functionality (solubility, viscosity)
- ✓ Print-head and liquid compatibility
- ✓ Polymer liquid – substrate interactions (surface tension vs. substrate energy)
- ✓ Polymer solidification (adhesion, mechanical integrity, functionality)
- ✓ Accuracy of placement and alignment

More specifically when using IJP for OFETs fabrication, technological concerns pertain to film continuity multilayer registration and alignment, device resolution and ink formulation. Researchers are actively addressing these technological challenges in order to develop a versatile IJP technology that can gain further momentum in the field of organic or printed electronics. Table 4-1 summarizes the strengths and drawback of each patterning technique.

Table 4-1: Properties, representative chemical structure, and carrier mobility of organic semiconductor materials used in OFETs with a comparison to silicon.

Patterning techniques	Strengths	Drawbacks
Shadow mask	- Simple, robust process - Enabled patterning of evaporated source/drain contacts and organic film - Cost-effective, large-area - Direct deposition on the surface	- Limited feature resolution - Difficult to pattern multilayers and circuits - Lack of alignment mechanism - No applicable to solution-processed polymers
Photolithography	- High feature resolution - Precise device definition - Ease of integration, standard IC compatible process - Enables higher complexity devices/circuits - Mature technology – provides a good starting point for building and studying OFET circuits	- Higher process complexity - Issues with solvent compatibility - Requires a compatible and robust making layer - Etching solutions and developers may cause damage to polymer films
Inkjet printing	- Non-contact, additive printing process - Direct patterning - Minimum material consumption - Low cost, fewer steps - Custom circuit design	- Typical system resolution: ~25μm, limited by spreading of ink droplet on the substrate - Film non-uniformity and discontinuity - Requires precise control of viscosity and careful choice of solvents
Hybrid photolithography/inkjet printing	- Non-disruptive patterning of polymer semiconductor layer by inkjet printing - High resolution by photolithography - Bridges the transfer to an all-printed	-Reliant on photolithography as a temporary solution for defining critical dimensions of the transistor

4-1-4 Self Assembled Monolayer (SAM)

When forming organic semiconductor layer on the substrate by vacuum vapor deposition method, self-assembled monolayer (SAM) is introduced to homogenize the arrangement of organic molecules. The film formation of SAM is a technique applying the self-aggregation effect of molecules and is chemically reasonable technology. The name "Self-assembled" is because molecules and atoms have autonomous order and create a uniform structure. It is known that when a monomolecular film formation by this chemical reaction is used for the gate insulating film of OFETs, the reactive functional groups of the molecule react with the insulating film with adsorption, and are evenly arranged by intermolecular interaction [13]. When proper organic semiconductors are deposited thereon, an organic semiconductor layer is formed on the SAM layer. Then, the electric field on the surface of the insulating film appearing due to the application of the gate voltage becomes uniform, and as a result, carriers tend to be accumulated on the surface of the oxide film. Figure 4-6 shows the process of SAM deposition on an oxide film.

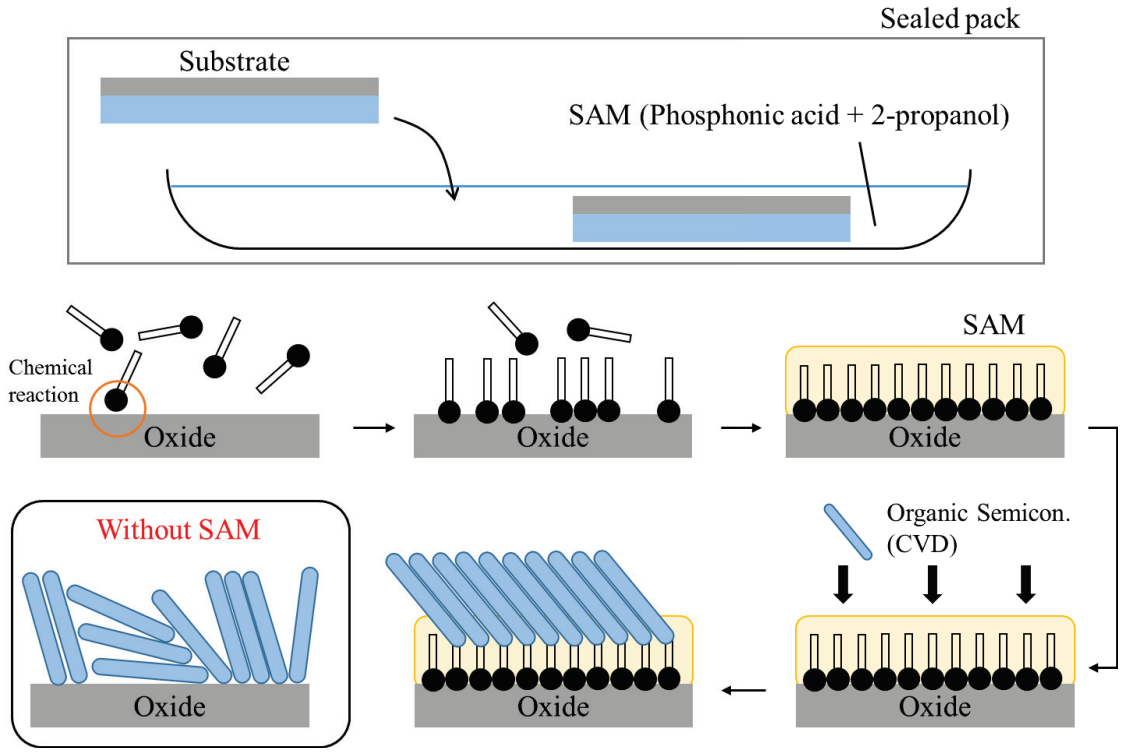


Fig. 4-6: Process flow of SAM layer forming on an oxide film [2].

The interface between the semiconductor layer and the oxide film in transistors is a decisively important part in which a channel (carrier path) is formed. By sandwiching the SAM layer, uniform molecular orientation as shown in Fig. 4-6 is achieved, and is expected to be a film with high crystallinity. If the crystallinity is high, an influence of carrier trapping at oxide interface and crystal grain boundaries can be suppressed. This leads to the realization of OFETs with high mobility [14].

4-2: Fabrication of OFETs and circuit

This section explains the device fabrication process employed in this research. The purpose of this fabrication is to investigate OFETs current characteristics and to verify that circuit based on organic device can operate or not. Here, the target circuit is CMOS inverter and ring oscillator. The fabrication starts with preliminary experiment, and continues to gate patterning, insulator (VIA) patterning, organic semiconductor patterning, and source & drain contact patterning.

4-2-1 Preliminary experiment

To design a ring oscillator circuit, as a first step, it is necessary to know the performance of a single transistor because ring oscillators are usually consists of an odd number of CMOS inverters. A simple CMOS inverter is consists of a single p-type transistor and n-type transistor. Figure 4-7 shows a circuit diagram of a 5-stage ring oscillator in logic level, a CMOS inverter in transistor level and 5-stage ring oscillator in transistor level.

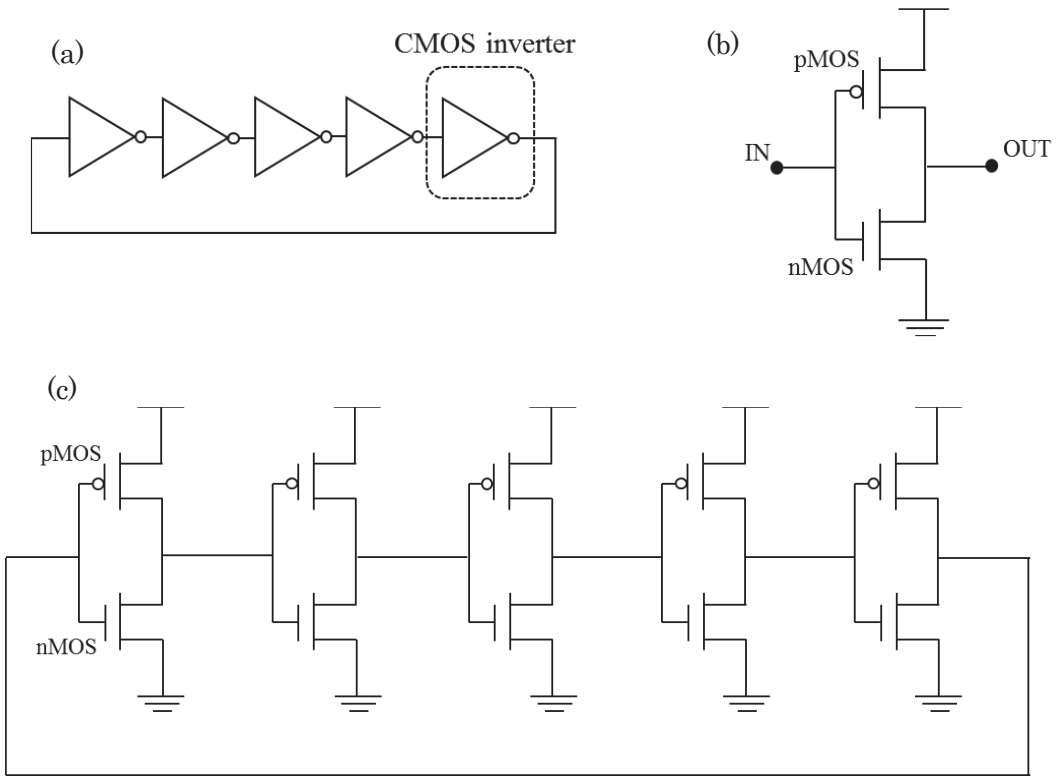
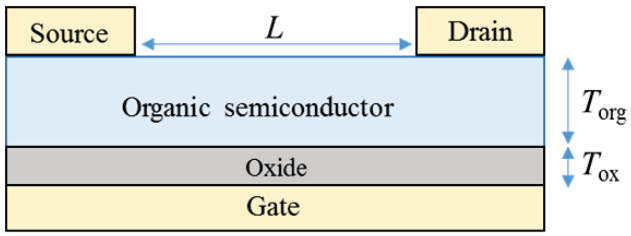


Fig. 4-7: circuit diagram of (a) 5-stage ring oscillator in logic level, (b) CMOS inverter in transistor level, and (c) 5-stage ring oscillator in transistor level.

Ideally, CMOS inverters constituting a ring oscillator are designed to have the balanced current of p-type and n-type MOSFET, that is, both of types should have the same threshold voltage ($|V_{th}|$) and the same current transfer curve. However, it was not clear the fabricated p-type and n-type MOSFET have the same $|V_{th}|$ value. Therefore, some experimental devices are fabricated for estimating the properties such as V_{th}, the mobility and the saturation current values. The device properties used for the preliminary measurement are summarized in table 4-2. Fabricated devices in this step aren't encapsulated, therefore, the measurement has to be done in the grove BOX with argon atmosphere and without any lighting interaction. Figures from 4-8 to 4-10 show measured *IV* characteristics of experimental p-type MOSFETs and Figures from 4-11 to 4-12 show measured *IV* characteristics of experimental n-type MOSFETs (only successfully measured data are shown).

Table 4-2: Summary of device properties used for the preliminary measurement.

Structure	Bottom-gate Top-contact 
Channel size	Length = 10, 20, 40, 50, 100, 200, 500, 1000 [um] Width = 200 [um]
Substrate	Heavily doped p-type silicon
Insulator	Al_2O_3 deposited by ALD method Tox = 150nm
Semiconductor	n-type: Perylenetetra carboxyldiimide (PTCDI) Torg = 50nm p-type: Dinaphtho-Thieno-Thiophene (DNTT) Torg = 50nm Physical vapor deposition (PVD)
Electrode	Gate: Cr + Au Source and Drain: Au
Patterning	Metal mask and photolithography
SAMs layer	Tetra-decyl-phosphonic acid (0.2 mmol/L)

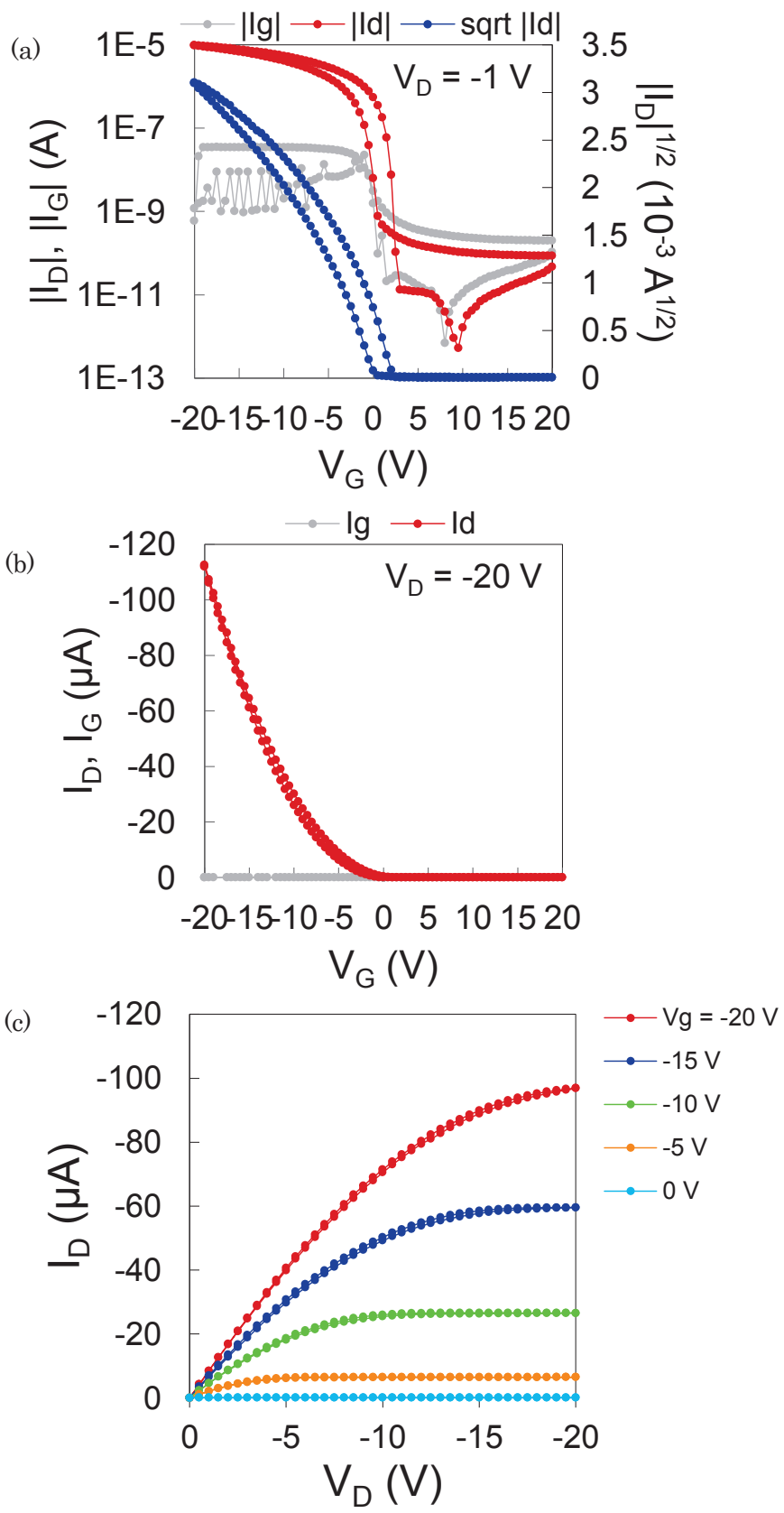


Fig. 4-8: *IV* characteristics of experimental p-type MOSFET, L=50um, W=500um: (a) I_{ds}- V_{gs} characteristics at V_{ds} = -1V, (b) I_{ds}- V_{gs} characteristics at V_{ds} = -20V, and (c) I_{ds}- V_{ds} characteristics at V_{ds} = 0, -5, -10, -15, -20V.

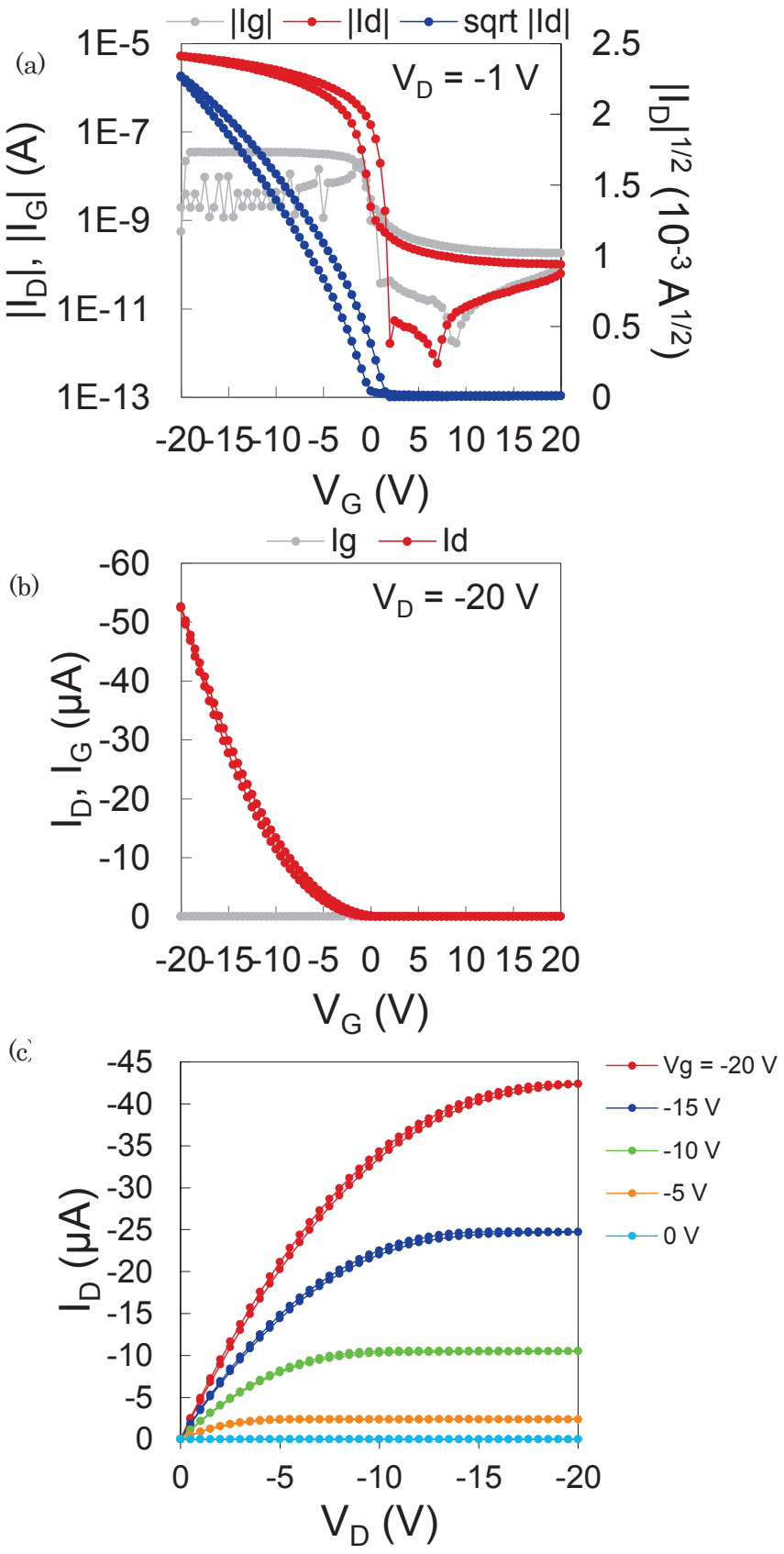


Fig. 4-9: *IV* characteristics of experimental p-type MOSFET, L=100um, W=500um: (a) I_{ds}- V_{gs} characteristics at V_{ds} = -1V, (b) I_{ds}- V_{gs} characteristics at V_{ds} = -20V, and (c) I_{ds}- V_{ds} characteristics at V_{ds} = 0, -5, -10, -15, -20V.

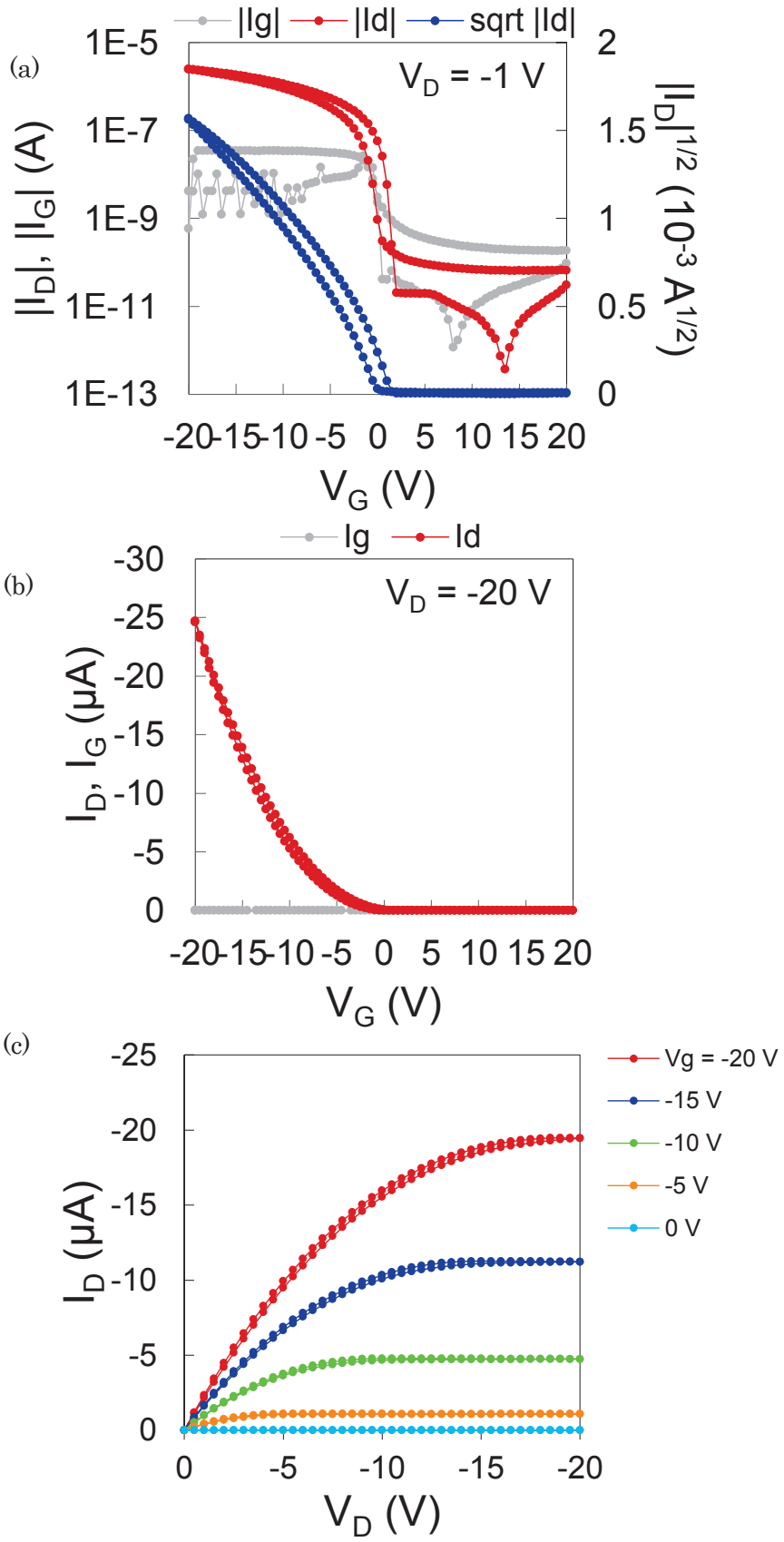


Fig. 4-10: *IV* characteristics of experimental p-type MOSFET, L=200um, W=500um: (a) I_{ds}- V_{gs} characteristics at V_{ds} = -1V, (b) I_{ds}- V_{gs} characteristics at V_{ds} = -20V, and (c) I_{ds}- V_{ds} characteristics at V_{ds} = 0, -5, -10, -15, -20V.

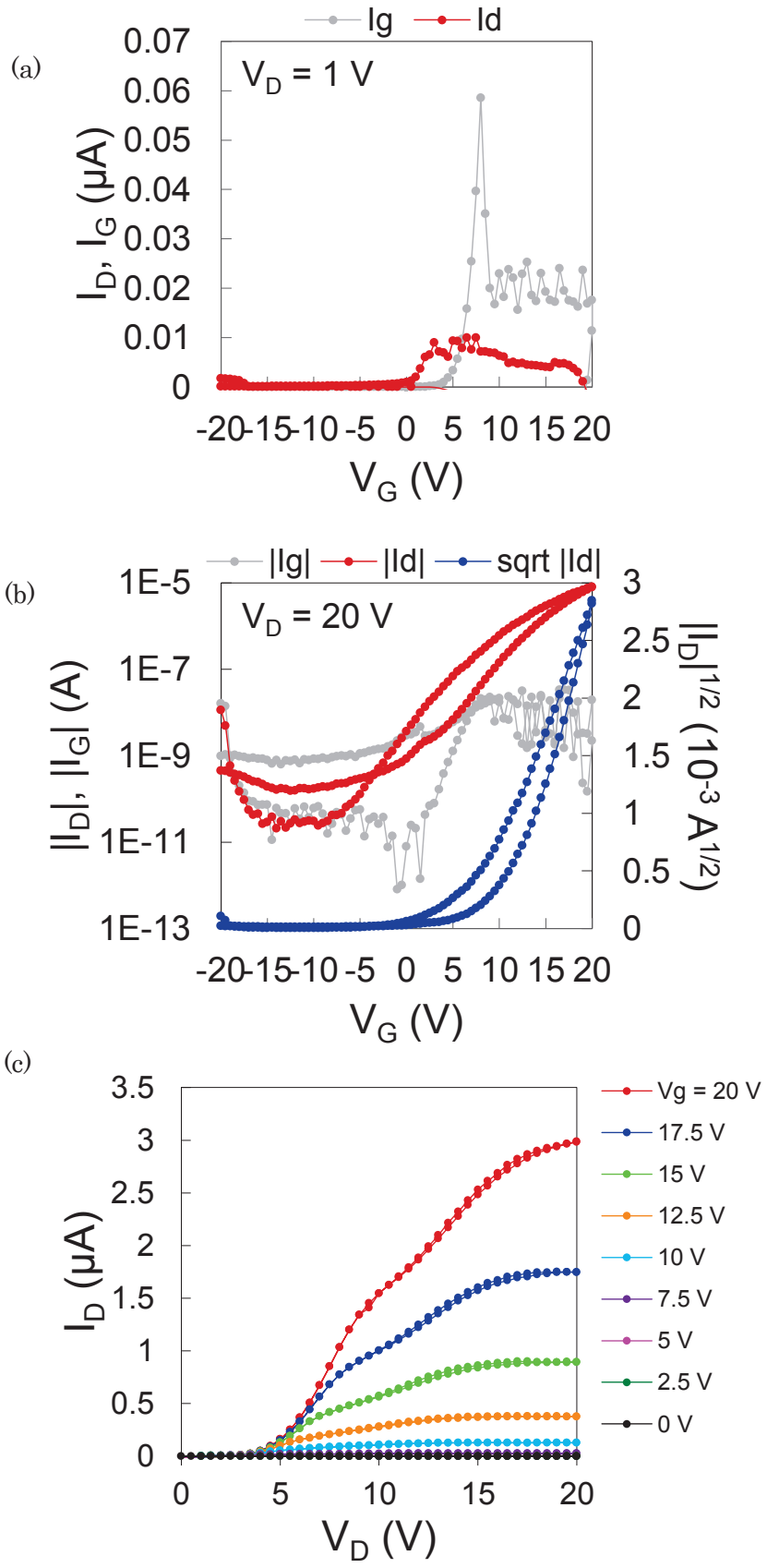


Fig. 4-11: *IV* characteristics of experimental n-type MOSFET, L=10um, W=500um: (a) I_{ds}- V_{gs} characteristics at V_{ds} = -1V, (b) I_{ds}- V_{gs} characteristics at V_{ds} = -20V, and (c) I_{ds}- V_{ds} characteristics at V_{ds} = 0 ~ -20V, 2.5V step.

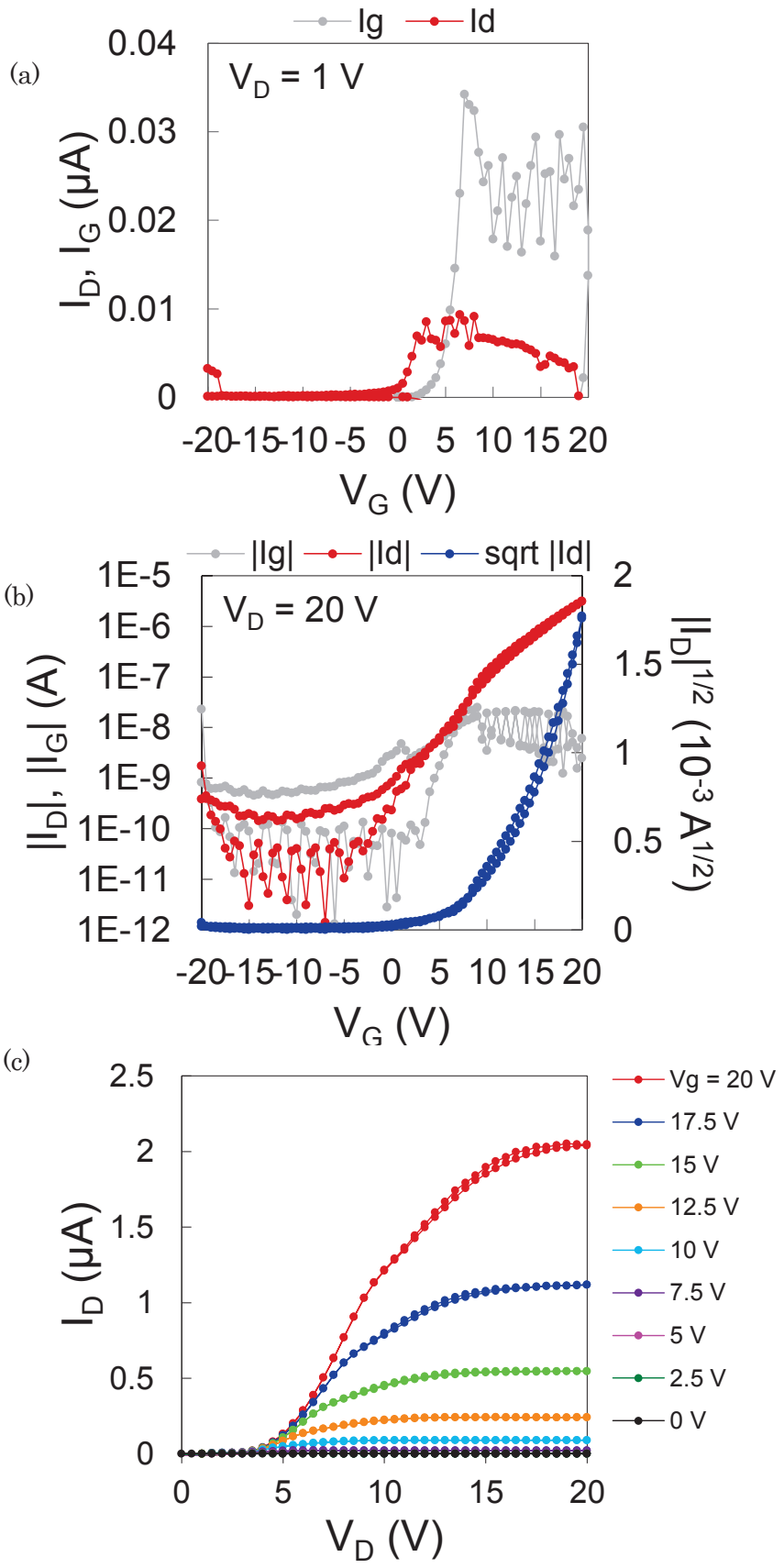


Fig. 4-12: *IV* characteristics of experimental n-type MOSFET, L=20um, W=500um: (a) I_{ds}- V_{gs} characteristics at V_{ds} = -1V, (b) I_{ds}- V_{gs} characteristics at V_{ds} = -20V, and (c) I_{ds}- V_{ds} characteristics at V_{ds} = 0 ~ -20V, 2.5V step.

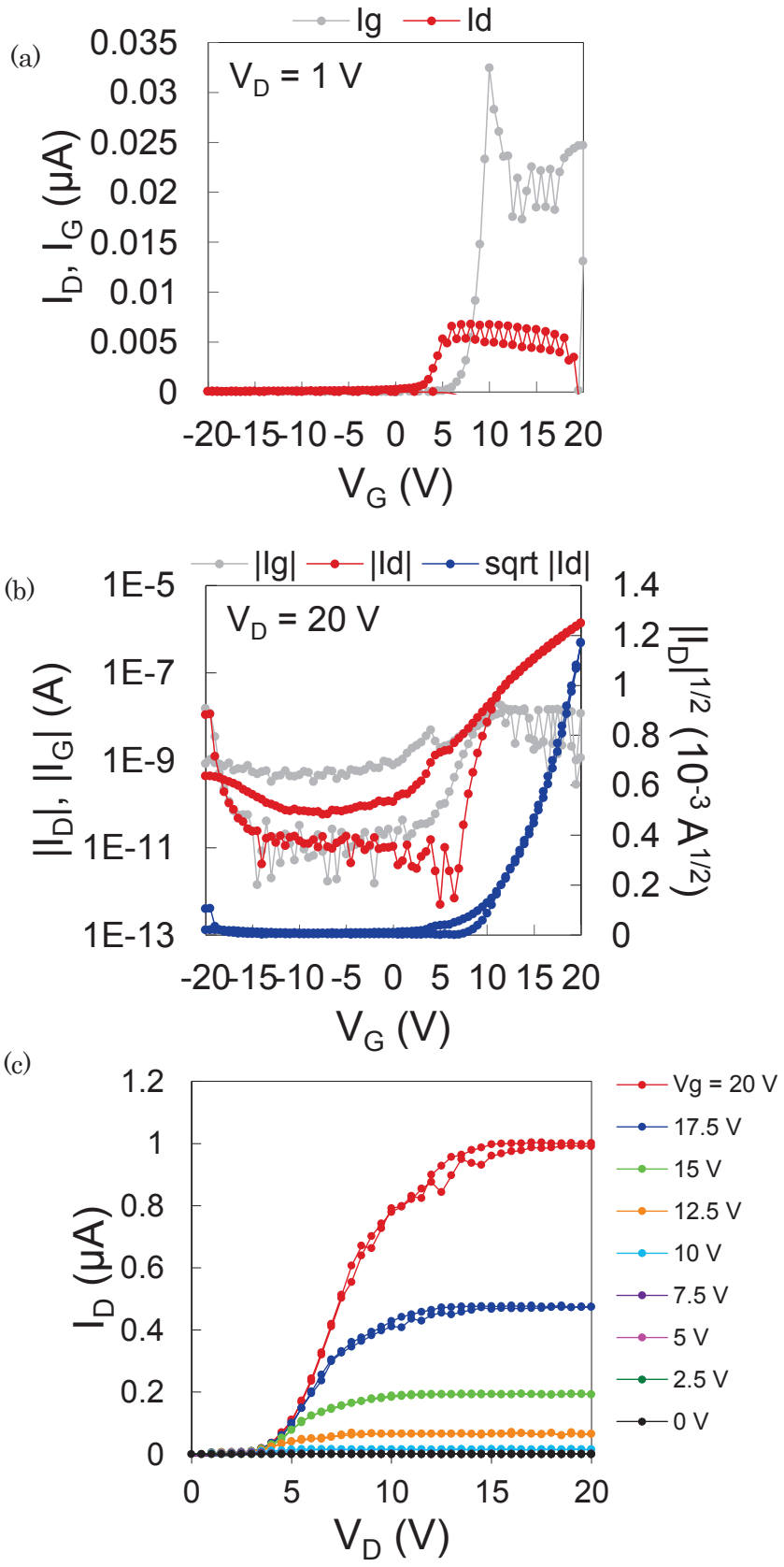


Fig. 4-13: *IV* characteristics of experimental n-type MOSFET, L=40um, W=500um: (a) I_{ds}- V_{gs} characteristics at V_{ds} = -1V, (b) I_{ds}- V_{gs} characteristics at V_{ds} = -20V, and (c) I_{ds}- V_{ds} characteristics at V_{ds} = 0 ~ -20V, 2.5V step.

From those measured data, p-type MOSFETs show preferable transistor behaviors that the threshold voltage values are stabled about V_{gs} = 0V, the current transfers smoothly in both linear region and saturation region, the On/Off ratio is over 10^4, and the estimated mobility is over 0.5 cm^2/Vs. on the other hand, p-type MOSFETs show poor transistor performances that threshold voltage values are unstable and fluctuated around V_{gs} = 5~7V, the subthreshold swings aren't steep, and the estimated mobility is 0.05 cm^2/Vs, while the On/Off ratio is stile kept at 10^4.

Based on the measured results and mobility estimations, the photomasks for patterning gate, insulator (VIA hole), semiconductor and source & drain are designed. The pattern of the characteristic measuring transistors, CMOS inverters, ring oscillators (5-stage, 7 stage) are designed in one photomask with paying attention to following points;

- ✓ It is necessary to design the channel length L and channel width W of transistors used in the CMOS inverter and the ring oscillator considering the current value, the mobility and the threshold value
- ✓ With reference to the experimental device fabrication, the channel length L has to be set as reasonable value (If the channel length is too short, resist solution may remain on photolithography or gold etching may not be successful)
- ✓ Designing those elements around the center of substrate in order to seal the device part in argon atmosphere after circuit fabrications (this is mainly for the protection of organic materials from oxidations)

The transistor size W/L is determined from the threshold value V_{th}, the insulator (Al_2O_3) relative dielectric constant ε_r, the insulator film thickness T_{ox}, the capacitance C of the insulator, and the mobility μ that is calculated from trans-conductance gm (= $\partial I_{ds}/\partial V_{gs}$) of the measured current characteristics. Those calculated parameters are shown in table 4-3.

Table 4-3: Summary of calculated parameters for balancing n-type and p-type MOSFET.

	n-type	p-type
μ (cm^2/Vs)	0.05	0.5
L (um)	20	100
dL (total)	20	20
W (um)	800	230
W/L	40	2.3
$\mu W/L$	2	1.15
ε_r	8.3	8.3
T_{ox}(nm)	150	150
C_i(pF/cm2)	48970	48970
C (pF)	15.6704	13.51572
V_{th}	5	0
V_{DD}	20	20

Normally, in a CMOS inverter, the threshold value of the inverter V_{thinv} is defined as $V_{thinv} = V_{in} = V_{out}$, and $V_{thinv} = V_{DD} / 2$ is preferable. Here V_{DD} is a power source value and corresponding to the drain voltage. However, the fabricated MOSFETs show a large difference in threshold voltage between p-type and n-type. Therefore, the device size is adopted so that the drain current of both p-type and n-type in the saturation region becomes equal. Using saturation current equation (3-53), saturation current is obtained as n-type: $I_{ds,n}$ = 11.01825μA, p-type: $I_{ds,p}$ = 11.2631μA. By designing the channel width of the n-type device to be large, it becomes possible to compensate for the low mobility and equalize the current value to p-type.

In order to form the transistors and circuits on the glass substrate, four photomasks have to be designed for gate, insulator (VIA hole), semiconductor, and source & drain. The layout of those masks are designed by "Tanner L-edit IC" made by Mentor Graphics Corporation. This L-edit can design a full image of IC such as transistors which is the most fundamental element in IC, electrodes, metal pads for measuring, and the others. Figure 4-14 displays the drawing of inverters in L-edit. Full layout of designed circuits is depicted in Fig 4-15 and the circuit part is depicted in Fig 4-16.

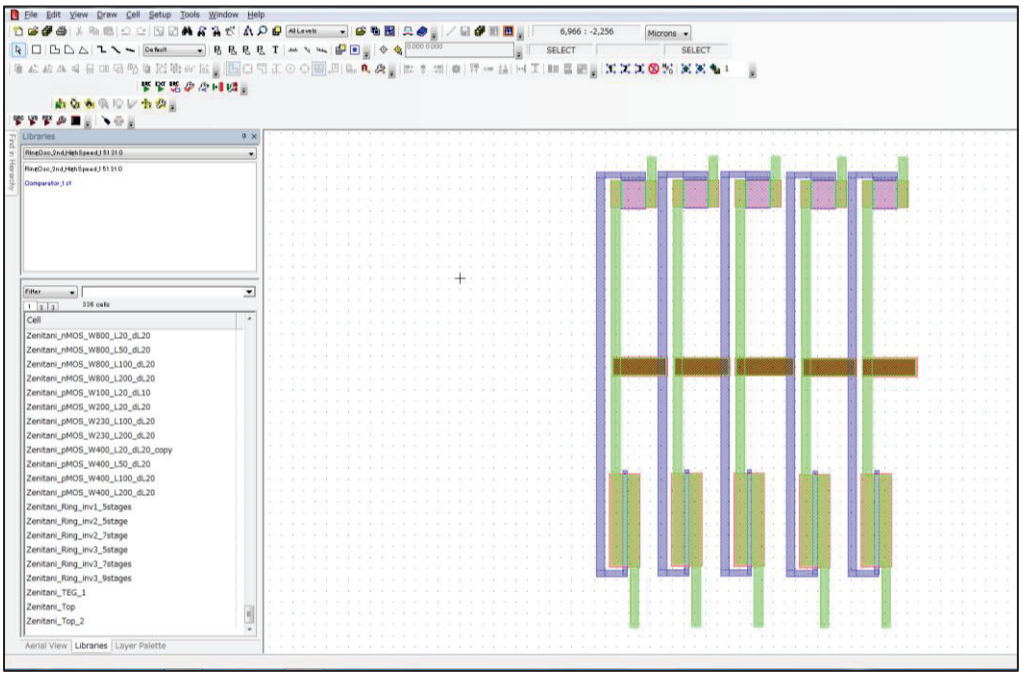


Fig. 4-14: L-edit working window of drawing the

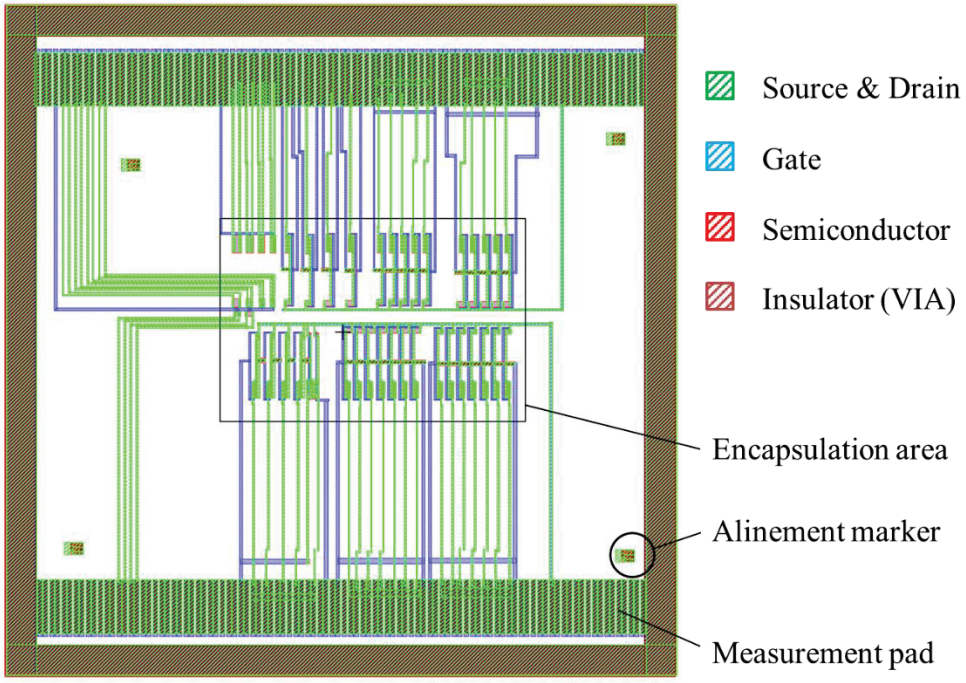


Fig. 4-15: Full layout of designed circuits, all photomask patterns are overlaid.

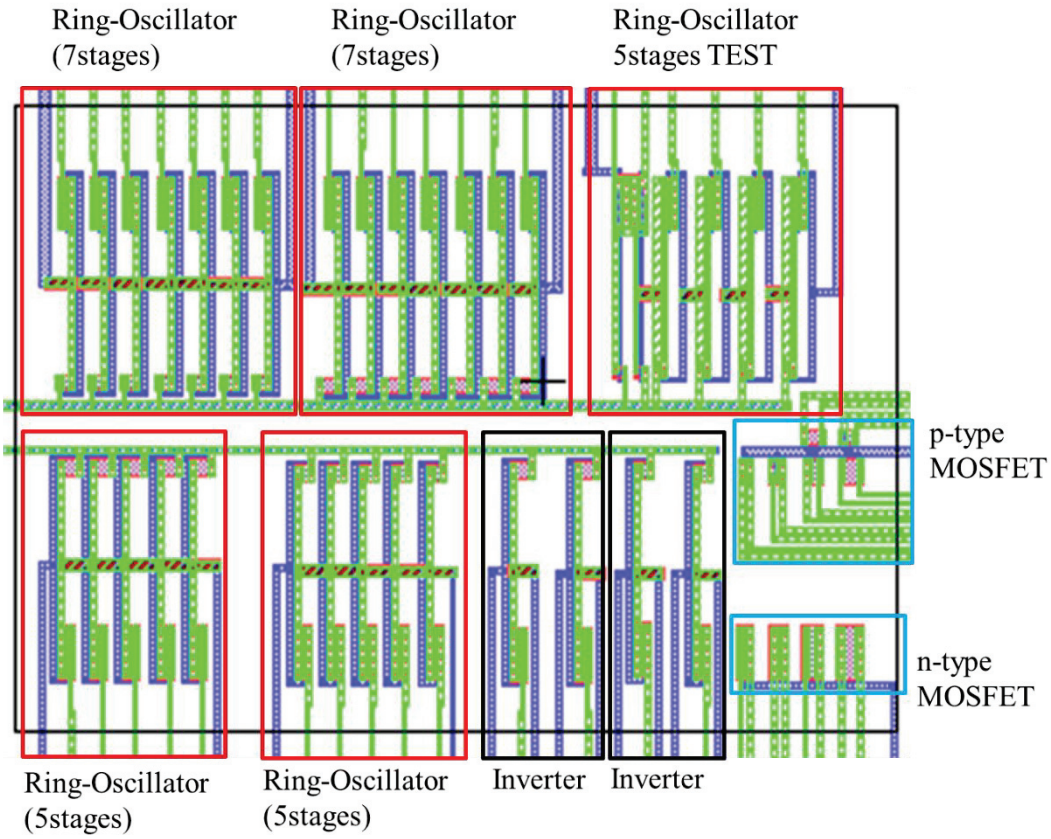
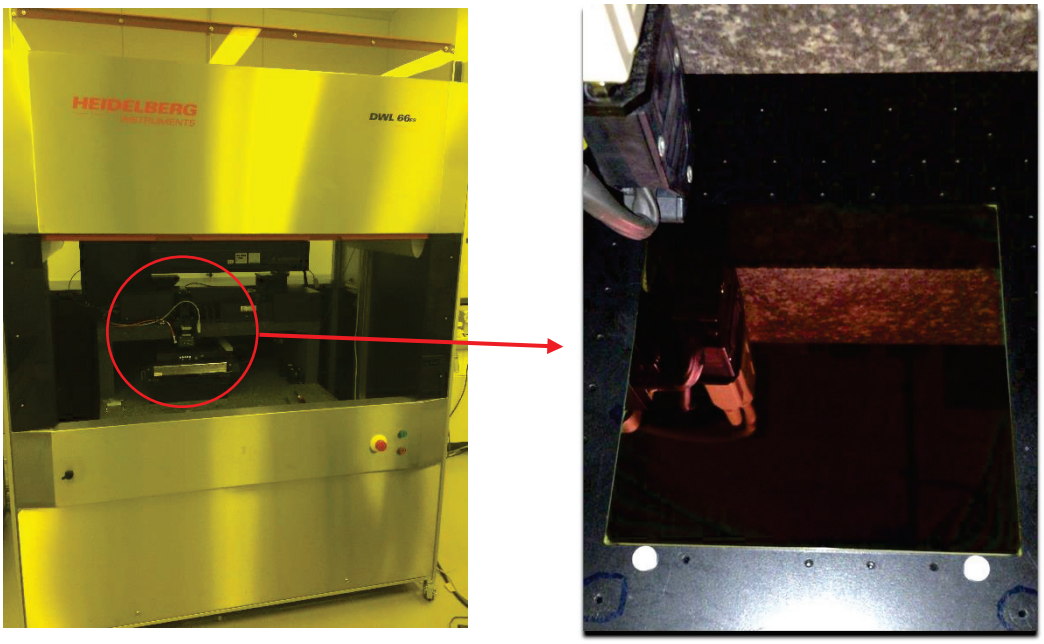
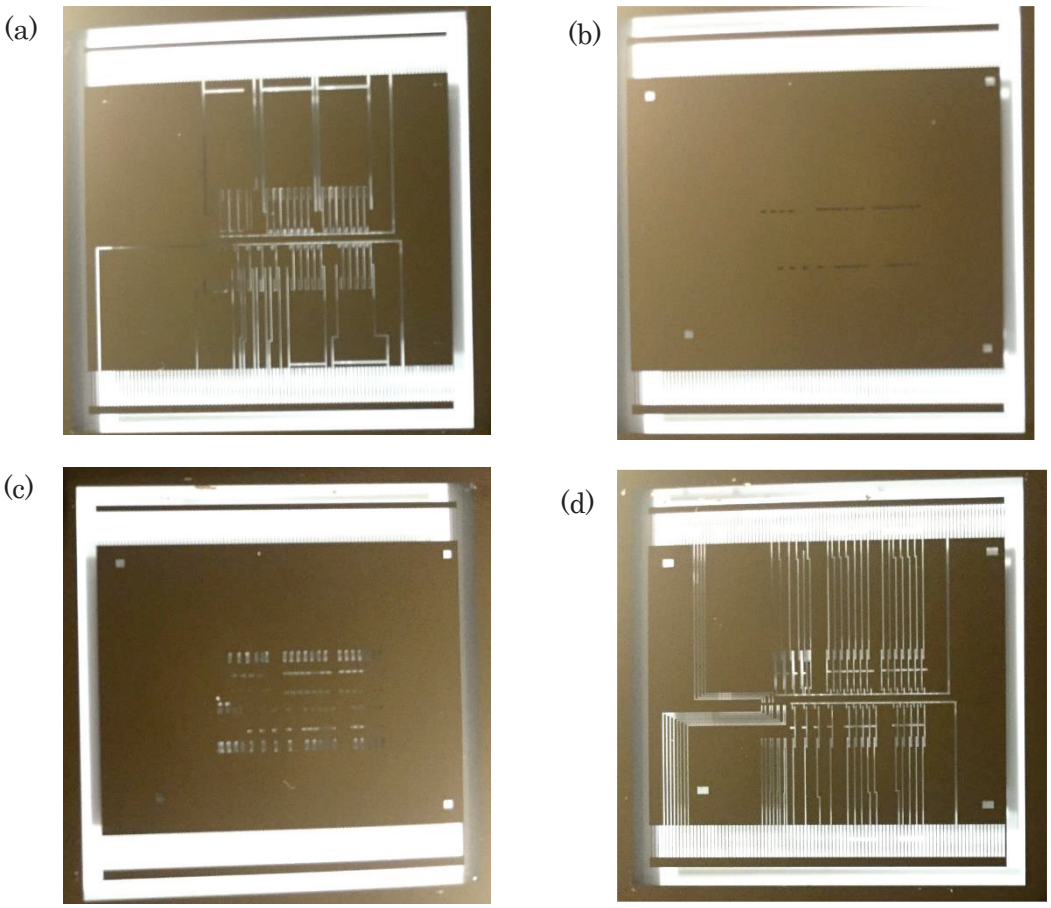


Fig. 4-16: Partial layout of designed circuits and transistors, all photomask patterns are overlaid.

For making the photomask, a laser drawing apparatus (DWL66FS) manufactured by JLC (showed in picture 4-1) is used. When producing a photomask, use a mask blank which is a glass substrate coated with photoresist on chromium/chromium- oxide film of about 100 nm thickness. Each designed mask layout is read into and laser drawing is performed with this system. After exposure, a fine pattern of photoresist is formed by development. Thereafter, the resist is removed. Each photomask is displayed in picture 4-2.



Picture 4-1: Photomask laser drawing apparatus (DWL66FS) manufactured by JLC) and its internal drawing stage.

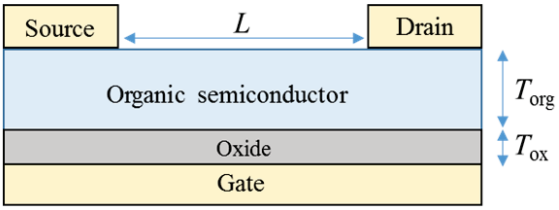


Picture 4-2: Fabricated photomasks (a) gate patterning mask, (b) insulator (VIA) patterning mask, (c) organic semiconductor (OSC) patterning mask, and (d) source & drain patterning mask.

4-2-2 Fabrication of OFETs

This section explains each fabrication process; gate patterning, insulator deposition and SAM treatment, organic semiconductor patterning, source and drain patterning. The OFETs properties are summarized in table 4-4. Adopted substrate is changed to the glass substrate. All of the patterning are performed by photolithography.

Table 4-4: Summary of device properties used for OFETs *IV* characteristics analysis.

Structure	Bottom-gate Top-contact 
Channel size	P-type (L, W) = (50, 400), (100, 400), (200, 400), (100, 230), (200, 230) N-type (L, W) = (20, 800), (50, 800), (100, 800)
Substrate	Glass substrate
Insulator	Al_2O_3 deposited by ALD method Tox = 150nm
Semiconductor	n-type: Perylenetetra carboxyldiimide (PTCDI) Torg = 50nm p-type: Dinaphtho-Thieno-Thiophene (DNTT) Torg = 50nm Physical vapor deposition (PVD)
Electrode	Gate: Cr + Au Source and Drain: Au
Patterning	Photolithography
SAMs layer	Tetra-decyl-phosphonic acid (0.2 mmol/L)

- Gate patterning (illustrated in Fig. 4-17)

(1) Cleaning the glass substrate by acetone and IPA (isopropyl alcohol) with ultrasonic cleaning for 1 minute in each, and drying

(2) Placing photoresist by spin-coating (3500 rpm, 40s) and pre-baking for 2 mins at 90 °C

(3) Alignment and UV exposure for 20s using gate photomask and baking for 90s at 110 °C

(4) Soaking the substrate in the developer for 60s and cleaning with running water

(5) Gate electrode deposition (Cr - Au - Cr) by physical vacuum vapor deposition (PVD)

(6) Removing photoresist (lift-off) and ultrasonic cleaning

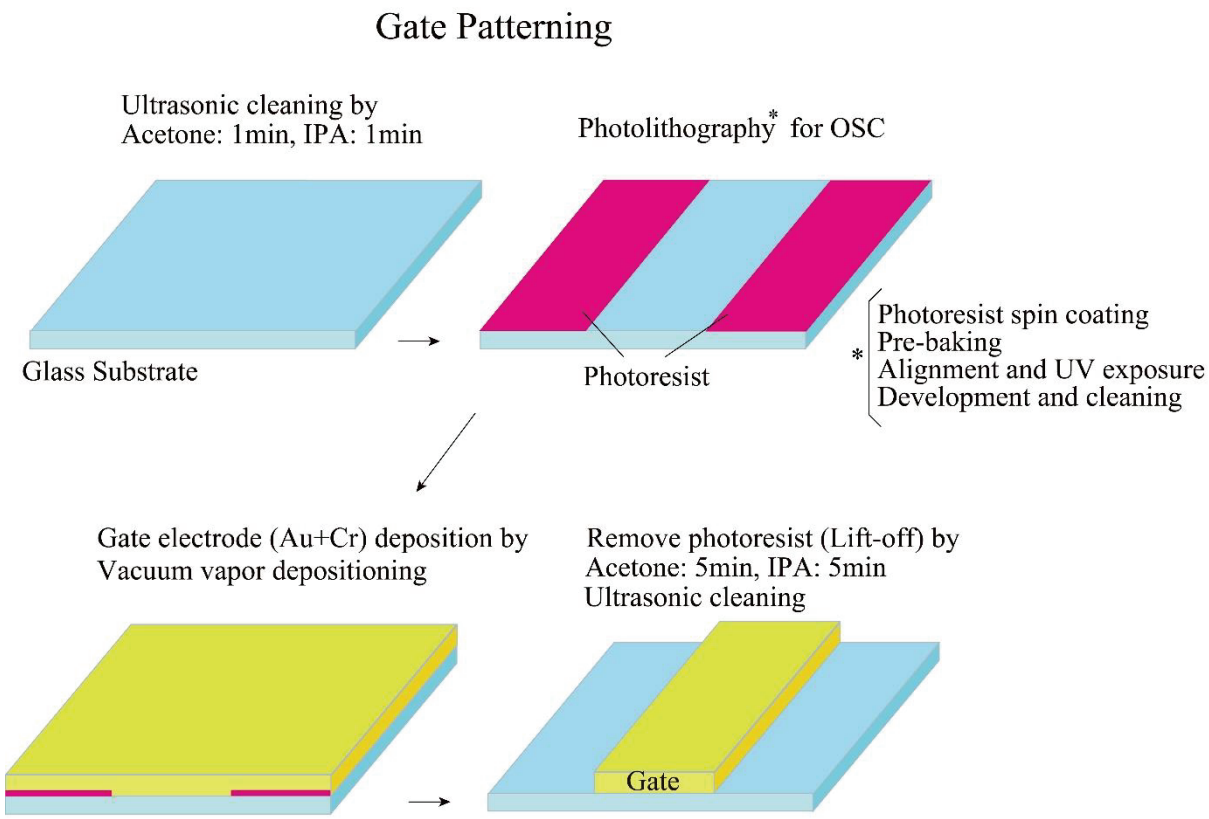


Fig. 4-17: Gate patterning process flow by photolithography.

- Insulator deposition and SAM treatment (illustrated in Fig 4-18)

(1) Deposition the insulator (Al_2O_3) on the substrate by ALD

(2) O_2 ashing and UV ozone cleaning to eliminate the impurities from the substrate. Soaking the substrate in Tetra-decyl-hosphonic acid solution for 10 hours to form SAM layer on the insulator

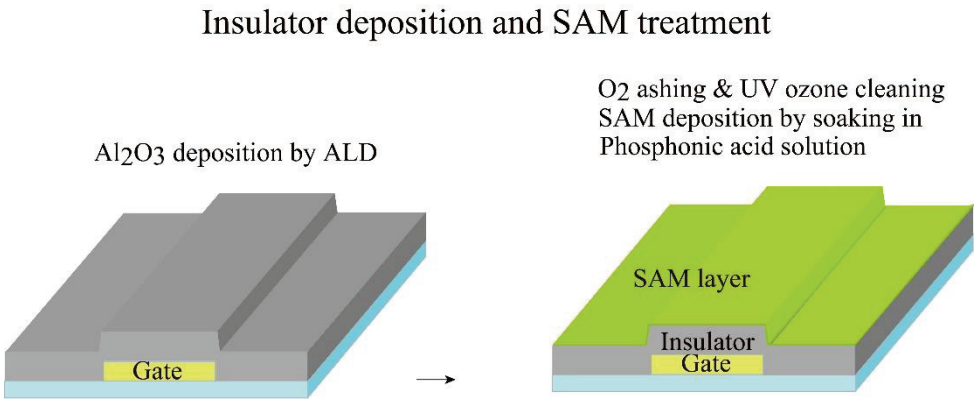


Fig. 4-18: Insulator deposition and SAM treatment on the insulator.

- Organic semiconductor patterning (illustrated in Fig. 4-19)

  (1) Ultrasonic cleaning and drying with baking (60 °C, 2 mins)

  (2) Organic semiconductor (OSC) deposition by PVD for p-type and n-type. (n-type deposition condition: 130 °C, 5.0 x 10^{-3} Pa, 1 Å/s / p-type deposition condition: 80 °C, 1.5 x 10-2 Pa, 1 Å/s)

  (3) Source and drain electrode deposition by PVD

  (4) Placing photoresist by spin-coating (500 rpm, 5s → 2000 rpm, 40s) and pre- baking for 20 mins at 60 °C

  (5) Alignment and UV exposure for 3s using semiconductor photomask and baking for 20 mins at 60 °C

  (6) Soaking the substrate in the developer for 90s twice and spin blowing (1000rpm, 20s)

  (7) Au etching by AURUM and cleaning with running water

  (8) Removing OSC by O_2 ashing

  (9) Removing the photoresist by strip solution (baking the substrate for 60s twice, dripping the strip solution and spin blowing 1000rpm, 20s)

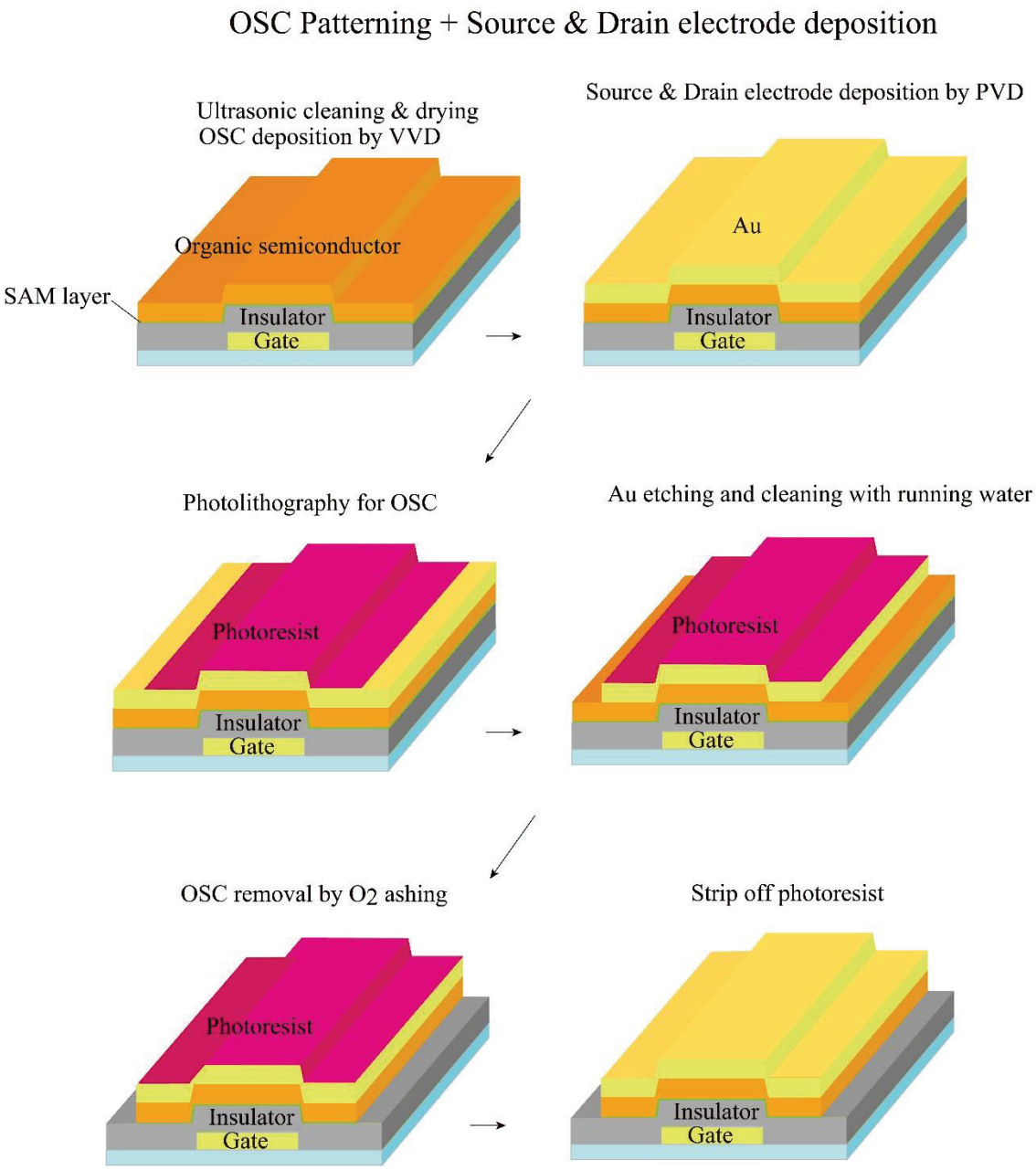


Fig. 4-19: Process flow of OSC patterning and source & drain deposition.

- Source and Drain patterning (illustrated in Fig. 4-20)

(1) Placing photoresist by spin-coating (500 rpm, 5s → 2000 rpm, 40s) and pre- baking for 20 mins at 60 °C

(2) Alignment and UV exposure for 3s using source & drain photomask and baking for 20 mins at 60 °C

(3) Soaking the substrate in the developer for 90s twice and spin blowing (1000rpm, 20s)

(4) Au etching by AURUM and cleaning with running water

(5) Removing the photoresist by strip solution (baking the substrate for 60s twice, dripping the strip solution and spin blowing 1000rpm, 20s)

(6) Drying the substrate in a vacuum chamber for 10 hours at 60 °C

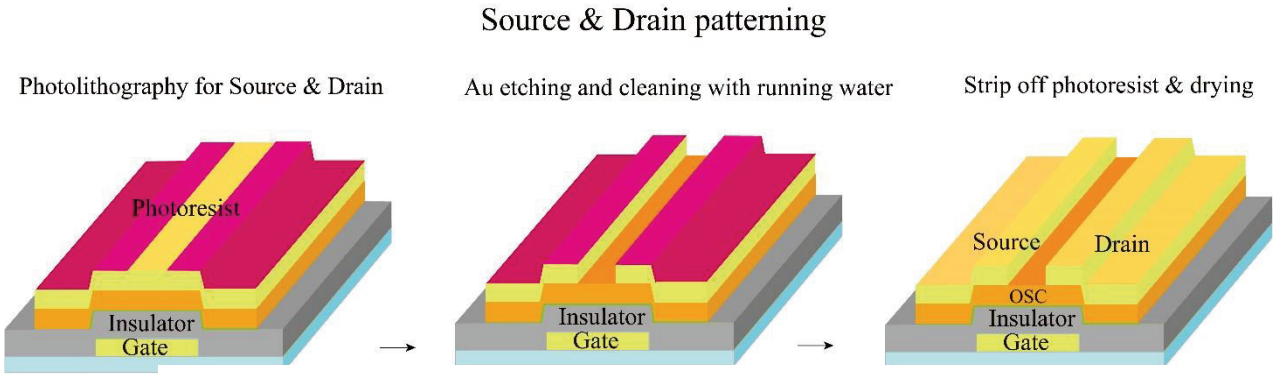


Fig. 4-20: Process flow of source & drain electrode pattering.

After all, the dried substrate is sealed/encapsulated in argon atmosphere. Some organic semiconductor materials show performance degradation in the air. PTCDI that is employed as a n-type material also shows such degradation in the air as depicted in Fig. 4-23. Therefore, a passivation with argon is necessary to preserve the materials and keep the original performance. A sealing glass surface is cleaned with UV ozone irradiation for 10 minutes in order to improve adhesiveness. A cleaned sealing glass is glued to the substrate using a pump syringe applying a cured resin around the rim of the sealing glass. Circuit part must come inside of the sealed part. This is because the properties of the device may be changed if the cured resin is put on the semiconductor portion. After

bonding, ultraviolet rays are irradiated to cure the resin. Picture 4-2 compares the unsealed substrate and the sealed substrate.

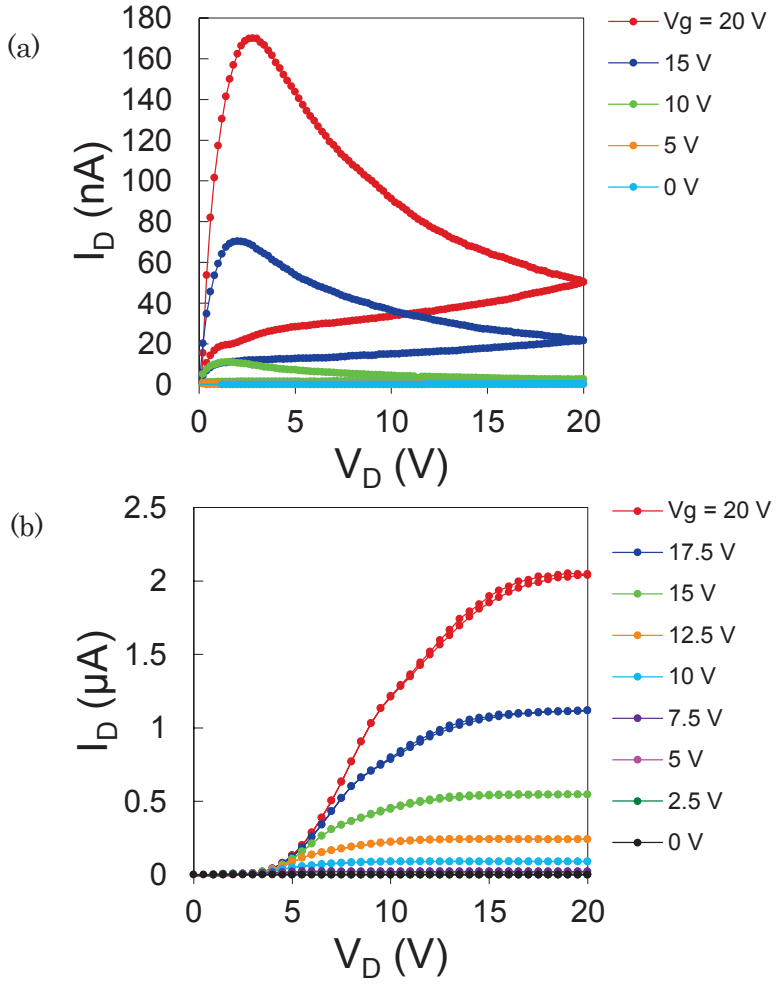
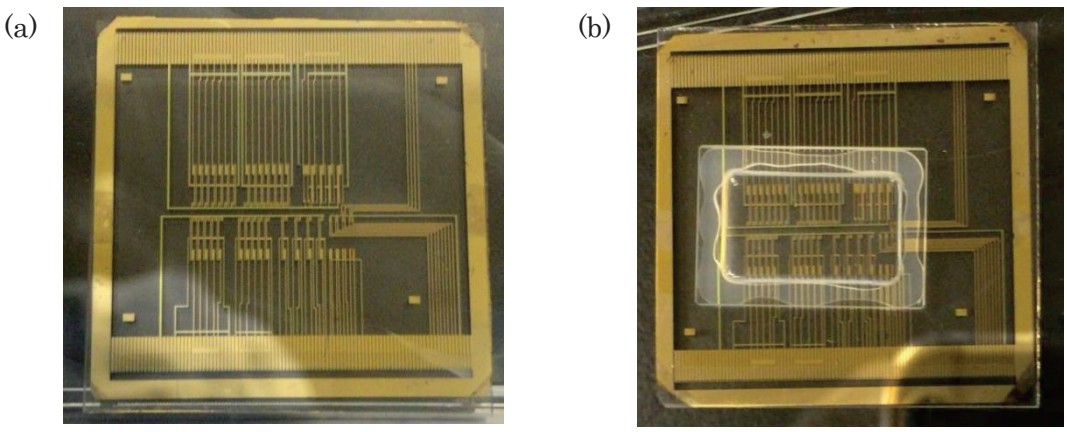


Fig. 4-21: Achievement of passivation observed in fabricated n-type MOSFET; (a) degraded I_{ds}- V_{ds} characteristics and (b) passivated I_{ds}- V_{ds} characteristics.



Picture 4-2: (a) Unsealed substrate and (b) sealed substrate.

4-2-3 Fabrication of circuits

As shown in Fig 4-16, CMOS inverters and ring oscillators are also fabricated on the same substrate in order to keep the compatibility of OFETs and circuits which use OFETs fabricated by the same fabrication technologies. The process flow of circuits is almost same to that of OFETs, but there is one additional patterning of insulator (VIA) before OSC patterning. This VIA hole is necessary to connect each stage (inverter) in the ring oscillator. Those process flow are shown in Fig. 4-24 to 4-26.

- Insulator/VIA hole patterning

(1) Placing photoresist by spin-coating (500 rpm, 5s → 3000 rpm, 30s → 5000rpm, 2s) and pre-baking for 20 mins at 90 °C

(2) Alignment and UV exposure for 10s using insulator (VIA) photomask

(3) Soaking the substrate in the developer for 60s, cleaning with running water, and baking for 20 mins at 120 °C

(4) Al_2O_3 etching by alumina etching solution

(5) Removing the photoresist by ultrasonic cleaning with NMP (N-methylpyrrolidone) and IPA

(6) O_2 ashing for removing organic matters and UV ozone cleaning

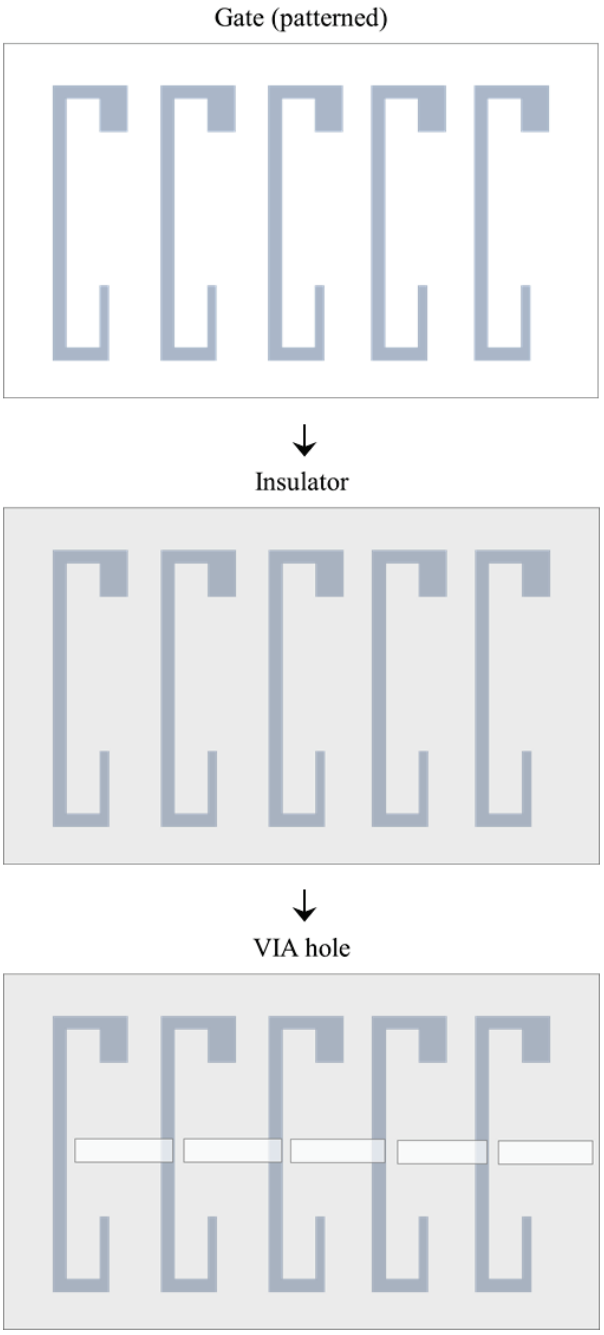


Fig. 4-22: Circuit fabrication process flow from gate patterning to insulator (VIA) patterning.

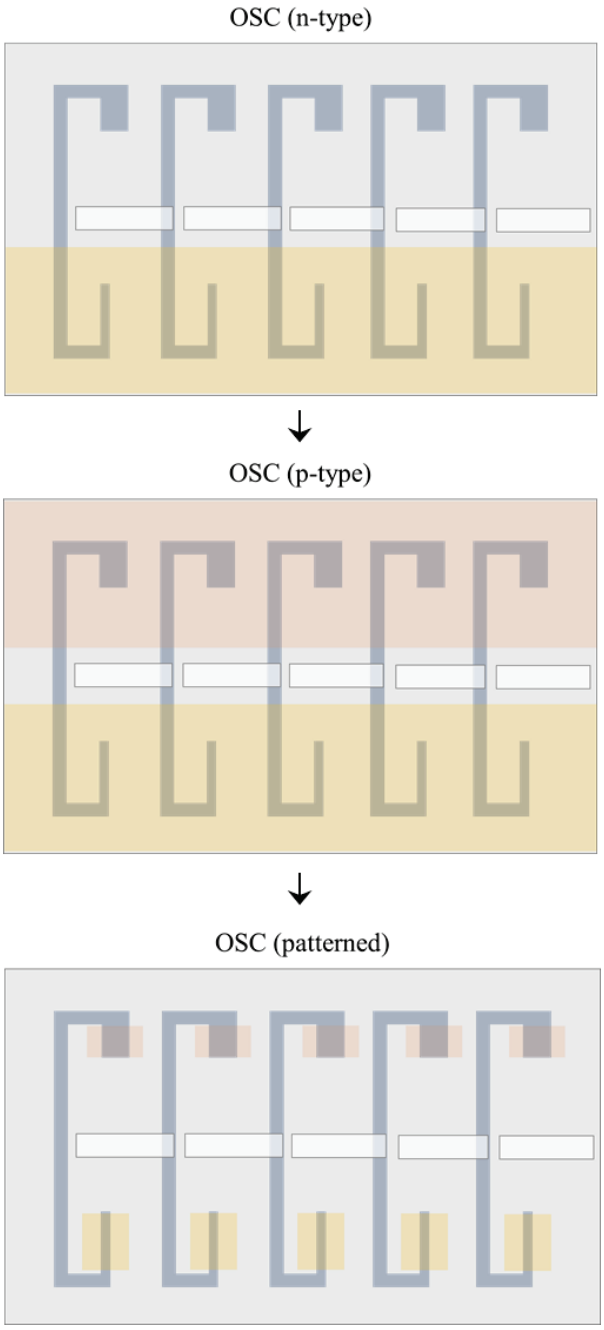


Fig. 4-23: Circuit fabrication process flow from OSC deposition to OSC patterning for both p-type and n-type.

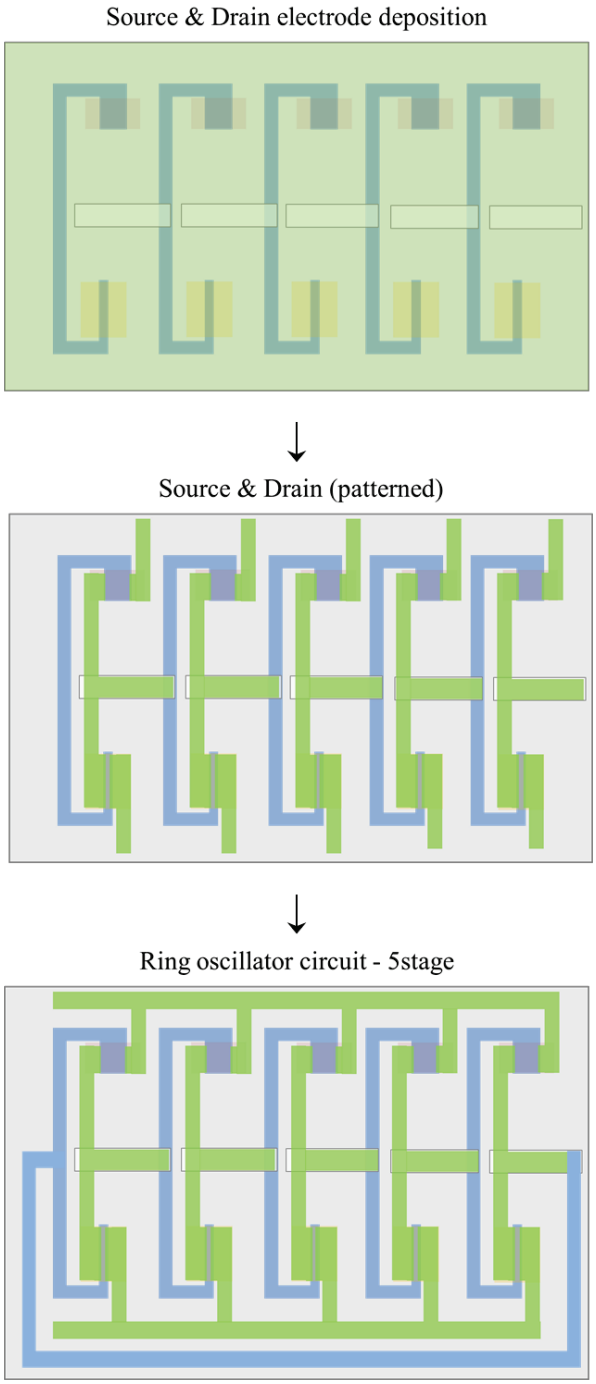
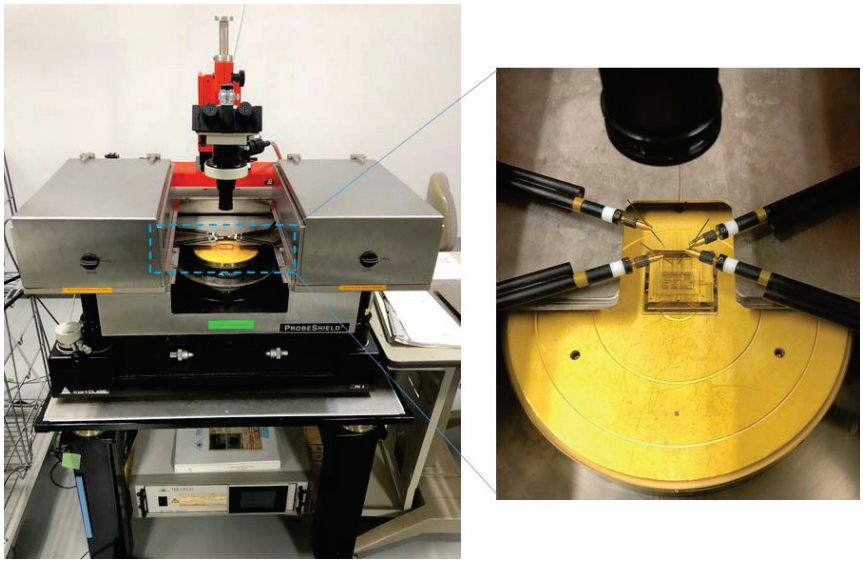


Fig. 4-24: Circuit fabrication process from source & drain deposition to source & drain patterning.

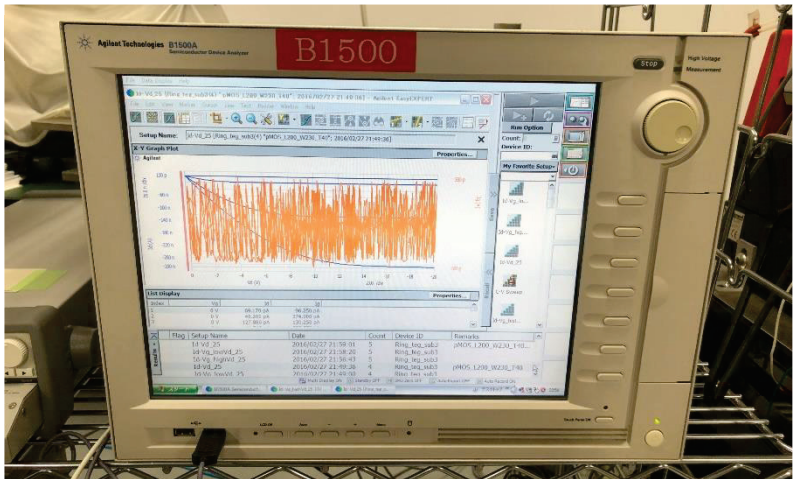
4-3: Measurement of *IV* characteristics

IV characteristics of fabricated devices are measured to observe whether they work as a transistor. Measurement instrument are shown in picture 4-3. Semiconductor parameter analyzer (B1500) manufactured by Agilent is used for the measurement. Measurement stage and probers are protected in the shield box.

(a)

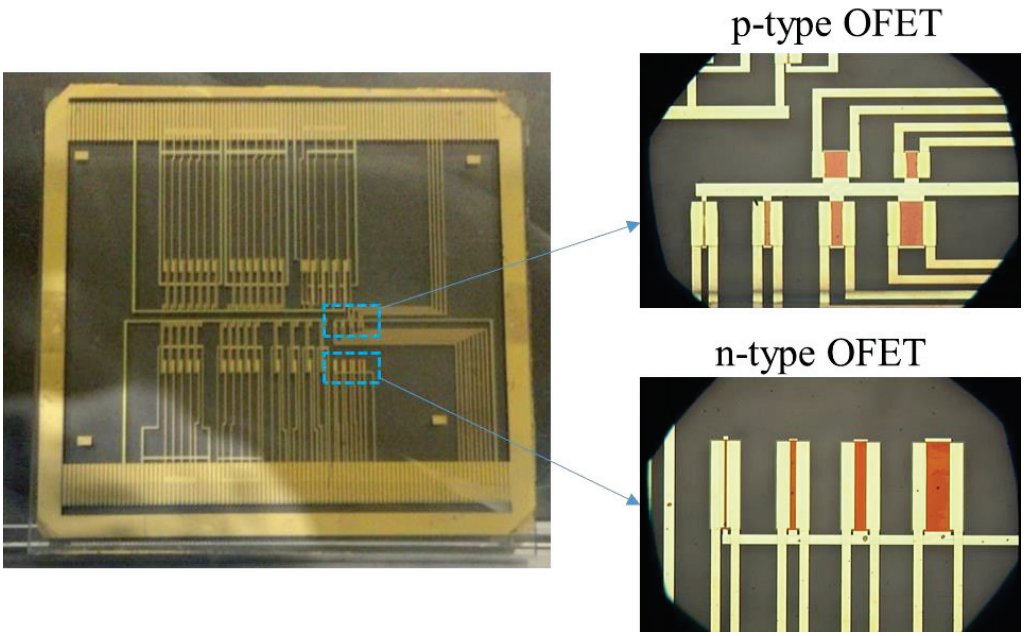


(b)



Picture 4-3: Measurement setup for analysis of OFETs *IV* characteristics; (a) Probers and measurement stage and (b) semiconductor parameter analyzer B1500 manufactured by Agilent.

OFETs are placed at right side of the substrate shown in picture 4-4. Some of the OFETs are influenced/damaged during the process at semiconductor, contact, and electrode. Measurement is conducted in two substrates; substrate (1) and substrate (2).



Picture 4-4: Microscope image of p-type OFETs and n-type OFETs.

Measurement under the following conditions is conducted in two substrates; substrate (1) and substrate (2), *IV* characteristics of measurable devices are shown in Fig. 4-25 to 4-31.

Measurement condition for p-type OFET

I_{ds}- V_{gs} at low V_{ds}: Vgs = 0 ~ -20V -0.1V step, Vds = 0 ~ -5V -0.5V step

I_{ds}- V_{gs} at high V_{gs}: Vgs = 0 ~ -20V -0.1V step, Vds = -5, -10, -15, -20V

I_{ds}- V_{ds} at varied V_{gs}: Vds = 0 ~ -20V -0.1V step, Vgs = 0, -5, -10, -15, -20V

Measurement condition for n-type OFET

I_{ds}- V_{gs} at low V_{ds}: V_{gs} = 0 ~ 20V 0.1V step, V_{ds} = 0 ~ 5V 0.5V step

I_{ds}- V_{gs} at high V_{gs}: V_{gs} = 0 ~ 20V 0.1V step, V_{ds} = 5, 10, 15, 20V

I_{ds}- V_{ds} at varied V_{gs}: V_{ds} = 0 ~ 20V 0.1V step, V_{gs} = 0, 5, 10, 15, 20V

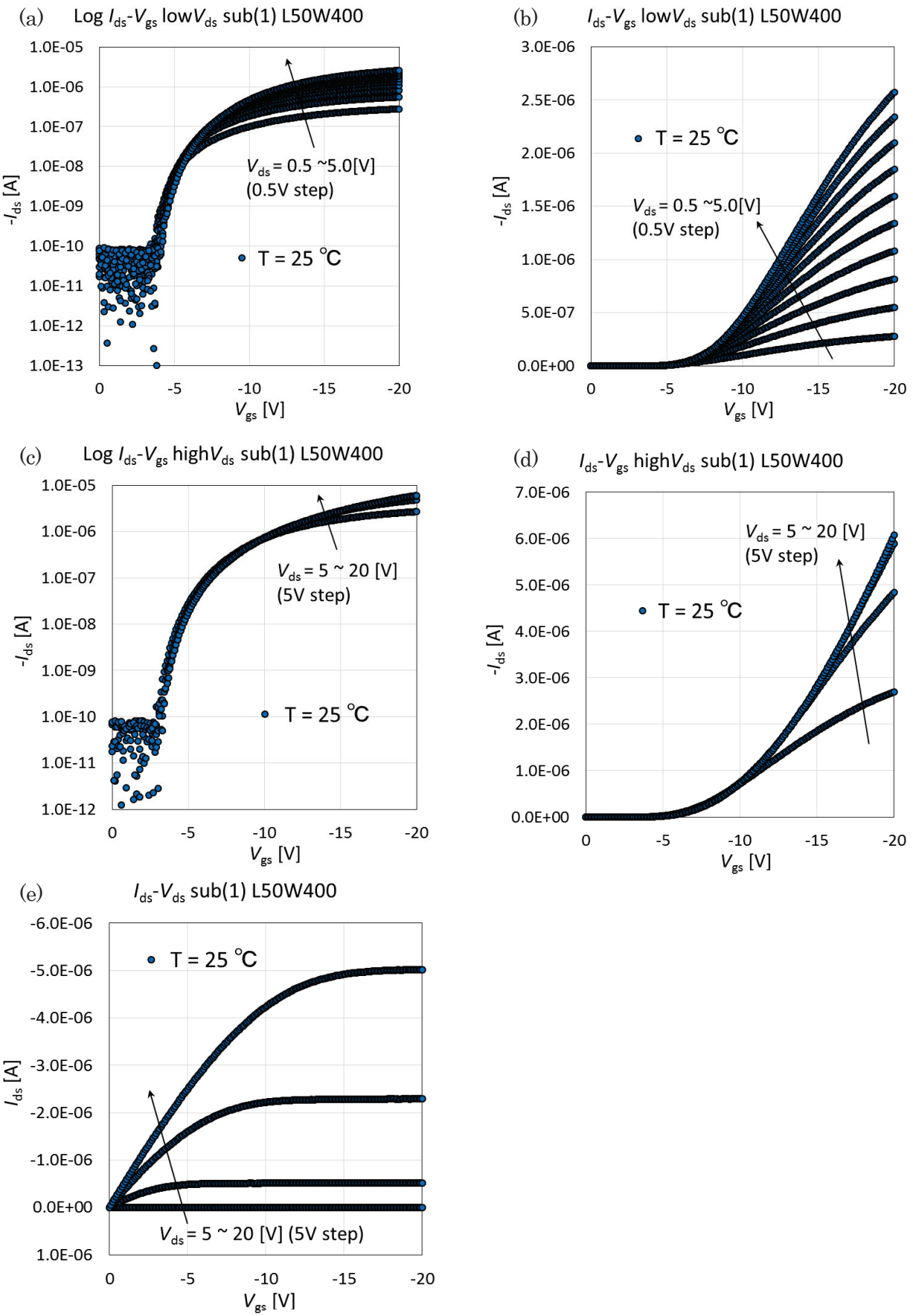


Fig. 4-25. Measurement result of p-type OFET *IV* characteristics in substrate (1), L = 50um, W = 400um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

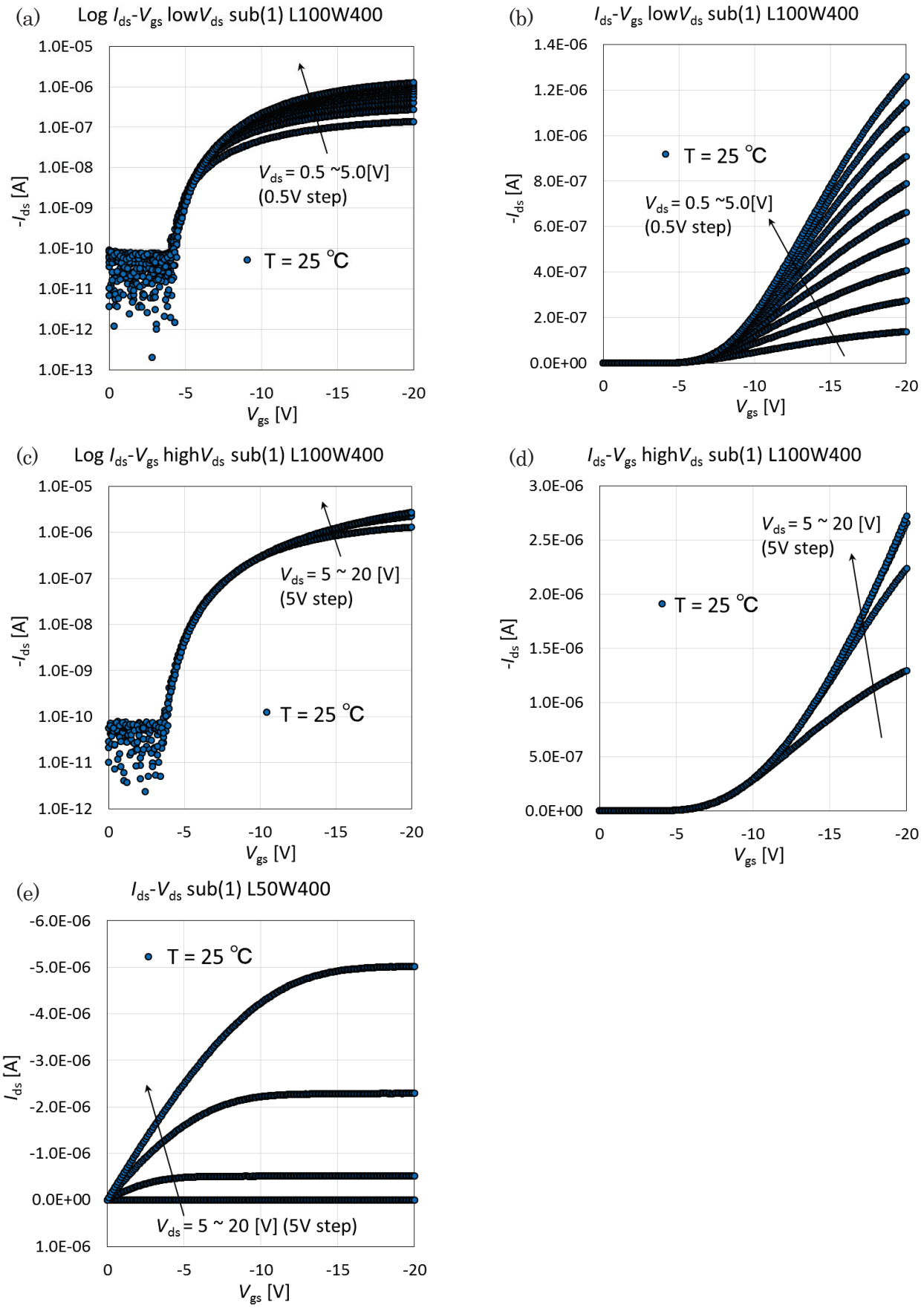


Fig. 4-26. Measurement result of p-type OFET *IV* characteristics in substrate (1), L = 100um, W = 400um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

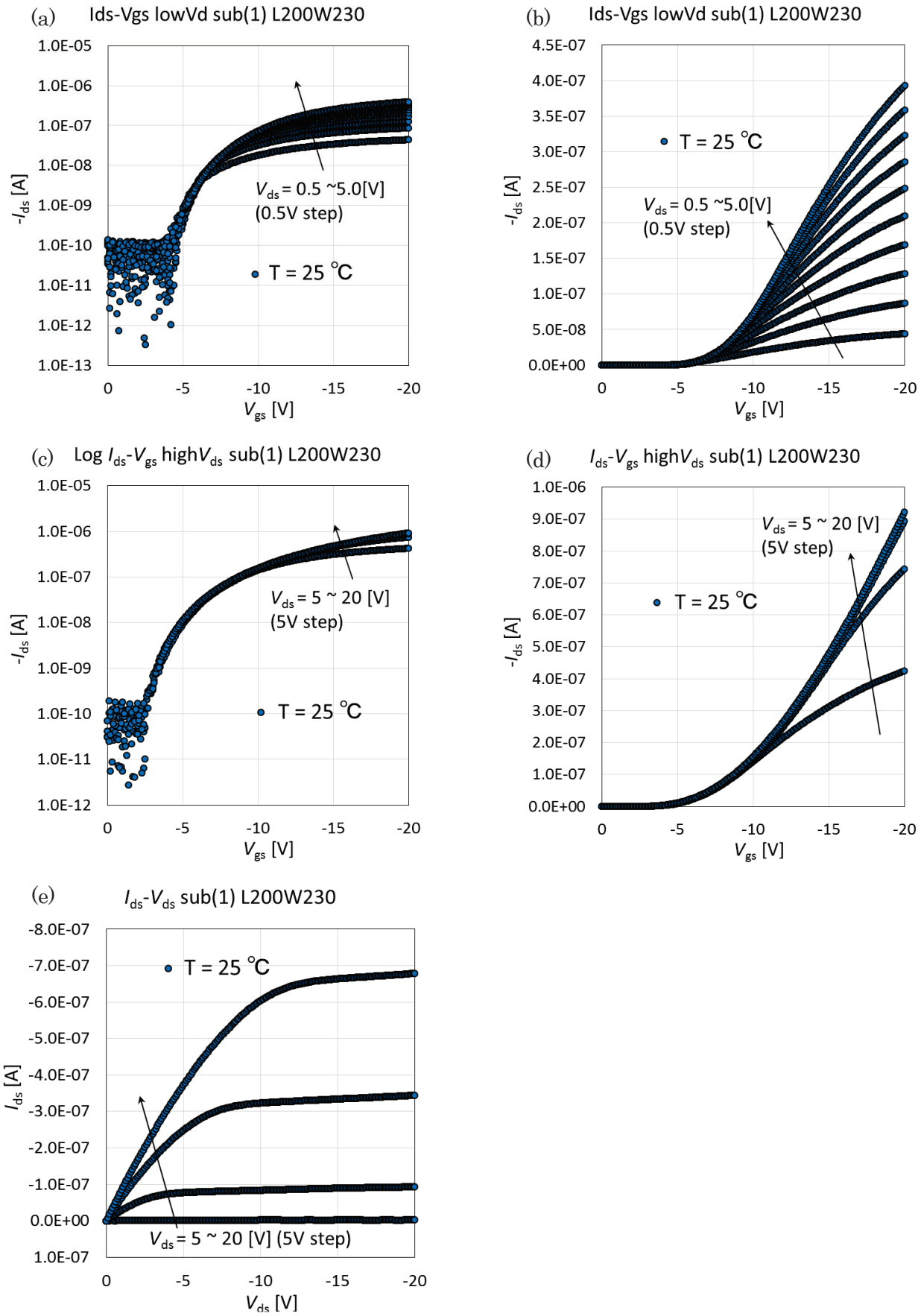


Fig. 4-27. Measurement result of p-type OFET *IV* characteristics in substrate (1), L = 200um, W = 230um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

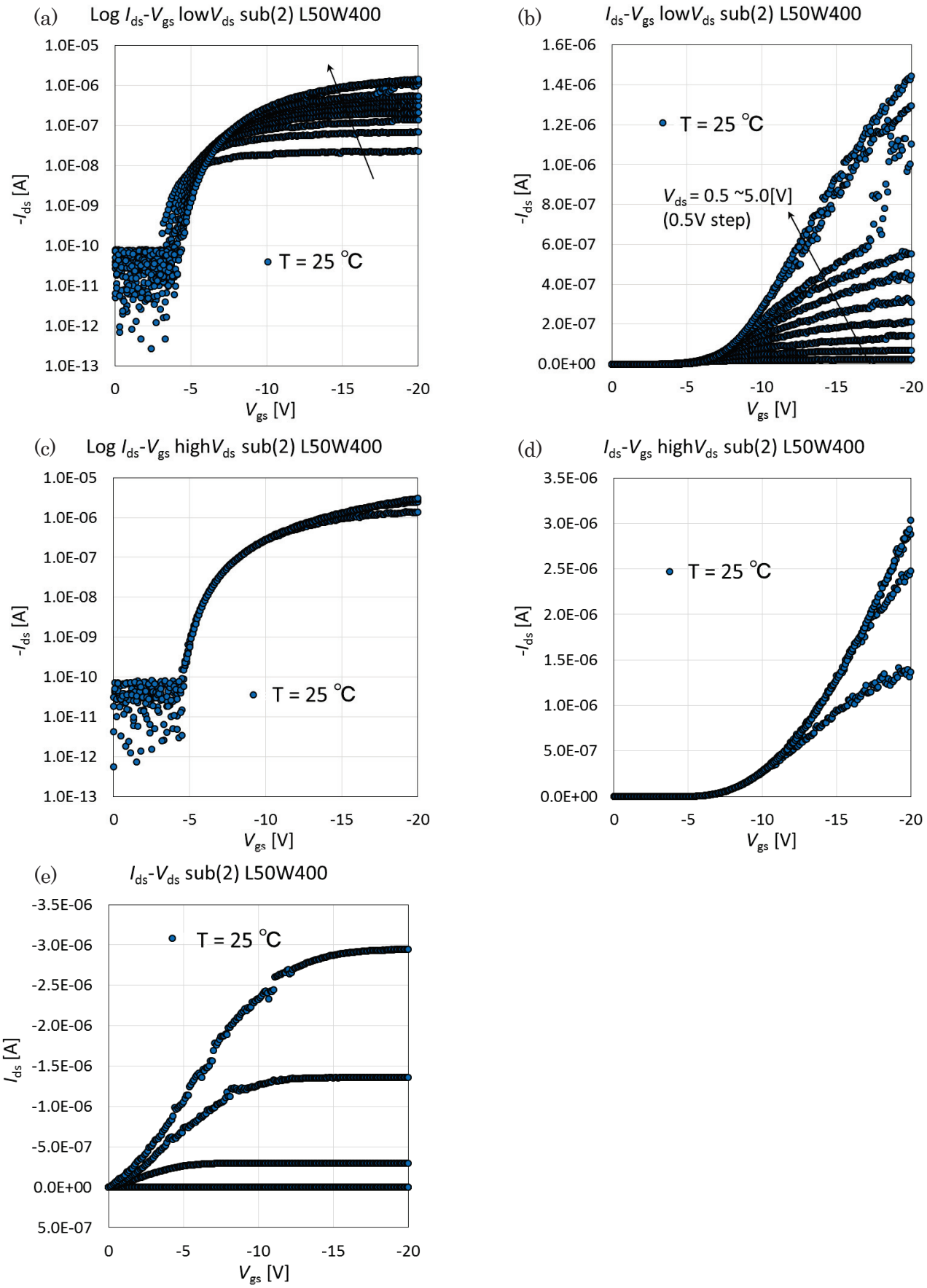


Fig. 4-28. Measurement result of p-type OFET *IV* characteristics in substrate (2), L = 50um, W = 400um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

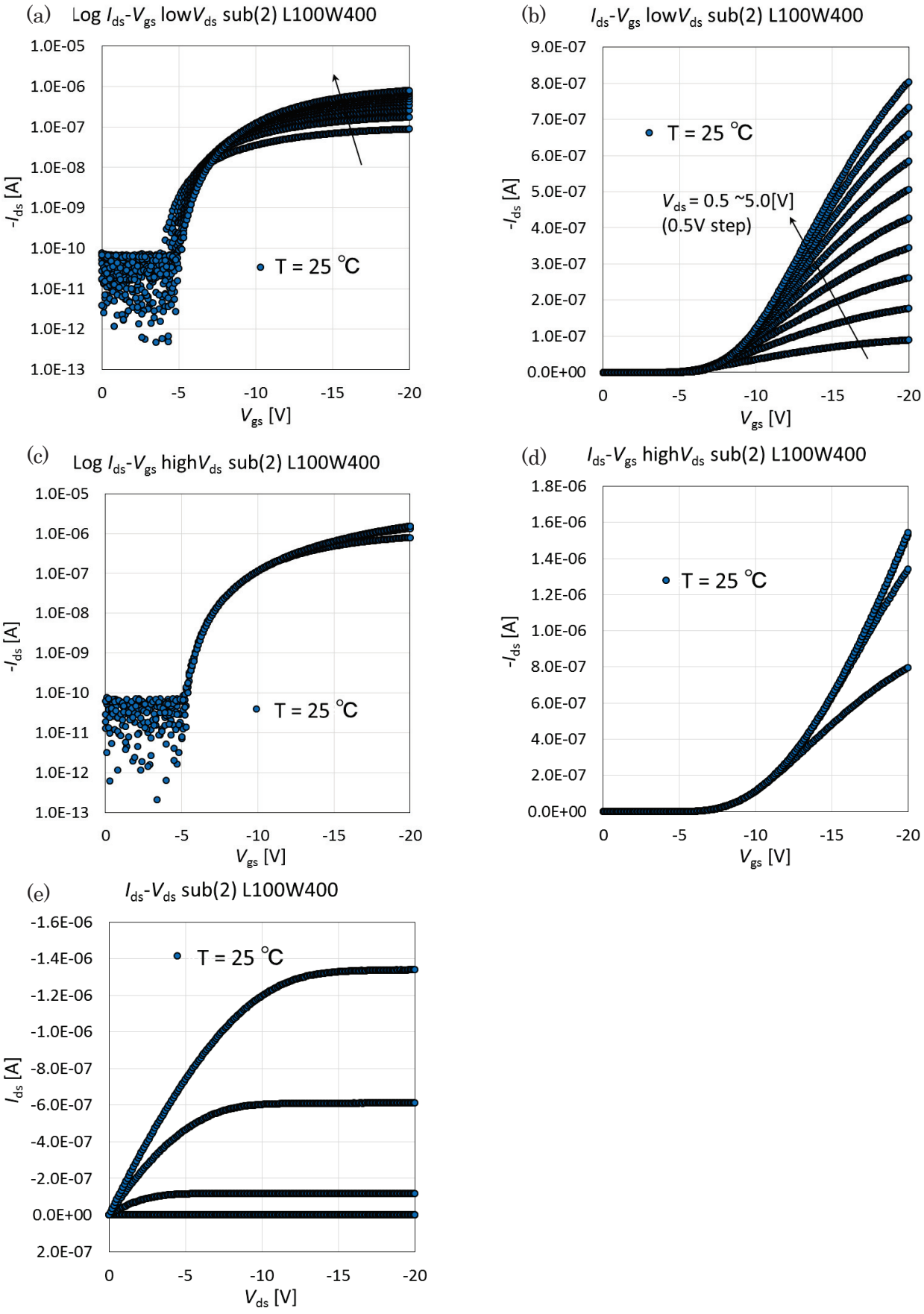


Fig. 4-29. Measurement result of p-type OFET *IV* characteristics in substrate (2), L = 100um, W = 400um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

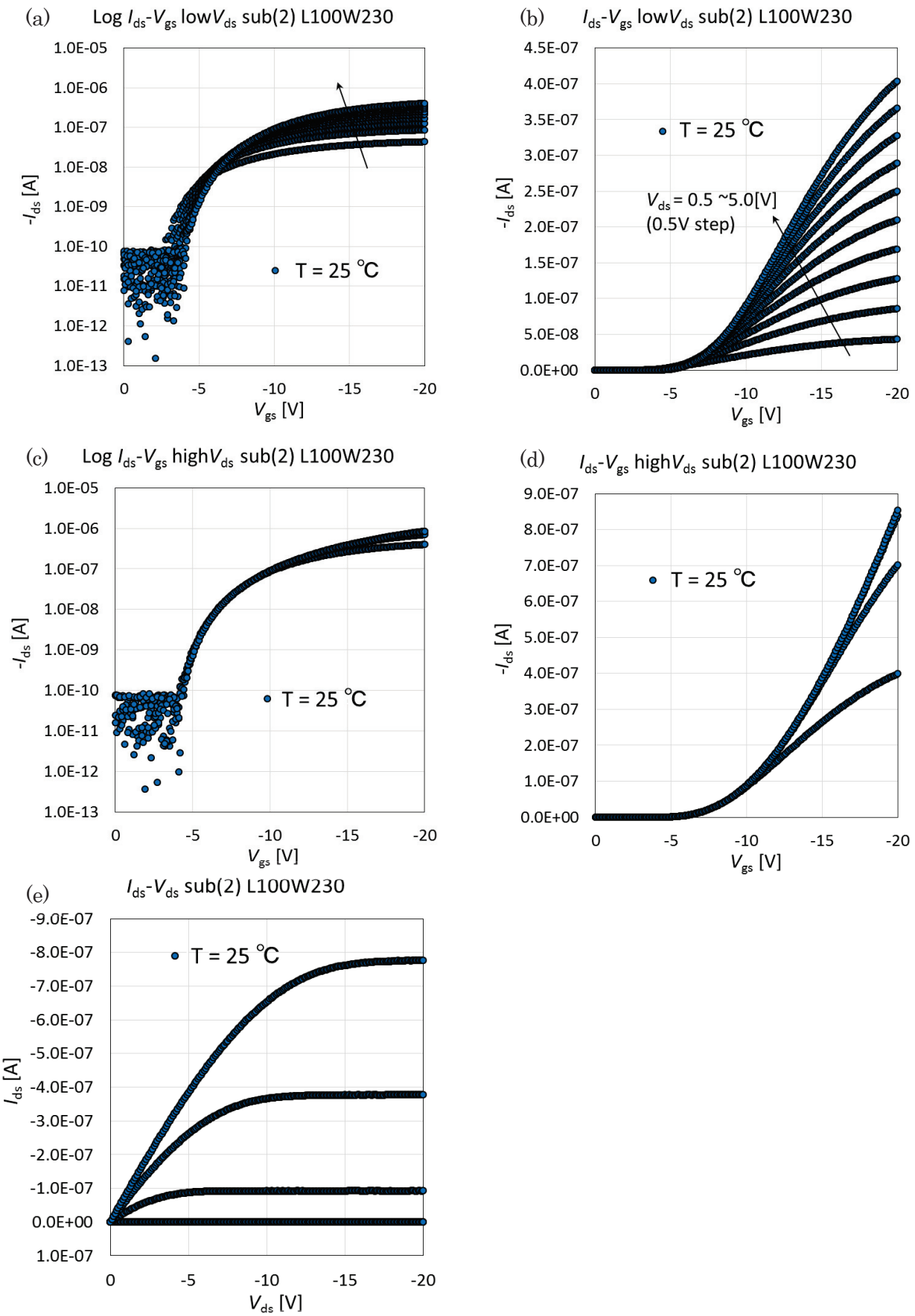


Fig. 4-30. Measurement result of p-type OFET *IV* characteristics in substrate (2), L = 100um, W = 230um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

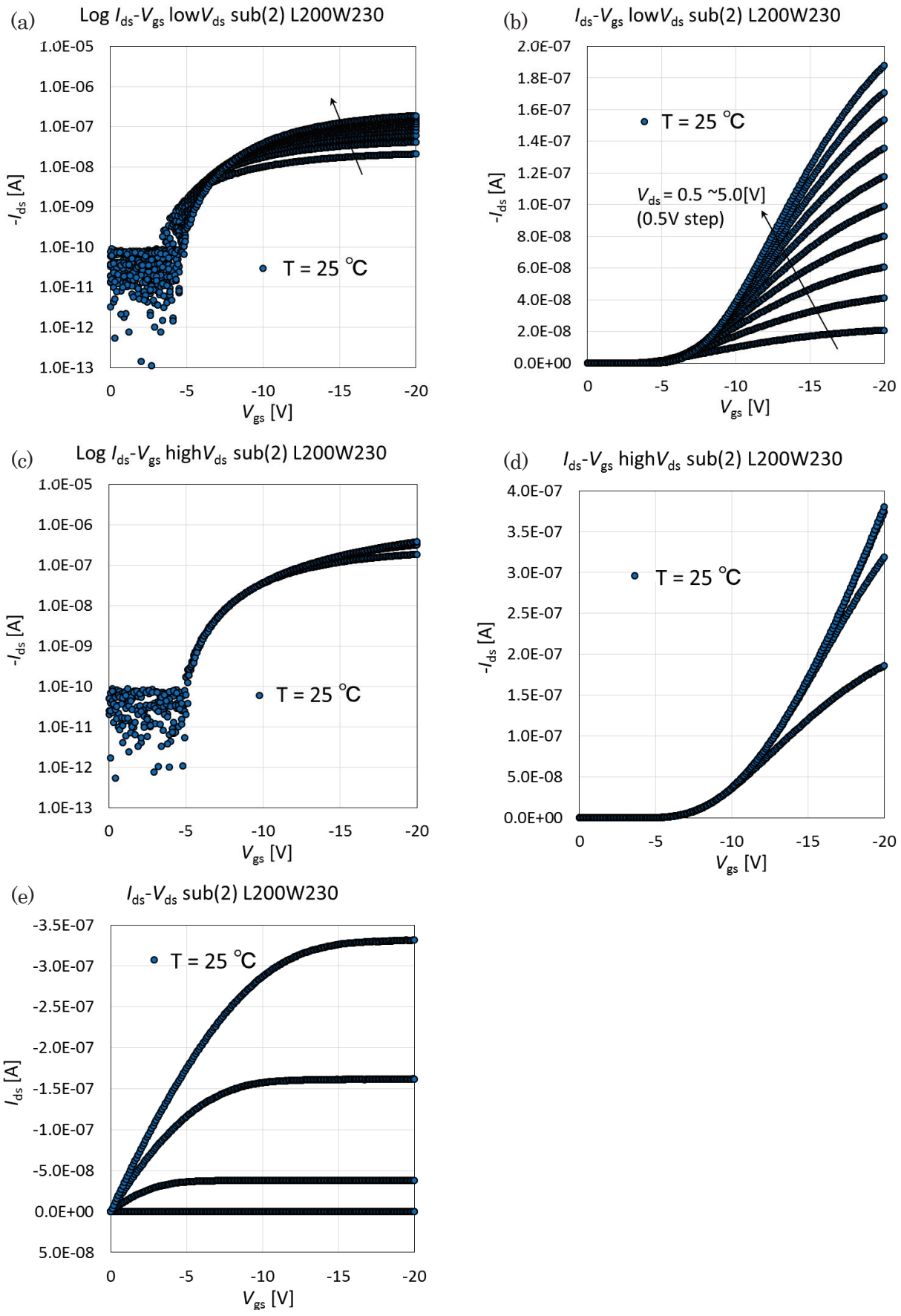


Fig. 4-31. Measurement result of p-type OFET *IV* characteristics in substrate (2), L = 200um, W = 230um : (a) Log I_{ds}- V_{gs} at low V_{ds}, (b) I_{ds}- V_{gs} at low V_{ds}, (c) Log I_{ds}- V_{gs} at high V_{ds}, (d) I_{ds}- V_{gs} at high V_{ds}, and (e) I_{ds}- V_{ds} at varied V_{gs}.

From the measurement results, the manufactured device showed excellent switching characteristics and linear characteristics as an organic MOSFET at normal temperature (25℃). The mobility in the saturation region was about 1.0 cm^2/Vs, and the On/Off ratio was observed to be 10^4 or more.

Chapter 5

Device Modeling of OFETs

5-1: Device model concept in HiSIM

5-1-1 Compact device model for circuit simulation: HiSIM

The circuit simulation model HiSIM (Hiroshima University STARC IGFET Model) is a compact device model based on drift-diffusion approximation [1]. Features of this model are;

- Parameters such as smoothing at the boundaries of cut-off/linear/saturation are not necessary, therefore, it is expected to be physically accurate.
- In order to solve a differential equation (Poisson equation), iteration is necessary to calculate the surface potential.
- Iteration increases computation time, which is not preferable as a simulator. HiSIM is devised to reduce the number of iterations by appropriately selecting the initial value of the surface potential
- Since electric charges, electric fields, and capacities are calculated from the surface potentials to obtain the current, there is no contradiction between these values.

HiSIM is a drift-diffusion model using a charge-sheet model that only the surface potential and physical value calculated from this surface potential determines the current characteristics, assuming that the depth direction of the MOSFET is integrated under the condition of the gradual channel approximation. That is, the surface potential of each point determines actual electric field induced by drain voltage, and electric charge and electric field at the channel induced by gate voltage with referencing to source level (source reference model). There are some other device models for circuit simulation such as BSIM (Berkeley Short-channel IGFET Model), PSP model, MEXTRAM etc.[2, 3, 4]

5-1-2 Calculation of surface potential in HiSIM

Calculation of the surface potential in HiSIM is fundamentally important process for obtaining critical parameters that determine device characteristics such as electric charges, electric fields, carrier mobility, depletion layer width, and others. The flow of calculation of the surface potential of HiSIM is described below [5].

First, total electric charge in channel $Q_s(x)$ is calculated from Poisson equation in channel described in equation (5-1), with using electric field $E(x)$ along with a vertical direction to channel described in equation (5-2) and Gaussian theory.

$$\frac{d\phi_s(x)}{dx^2} = -\frac{q}{\varepsilon_{si}}\left[p_{p0}\left\{\exp\left(\beta\phi_f - 1\right)\right\} - n_{p0}\left\{\exp\left(\beta\phi_f - 1\right)\right\}\right]. \tag{5-1}$$

$$\begin{aligned} E(x) = \pm\frac{\sqrt{2}k_B T}{qL_D}&\left[\exp\left\{\beta\left(\phi_s(x) - V_{bs}\right)\right\} + \beta\left(\phi_s(x) - V_{bs}\right) - 1\right] \\ &+ \frac{p_{p0}}{n_{p0}}\left[\exp\left\{\beta\left(\phi_s(x) - \phi_f(x)\right)\right\} + \beta\left(\phi_s(x) - \phi_f(x)\right)\right]^{\frac{1}{2}} \end{aligned}. \tag{5-2}$$

Then, $Q_s(x)$ is described as;

$$\begin{aligned} Q_s(x) &= \varepsilon_{si}E_s \\ &= qN_{sub}L_D\sqrt{2}\left[\begin{array}{l} \left\{\exp\left(-\beta\left(\phi_s(x) - V_{bs}\right)\right) + \beta\left(\phi_s(x) - V_{bs}\right) - 1\right\} \\ + \dfrac{p_{p0}}{n_{p0}}\left\{\exp\left\{\beta\left(\phi_s(x) - \phi_f(x)\right)\right\} + \beta\left(\phi_s(x) - \phi_f(x)\right)\right\} \end{array}\right]^{\frac{1}{2}}. \end{aligned} \tag{5-3}$$

Here, q is element charge, k_B is Boltzmann constant, T is temperature, $\Phi_s(x)$ is surface potential at x, $\Phi_f(x)$ is Fermi potential, V_{bs} is applied voltage form source to bulk, p_{p0} is hole density in p-type semiconductor, n_{p0} is electron density in p-type semiconductor, and L_D is deletion width.

Qs(x) can be also described using the oxide capacitance Cox and applied gate voltage V_g as;

$$\begin{aligned} Q_s(x) &= C_{ox}\left\{V_g - \phi_s(x)\right\} \\ C_{ox} &= \frac{\varepsilon_{ox}}{T_{ox}}. \end{aligned} \tag{5-4}$$

Here, ε_{ox} is the permittivity of oxide layer and T_{ox} is the thickness of oxide layer.

From equation (5-3) and (5-4), a following equation is obtained;

$$C_{ox}\left\{V_g-\phi_s(x)\right\}=qN_{sub}L_D\sqrt{2}\left[\begin{array}{l}\left\{\exp\left(-\beta\left(\phi_s(x)-V_{bs}\right)\right)+\beta\left(\phi_s(x)-V_{bs}\right)-1\right\}\\+\dfrac{p_{p0}}{n_{p0}}\left\{\exp\left\{\beta\left(\phi_s(x)-\phi_f(x)\right)\right\}+\beta\left(\phi_s(x)-\phi_f(x)\right)\right\}\end{array}\right]^{\frac{1}{2}}. \quad (5\text{-}5)$$

The surface potential can be obtained from this equation. However, from this equation, the surface potential cannot be determined analytically as "$\varphi_s(x)$ = ~". Therefore, HiSIM uses iteration to obtain the surface potentials φ_{s0} and φ_{sL}. The potential distribution along the channel are empirically known and the surface potential change during the MOSFETs operation is universally observed from 0 ~1V. Figure 5-1 compares the potentials of 2-dimensional device simulation result and HiSIM simulation result. Potential distributions are accurately reproduced, which enables reliable calculation of the other important physical parameters.

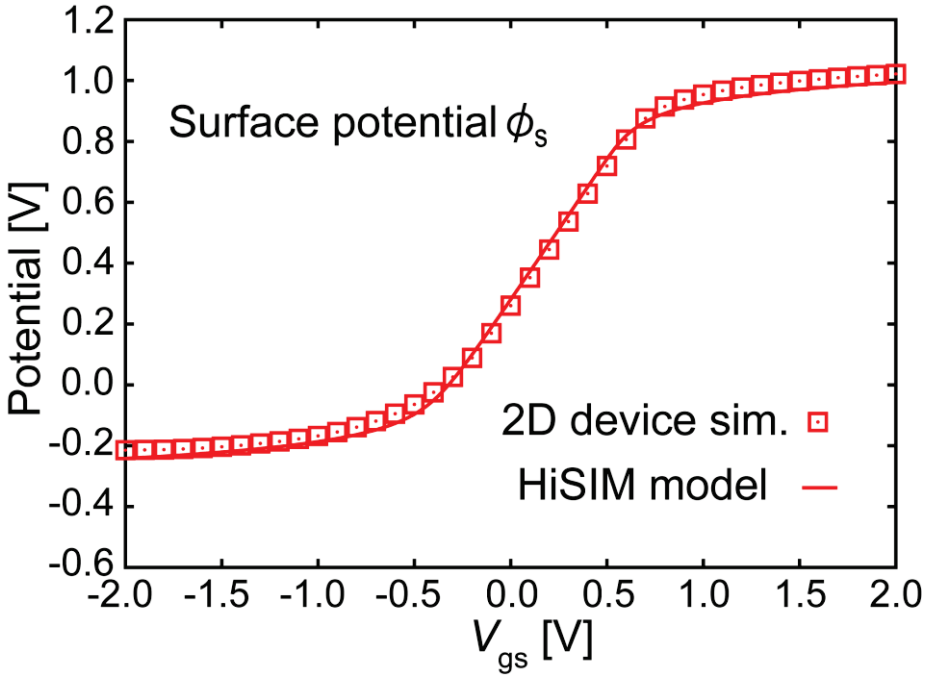


Fig. 5-1: Comparison of the surface potential at source side result from 2D-device simulation and HiSIM model.

5-2: Construction of carrier mobility model for OFETs

This section explains a construction of carrier mobility model for OFETs. The model is based on the important conduction theories; "Hopping conduction" and "Poole-Frenkel conduction". Developed carrier mobility model will be implemented in an organic device model: HiSIM-organic.

5-2-1 Hopping conduction

As explained in Chapter 3, carrier transport in OFETs is derived from the carrier movement between molecules and/or grains by hopping via neighboring delocalized energy states as illustrated in Fig. 5-2. Channel width in FETs is usually about 2~3 nm where induced carriers are strongly attracted to the interface of semiconductor and insulator. OFETs are also expected to have similar channel width as long as their crystallinity at carrier path is high with homogenized molecules.

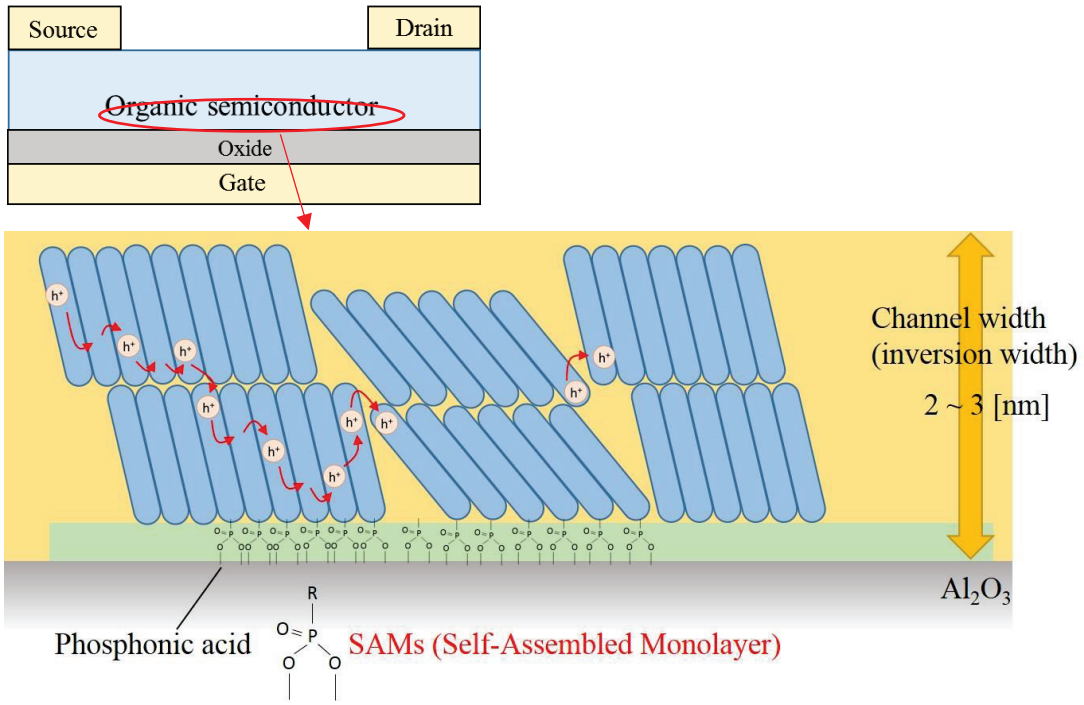


Fig. 5-2: Schematic mechanism of hopping conduction between molecules and grains.

Important factors in hopping conduction are the distance between localized states and energy differences, and both factors must be considered in the model. Figure 5-3 shows how carriers hop between localized energy states *i* and *j* in organic semiconductors.

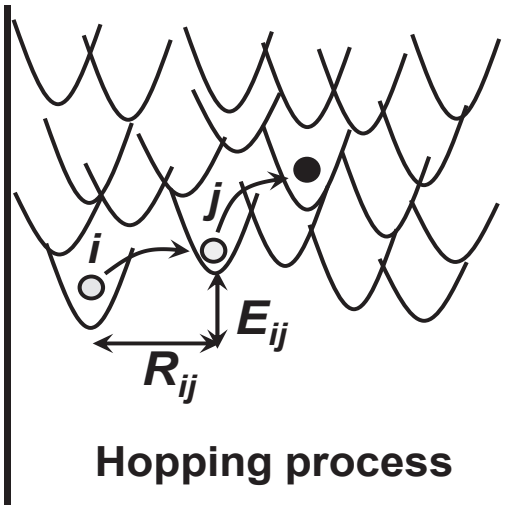


Fig. 5-3: Carrier hopping process between localized energy level *i* and *j*.

Here, R_{ij} and E_{ij} represent the distance between *i* and *j*, and the energetic difference between *i* and *j* respectively. As a common sense, hopping probability is higher at closer distance and closer energy difference.

Assuming the carriers is electron, the effect of energy variation is consider at first. Suppose that carriers captured in a localized energy level jump to the next level. When the energy level of *i* is E_i, the density of the carrier trapped with E_i (N_T) or less is expressed as equation (5-6);

$$N_T = \int_{E_i}^{\infty} g(E) f(E) dE \,, \tag{5-6}$$

Where, $g(E)$ is the energy function of density of state (DOS) and $f(E)$ is fermi distribution function.

Next, the effect of distance variation is considered. When carriers move between the two neighboring energy level *i* and *j*, the threshold radius *B* is expressed as equation (5-7);

$$\frac{4\pi}{3} R_{ij}^3 N = B \,. \tag{5-7}$$

Here, *N* represents the uncaptured carrier density and written as;

$$N = \int_{E_i}^{\infty} g(E)\left[1 - f(E)\right] dE \,. \tag{5-8}$$

From equation (5-7) and (5-8), hopping distance between *i* and *j* becomes [6, 7];

$$R_{ij} = \left[\frac{4\mu}{3B} \int_{E_i}^{\infty} g(E)\left[1 - f(E)\right] dE \right]^{-1/3} . \tag{5-9}$$

Now the Miller-Abraham hopping rate <τ> within the band gap is considered. The distribution function of the uncaptured carrier density is [1-f(E)] in equation (5-8) and using the relation of [1-f (E)] = exp ((E - E_F) / $k_B T$) f(E), the hopping rate <τ> is expressed as equation (5-10) [7];

$$\langle \tau \rangle = \frac{\nu^{-1} \exp\left(\frac{E_F - E_t}{k_B T} \right) \int_{E_i}^{\infty} g(E) f(E) dE}{\int_{E_i}^{\infty} g(E)\left[1 - f(E)\right] dE} . \tag{5-10}$$

Here ν is molecular vibration frequency and E_F is semiconductor fermi energy. In this equation, the energy level at j is interpreted to transport energy level; $E_j = E_t$. Under a weak electric field range, electric mobility μ is calculated using Einstein diffusion relation;

$$\mu = \beta D , \tag{5-11}$$

where $\beta = q/k_B T$, q is elemental charge, and D is diffusion coefficient of carriers. D for organic semiconductor is estimated to be [8, 9];

$$D = \langle \tau \rangle^{-1} R_{ij}^{\ 2} . \tag{5-12}$$

Using equation (5-11) and (5-12), the mobility is written as;

$$\mu = \frac{qD}{k_B T} = \frac{q}{k_B T} R_{ij}^2 \langle \tau \rangle^{-1} . \tag{5-13}$$

This equation considers both the distant and energetic disorder effects of OSC on mobility.

Inserting equation (5-9) and (5-10) to (5-13), then hopping mobility is obtained as;

$$\mu = \nu \frac{q}{k_B T} \frac{3B}{4\pi R_{ij} N_T} \exp\left(\frac{E_F - E_t}{k_B T} \right) . \tag{5-14}$$

This mobility equation is expressed as a function of energy. When describing using terminal voltage of transistors, equation (5-15) expressing the relation of the gate voltage (surface potential corresponding thereto) and energy is used.

$$E_f - E_t = \phi_s - E_g + k_B T \ln\left(N_L / n_i\right). \tag{5-15}$$

Here, $E_g = E_{HOMO} - E_{LUMO}$ is the bandgap of organic semiconductor, and N_L and n_i are effective DOS and intrinsic carrier concentration respectively. Note that the value of E_t is modified with respect to E_{LUMO} by adjusting the value of N_L and n_i in the term $k_B T \ln(N_L / n_i)$ of equation (5-15).

Finally, in order to model the equation (5-14) as a carrier mobility, setting a model parameter $M_B = \nu(q/k_B T)(3B/4\pi R_{ij} N_T)$, then hopping conduction mobility model is obtained as;

$$\mu_{HOP} = M_B \exp\left(\frac{E_F - E_t}{k_B T}\right). \tag{5-16}$$

Equation 5-16 is well describing the hopping and well simplified for the compact model. The parameter M_B is proportional to $1/R_{ij}$ and $1/N_T$, namely, highly crystallized OFETs (that have small spatial disorder, less captured carrier) should have larger M_B value. In other words, MB represents the hoping probability factor that is changed by organic materials and its crystallinities and not changed by external voltage in principle.

5-2-2 Poole-Frenkel conduction

Poole-Frenkel conduction model can describe the movement of charge by the Coulomb potential of the charge trap. This model takes electric field dependence of mobility into consideration and is widely known as a mobility model of organic semiconductors. In the process of carrier hopping between molecules or grains, the energy barrier decreases due to the electric field effect, so the mobility has electric field dependence [10, 11]. Figure 5-3 schematically shows the mechanism of barrier lowering of the Poole-Frenkel conduction model.

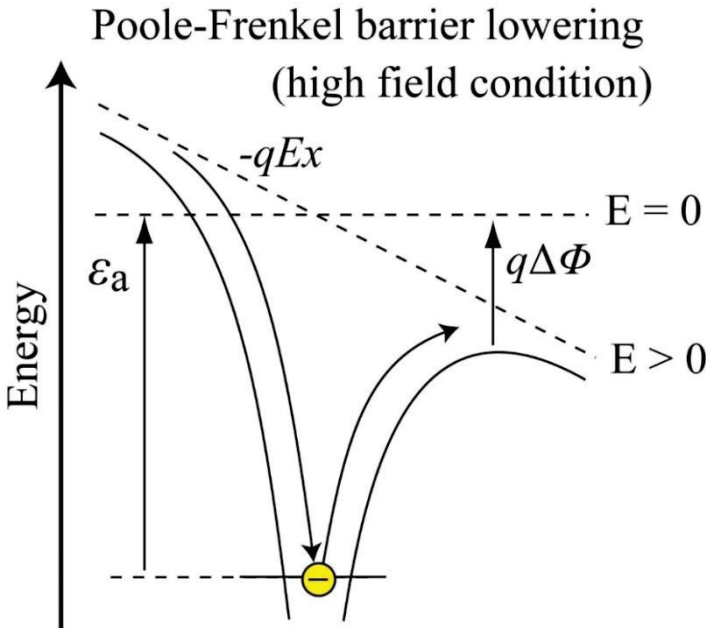


Fig. 5-3: Potential-barrier lowering of Poole-Frenkel conduction. [10, 11]

Assuming the mobility represented by Poole-Frenkel conduction as μ_{PF}, it can be expressed as equation 5-17 using the barrier lowering $\Delta\Phi$ [12].

$$\mu_{PF} = \mu_0 \exp\left(-\frac{\varepsilon_a - q\Delta\phi_{PF}}{k_B T}\right). \tag{5-17}$$

Here, ε_a is the activation energy of trapped carriers under no electric field, which corresponds to the barrier height. Theoretically, the barrier lowering is determined by the dielectric constant ε of the material and is described by $\Delta\Phi = \sqrt{(qE / 4\pi\varepsilon)}$. Here E is applied the electric field along the channel.

When implementing this as a carrier mobility model in HiSIM-Organic, it is treated as equation (5-18) using fitting parameters β, γ, δ [10, 11].

$$\mu_{\mathrm{PF}} = M_{\mathrm{PF0}} \exp\left(-\frac{\delta}{k_{\mathrm{B}}T}\right) \exp\left[\left(\frac{\beta}{k_{\mathrm{B}}T} - \gamma\right)\sqrt{E_{\parallel}}\right]. \tag{5-18}$$

Here, $E_{\parallel}$ is the electric field along the channel calculated by

$$E_{\parallel} = (\phi_{sL} - \phi_{s0}) / (L_{eff} - \Delta L). \tag{5-19}$$

ϕ_{s0} and ϕ_{sL} represent the surface potential at source edge and drain edge respectively. L_{eff} and ΔL are the effective channel length and pinch-off length in saturation region respectively. M_{PF0} is the mobility at low gate voltage condition, δ is the parameter determines temperature dependency. These parameters vary depending on the organic semiconductor material, thereby it is necessary to optimize the value of the parameter depending on the material and manufacturing method of the device. Further discussions are done in chapter 5-4.

Based on Matthiessen 's rule, a mobility model based on the theory of Hopping conduction and Poole - Frenkel conduction is described as equation (5-20).

$$\frac{1}{\mu_{ORG}} = \frac{1}{\mu_{HOP}} + \frac{1}{\mu_{PF}}. \tag{5-20}$$

Total mobility μ_{ORG} shows the curve as depicted in Fig. 5-4. It is obvious that dominant regions of hopping and Poole-Frenkel conduction are different by gate voltage. Hopping conduction is dominant at very low gate voltage region (less than 3V in this case) with a steep rise. Originally, hopping conduction is derived from low field diffusion mobility (explained in chapter 5-2), therefore it is natural to be dominant at low gate voltage. While, Poole-Frenkel is dominant at higher voltage region (more than 3V in this case). Such curve is not preferable to reproduce *IV* characteristics, since this crossing region has the threshold voltage. Also OFETs IV characteristics never show angular shape at low gate voltage. This indicates that there must be other mechanism to be considered in particular to the low/middle gate voltage region.

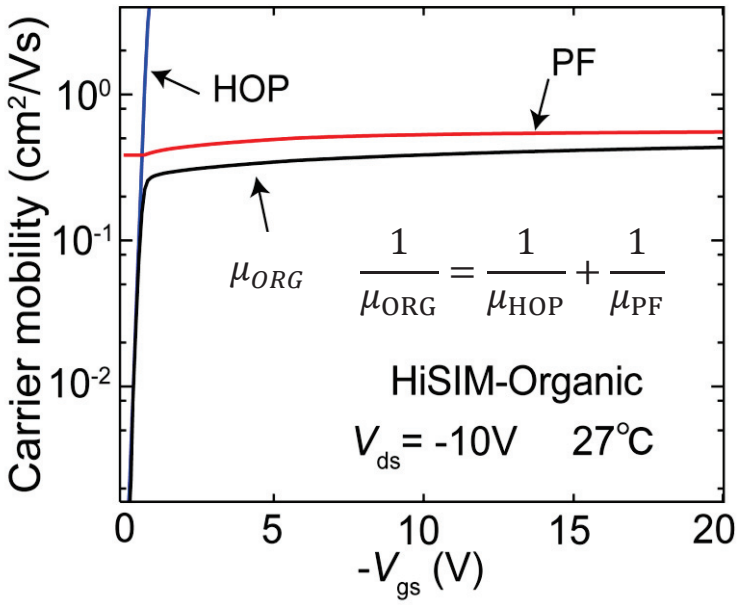


Fig. 5-4: Carrier mobility curve with hopping and Poole-Frenkel conduction as a function of gate voltage V_{gs}. [10, 11]

Poole-Frenkel conduction can be confirmed by plotting I_{ds}/V_{ds} as a function of $\sqrt{V_{ds}}$ (PF plot). If the current is conducted only by Poole-Frenkel, plotted result become a straight line [13]. However, obtained plots shown in Fig. 5-5 never become a straight line, this also indicates that carrier conduction in OFETs cannot be explained by only Poole-Frenkel.

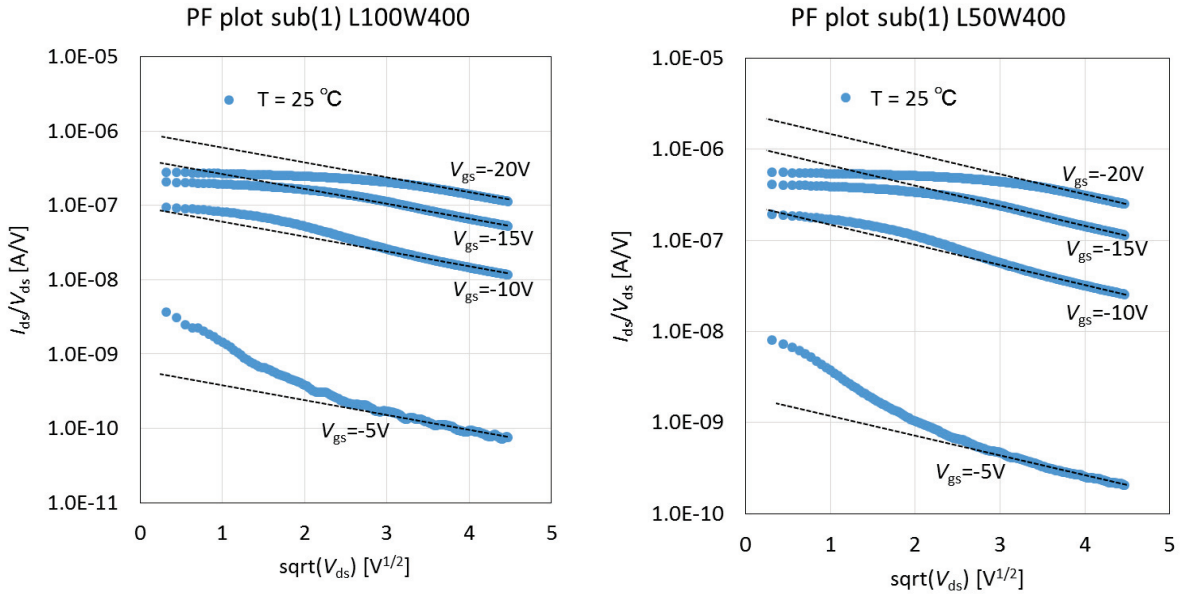


Fig. 5-5: I_{ds}/V_{ds} as a function of sqrt(V_{ds}) (Poole-Frenkel plot).

5-2-3 Coulomb scattering

Coulomb force is a force that works on all substances/matters including atoms and electrons/holes. Conduction carriers also feel the force and are scattered if the force is strong enough to affect or if carriers' movement are slow enough to be affected (based on Rutherford scattering) [14]. Scattering mechanism of carriers is already clarified in inorganic semiconductor devices and Coulomb scattering due to ionized impurities appears at low electric field. In the organic semiconductor, since the doping is not aggressively carried out, the idea of impurity ions is not taken into consideration (unintentional impurities may exist), but carriers trapped in crystal grain boundaries and ions presenting in the oxide film scatters carriers moving in organic semiconductor layer [15]. Figure 5-6 shows a concept that carriers moving in organic semiconductor are scattered by Coulomb force.

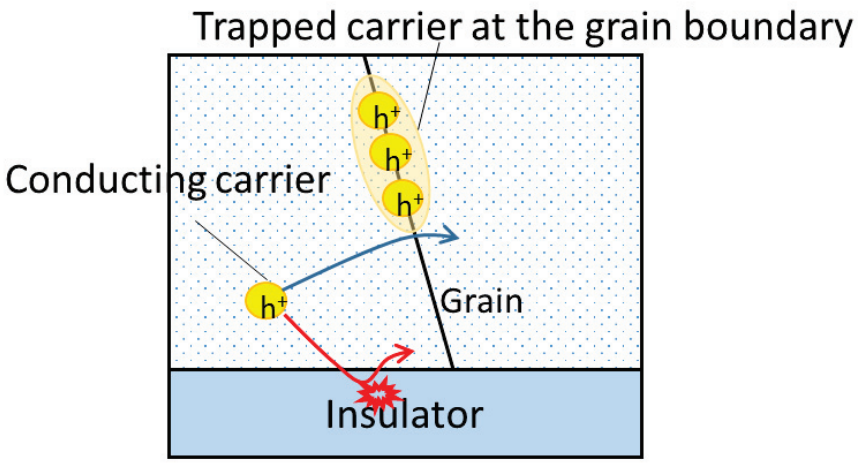


Fig. 5-6: Schematic that conducting carrier is scattered by Coulomb force from ions in the insulator and trapped carriers at grain boundary.

Coulomb scattering (interpreted as coulomb mobility μ_{CB}) can be described by equation (5-21) using inversion charge Q_i and introducing parameters MUECB0 and MUECB1.

$$\mu_{CB} = MUECB0 + MUECB1 \cdot \frac{Q_i}{q \times 10^{11}} . \tag{5-21}$$

This equation is empirically obtained for inorganic MOSFETs but still usable in OFETs. Although Q_i may be better to be a trapped charge N_T, it is dared to use Q_i so as to avoid complication of trap calculation and conversion error. Therefore, the parameter MUECB1 should be modified accordingly.

Thereafter, total mobility μ_0 is calculated by;

$$\frac{1}{\mu_0} = \frac{1}{\mu_{CB}} + \frac{1}{\mu_{HOP}} + \frac{1}{\mu_{PF}} . \tag{5-22}$$

Carrier mobility considering these three effects as a function of gate voltage is plotted in Fig. 5-7, showing that three conduction theories have each dominant region in gate voltage; Hopping conduction is dominant at very low gate voltage, Coulomb scattering (Coulomb mobility) is dominant at low-middle gate voltage, and Poole-Frenkel conduction is dominant at high gate voltage.

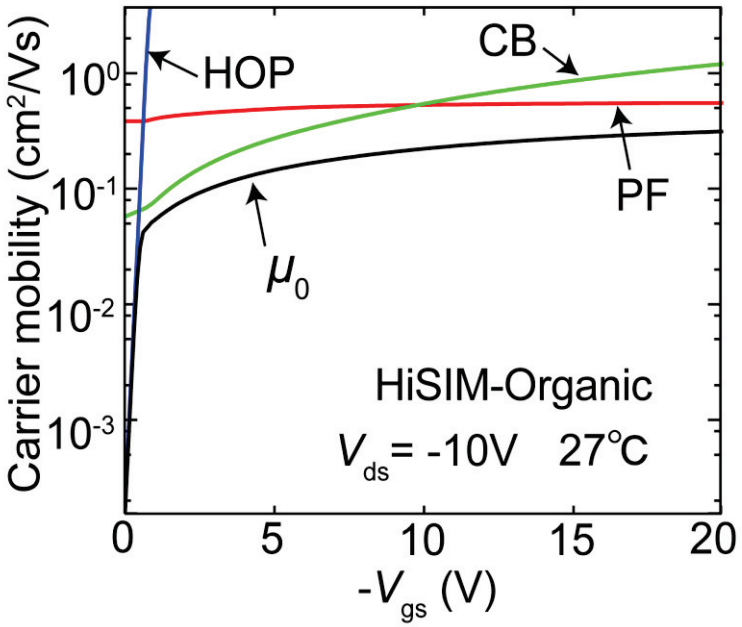


Fig. 5-7: Carrier mobility curve with three conduction theories as a function of gate voltage V_{gs}.

5-3: Carrier trapping effect

As mentioned in Chapter 3 and 5-2, there are many traps in organic semiconductors. A lot of efforts have been made to reduce the influence of traps by improving interface treatment and crystallinity, but it is almost impossible to completely eliminate traps from inorganic and organic devices. Figure 5-8 shows the 2-dimensional device simulation results of the carrier trapping effect on the current characteristics of a MOSFET. Here, it is assumed that traps exist at the interface between the semiconductor and the oxide film. As the number of traps increases, the current decreases in the region where the gate voltage is low, and it can be seen that the threshold is shifted.

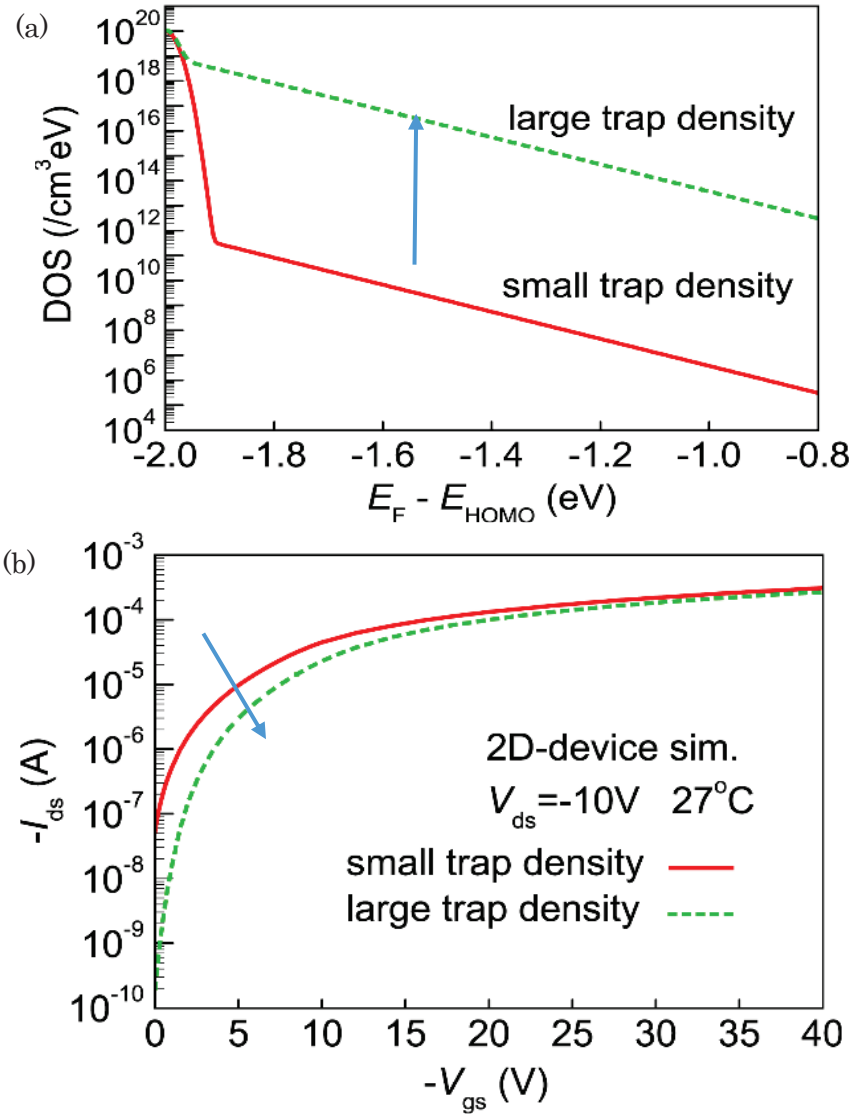


Fig. 5-8: Carrier trapping effect on *IV* characteristics result of 2D device simulation: (a) Trap density of state (DOS) as a function of energy, and (b) I_{ds}-V_{gs} characteristics.

Also, the existence of traps can be confirmed from the measurement of the fabricated device. Figure 5-9 shows the results of Hysteresis measurements. Comparatively large difference of current between Forward sweep and reverse sweep, that indicates carriers are trapped during the measurement and the current is degraded.

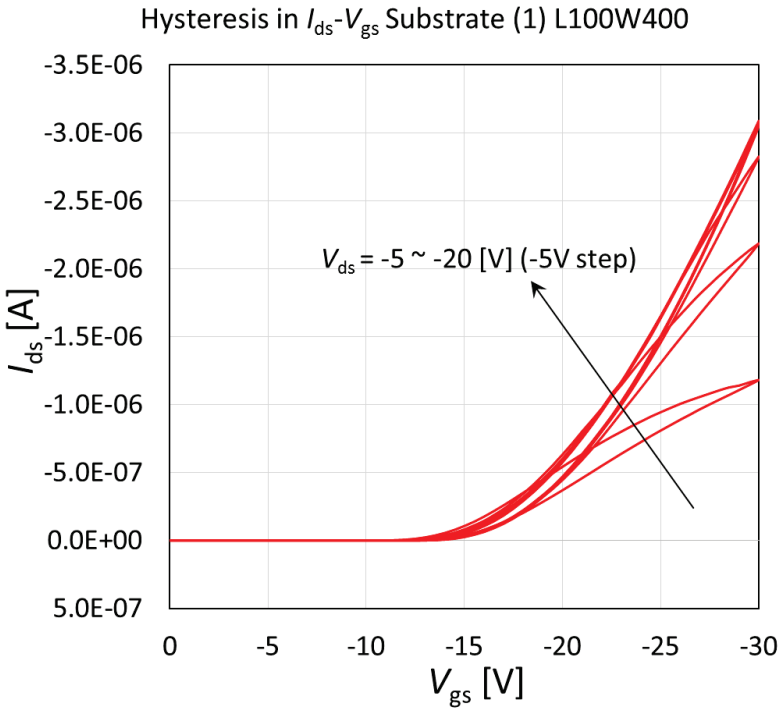


Fig. 5-9: Hysteresis effect observed in Ids-Vgs characteristics result of fabricated OFET.

It is considered that there are two types of trap (illustrated in Fig. 5-10) for organic semiconductors as follows:

(1) Behaving as if the carriers that aren't able to cross the distance barriers and/or potential barriers that exist between grain boundaries (or molecules) are trapped there. This carrier trapping is considered in the conduction model described in 5-2. In addition, since this carrier trapping occurs in principle within the semiconductor layer, hence it is considered that the influence on the surface potential is small in comparison to trapping that occurs at the interface.

(2) The other is that carriers are trapped by defects (dangling etc.) existing at the semiconductor-oxide film interface (interface trap). When the interface trap occurs, the surface potential is

modulated and the electric field weakens. As a result, the carrier density decreases and current characteristics deteriorate. Therefore, the influence of this interface trap must be taken into account when determining the surface potential.

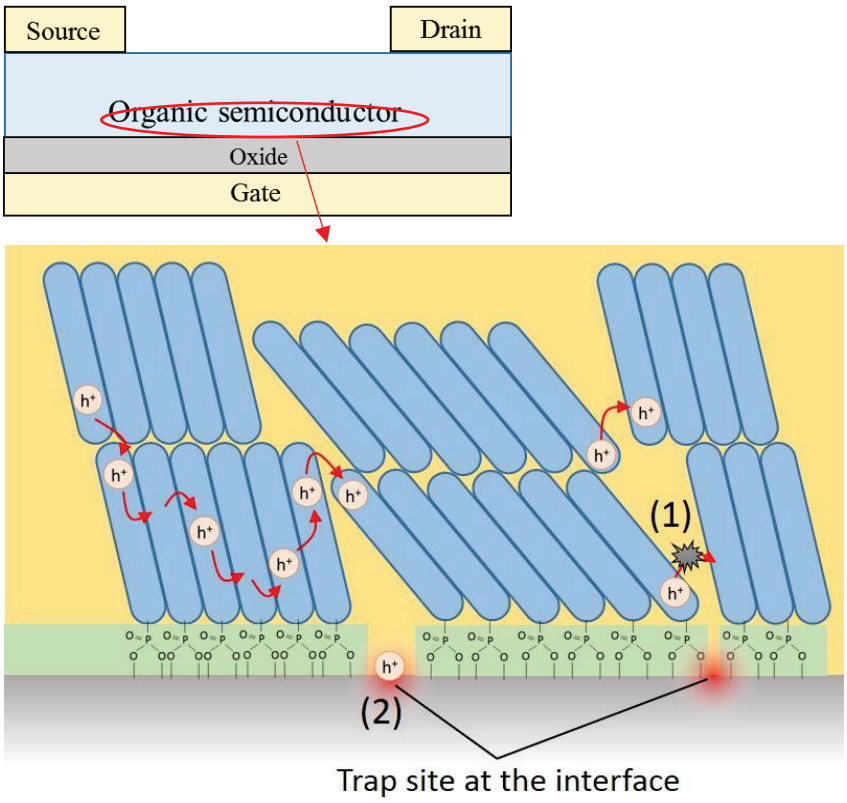


Fig. 5-10: Carrier trapping in organic semiconductors at (1) grain boundary or intermolecular and (2) interface of semiconductor and oxide layer

HiSIM-Organic solves Poisson's equation (5-23) with a consideration of all charges induced within the MOSFET including trap charge [5-7, 10, 11].

$$\nabla^2\phi_s = -\frac{q}{\varepsilon_s}\left(p - n + N_D - N_A + N_{trap\_D} - N_{trap\_A}\right). \tag{5-23}$$

where q is the elementary charge. p, n, N_D, and N_A represent hole, electron, donor, and acceptor density, respectively. ϕ_s is the surface potential to be solved for together with the Gauss law;

$$\varepsilon_{ox} \cdot E_{ox} = \varepsilon_{org} \cdot E_{org}, \tag{5-24}$$

where ε_{ox} and ε_{org} are the permittivity in the oxide and in the organic semiconductor, respectively. E_{ox}

and E_{org} are the vertical electric fields in the gate oxide and at the organic semiconductor surface, respectively. Due to the inhomogeneity of the organic substrate, trapped charges cannot be ignored. The acceptor-like trap density distribution $g_A(E)$ is usually approximated by a logarithmic function of energy E;

$$g_A(E) = g_c \exp\left(\frac{E_F - E_{LUMO}}{E_S}\right), \tag{5-25}$$

where g_c is the density at E_F-E_{LUMO}= 0 (E_F: Fermi energy, E_{LUMO}: Lowest Unoccupied Molecular Orbital energy), and the inverse of E_s is the slope of the density of states. For the donor-like trap density is described by the same equation as equation (5-25) with but E_{HOMO} for E_{LUMO}. Two independent trap-density distributions are considered as schematically shown in Fig. 5-10: One represents the shallow trap density distribution and the other represents the deep trap density distribution. Since holes dominate for the studied case, the donor-like traps are considered here.

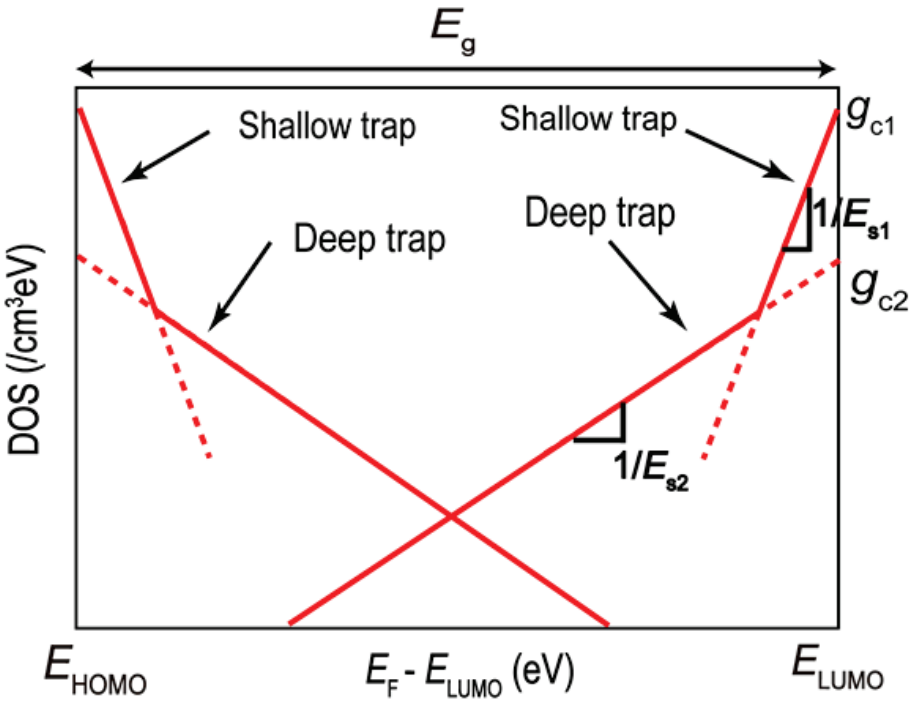


Fig. 5-10: Schematic of the acceptor-type and donor-type trap density-of-states (DOS) distribution in the bandgap.

The trap density is written after the integration of the density of states by energy as

$$N_{\text{trap-D}} = N_0 \exp\left(\frac{E_{\text{F}} - E_{\text{HOMO}}}{E_{\text{S}}}\right), \tag{5-26}$$

$$N_0 = g_{\text{c}} E_{\text{S}} \frac{\frac{k_{\text{B}}T}{E_{\text{S}}}}{\sin\left(\frac{k_{\text{B}}T}{E_{\text{S}}}\right)}. \tag{5-27}$$

Here, T and k_{B} are the lattice temperature and the Boltzmann constant, respectively. The energy difference E_{F}-E_{HOMO} (eV) can be written as a function of the surface potential ϕ_{s} which is further transformed into a function of V_{g} as;

$$E_{\text{F}} - E_{\text{HOMO}} = \phi_{\text{s}}(V_{\text{g}}) - E_{\text{g}} + k_{\text{B}}T \ln\left(\frac{N_{\text{H}}}{n_{\text{i}}}\right). \tag{5-28}$$

In equation (5-28), E_{g} is the band gap of the studied material. N_{H} and n_{i} are the effective density of states and the intrinsic carrier density of 450cm^{-3}, respectively. Though the crystalline-silicon value for the density of states is extracted to be 2.5×10^{19}cm^{-3}, the value is adjusted to 1.0×10^{18}cm^{-3} for N_{H} to obtain a reasonable density of states in the OFET as a function of the carrier energy. Since the surface potential ϕ_{s} increases as V_{gs} increases, the E_{F}-E_{HOMO} value approaches to zero according to the V_{gs} increase. Figure 5-11(a) depicts the influence of the trap density calculated with HiSIM-Organic. For the large trap density, the current magnitude in the characteristic is drastically reduced and a particularly strong suppression is observed in the subthreshold swing. The density of states applied for the calculation is depicted in Fig. 5-11(b).

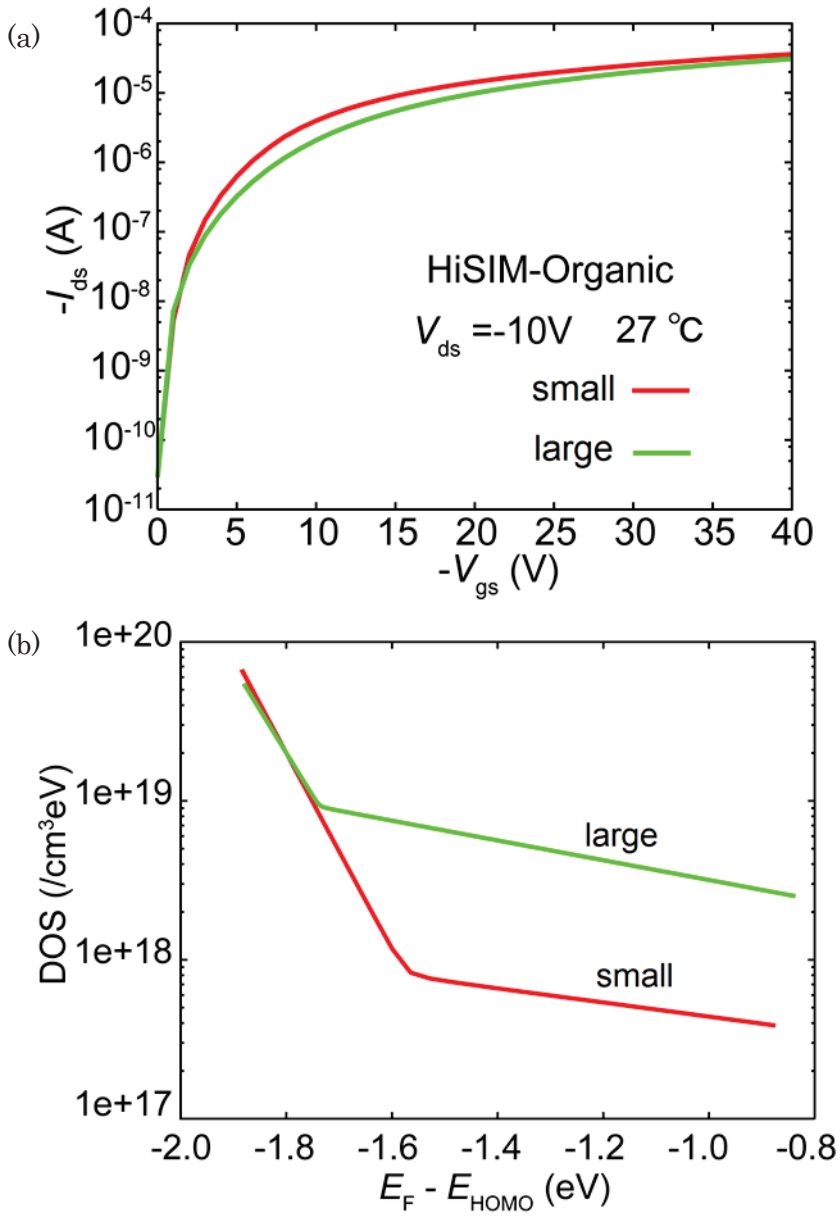


Fig. 5-11: Carrier trapping effect on *IV* characteristics result of HiSIM-Organic: (a) I_{ds}- V_{gs} characteristics, and (b) Trap density of state (DOS) as a function of energy.

5-4: Temperature dependence analysis

The influence of heating in inorganic semiconductor devices is inevitable. Heating by operation of the device is called as self-heating effect. This is because the carriers are accelerated by the electric field during device operation, and the moving kinetic energy of carriers raises lattice temperature by colliding to the lattice. Conversely, when the device temperature rises due to the external environment, the lattice vibration is amplified by heat and scattering of carriers is increased, thereby the current value decreases. Figure 5-12 depicts the 2D device simulation results of I_{ds}-V_{gs} for comparing normal temperature and elevated temperature.

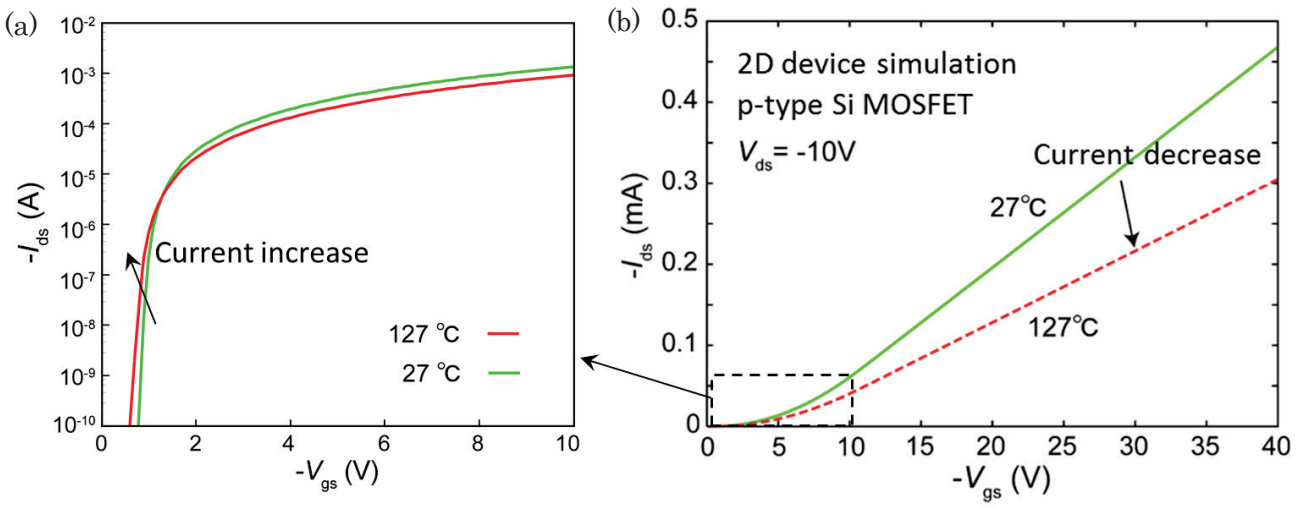


Fig. 5-12: Temperature dependence of Si MOSFET result of 2D device simulation: (a) I_{ds}-V_{gs} characteristics logarithmic plot and (b) I_{ds}-V_{gs} characteristics linear plot.

Current decrease can be observed from linear plot and some current increase is observed from logarithm plot in low gate voltage region. This current increase is due to the increase of intrinsic carrier density in semiconductor layer. Inorganic MOSFETs that have a monocrystalline (lattice-forming) semiconductor layer including Si MOSFETs show a universality on temperature dependence as depicted in Fig. 5-13. As gate voltage increases up to a certain value (temperature coefficient point), intrinsic carriers are activated and carrier density increase resulting in current increase. As gate voltage increases more than temperature coefficient point, phonon vibration scattering effect becomes dominant resulting in current decrease.

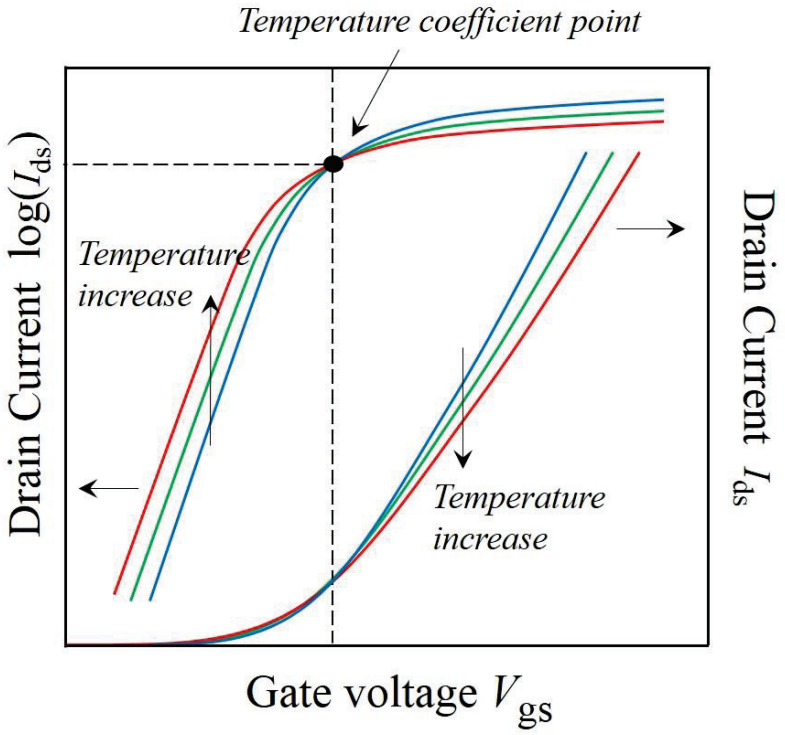


Fig. 5-13: Universality on temperature dependence of inorganic crystalline MOSFETs.

Even in organic semiconductor devices, the influence by heat is remarkable. In the case of organic semiconductors, the temperature dependence varies by materials due to the difference of physical quantities (permittivity, bandgap etc.), crystallinity of semiconductor film, trap densities. In principle, OFETs should not be operated in high temperature environment because organic molecules are bonded with intermolecular force (Van der Waals force) which is much weaker than covalent bond seen in inorganic semiconductor material. Therefore, elevating the temperature causes molecular vibrations, decompositions or some other crucial damages as illustrate in Fig 5-14.

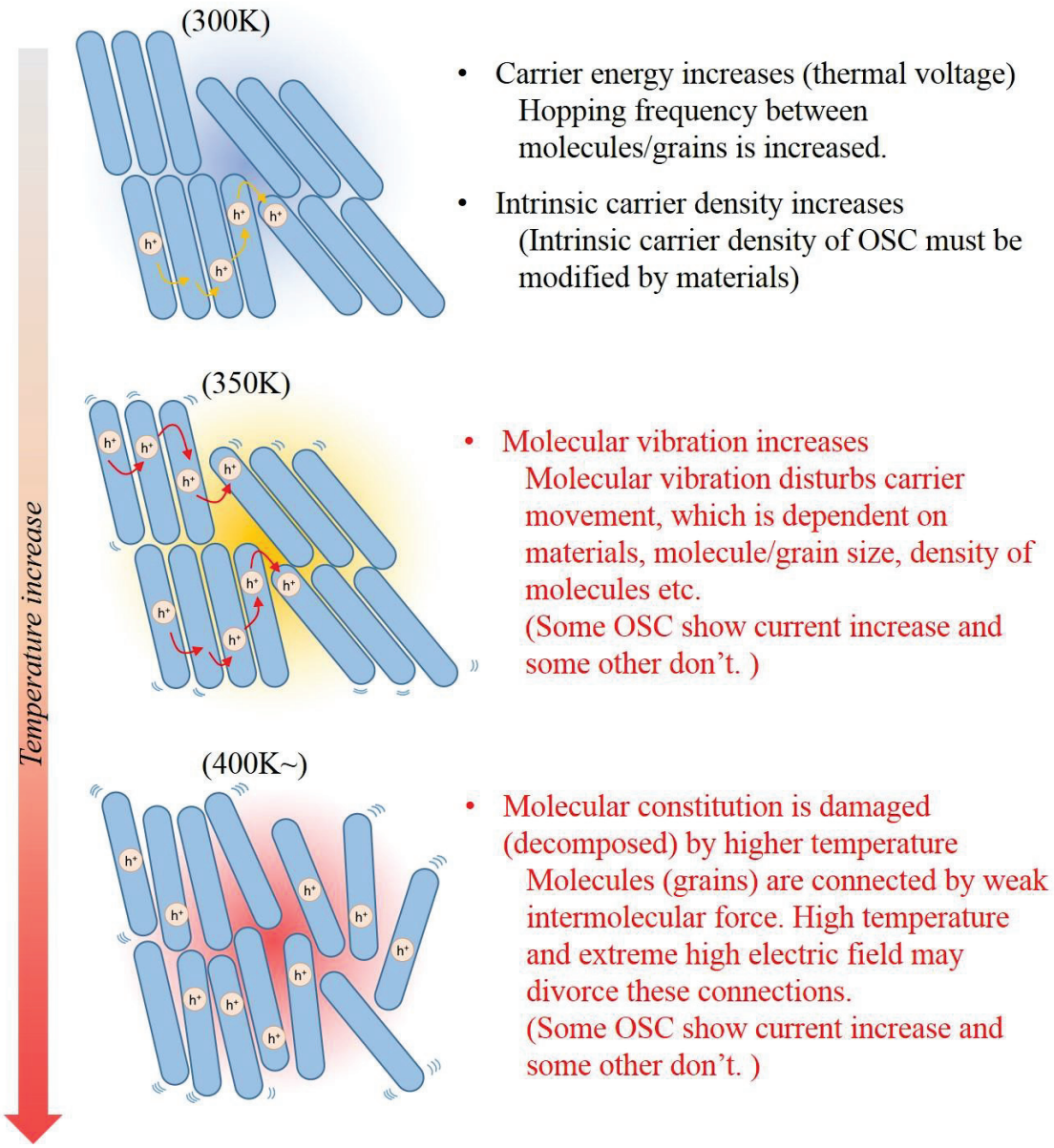
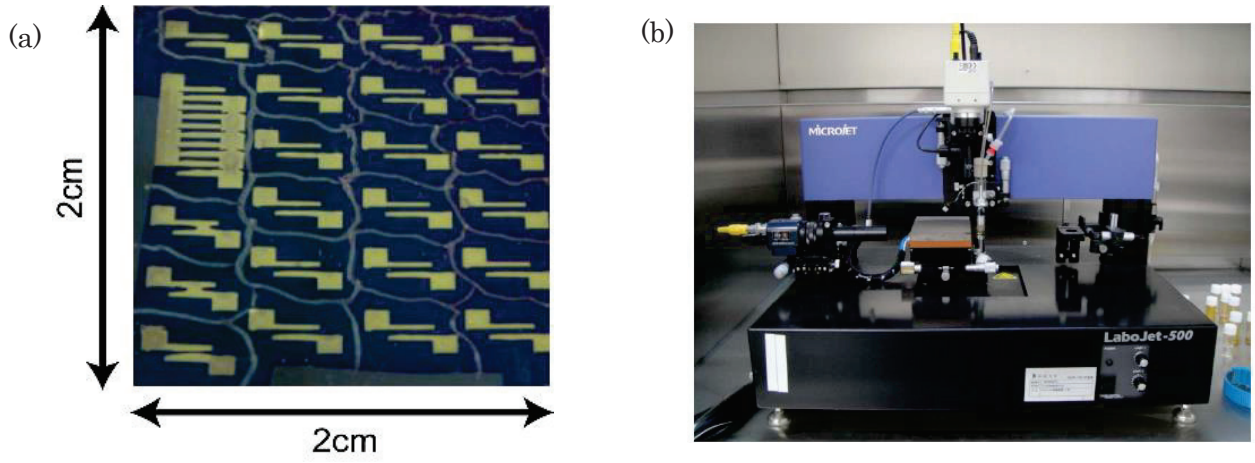


Fig. 5-14: Schematic of influence of elevation temperature on organic molecular constitutions

Notable feature of OFETs temperature dependence is that a universality cannot be observed as inorganic crystalline MOSFETs. That is, there are variety of OFET temperature dependences with no consistent tendencies. Measurements of OFET temperature dependence in different substrates (1~3) are shown in Fig. 5-15 and 5-18. And some other measurements are shown in Fig 5-19 as a reference. Substrate (1) and (2) are the fabricated in chapter 4. Substrate (3) is fabricated by Mr. Hayashi [11] using the IJP patterning for source and drain contact. Picture of a fabricated substrate and IJP instrument [16] are shown in picture 5-1. The device properties are summarized in table 5-1.



Picture 5-1: (a) Fabricated OFETs with use of IJP patterning for source and drain contact and (b) IJP instrument; LaboJet-500, manufactured by MICROJET. [16]

Table 5-1: Summary of device properties fabricated on substrate (3).

Structure	Bottom-gate Top-contact
Channel size	Length = 90 [um] Width = 1500 [um]
Substrate	Heavily doped p-type silicon
Insulator	SiO2 *T*ox = 200nm
Semiconductor	p-type: Dinaphtho-Thieno-Thiophene (DNTT) Torg = 50nm Physical vapor deposition (PVD)
Electrode	Gate: Ag (PVD) Source and Drain: Au
Patterning	Inkjet patterning for Source and Drain
SAMs layer	Tetra-decyl-phosphonic acid (0.2 mmol/L)

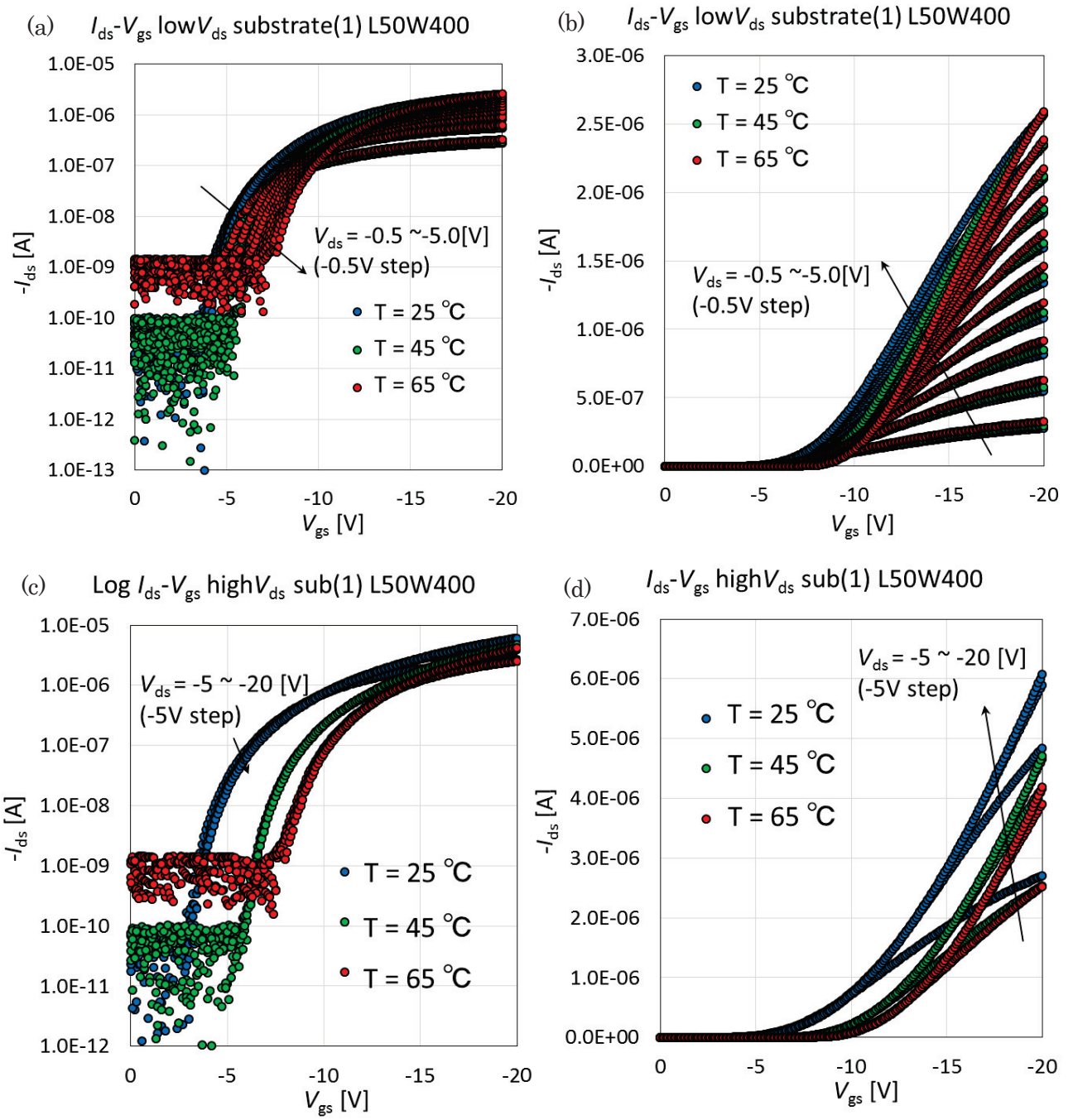


Fig. 5-15: Measurement of OFET temperature dependence in substrate (1) L=50um, W=400um: (a) I_{ds}- V_{gs} at low V_{ds} logarithm plot, (b) I_{ds}- V_{gs} at low V_{ds} linear plot, (c) I_{ds}- V_{gs} at high V_{ds} logarithm plot, and (b) I_{ds}- V_{gs} at high V_{ds} linear plot

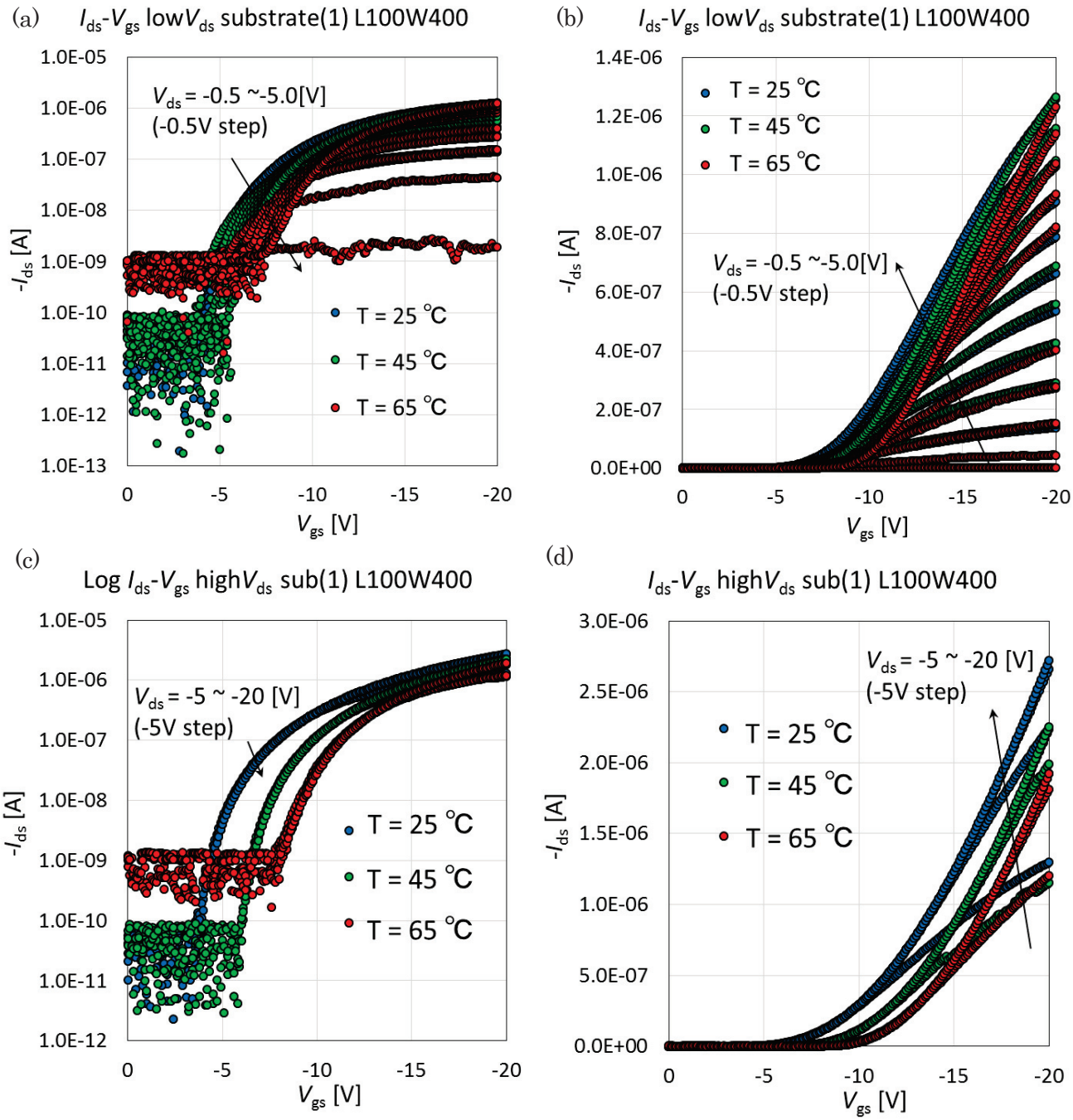


Fig. 5-16: Measurement of OFET temperature dependence in substrate (1) L=100um, W=400um: (a) I_{ds}-V_{gs} at low V_{ds} logarithm plot, (b) I_{ds}-V_{gs} at low V_{ds} linear plot, (c) I_{ds}-V_{gs} at high V_{ds} logarithm plot, and (b) I_{ds}-V_{gs} at high V_{ds} linear plot

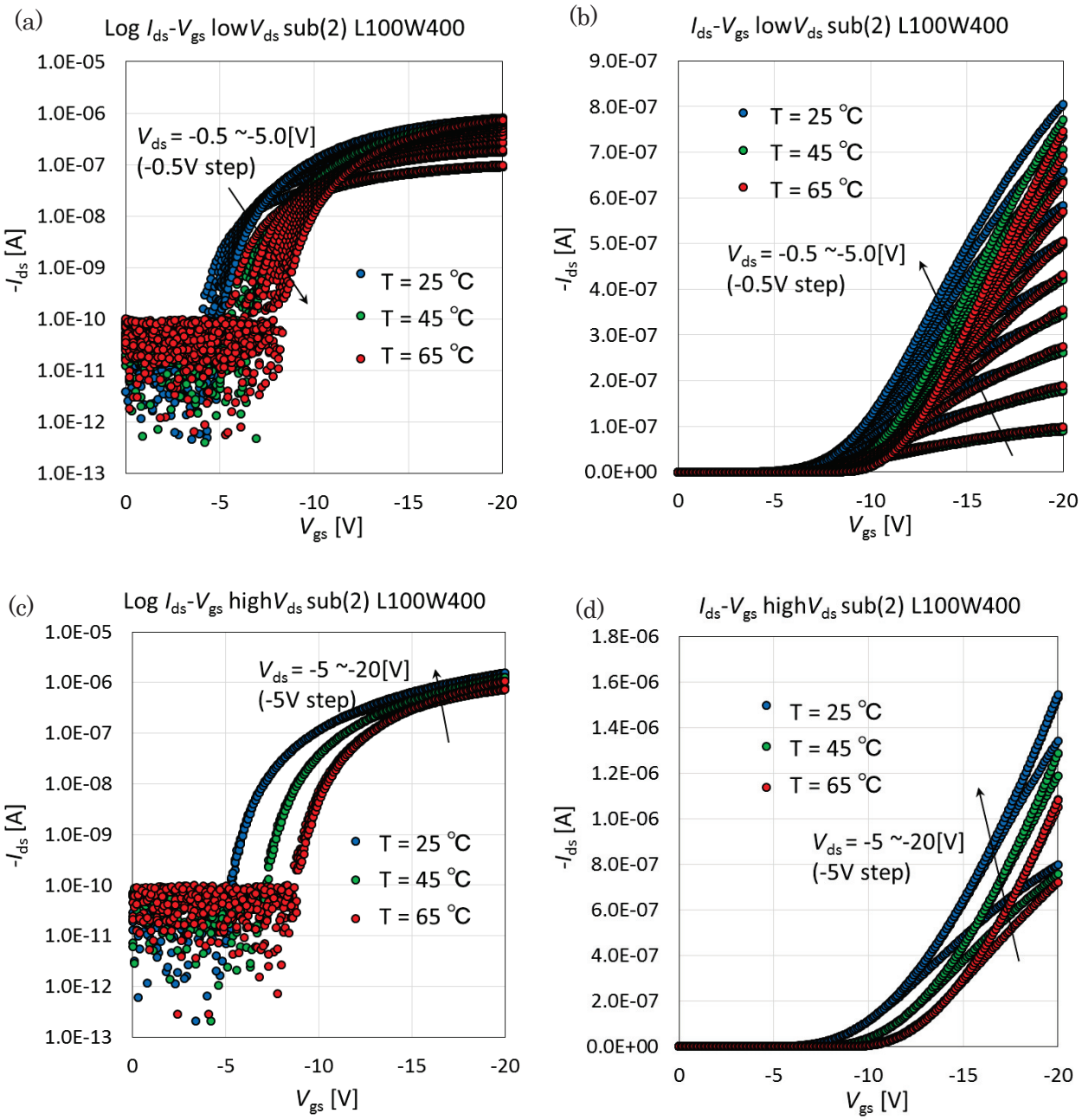


Fig. 5-17: Measurement of OFET temperature dependence in substrate (2) L=100um, W=400um: (a) I_{ds}- V_{gs} at low V_{ds} logarithm plot, (b) I_{ds}- V_{gs} at low V_{ds} linear plot, (c) I_{ds}- V_{gs} at high V_{ds} logarithm plot, and (b) I_{ds}- V_{gs} at high V_{ds} linear plot

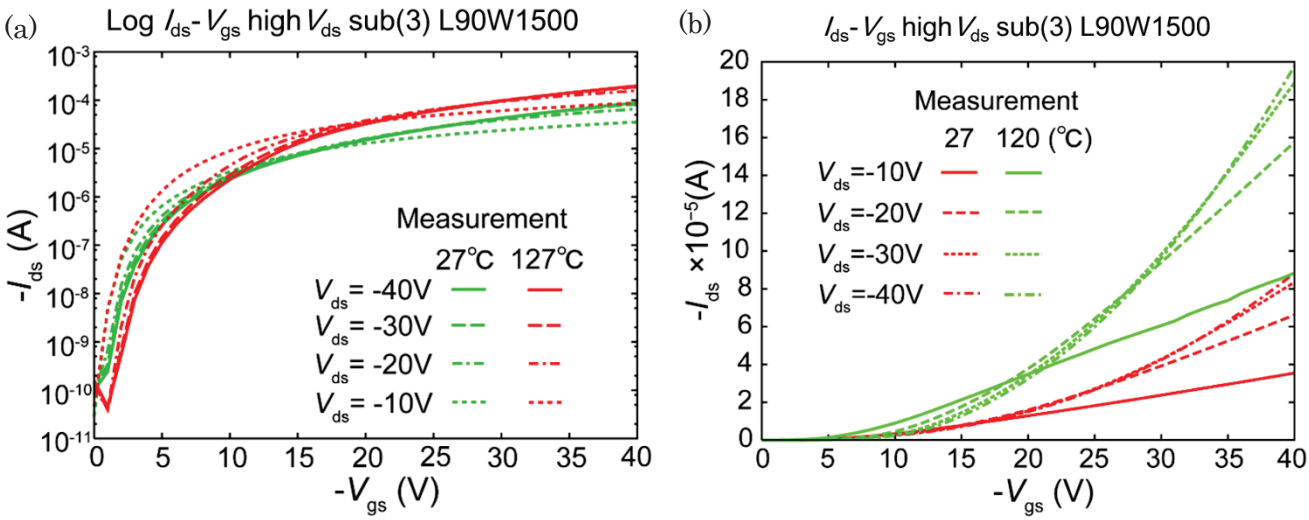


Fig. 5-18: Measurement of OFET temperature dependence in substrate (3) L=90um, W=1500um: (a) I_{ds}- V_{gs} at high V_{ds} logarithm plot, (b) I_{ds}- V_{gs} at low V_{ds} linear plot.

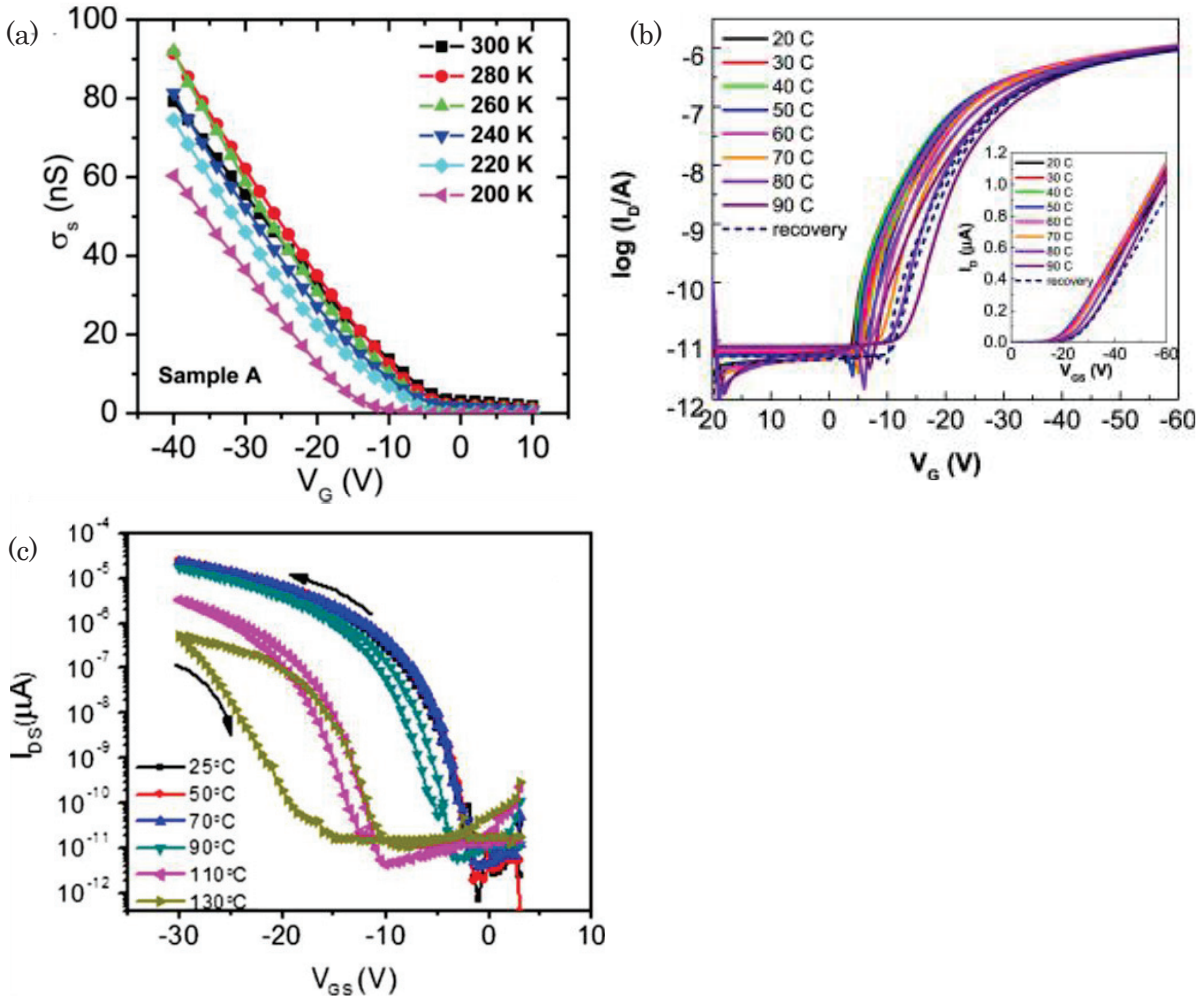


Fig. 5-19: Measurement of OFET temperature dependence from related literatures: (a) Conductivity σ_s vs. Gate voltage V_g of DNTT OFET, (b) I_{ds}- V_{gs} of DNTT OFET, and (c) I_{ds}- V_{gs} of pentacene OFET.

Those measurement data show incoherent OFET temperature dependency in elevating temperature; some devices show thermal-active temperature dependency and some others show thermal-negative temperature dependency. This is because of the difference of materials and the processes. Performance of OFETs has been improved thanks to continuous inventions of organic materials and fabrication technologies. This diversity realize various types of device characteristics, however, this loses versatility of organic device model. The requirement for the OFET device model is being adaptable to the various organic materials.

Developed carrier mobility model (explained in chapter 5-2) is adaptable to such incoherent temperature dependency since it is modeled based on the organic semiconductor physics, has proper parameters. developed model considers the temperature effect mainly through the exponential factor $\exp(-\delta/k_B T)$ in equation (5-17), where δ is a crucial model parameter for thermally activated charge transport which basically defines the change of charge carrier energy from the phonons in the systems.[28-29] The second parameter β, which also contributes to the temperature dependence, has in comparison a much less pronounce influence. Figure 5-20 shows carrier mobility μ as a function of temperature. It is observed that the carrier mobility and its temperature gradient are strongly depending on the parameter δ of the Poole-Frenkel mobility.

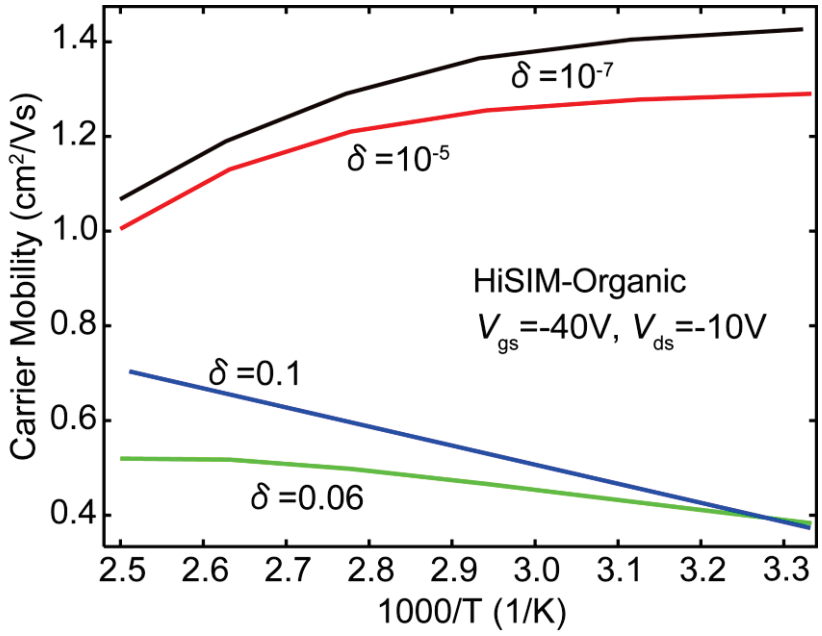


Fig. 5-20: Carrier mobility change due to the temperature dependence parameter σ as a function of temperature (Alenius plot).

5-5: *IV* fitting and parameter extraction

Using HiSIM-Organic, OFETs *IV* characteristics are fitted to the measured *IV* characteristics for normal temperature and elevated temperature. The points for fitting of OFETs *IV* characteristics are;

- Since fabricated OFETs have traps (explained in chapter 5-2), carrier trapping effect must be introduced in the surface potential calculation. Shallow trap and deep trap have effect in different region, namely, shallow trap is effective at low to middle gate voltage region where threshold voltage appears, and deep trap is effective at very low gate voltage (a vicinity of V_{gs}- V_{th} =0V).
- Carrier mobility models; Hopping, Coulomb, and Poole-Frenkel conduction have also different effective region. Hopping conduction is effective at very low gate voltage region, Coulomb scattering is effective at low-middle gate voltage region, and Poole-Frenkel is effective at high gate voltage region.
- Trapping effect, hopping conduction and Coulomb scattering have similar dominant region at low gate voltage. Balancing these three factors is the most important and difficult point for the fitting.

Paying attention to the above points, *IV* fitting is performed with optimizing parameters. The results are shown in Fig. 5-21 for substrate(1) and Fig. 5-22 for substrate(3). It can be seen that IV characteristics of both substrate (1) and (3) are reproduced by HiSIM-Organic with high accuracy. Measurement results of both substrate have anomalous threshold voltage shift by different temperature and drain voltage, therefore, threshold voltage in each condition are modulated with trap parameters in this time.

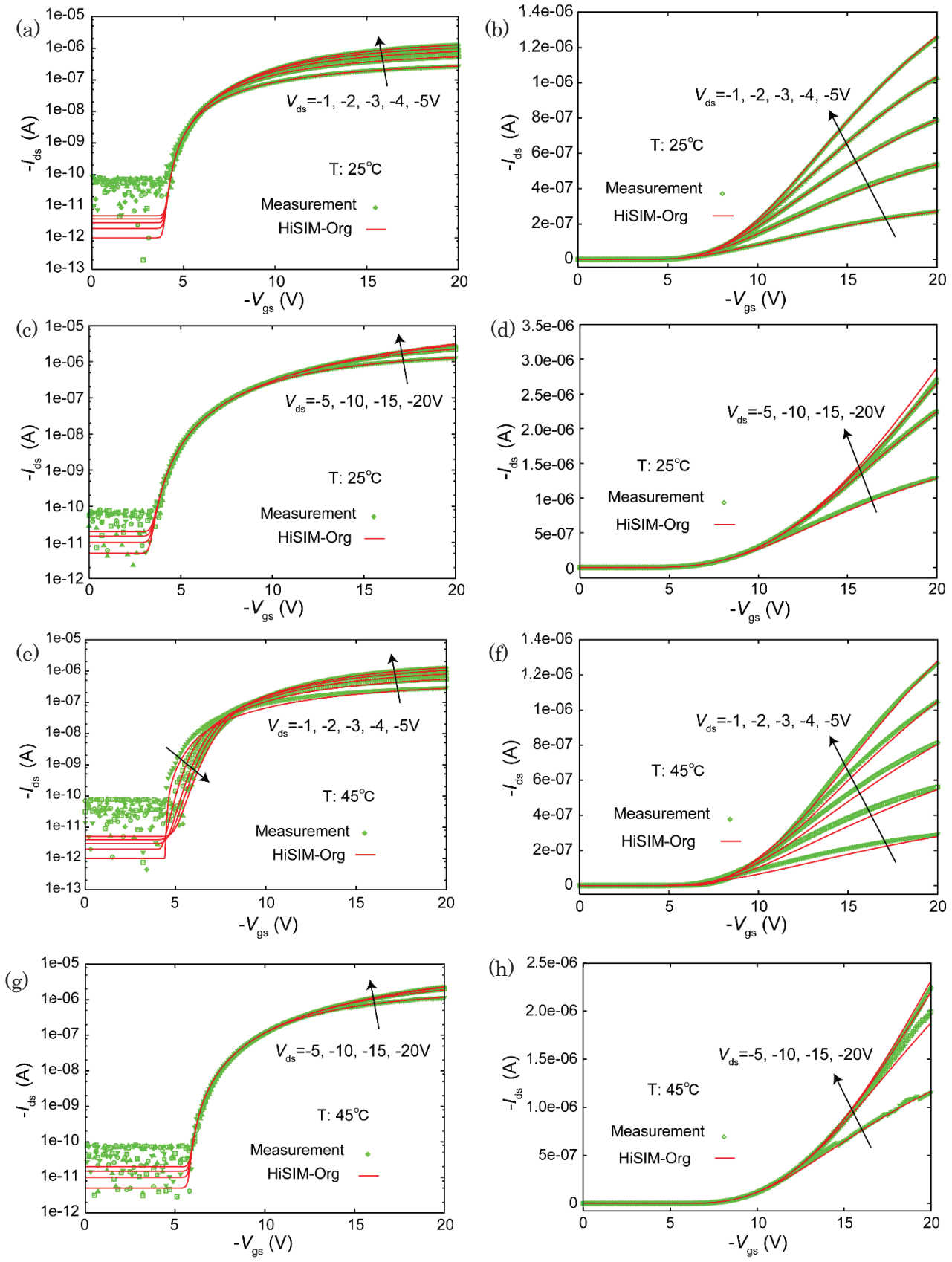


Fig. 5-20: *IV* fitting results for substrate (1): (a) Log I_{ds}- V_{gs} at low V_{ds} in 25 °C, (b) I_{ds}- V_{gs} at low V_{ds} in 25 °C, (c) Log I_{ds}- V_{gs} at high V_{ds} in 25 °C, (d) I_{ds}- V_{gs} at high V_{ds} in 25 °C, (e) Log I_{ds}- V_{gs} at low V_{ds} in 45 °C, (f) I_{ds}- V_{gs} at low V_{ds} in 45 °C, (g) Log I_{ds}- V_{gs} at high V_{ds} in 45 °C, (h) I_{ds}- V_{gs} at high V_{ds} in 45 °C,

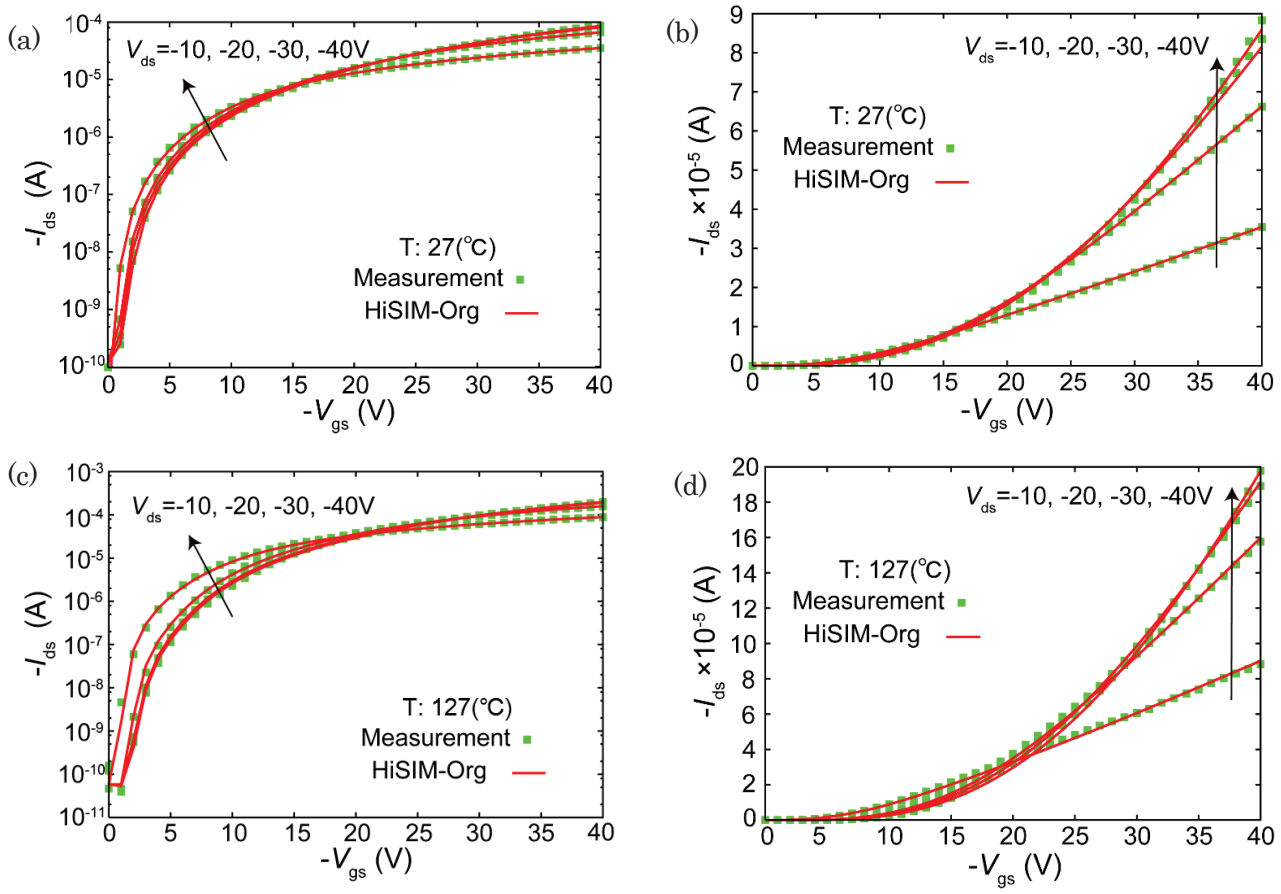


Fig. 5-21: *IV* fitting results for substrate (3): (a) Log I_{ds}- V_{gs} in 27 °C, (b) I_{ds}- V_{gs} in 25 °C,, (c) Log I_{ds}- V_{gs} in 127 °C, (d) I_{ds}- V_{gs} in 127 °C,,

5-5: Discussion

IV fitting is accomplished with remarkable reproducibility in normal temperature and elevated temperature. However, in terms of the degree of difficulty for parameter extraction, it is not much available because the balancing trapping effect and mobility contribution in low gate voltage region. Another reason of the difficulty is that measured OFETs have strong threshold voltage V_{th} shift by varied temperature and drain voltage V_{ds}. V_{th} shift by Vds becomes larger in higher temperature condition as shown in Fig. 5-23?.

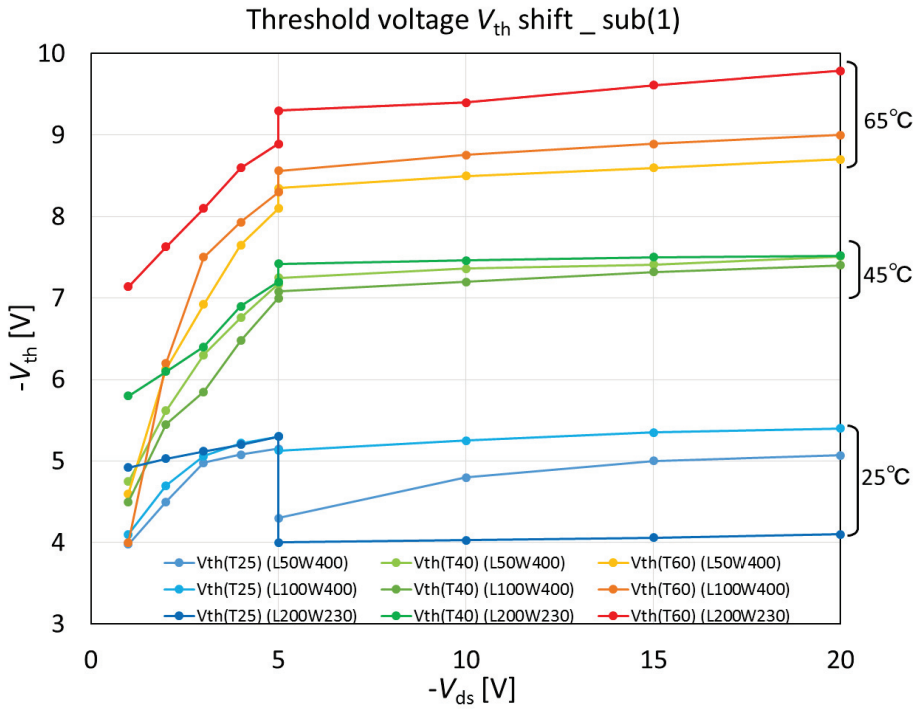


Fig. 5-23?: Threshold voltage V_{th} shift by varied temperature and drain voltage V_{ds}.

In order to reproduce such V_{th} shift, trap determinant parameters have to be modulated in each condition with fixed mobility parameters (each condition has the same mobility parameters) as illustrate in Fig 5-24? for substrate(1) and Fig. 5-25? for substrate (3).

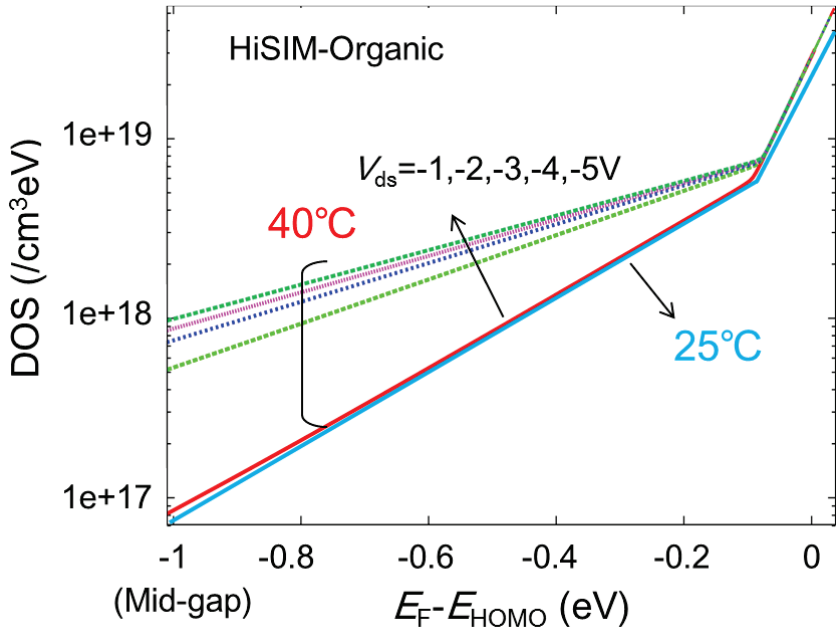


Fig. 5-24?: Trap density of state (DOS) changes by temperature and V_{ds} as a function of E_F-E_{HOMO}.

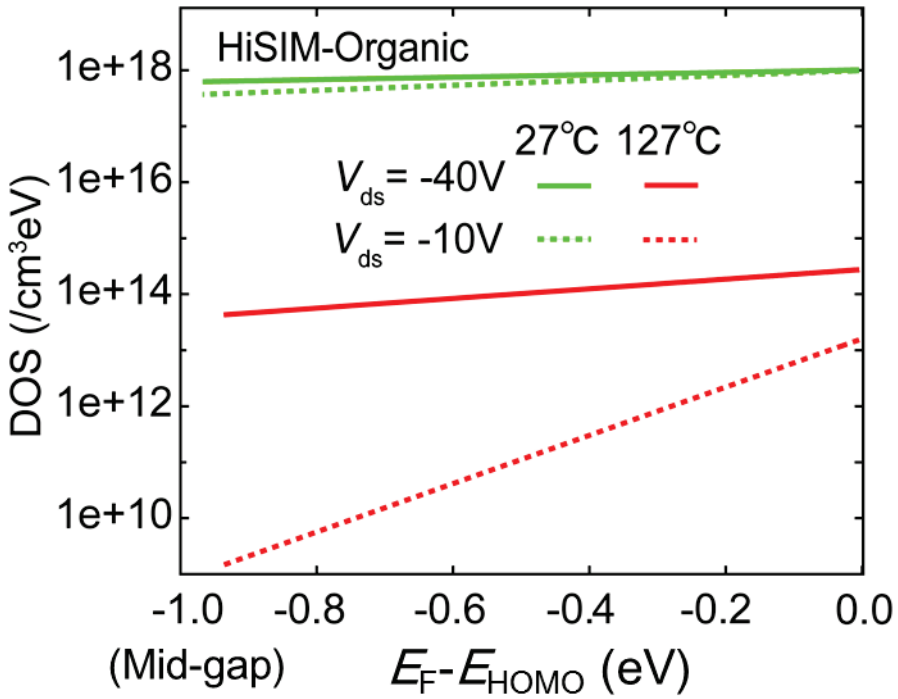


Fig. 5-25?: Trap density of state (DOS) changes by temperature and V_{ds} as a function of E_F-E_{HOMO}.

The complication of V_{th} shift in Ids-Vgs is caused by the instantaneous current deterioration. Organic semiconductor layer has traps within its layer and the interface of insulator. Carrier trapping is a crucial origin of current deterioration that is observed in polycrystalline or amorphous Si MOSFETs as well as OFETs. But those current deterioration amplitudes are different. Deterioration phenomena can be observed from long pulse transient measurement (*IV-t* measurement). Figure 5-26 shows the measurement circuit setup and *IV-t* measurement result of poly Si MOSFET [17]. Usually poly Si MOSFETs and other amorphous type MOSFETs show some deterioration (this is not equal to the aging) and settling after some time.

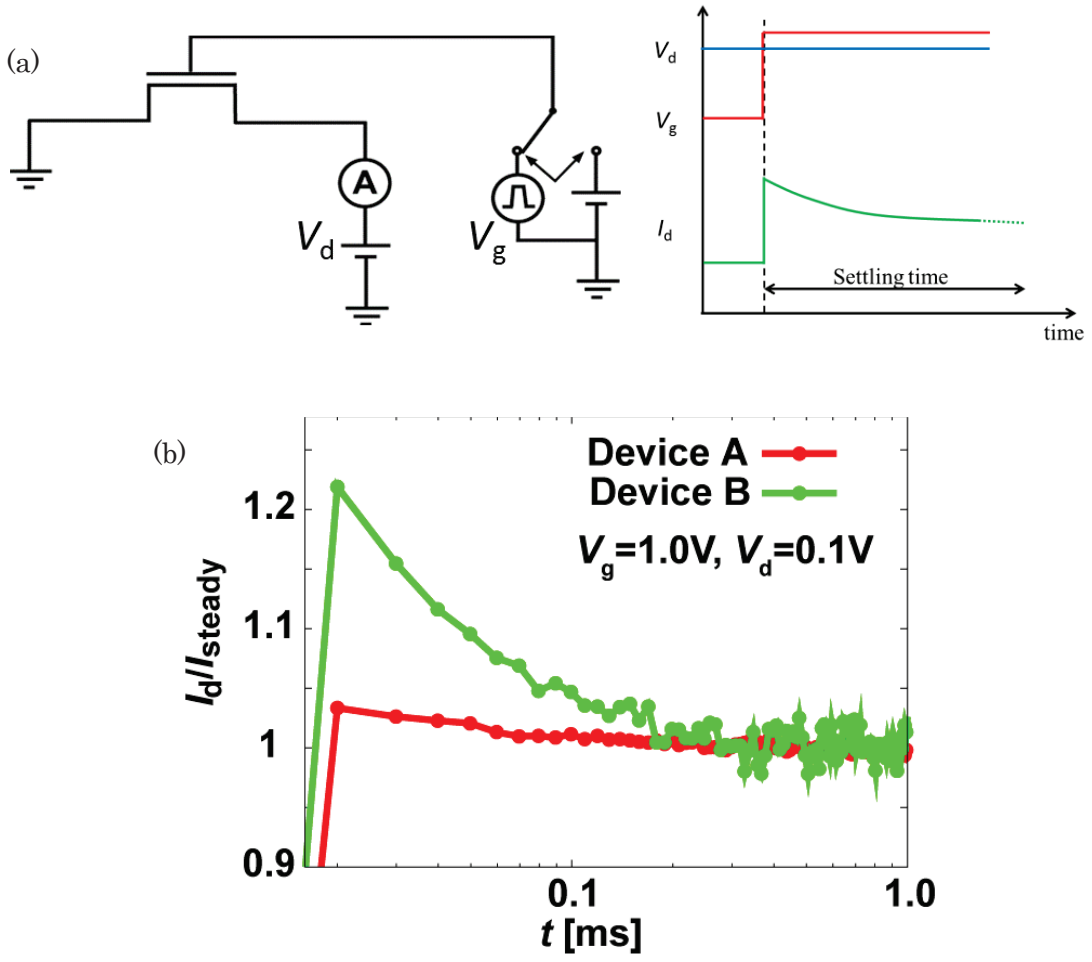


Fig. 5-26: (a) IV-t measurement circuit, and (b) measurement result of poly Si MOSFET. [17]

On the other hand, fabricated OFET doesn't show such quick settlement, but shows successive current deterioration even after a few second shown in Fig. 5-27. However, a quick recovery is also observed in continuous pulse measurement despite of large current deterioration, which is shown in Fig. 5-28.

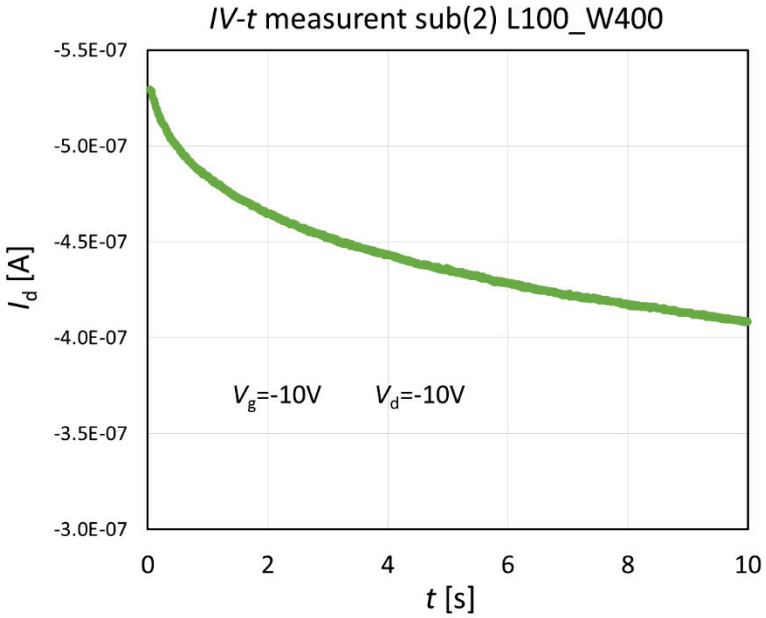


Fig. 5-27: *IV-t* measurement result of OFET, substrate(2) L=100um, W=400um.

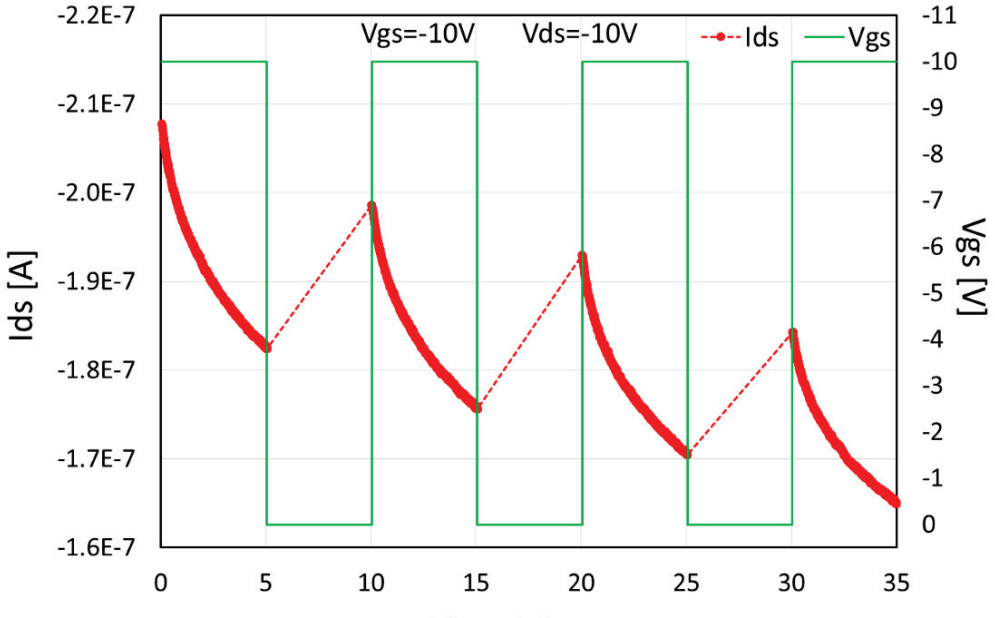


Fig. 5-27: *IV-t* measurement result of OFET, substrate (2), L=100um, W=400um.

Chapter 6

Operation Verification of Organic-based Circuit

6-1: CMOS inverter and ring oscillator

Extracted parameters in chapter 5-5 are introduced in the circuit simulations. As shown in Fig. 6-1, ring oscillator consists of odd number of CMOS inverters in this circuit. CMOS inverter have p-type MOSFET (drain is connected to power source and source is connected to n-type MOSFET) and n-type MOSFET (drain is connected to the earth and source is connected to p-type MOSFET) [1, 2].

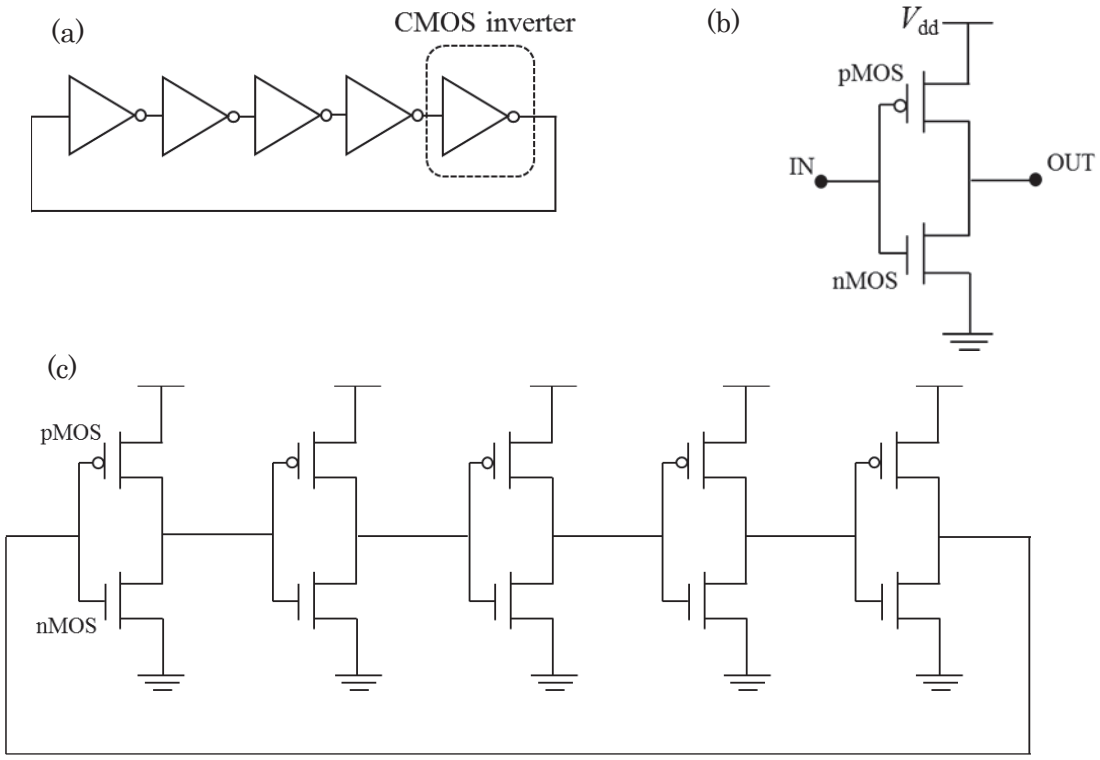


Fig. 6-1: Circuit diagram of (a) 5-stage ring oscillator in logic level, (b) CMOS inverter in transistor level, and (c) 5-stage ring oscillator in transistor level.

Figure 6-2 shows measurement results of CMOS inverter from substrate (1) and substrate (2). The measurement is performed with following condition.

Measurement condition CMOS inverter

Input voltage = 0 ~ 20V 0.1V step, Power Source V_{dd} = 20V.

These CMOS inverters are designed to be the same saturation current of p-type and n-type MOSFET, therefore, the inverter saturation points (namely, the point where input voltage = 10V) are obtained at almost the center of output voltage. But all of them have poor voltage drop at input voltage = 10-20V where p-type MOSFET is off in state and n-type MOSFET is in on state. This phenomena are caused by the difference of threshold voltage difference between p- and n- type.

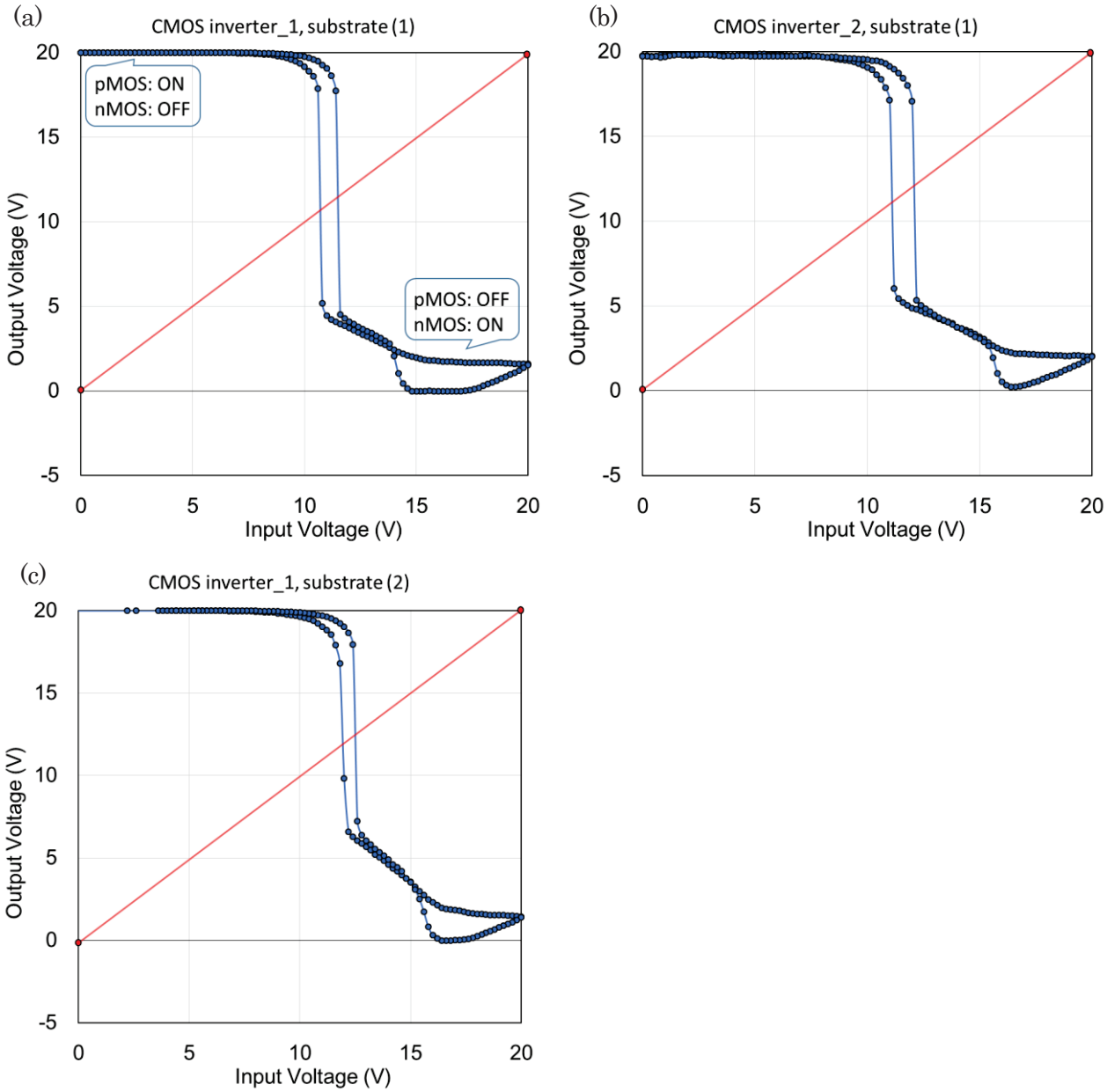


Fig. 6-2: CMOS inverter: (a) & (b) measured result in substrate (1) and (c) measured result in substrate (2).

6-2: Comparison of measured and simulated result

Measured ring oscillator and simulated oscillator are compared in Fig. 6-3 and 6-4. Even though wave form shapes are different between measurement and simulation, oscillation frequencies are very close. Obtained frequency values are summarized in table 6-1.

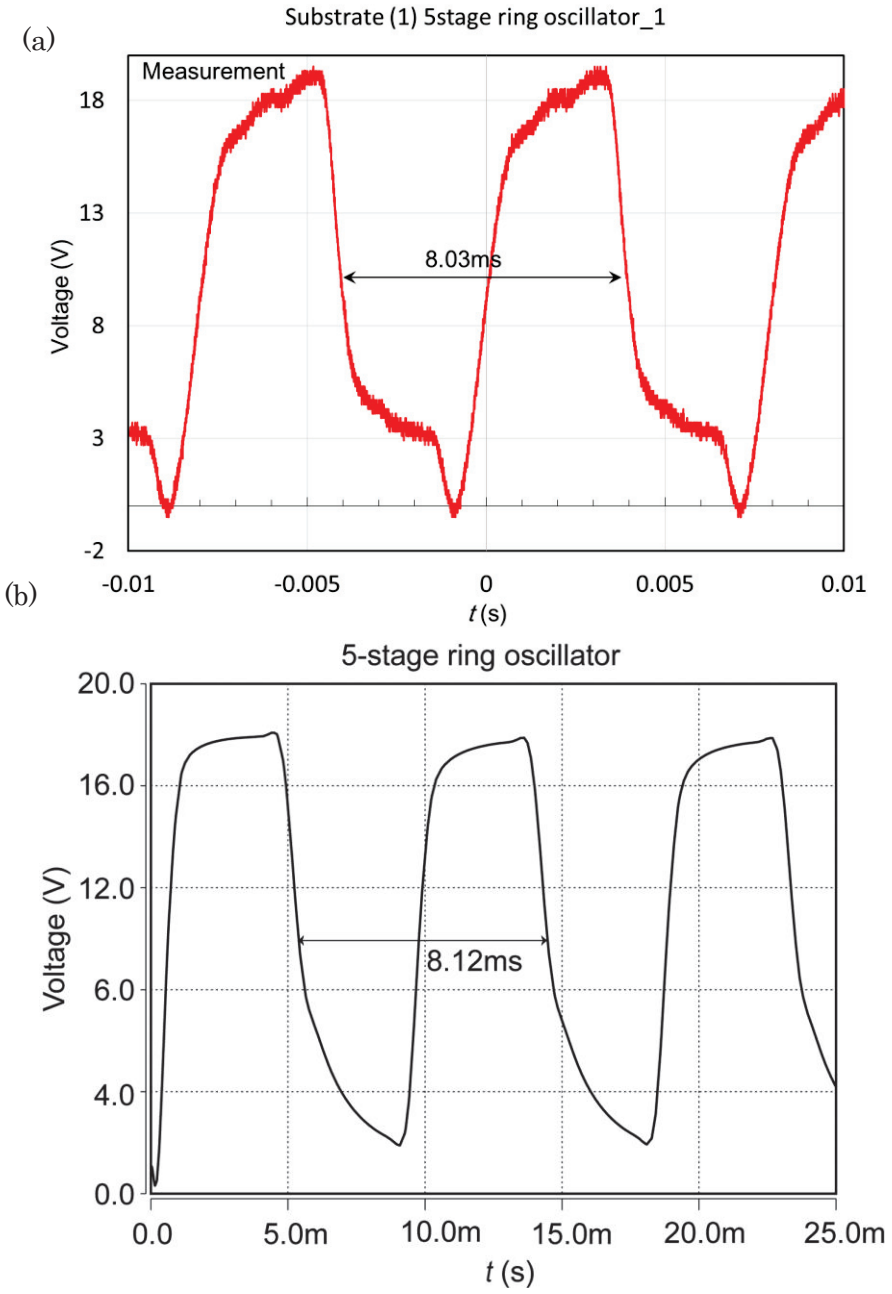


Fig. 6-3: 5-stage ring oscillator wave form of (a) measured result in substrate (1) and (b) simulated result.

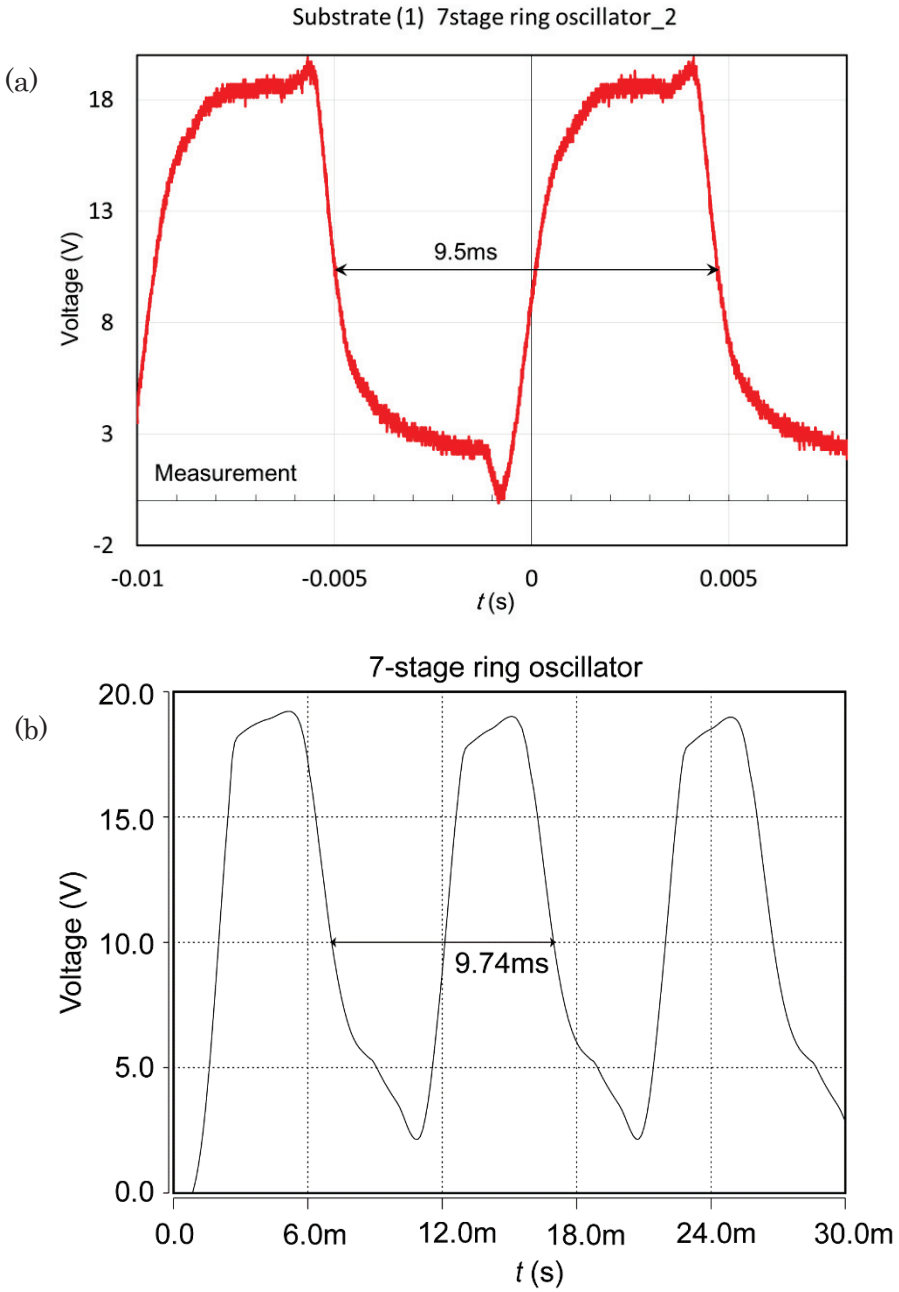


Fig. 6-4: 5-stage ring oscillator wave form of (a) measured result in substrate (1) and (b) simulated result.

Table 6-1: comparisons of ring oscillator frequency for 5-stage and 7-stage.

Ring oscillator	5-stage	7-stage
Measurement	T=8.03ms, f=124.5Hz	T=9.5ms, f=105.3Hz
Simulation	T=8.12ms, f=123.2Hz	T=9.74ms, f=102.7Hz

Ring oscillator wave form gives an inverter transit delay t_d with using equation (6-1);

$$t_d = \frac{T}{2N}, \tag{6-1}$$

where, T is oscillation period and N is the number of inverter stage. Delay of measured 5-stage ring oscillator is 0.80 and that of 7-stage is 0.68 that are comparatively close.

Various materials are employed in OFETs and each materials have different properties. In other words, OFETs performance vary with materials and their combinations. This research emphasizes on the mobility model construction, more model verifications using sufficient amount of OFETs measurement data should be performed to aim more practical model that encourages further development of organic products design. However, developed model is still able to reproduce the fabricated OFETs characteristics and to predict the oscillation frequency accurately, which indicates this model is highly adaptable to various simulations.

Chapter 7
Conclusion

In recent years, devices using organic semiconductor materials attract much attention because they enable new product applications that could not be realized with conventional semiconductor materials. Advantages of organic devices are low-cost simple process by printing technology, flexibility, large area, and diversity of materials and functions. A large number of researches that anticipate the future of organic electronics are being carried out actively in the world. This research was motivated by such a situation and aimed to find new applications of organic devices that can be accepted even in disadvantaged areas such as non-electrified area. This research focused on OPV and OFET to design a boost converter circuit. However, there was no standardized OFET model to design organic circuits. Therefore, the first priority in this research was set to develop OFET device model. Developed model was used in the circuit design. The simulated data using developed model was compared to the measured data for a verification.

This thesis consisted of 6 chapters as main contents. Chapter 1 overviewed the history of inorganic and organic semiconductor and their developments. Three major electronic products; Transistor, Electro-luminescence (EL), and Photovoltaic (PV) were explained to compare features of inorganic and organic products. This clarified the advantage of organic products and helps to consider new application areas. Chapter 2 included a study on new product design of OPV in non-electrified areas implemented with the support of "TAOYAKA program". This chapter started with an outline of the global energy situation and the roles played by renewable energy, and continued to the needs survey conducted in the non-electrified villages in India. A possible solution was discussed from a viewpoint of circuit application toward low energy conversion efficiency of OPV that was found in the survey. Specifically, the solution was to design DC-DC boost converter with organic devices and integrate into the OPV sheet. Chapter 3 is to explain device physics of OFET. Both silicon MOSFETs and OFETs

were explained to identify common and different points properly. Chapter 4 explained important techniques for OFETs fabrication and shows the process that the author had followed. The latter part in this chapter described the measurement results to understand current characteristics which is particular to OFETs. Chapter 5 was focused on device modeling of OFETs. Basic concept of compact device model for circuit simulation: HiSIM was explained at first. HiSIM had been developed based on silicon MOSFET properties, therefore, the features of carrier transport in OFETs had to be considered and described as a carrier mobility model. The process of describing the carrier transport of OFETs was shown step by step. Thereafter, temperature dependence was analyzed because OFETs show different features from Si MOSFETs in an elevated temperature. It was demonstrated that developed model can reproduce such unique temperature dependence. Even though *IV* fitting was accomplished with high reproducibility, parameter modification for elevated temperature and trap determinants were really difficult. It is also discussed that fabricated OFETs has fast degradation phenomena which may deserve to be considered in the model. Chapter 6 is for operation verification of organic-based circuit. DC-DC boost converter (introduced in chapter 2) needs ring oscillator to be operated by pulse signal. Accordingly, oscillation frequency of measured and simulated data were compared to verify whether accurate prediction by developed model is available or not. Simulated frequency was close to the measured data.

Organic electronics is still immature but fast-developing and promising technology. It is sure that further core technology developments and application-driven product designs will be advanced more and more. The organic device model developed in this research is likely to be utilized in the industrialization of organic products. It is also expected that the device model itself can be developed to further more reliable one by establishing the materials and manufacturing methods of organic semiconductor devices.

Acknowledgement

本研究にあたり、様々な御助言をして頂き、これまでの活動を温かく見守って下さった広島大学工学研究科の餘利野直人教授に心から感謝致します。

本研究に関する論文執筆にてご助力頂き、研究倫理についてもご教授下さった広島大学 HiSIM 研究センター所長の Mattausch Hans Jürgen 教授に心から感謝致します。

半導体デバイスに関する知識と様々な研究活動について熱心な御指導と御助言をして頂き、また大学院リーディングプログラム「たおやかプログラム」への参加を推薦して下さった広島大学先端物質科学研究科の三浦道子特任教授に心から感謝致します。

有機半導体に関して様々な知識を共有してくださり、また研究のサポートをして下さった HiSIM 研究センターの Tapas Kumar Maiti 助教授に心から感謝致します。

有機トランジスタの製造に関する知識や技術をご教授下さった、大阪府立産業技術総合研究所の中山健吾様、宇野真由美様に心から感謝致します。

研究面だけでなく、様々な面でのサポートをして頂いた、三宅正尭准教授、菊地原秀行特任助教、飯塚貴弘准教授、Dondee Navarro 准教授、Sandip Bhattacharya 研究員、Fernando Avila 研究員に心から感謝致します。

Linux や Windows において技術的なサポートをして下さった技術センターの落祥弘様に感謝致します。

たおやかプログラムにおけるインドでのフィールドワークにて多くのサポートをして下さり、技術者としての心得を教えて下さった国際協力研究科の金子慎治教授に心から感謝致します。

インドでのフィールドワークにて、太陽電池利用の現状とエネルギー情勢について様々な情報を共有して頂いた、CREDA の Rajeev さん、Sanjeev さんに心から感謝致します。

たおやかプログラムでの活動にて様々なサポートをしてくださったたおやかプログラム事務室及びたおやか技術創生事務の皆様に感謝致します。

研究に関して様々な助言をして頂いた、極微細デバイス工学研究室の卒業生である福永幸哉様、上野文也様、大舘悠平様、田之上寛様、井上拓也様、松浦快様、北村雅史様、西村知也様、斎藤敦様、松井良祐君、谷本祐太君、宮奥洋介君、問田真基君に感謝致します。

あまり先輩らしい事をしてあげられなかったにもかかわらず、様々な場面で慕ってくれた、極微細デバイス工学研究室の後輩である、岡田泰裕君、佐藤健志郎君、刀根彰宏君、荒木孝太君、鈴木大君、平野陽子さんに感謝致します。転学後、温かく迎えてくれた電力エネルギー工学研究室の後輩達に感謝致します。

多くの事を教え合い、挫けそうな時は互いに支えあった同輩の中村優希君、張ショウイクさん、Alam さん、Sunandan Datta 君、そしてたおやかプログラムにて関わったすべての学生皆様に心から感謝致します。

最後に、博士課程後期に進むことに理解を示し、故郷からずっと応援してくれた祖母、母、兄と亡き父に心から感謝致します。

2019 年 1 月 18 日　銭谷　宙

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List of Publication

A. Published international journal papers (peer reviewed)

1. H. Zenitani, H. Kikuchihara, U. Feldmann, H. Miyamoto, H. J. Mattausch, M. Miura-Mattausch, T. Nakagawa, and N. Sugii. “Mobility model for advanced SOI-MOSFETs including back-gate contribution”. Japanese Journal of Applied Physics 54(4S):04DC03, April 2015.
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B. International Conference Papers (peer reviewed)

1. H. Miyamoto*, Y. Fukunaga, H. Zenitani, H. Kikuchihara, H.J. Mattausch, T. Nakagawa, N. Sugii, and M. Miura-Mattausch. "Modeling of short-channel effect for ultra-thin SOI MOSFET on ultra-thin BOX". Technical Proceedings of the 2014 NSTI Nanotechnology Conference and Expo, Washington DC, June 2014.
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4. Y. Okada*, Y. Tanimoto, T. Mizoguchi, H. Zenitani, H. Kikushihara, H.J. Mattausch, M. Miura-Mattausch. "Compact modeling of GaN HEMT based on device-internal potential distribution". International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Washington DC, USA, September 2015.
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7. H. Zenitani*, A. M. Jahangir, "Exploring New Applications of Future Organic PV in Non-electrified Areas", International Conference of Grand Renewable Energy 2018, Yokohama, Japan, June 2018.

Table for related papers in each chapter

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Chapter 2	Organic Photovoltaic	A-4	B-7
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Chapter 5	Device Modeling of Organic MOSFETs	A-1, 2, 3, 5	B-1, 2, 3, 4, 6
Chapter 6	Operation Verification of organic-based circuit	A-2, 4	B-3, 5
Chapter 7	Conclusion	A-2, 3, 4	B-3, 5, 7

*Chapter 2 includes TAOYAKA Onsite Team Project.

Award

1. HIRAKU 3MT Competition 2017, Sponsor awards (JSW Awards), “Organic solar PV plays an active part at the disadvantaged area in the world!?”