博士論文

Compact Modeling of Gallium-Nitride-based High Electron Mobility Transistor for High-Power Circuit Applications

（高電力用途における窒化ガリウム高電子移動度トランジスタのコンパクトモデル）

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主論文

Doctoral Dissertation

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(高電力用途における窒化ガリウム高電子移動度トランジスタのコンパクトモデル)

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Preface

Power semiconductor devices composed of different materials have been developed for different inverter and converter circuit applications at different power supply voltages. Among them, Gallium-Nitride-based High-Electron-Mobility-Transistor (GaN-HEMT) is considered to be very attractive in the view of its applicability for both high power and high speed simultaneously. In fact, as the GaN material can realize lower power loss in certain application ranges because its on-resistance is lower than those of silicon-based materials, GaN-HEMTs have already been successfully utilized for blue light-emitting diode applications. GaN-HEMTs generate a high-density two-dimensional electron gas (2DEG) structure at the heterojunction interface between AlGaN and GaN layers. Owing to the wide bandgap together with the high electron mobility, it is expected that GaN-based power devices can realize lower on-resistance and higher breakdown voltage. This indicates that constructing eco-systems can be achieved by GaN-based power devices.

Circuit simulation is an important technology for the integrated circuit (IC) design and SPICE (Simulation Program with Integrated Circuit Emphasis) is used as an essential computer-aided design tool for the design purpose. It allows to simulate circuits prior to their fabrication and predict detailed circuit performance. A compact model mathematically represents the device characteristics under various bias conditions. The model parameters, along with the equations in the compact model, directly affect the final outcome of the terminal currents. To predict circuit performance, an accurate extraction and understanding the device model parameters is essential. The compact model is therefore also a powerful tool for the power electronics design. Although some previous models for GaN-based power devices

were proposed, the power efficiency prediction has not been well analyzed. In power-circuit design, the power efficiency is a particularly important concern for high-power applications. In order to accurately predict power efficiency for circuit optimization, compact models applied for circuit simulation must be sufficiently accurate. Not only accurate prediction of DC and AC characteristics, but also that of circuit performances, such as the conduction loss and the switching loss, is required.

The HiSIM (Hiroshima University STARC IGFET Model) compact model is the result of research work pioneering the application of the surface-potential modeling to MOSFETs fabricated with advanced technologies, which was carried out as a cooperation between Hiroshima University and the Semiconductor Technology Academic Research Center (STARC). This thesis presents a newly developed compact model for the GaN-HEMT device called "HiSIM-GaN". The developed model includes two specific features of the GaN-HEMT to reproduce the power efficiency accurately. One is the two-dimensional electron gas induced at the heterojunction, which is modeled by considering the potential distribution across the junction including the trap density contribution. The second feature is the field plate (FP), which is introduced to delocalize the electric-field peak that occurs at the electrode edge. It is demonstrated that measured DC/AC characteristics are well reproduced with the developed compact model HiSIM-GaN.

Furthermore, the capabilities of the developed model are demonstrated by reproduction of the measured power efficiency of a boost converter circuit, enabled through separate extraction of the parasitic FP contributions. In addition, physical trap-density modeling is verified to be also of key importance for accurate prediction of the power efficiency. It is concluded that extraction and modeling of FP effects, parasitic components and carrier-trapping effects in the GaN-HEMT device are essential for predicting the switching waveform and the power efficiency of GaN-HEMT circuits accurately.

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Chapter 1

Introduction

1.1 Backgrounds

The first electronics revolution began in 1948 with the invention of the transistor by American scientists J. Bardeen, W. H. Brattain, and W. B. Shockley from the Bell Telephone Laboratories [1]. Later they were awarded a Nobel Prize for this invention. Most of today's advanced electronic technologies are traceable to that invention. Since, semiconductor devices have made dramatical progress. Currently, crystal growth techniques and mature silicon device-process technologies occupy a large portion of the development efforts in the field of the semiconductor devices. In accordance with the silicon device scaling-law, integration density, processing speed and low power consumption are progressing by advancing on the road of miniaturization. As a result, the gate length of the silicon-based metal-oxide-semiconductor field effect transistor (MOSFET) has been reduced to 20nm grade. On the other hand, if the gate length is short, the power supply voltage must be reduced to keep device-internal electric fields lower than the breakdown electric field. Since the power supply voltage can be reduced only to about 250mV theoretically, there are the limitations to the gate-length reduction. This limitation for the gate-length reduction is considered to be about 7nm. Furthermore, the saturation velocity of 1.0×10^7cm/s for Si-based devices is relatively low. For achieving still higher speeds and higher output powers, therefore, compound semiconductors are utilized.

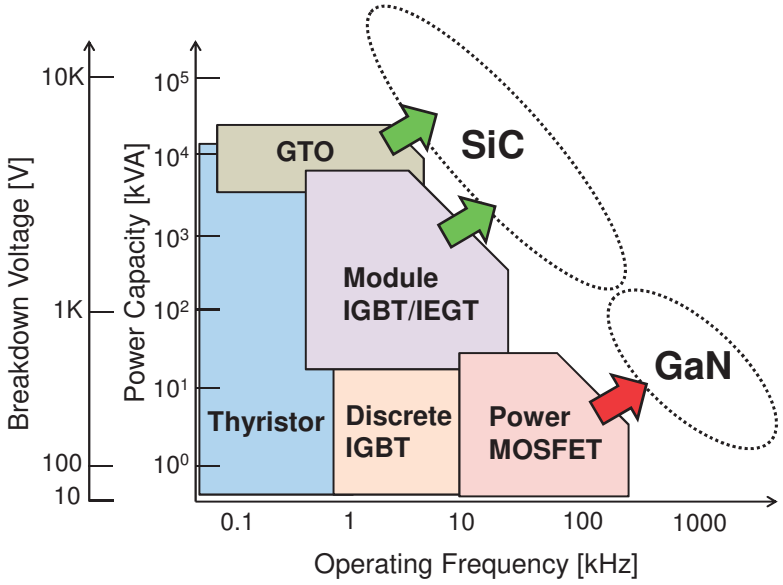

Figure 1.1: A classification of power electronics devices.

Power semiconductor devices composed of different materials have been developed for different inverter and converter circuit applications at different supply voltages. These high power devices determine the circuit-switching characteristics in applications such as voltage conversion or motor control. Figure 1.1 shows a classification of different power-electronic device types with respect to the operating frequency and power capacity, identifying the high-efficiency application areas of each device type [2]. The low power-loss feature of a switching device is an essential factor in the energy conservation. The power loss of a switching device is divided into the conduction loss and the switching loss. An ideal electrical switch is one that shows zero resistance in the on state, and a resistance of infinity in the off state. However, these two requirements always have a trade-off relationship. In the electric power conversion, handling of high voltages is often required, while the power loss should be minimized as much as possible. From these requirements, switching devices are usually classified by the indexes of specific on-resistance (R_{on}) and blocking voltage.

Conventionally, power electronics has been developed on the basis of Si-based devices such as the metal-oxide-semiconductor field effect transistor (MOSFET),

the gate turn-off thyristor (GTO), and the insulated gate bipolar transistor (IGBT). However, these Si-based power device characteristics are reaching the material limit. Therefore, the expectation of small and low power loss switching devices based on wide band-gap semiconductors such as Silicon-Carbide (SiC) and Gallium-Nitride (GaN) has increased owing to their superior material properties. A specific on-resistance mainly consists of the resistance of the drift region and that of the channel region for power semiconductors. Using SiC and GaN materials, the resistanc
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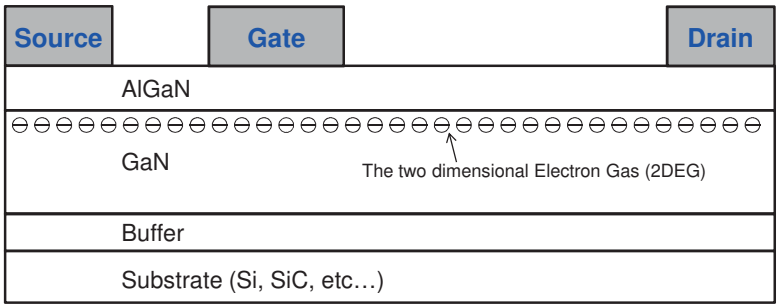

Figure 1.2: Cross-sectional schematic of the typical GaN-HEMT device.

Gallium Nitride (GaN) devices had already been noted about twenty years toward the high-temperature and high-voltage applications. By M. A. Khan et al., the first GaN-based MESFET (Metal-Semiconductor Field Effect Transistor)

Table 1.1: Comparison of typical power semiconductor material properties. BFOM is Baliga's figure of merit for power transistor performance calculated by ($\epsilon_r \mu E_g^3$).

	Si	**4H-SiC**	**GaN**
Band gap E_g (eV)	1.12	3.2	3.4
Dielectric constant ϵ_r	11.9	10	9.5
Critical electric-field E_c (MV/cm)	0.3	3	3.3
Electron mobility μ ($cm^2V^{-1}s^{-1}$)	1300	650	900
Electron velocity saturation V_s (10^7cm/s)	1	2	2.5
Baliga's FOM ratio	1	9.8	15.5

was reported in 1993, and after that, AlGaN/GaN HEMT was also reported in 1994 [3, 4]. When I. Akasaki, H. Amano, and S. Nakamura were awarded a Nobel Prise in 2014, the competition in the field of the GaN-based device development has accelerated all at once.

GaN-HEMTs are considered to be very attractive in view of their applicability for both high power and high speed simultaneously [5]. In fact, as the GaN material can realize lower power loss in certain application ranges because its on-resistance is lower than those of silicon-based materials, GaN-HEMTs have already been successfully utilized for blue light-emitting diode applications [6–8]. Table 1.1 shows a comparison of important typical power semiconductor material properties [9, 10]. The most important point about the channel layer in the AlGaN/GaN HEMT structure is a high-density two-dimensional electron gas (2DEG) structure, which is induced at the AlGaN/GaN hetero-junction interface by the spontaneous polarization as well as the piezoelectric polarization due to the strain. The 2DEG charge density at the AlGaN/GaN hetero-junction reaches more than $10^{13}cm^{-2}$. Due to the high saturation velocity (2.5×10^7cm/s) and the high critical electric field (2×10^6V/cm) compared with Si-based devices, GaN-based devices are suitable for the high frequency operation and the high power application. According to Baliga's figure of merit (FOM), where the value is set to one for Si, SiC and GaN devices provide values superior to those of Si-based devices. In particular,

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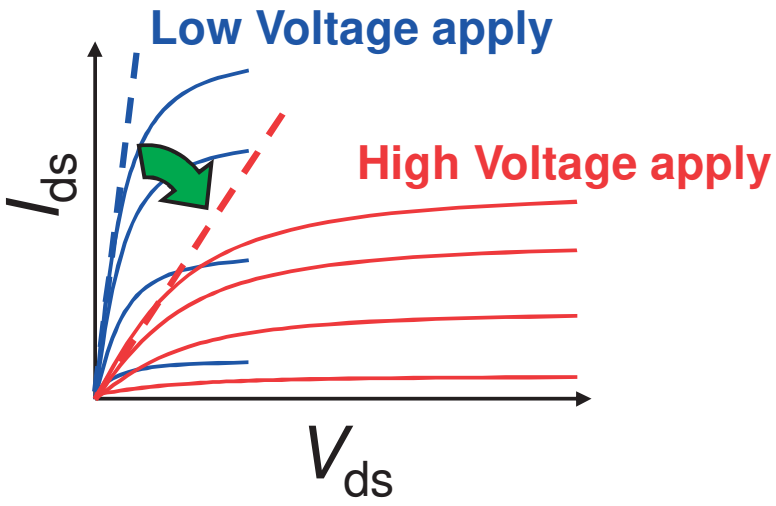

Figure 1.4: Effect of the current collapse on the I_{ds}-V_{ds} characteristic. The on-resistance increases and the saturation current decreases for the high voltage application.

The current collapse phenomena strongly depends on the electric field at the 2DEG channel due to the acceleration of the channel electrons. A part of the

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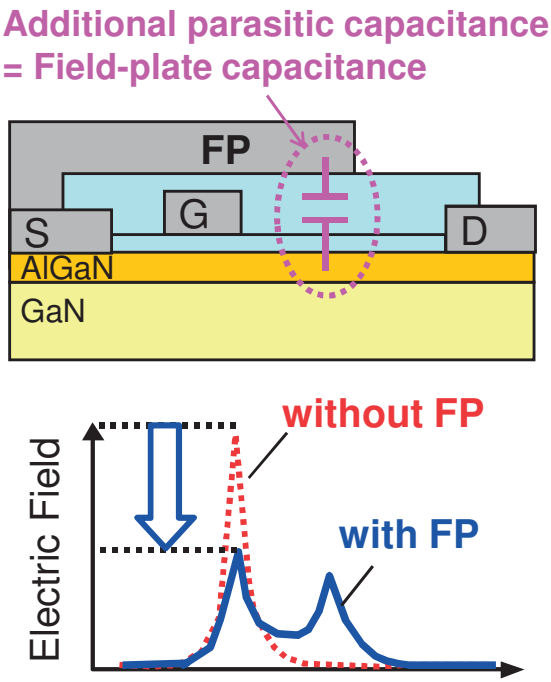


Figure 1.5: Cross-sectional schematic of the effect of a field-plate for the GaN-HEMT device.

As a high drain voltage is applied, the electrical flux lines are induced from

the edge of the drain electrode to that of the gate electrode. Therefore, an electric field concentration is caused at the edge of the gate electrode and the current collapse phenomena is induced by the accelerated electrons in the 2DEG region by the high electric field. A significant improvement of the device performance has been achieved by adopting the field plate (FP) technique [14]. With its origins in the context of high-voltage p-n junctions the main functions of the field plate are to reshape the electric field distribution in the channel and to reduce its peak value on the drain side of the gate edge. The benefit is an increase of the breakdown voltage and a reduced high-field trapping effect [15]. Figure 1.5 shows the cross-sectional schematic of the field-plate effect for the GaN-HEMT device. By spreading the concentration point of the electric field, the peak value of the maximum electric filed is relaxed. Hence, the current collapse phenomenon is also suppressed by decreasing the trapping event at the 2DEG region. However, an additional parasitic capacitance is induced by the existence of the field-plate as shown in Fig 1.5. This parasitic capacitance plays an important role for the switching characteristics of power semiconductors. Therefore, estimation of the capacitance caused by the field-plate is a key task for the accurate prediction of the power efficiency.

The structural parameters for the FP are mainly the length along the FP and the dielectric-thickness under the FP electrode. The lengths of FP-regions along with their gate-capacitances or equivalently, dielectric-thicknesses of FPs, for given dielectric permitivity, are design-parameters which are usually optimized to get the desired the breakdown voltage for a given gate-length and drain-gate spacing.

1.2.3 High Speed Switching

Figure 1.6 compares the non-linear C-V characteristics of the GaN-HEMT device to a Si-based IGBT and a Super-Junction MOSFET, which clearly indicates all of the three parasitic capacitances (the input capacitance C_{iss}, the output capacitance C_{oss}, and the reverse transfer capacitance C_{rss}). As shown in Fig 1.6, the

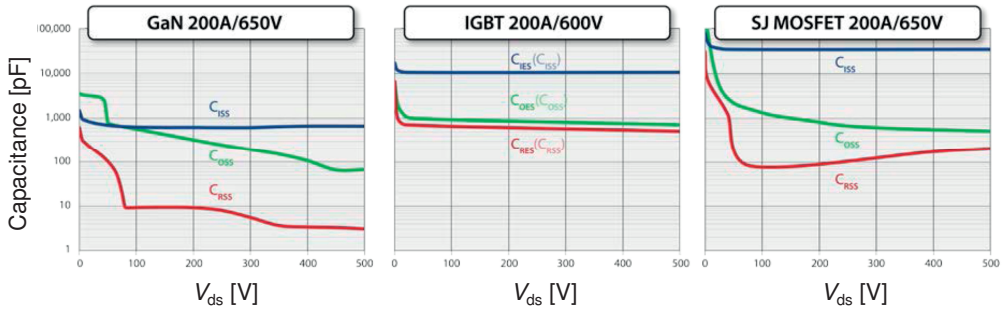
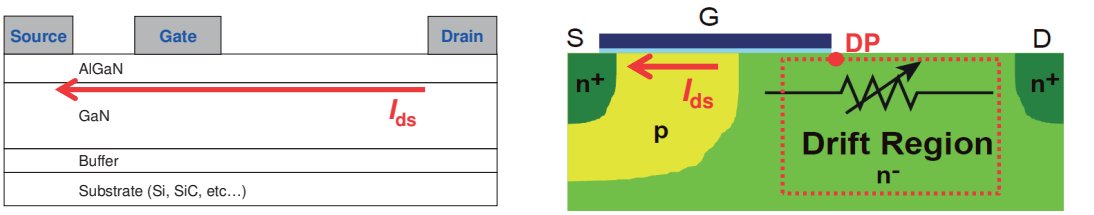


Figure 1.6: Comparison of measured C-V characteristics with the conventional GaN-HEMT, Si-based IGBT, and Si-based SJ- MOSFET [16].

GaN-based device has significantly lower capacitance than the Si-based devices. Particularly, the non-linearity of Si-based devices is more prominent so that the capacitance at low voltage is usually tens of times larger than the capacitance at high voltage. The strong non-linear property makes Si-based devices to exhibit longer turn-on and turn-off delay time as well as voltage/current rising/falling transition time. Consequently, it is even harder for Si-based devices to be used at high MHz frequencies. As a comparison, the non-linearity of the GaN-HEMT parasitic capacitor is much alleviated so that the switching transition can be finished significantly faster than with Si-based devices. Because lower capacitance leads to high speed switching, GaN-based devices can realize the construction of highly efficient systems.

1.3 Requirement of Compact Models

Generally, power semiconductor devices are utilized for the high-power analog circuit. In order to estimate the analog behavior accurately, compact model are required for a considerable wide range of the operating voltage and with high reproducibility of current-voltage (I-V) and capacitance-voltage (C-V) characteristics as specific features for the high power electronics circuit design. As an industry-standard compact model for power MOSFETs, by considering the resistance effect at the drift region and anomalous characteristics for the capacitances of high-voltage MOSFETs, which become more pronounced with lower concentra-



(a) Simplified GaN-HEMT

(b) High-Voltage MOSFET (HV-MOSFET)

Figure 1.7: Current flow of the GaN-HEMT and the HV-MOSFET.

tions of the drift region, HiSIM_HV has been mainly utilized for the circuit design using power MOSFETs [17, 18].

As mentioned earlier, GaN is an attractive material for the next generation power semiconductors. In order to design for GaN-based systems, accurate device-level compact models that describe the stand-alone device terminal characteristics as well as device behavior in circuits are critically required. Figure 1.7a shows the current flowing of the GaN-HEMT. The drain-source current of the GaN-HEMTs flows through the 2DEG channel caused at the AlGaN/GaN interface. On the other hand, as shown in Figure 1.7b, the drain-source current of the high-voltage MOSFET (HV-MOSFET) flows through the channel and drift region. Here, as common point of the HV-MOSFET and the GaN-HEMT, the carrier mobility is determined by the concentration of the channel region. In HiSIM and HiSIM_HV models, the mobility model is described by the scattering mechanism in the channel interface region. Therefore, HiSIM and HiSIM_HV models can be applied to modeling of the DC operation for GaN-HEMTs. However, specific features of GaN-HEMTs cannot be expressed by existing bulk-MOSFET models. Recently, concerning the specific features of GaN-HEMTs, several previous models describe those features based on the GaN-HEMT structure properties [19–25]. However, these existing compact models largely ignore the effects of the heterojunction induced 2DEG. Therefore, in this thesis, the developed compact model HiSIM-GaN explicitly considers the potential distribution from gate electrode to substrate by solving the Poisson equation, including all induced charges in GaN and AlGaN

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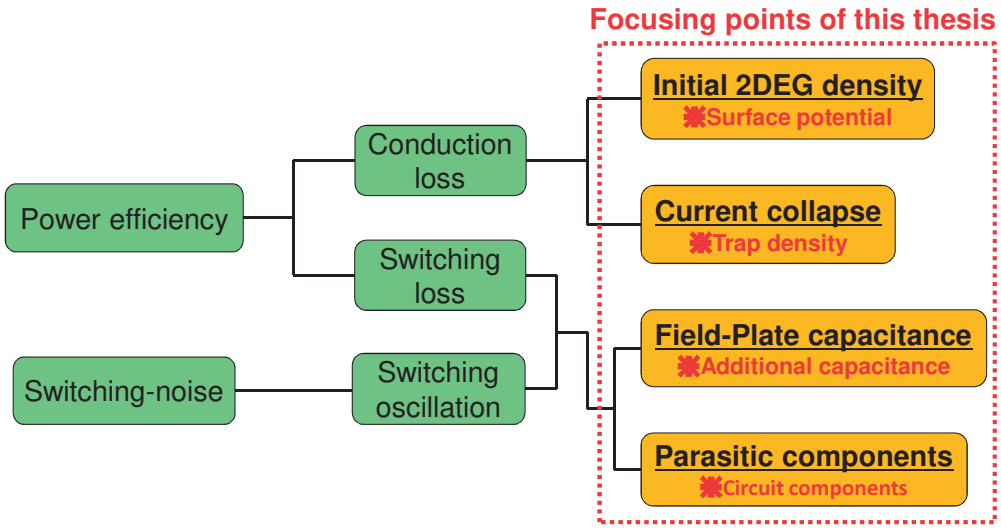

Figure 1.9: Focusing points of this thesis.

The power efficiency and the switching noise are key factors for power electronics as shown in Figure 1.8. In order to accurately predict power efficiency and switching noise for circuit optimization, compact models applied for circuit simulation must be accurate [27]. Figure 1.9 shows focusing points of this thesis. In circuit design, the power efficiency is an important concern for high-power

applications. In addition, the switching waveform is also a considerable concern to analyze the Electro Magnetic Interface (EMI) switching-noise. In general, the power efficiency is determined by the conduction loss and the switching loss. On the other hand, the switching noise is determined by the oscillation during the turn-on and the turn-off switching. Here, conduction loss is strongly affected by initial 2DEG density and current collapse phenomena. Furthermore, switching loss and oscillations are affected by field-plate capacitance and circuit parasitic components. Therefore, objective of the thesis is to investigate contributions of these focusing points upon studied circuit performances using the developed HiSIM-GaN compact model for GaN-HEMT power device.

1.5 Objectives

The objectives of this thesis are:

1. To develop a surface-potential-based GaN-HEMT model "HiSIM-GaN" that includes all possible induced charges, the inherent 2DEG charge and the trapped charge explicitly within Poisson equation.

2. To investigate GaN-HEMT capacitance characteristics with 2D device simulation and develop the new capacitance model for field-plate effects.

3. To reproduce measured DC/AC characteristics of the studied GaN-HEMT device and the switching waveform and the power efficiency of the GaN-based boost converter circuit.

4. To investigate influences of the specific features of GaN-HEMT on boost converter circuit operations using HiSIM-GaN.

1.6 Thesis Organization

This thesis consists of 6 chapters.

Chapter 2 (Physics-based Compact Modeling) reviews the fundamental concepts and modeling of MOSFET for circuit simulation. The analytical formulation of current and charges of the surface-potential-based model HiSIM is presented. Furthermore, specific features of the industry-standard compact model HiSIM_HV for power MOSFETs is presented.

Chapter 3 (Modeling for DC Characteristics) reviews the newly developed compact model HiSIM-GaN. HiSIM-GaN is based on the Poisson equation including trap density and all charges induced within the studied device. This chapter presents the surface-potential-based modeling of the 2DEG charge, which solves the Poisson equation explicitly. It is demonstrated that measured DC characteristics are well reproduced with the developed model.

Chapter 4 (Modeling of Field Plates) presents two new capacitance modeling approaches for field-plates. As the first approach, an empirical capacitance model is developed. As the second approach, a physical capacitance model is proposed. The proposed physical model is based on the surface potential calculated from the Poisson equation and successfully reproduces the simulated capacitance characteristics by TCAD device simulation and also the experimental measurement results.

Chapter 5 (Analysis of Circuit Performance) reviews an analysis of the switching characteristic of a boost converter circuit. In addition, the quantitative contributions of focusing points for GaN-HEMTs, which are trap density effects, field-plate capacitance effects, and parasitic components, upon the switching waveform and the power efficiency have been verified.

Chapter 6 (Conclusions and Future works) summarizes this thesis and suggests further research works which continues after this thesis work.

Appendix A (Normally-off Operation) reviews various structures for the normally-off operation of GaN-HEMTs power devices.

Appendix B (Parameter Extraction Procedure) reviews the parameter extraction procedure of the developed HiSIM-GaN compact model.

Chapter 2

Physics-based Compact Modeling

2.1 Introduction

This chapter describes the importance of circuit simulation, the device physics of observed MOSFET phenomena and the modeling approach of the surface-potential-based MOSFET model HiSIM (Hiroshima-university STARC IGFET Model) [28]. Furthermore, specific features of the industry-standard compact model HiSIM_HV for power MOSFETs are presented [29].

2.2 Importance of Circuit Simulation

Circuit simulation is an important technology behind the progress in integrated circuits. An important feature in today's circuit simulation tools is that it is not necessary to write down the sets of algebraic and integro-differential equations to describe the circuit behavior. The circuit designers have only to describe the circuit configuration and parameter values. The simulation program creates the equations, solves them and gives the results in terms of the circuit-variable responses [30].

To design an integrated circuit using as much performance of semiconductor devices as possible, circuit simulator which can accurately predict circuit operations and performances, has a very important role. For this purpose, device models for the circuit simulation are essential to describe characteristics of nonlinear circuit elements (i.e. various semiconductor devices) accurately. To achieve sufficient

simulation speed for practical commercial use and stable convergence, these models have to describe the device physics with not only physically accurate but also computationally-efficient simple analytical equations. Thus, in general, they are called "compact models". [31, 32]. Compact Models are the bridge between technology, circuit simulations and design. Accurate compact models help guarantee functionality and high yield of products at the design verification stage. Compact Model Coalition (CMC) is a working group in the electronic-design-automation (EDA) industry formed to choose, maintain and promote the use of standard compact models. Table 2.1 shows the standardized compact models on the CMC [33]. As can be seen, various device model have been standardized till now.

Table 2.1: Standardized compact models on the Compact Model Coalition (CMC)

	Bulk MOSFET	**LDMOS/ HVMOS**	**SOI MOSFET**	**Bipolar**	**Varactor & Diode**
UC Berkeley	BSIM4 BSIM6		BSIM-SOI BSIM-CMG BSIM-IMG		
Hiroshima Univ.	HiSIM2	HiSIM_HV	HiSIM-SOI HiSIM-SOTB		
LETI	PSP				
UC San Diego				HICUM L2	
Auburn Univ.				MEXTRAM	
CMC original					MOSVAR CMC_Diode

2.3 Compact Model Concept

The cross section of an n-channel metal-oxide-semiconductor field effect transistor (MOSFET) is shown in Figure 2.1. The device consists of a p-type substrate, in which two n^+ diffusion regions, the drain and the source, are formed. The middle part of the MOSFET is the metal-oxide-semiconductor (MOS) structure. The effective channel length L_{eff} is the distance between the source and the drain, and the channel width W is the lateral extent of the MOSFET. The thickness of the oxide layer covering the channel region is t_{ox}. In MOSFET operation, a channel

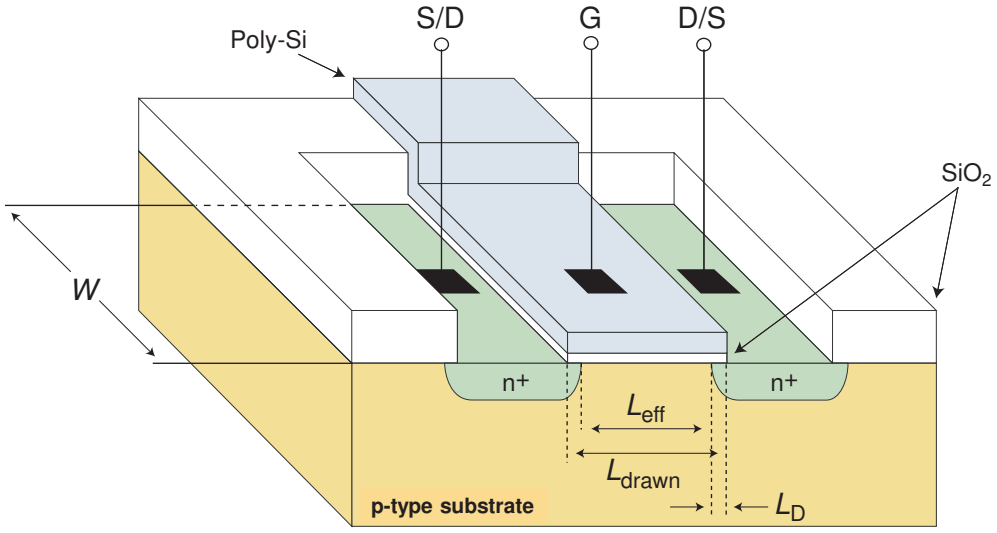

Figure 2.1: Three dimensional illustration of the structure of an n-MOSFET

composed of mobile carriers is formed below the gate oxide. The carriers enter through the source, leave through the drain, and are subject to the applied gate voltage. The carrier flow between the source and drain, called the drain current, is controlled by the electric field generated by the gate voltage. Conventionally, the source voltage is defined as the ground potential. The drain voltage is V_{ds}, the gate voltage is V_{gs} and the substrate voltage is V_{bs}.

In order to describe analytically the MOSFET characteristics, the following basic device equations must be solved simultaneously.

- Poisson equation

$$\nabla^2\phi = -\frac{q}{\epsilon_{\mathrm{Si}}}\left(N_{\mathrm{D}} - N_{\mathrm{A}} + p - n\right) \tag{2.1}$$
$$n = n_{\mathrm{i}} \exp\left[\frac{q(\phi - \phi_{\mathrm{n}})}{kT}\right]$$
$$p = n_{\mathrm{i}} \exp\left[\frac{q(\phi_{\mathrm{p}} - \phi)}{kT}\right]$$

- Current-density equations

$$j_{\mathrm{n}} = -q\mu_n n\frac{\partial\phi}{\partial y} + qD_n\nabla n \tag{2.2}$$
$$j_{\mathrm{p}} = -q\mu_p p\frac{\partial\phi}{\partial y} - qD_p\nabla p$$

- Continuity equations

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla j_{\mathrm{n}} \qquad (2.3)$$
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla j_{\mathrm{p}}$$

where p, n, N_{D}, N_{A}, and n_{i} are hole, electron, donor, acceptor, and intrinsic carrier concentration, respectively. ϕ, ϵ_{Si}, k, T, q, are the potential, the silicon permittivity, the Boltzmann constant, the lattice temperature in Kelvin, and the electron charge, respectively. μ is the carrier mobility and D is the carrier diffusion constant.

2.4 Analytical MOSFET Modeling: The Surface-Potential-Based MOSFET Model HiSIM

The analytical derivation of a closed-form MOSFET current-voltage (I-V) relationship for circuit-simulation requires that several approximations be made to solve the basic device equations. HiSIM is a compact model developed based on the drift-diffusion approximation. The key quantities in this model are the surface potentials at the source and drain nodes which are employed in the gradual channel approximation. The surface potentials are computed iteratively using the Poisson equation as a function of applied voltages. The continuity equation is not solved but is a task given to the circuit simulator. The HiSIM formulation results to a unified expression for all regions of operation.

2.4.1 Drain Current Formulation

The MOSFET drain current I_{ds} as expressed in terms of the quasi-Fermi potential ϕ_{f} is given by

$$I_{\mathrm{ds}} = W q \mu_{\mathrm{eff}} n(y) \frac{d\phi_{\mathrm{f}}}{dy} \qquad (2.4)$$

where $\mu_{\rm eff}$ is the effective carrier mobility, $n(y)$ is the carrier density at position y along the channel. The Fermi potential expressed in surface potential $\phi_{\rm s}$ is

$$\frac{d\phi_{\rm f}}{dy} = -\frac{d\phi_{\rm s}(y)}{dy} + \frac{1}{\beta}\frac{d{\rm ln}n(y)}{dy} \tag{2.5}$$

where $\beta = q/kT$. Substituting Equation 2.5 to 2.4 gives a current equation which consists of two terms

$$I_{\rm ds} = Wq\mu_{\rm eff}n(y)\Big(- \frac{d\phi_{\rm s}(y)}{dy} + \frac{1}{\beta}\frac{d{\rm ln}n(y)}{dy}\Big) \tag{2.6}$$

The first term denotes the drift current which is the carrier flow due to the electric field along the channel. The second term denotes the diffusion current which exists due to a difference in charge concentration gradients. Charges diffuse from regions of high charge concentration to low concentration giving rise to electric current.

Using the gradual channel approximation and assuming uniform channel doping, HiSIM derives a drain current equation as a function of the surface potentials as

$$\begin{aligned} I_{\rm ds} &= \frac{W}{L}\mu_{\rm eff}\frac{I_{\rm DD}}{\beta} \qquad (2.7)\\ I_{\rm DD} &= C_{\rm ox}(\beta(V_{\rm g} - V_{\rm fb} + dV_{\rm th}) + 1)(\phi_{\rm sL} - \phi_{\rm s0}) - \frac{\beta}{2}C_{\rm ox}(\phi_{\rm sL}^2 - \phi_{\rm s0}^2)\\ &\quad - \frac{2}{3}(qN_{\rm sub}L_{\rm D}\sqrt{2})\Big[\{\beta(\phi_{\rm sL} - V_{\rm bs}) - 1\}^{3/2} - \{\beta(\phi_{\rm sL} - V_{\rm bs}) - 1\}^{3/2}\Big]\\ &\quad + (qN_{\rm sub}L_{\rm D}\sqrt{2})\Big[\{\beta(\phi_{\rm sL} - V_{\rm bs}) - 1\}^{1/2} - \{\beta(\phi_{\rm sL} - V_{\rm bs}) - 1\}^{1/2}\Big]\\ L_{\rm D} &= \sqrt{\frac{\epsilon_{\rm Si}kT}{N_{\rm sub}q^2}} \end{aligned}$$

where $\phi_{\rm s0}$, $\phi_{\rm sL}$ are the surface potentials at the source and drain ends and $L_{\rm D}$ is the Debye length, respectively.

2.4.2 Evaluation of Charges

The charge-sheet approximation assumes that the inversion charges are located at the silicon surface like a sheet of charge and that there is no potential drop or band bending across the inversion layer. The total charge density $Q_{\rm s}$ in the channel at

position y is

$$Q_{\mathrm{s}}(y) = Q_{\mathrm{b}}(y) + Q_{\mathrm{i}}(y) \tag{2.8}$$

where $Q_{\mathrm{b}}(y)$ is the bulk charge density and $Q_{\mathrm{i}}(y)$ is the inversion charge density.

$Q_{\mathrm{s}}(y)$ in terms of the surface potential is given by

$$Q_{\mathrm{s}}(y) = C_{\mathrm{ox}}[V_{\mathrm{gs}} - V_{\mathrm{fb}} + dV_{\mathrm{th}} - \phi_{\mathrm{s}}(y)] \tag{2.9}$$

where $C_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$. $\varepsilon_{\mathrm{ox}}$ is the oxide permittivity and V_{fb} is the flat-band voltage. dV_{th} is the change in the threshold voltage V_{th} due to pocket-implantation and short-channel effects.

Under homogeneous substrate impurity distribution, the bulk charge density is

$$Q_{\mathrm{b}}(y) = -qN_{\mathrm{sub}}L_{\mathrm{D}}\sqrt{2}\Big[\exp\{-\beta(\phi_{\mathrm{s}}(y) - V_{\mathrm{bs}})\} + \beta(\phi_{\mathrm{s}}(y) - V_{\mathrm{bs}}) - 1\Big]^{1/2} \tag{2.10}$$

where N_{sub} is the bulk doping concentration and L_{D} is the Debye length.

The inversion charge density is derived as

$$\begin{aligned} Q_{\mathrm{i}}(y) &= qn(y) && (2.11)\\ &= -C_{\mathrm{ox}}[V_{\mathrm{gs}} - V_{\mathrm{fb}} + dV_{\mathrm{th}} - \phi_{\mathrm{s}}(y)] + qN_{\mathrm{sub}}L_{\mathrm{D}}\sqrt{2}[\exp\{-\beta(\phi_{\mathrm{S}}(y) - V_{\mathrm{bs}})\} \\ &\quad + \beta(\phi_{\mathrm{S}}(y) - V_{\mathrm{bs}}) - 1]^{1/2} && (2.12) \end{aligned}$$

Q_{i} is partitioned into two components: charges associated with the source Q_{S} and charges associated with the drain Q_{D} as [34],

$$Q_{\mathrm{D}} = W\int_0^L \frac{y}{L}Q_{\mathrm{i}}(y)dy \tag{2.13}$$

$$Q_{\mathrm{S}} = W\int_0^L \Big(1 - \frac{y}{L}\Big)Q_{\mathrm{i}}(y)dy \tag{2.14}$$

Q_{G} is the charges associated with the gate which is calculated as

$$Q_{\mathrm{G}} = -(Q_{\mathrm{B}} + Q_{\mathrm{I}}) \tag{2.15}$$

where Q_{B} and Q_{I} are the integrated bulk and inversion carrier densities, respectively.

2.4.3 Calculation of Surface Potential

From the Poisson equation, the charge density is calculated as

$$\frac{d^2\phi_{\rm s}(y)}{dy^2} = -\frac{q}{\varepsilon_{\rm Si}}[p_{\rm p0}\{\exp(\beta\phi_{\rm f}-1)\} - n_{\rm p0}\{\exp(\beta\phi_{\rm f}-1)\}] \tag{2.16}$$

where $p_{\rm p0}$ is the density of holes and $n_{\rm p0}$ is the density of electrons in the p-region at thermal equilibrium.

The solution of the above equation leads to electric field $\mathcal{E}$ along the lateral direction

$$\begin{aligned}\mathcal{E}(y) &= \frac{d^2\phi_{\rm s}(y)}{dy^2} &(2.17)\\ &= \pm\frac{\sqrt{2}kT}{qL_{\rm D}}\Big[\{\exp(\beta(\phi_{\rm s}(y)-V_{\rm bs}))+\beta(\phi_{\rm s}(y)-V_{\rm bs})-1\}\\ &+\frac{p_{\rm p0}}{n_{\rm p0}}\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y)))+\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y))\}\Big]^{1/2} &(2.18)\end{aligned}$$

Using Gauss' theorem, $Q_{\rm s}$ becomes

$$\begin{aligned}Q_{\rm s}(y) &= \varepsilon_{\rm Si}\mathcal{E}_{\rm s} &(2.19)\\ &= qN_{\rm sub}L_{\rm D}\Big[\{\exp(-\beta(\phi_{\rm s}-V_{\rm bs}))+\beta(\phi_{\rm s}-V_{\rm bs})-1\}\\ &+\frac{p_{\rm p0}}{n_{\rm p0}}\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y)))+\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y))\}\Big]^{1/2} &(2.20)\end{aligned}$$

Adding Equations. 2.10 and 2.12, and equating to 2.20,

$$\begin{aligned}C_{\rm ox}[V_{\rm gs}-V_{\rm fb}+dV_{\rm th}-\phi_{\rm s}(y)] = qN_{\rm sub}L_{\rm D}\Big[&\{\exp(-\beta(\phi_{\rm s}-V_{\rm bs}))+\beta(\phi_{\rm s}-V_{\rm bs})-1\}\\ &+\frac{p_{\rm p0}}{n_{\rm p0}}\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y)))+\{\exp(\beta(\phi_{\rm s}(y)-\phi_{\rm f}(y))\}\Big]^{1/2}\end{aligned} \tag{2.21}$$

From this equation, the surface potentials $\phi_{\rm s0}$ and $\phi_{\rm sL}$ are calculated by iteration.

2.4.4 Mobility Model

In HiSIM, the carrier mobility μ_0 at low electric field is modeled following the universal mobility which consists of contributions from Coulomb scattering $\mu_{\rm CB}$, phonon scattering $\mu_{\rm PH}$, and surface roughness scattering $\mu_{\rm SR}$

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\rm CB}} + \frac{1}{\mu_{\rm PH}} + \frac{1}{\mu_{\rm SR}} \tag{2.22}$$

The contributions are schematically depicted in Figure 2.2. Coulomb scattering accounts for carrier collisions with charged (ionized) impurity atoms. Phonon scattering accounts for carrier collisions with the silicon lattice or acoustic phonons. Surface roughness occurs at high electric field as carriers are distributed closed to the surface. Each contribution is modeled as

$$\mu_{\mathrm{CB}} = \mathrm{MUECB0} + \mathrm{MUECB1}\frac{Q_{\mathrm{i}}}{q \cdot 10^{11}} \tag{2.23}$$

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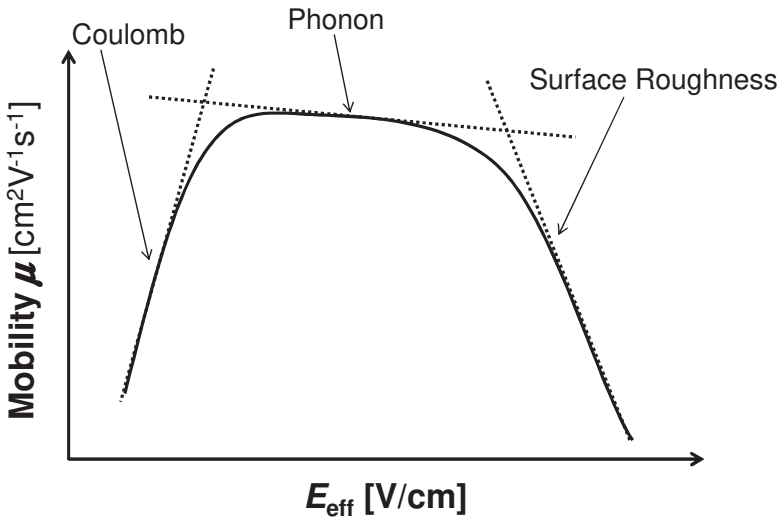

Figure 2.2: Universal mobility curve at low electric field.

case, the high-field electron mobility is modeled as

$$\mu_{\text{eff}} = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 \mathcal{E}_{\text{y}}}{v_{\text{max}}}\right)^{\text{BB}}\right)^{1/\text{BB}}} \tag{2.27}$$

where BB is set to 2 for nMOS and 1 for pMOS. v_{max} is taken as $1{\times}10^7$ cm/s considering bulk carriers. v_{max} is related to carrier velocity overshoot as

$$v_{\text{max}} = \frac{v_{\text{max}}}{1 - \frac{\text{VOVER}}{L_{\text{gate}}^{\text{VOVERP}}}} \tag{2.28}$$

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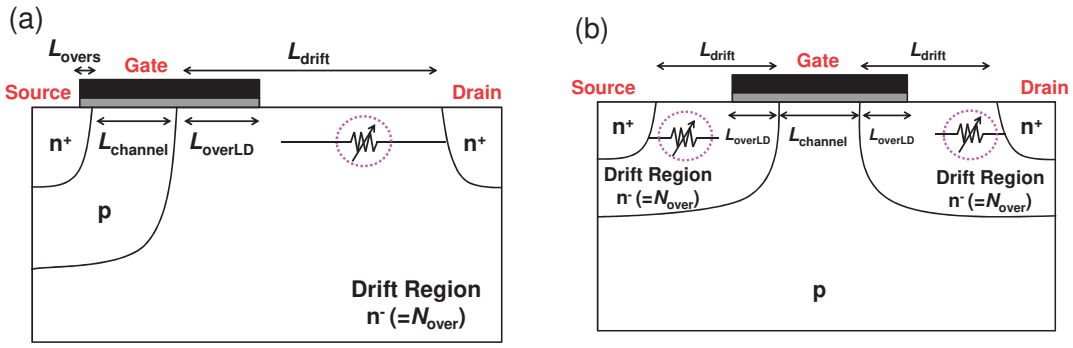

(a) Laterally-Diffused MOS (LDMOS)

(b) High-Voltage MOS (HVMOS)

Figure 2.3: Cross-sectional schematics of (a) the typical Laterally-Diffused MOS (LDMOS) device structure and (b) the typical High Voltage MOS (HVMOS) with the respective structure parameters.

HiSIM_HV has been extended for power MOSFETs by considering the resistance effect explicitly. There are two types of structures commonly used for high voltage applications. One is the asymmetrical laterally diffused structure called LDMOS as shown in Figure 2.3a and the other is originally the symmetrical structure, which is called HVMOS as shown in Figure 2.3b.

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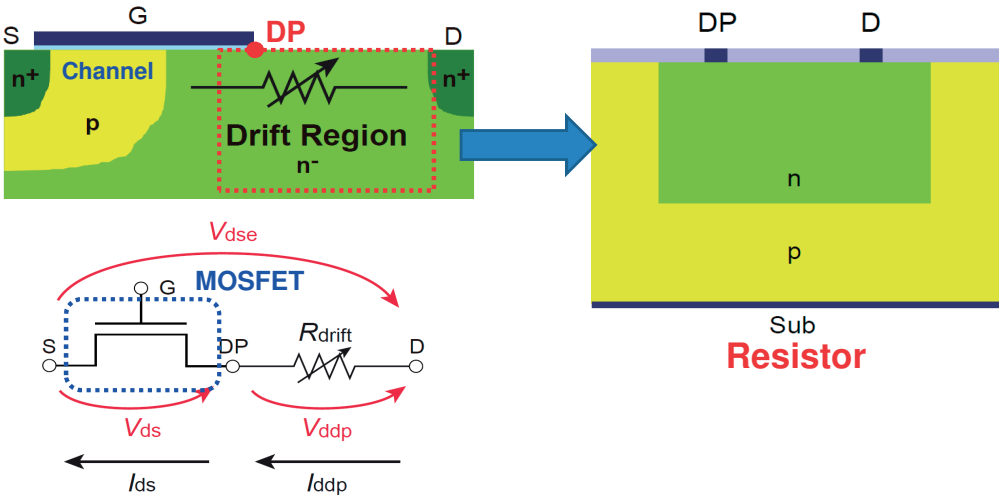

Figure 2.4: Modeling concept of the drift region resistance.

The current flowing the drift region I_{ddp} is modeled as

$$I_{\mathrm{ddp}} = W \cdot X_{\mathrm{ov}} \cdot q \cdot \mu_{\mathrm{drift}} \cdot N_{\mathrm{drift}} \cdot \frac{V_{\mathrm{ddp}}}{L_{\mathrm{drift}}} \tag{2.30}$$

where μ_{drift}, N_{drift}, and L_{drift} are the mobility in the drift region, the doping concentration in the drift region, and the length of the drift region, respectively, as shown in Fig 2.3a. Furthermore, X_{ov} is the effective width of the current flow of the drift region as shown in Figure 2.5. In HiSM_HV, X_{ov} is modeled as

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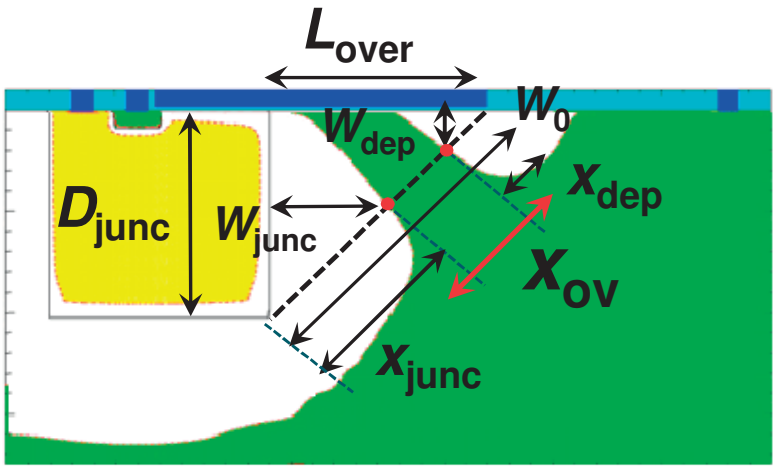

Figure 2.5: Modeling current-flow in the overlap drift region.

Here W_{dep} and W_{junc} are a functions of NOVER. NOVER is the impurity concentration in the drift region affecting both I-V characteristics and C-V characteristics. Therefore, the accurate estimation of NOVER is the key task for representing the power MOSFET characteristics in HiSIM_HV [35].

2.5.2 Capacitance Model

The wide range of the switching operations from a few volts to several hundred volts is realized in the high voltage MOSFETs with a drift region of low-impurity concentration, which provides the required high-voltage-blocking capability. This has been observed to lead to anomalous characteristics for the capacitances of high

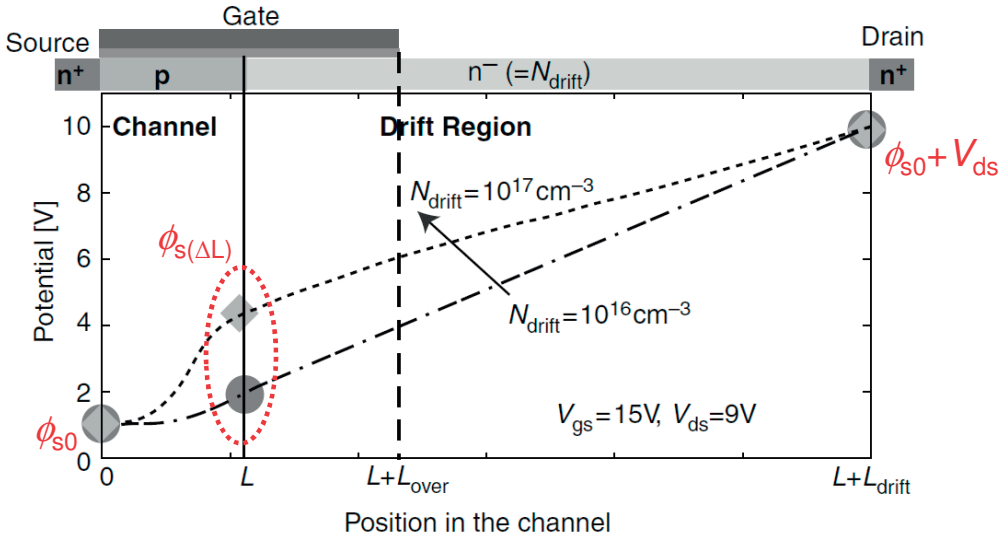

Figure 2.6: Calculated potential distribution along the channel and the drift region of the LDMOS with the HiSIM_HV model (shown with symbols) for two drift region doping concentrations 10^{17}cm^{-3} and 10^{16}cm^{-3}. Lines are 2-dimensional device simulation results.

voltage MOSFET, which become more pronounced with lower impurity concentrations of the drift regions.

HiSIM_HV consistently calculates the potential distribution along the channel and the drift region from the source to the drain contact. The changes in the potential distribution for different impurity concentration in the drift region can therefore be accurately calculated, as demonstrated with the LDMOS structure in Figure 2.6 for drift-region-doing-cases of 10^{17}cm^{-3} and 10^{16}cm^{-3}. In HiSIM_HV, hence, the concentration of the substrate NSUB is much greater than that of the overlap region NOVER, it is approximated that the increase of the potential is occurred mainly into the overlap drift region. Therefore, the surface potential at the edge of the gradual-channel approximation ϕ_{sL} is the nearly equal to the surface potential at the drain edge $\phi_{\text{s}(\Delta\text{L})}$. Consequently, due to this accurate potential-distribution determination, HiSIM_HV is able to capture the scaling properties of the high voltage MOSFET capacitances with respect to drift region doping accurately [36].

Chapter 3

Modeling for DC Characteristics

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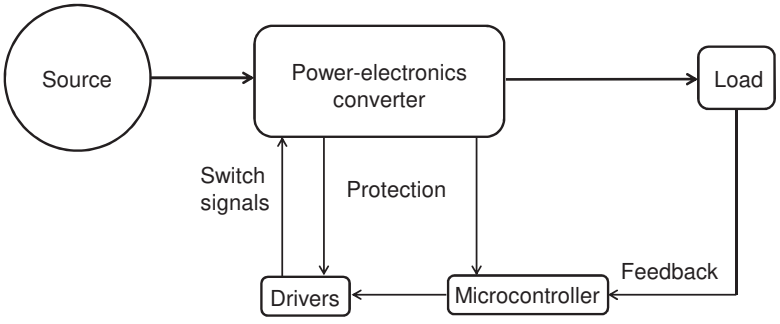

Figure 3.1: Block diagram of a power electronics circuit.

A newly developed compact model HiSIM-GaN (Hiroshima University STARC IGFET Model for GaN high electron mobility transistors (HEMTs)) is developed. The developed model includes two specific features of GaN-HEMT to reproduce the power efficiency accurately. One is the two-dimensional electron gas (2DEG)

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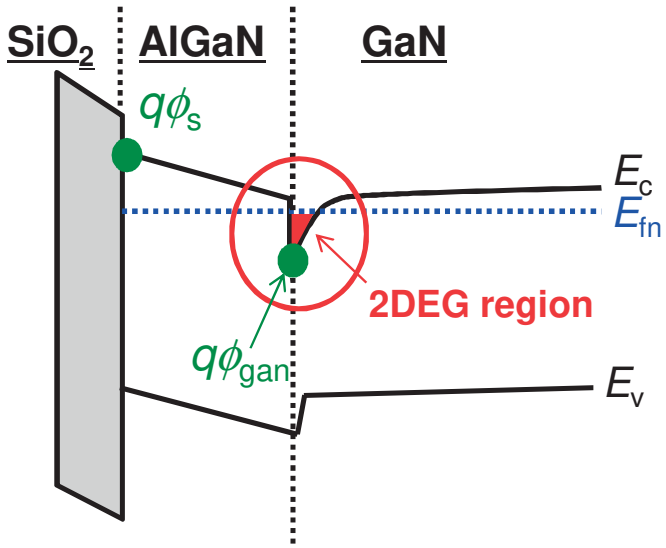

(b) Schematic of energy band diagram for GaN-HEMTs.

Figure 3.2: (a) Cross-sectional schematic and (b) schematic of energy-band diagram of a simplified GaN-HEMT. E_c, E_v, and E_{fn} are the lower conduction-band edge, the upper valence-band edge and the quasi-Fermi level for electrons, respectively.

Figure 3.2a shows a schematic of the simplified GaN-HEMT. Figure 3.2b shows a schematic of the energy band diagram for the GaN-HEMT. As shown in Fig. 3.2b, the 2DEG structure is induced at the AlGaN/GaN heterojunction interface by the spontaneous polarization as well as the piezoelectric polarization due to the strain. The charge density caused by this spontaneous piezoelectric polarization of GaN and AlGaN reaches more than $10^{13}\mathrm{cm}^{-2}$ [37]. The 2DEG composes an inherent channel inversion charge which can be modified by applying the gate voltage. However, the AlGaN layer between the gate insulator and the channel in the GaN layer weakens the gate control and also induces the inversion layer. Another important difference of the GaN-HEMT in comparison to a conventional Si-MOSFET is the non-doped substrate, which causes in principle a steep subthreshold current characteristics. Regrettably, due to the existence of trap sites at the interfaces of different layers, the subthreshold current slope is usually degraded from this expected steep characteristics [38]. Here, important potential values for characterizing the device features are the surface potential value ϕ_{s} at the AlGaN surface and that of ϕ_{gan} at the GaN surface. In order to relax the electric field induced below the gate edge of the 2DEG region at the AlGaN/GaN interface, a structure with dual field plates on the gate and the source electrodes has been developed [37, 39].

As described in the previous chapter, HiSIM is the first complete surface-potential-based compact MOSFET model for circuit simulation based on an explicit solution of the Poisson equation [40–42]. Despite the specific features of GaN-HEMTs, there are several models that describe the device characteristics based on the GaN-HEMT features [19–25]. Existing compact models ignore the feature of the heterojunction inducing 2DEG. Therefore, HiSIM-GaN has been developed by considering the potential distribution explicitly from the gate electrode to the substrate by solving the Poisson equation, where charges induced in GaN and AlGaN layers together with trapped charge at the AlGaN/GaN interface are considered [43].

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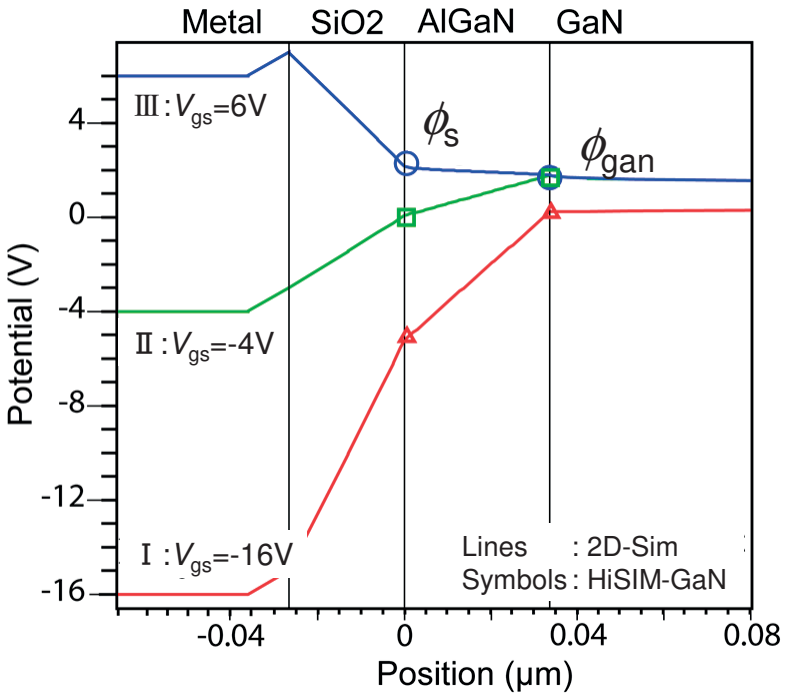


(b) Potential distribution along the vertical direction for different V_{gs} condition.

Figure 3.3: Comparison of modeled potential distributions with 2D device simulation results.

Figures 3.3a and 3.3b compares calculated potential values of HiSIM-GaN to those of 2D device simulation results. The potential at the GaN surface ϕ_{gan} and that at the AlGaN surface ϕ_{s} are depicted as a function of the gate-source voltage V_{gs} for the drain-source voltage V_{ds} of zero. It is seen that the inherent 2DEG is formed around V_{gs}=-15 V, and the inversion charge at the GaN surface further increases as V_{gs} increases. Beyond V_{gs}=0 V, the strong inversion condition is formed even at the AlGaN surface. These three different operation conditions (I, Ⅱ, and Ⅲ) can be clearly distinguished as can be seen in Fig. 3.3a [43]. The conventional modeling approach, which approximates the inversion charge increase as a function of V_{gs}, is valid only for region Ⅱ. However, region I is the most trap sensitive part for the the long-term device degradation. Region Ⅲ cannot be ignored as well for optimizing circuit performances by modifying the device structure and bias conditions. Additionally, GaN HEMT is suffering from non-negligible trap effects, and thus the Poisson equation including all possible charges within the device must be considered. The total charge density within the semiconductor Q_{total} can be written as

$$Q_{\mathrm{total}} = Q_{\mathrm{gan}} + Q_{\mathrm{algan}} + Q_{\mathrm{trap}} \tag{3.1}$$

where Q_{gan} and Q_{algan} are charges induced in GaN and AlGaN, respectively. Q_{trap} is the trap density, which is occurred during application of high voltage. Since both AlGaN and GaN layers are non-doped, the depletion condition does not occur for the studied device. Within the regions I and Ⅱ in Fig. 3.3b, Q_{algan} can be ignored and only Q_{gan} together with Q_{trap} exist. Thus the Poisson equation is reduced to a simpler form as

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\varepsilon_{gan}}(-n_{gan} - n_{algan} - N_t) \tag{3.2}$$

where $\varepsilon_{\mathrm{gan}}$ is the permittivity of GaN, n_{gan} is the induced charge in the GaN layer, n_{algan} is the induced charge in the AlGaN layer, and N_{t} is the trap density at the

GaN surface. Furthermore, n_{gan} in the GaN layer is written as

$$n_{\mathrm{gan}} = n_{\mathrm{i,gan}} \exp(\beta \phi_{\mathrm{gan}}) \tag{3.3}$$

where $n_{\mathrm{i,gan}}$ is the intrinsic carrier density in the GaN layer, β is the inverse of the thermal voltage (q/kT). The trap density distribution is usually approximated by a logarithmic function of the energy difference E_{f}-E_{c}.

$$g_{\mathrm{A}}(E) = g_{\mathrm{c}} \Big\{ \exp\Big(\frac{E_{\mathrm{f}} - E_{\mathrm{c}}}{E_{\mathrm{s}}} \Big) \Big\} \tag{3.4}$$

where g_{c} is the density at E_{f}-E_{c}=0, and the inverse of E_{s} is the slope of the density-of-state. Two independent trap-density distributions are considered as schematically shown in Figure 3.4. One represents the shallow trap density distribution and the other represents the deep trap density distribution [44]. Circuit simulators work only with node potentials. Therefore, the density-of-states must be integrated with respect to the energy and calculated as a function of E_{f}-E_{c} [45].

$$N_{\mathrm{t}} = N_0 \Big\{ \exp\Big(\frac{E_{\mathrm{f}} - E_{\mathrm{c}}}{E_{\mathrm{s}}} \Big) \Big\} \tag{3.5}$$

$$N_0 = g_{\mathrm{c}} E_{\mathrm{s}} \left\{ \frac{(kT/qE_{\mathrm{s}})}{\sin(kT/qE_{\mathrm{s}})} \right\} \tag{3.6}$$

where the elementary charge, the Boltzmann constant, and the temperature in Kelvin are denoted by q, k, and T, respectively. The conduction band edge and the fermi level are denoted by E_{c} and E_{f}, respectively, and E_{s} and g_{c} are model parameters describing the trap state density. These parameters are extracted with measured I-V characteristics.

The total charge density within the GaN layer Q_{gan} is written as a function of the surface potential ϕ_{gan} as

$$Q_{\mathrm{gan}} = \sqrt{\frac{2q\varepsilon_{\mathrm{gan}} n_{\mathrm{i,gan}}}{\beta}} \{ \exp(\beta \phi_{\mathrm{gan}}) - 1 \}^{1/2} \tag{3.7}$$

It is assumed that the carrier trapping occurs at the defects in the AlGaN/GaN layers and the passivation interface with a relatively long time constant, and that the trapped carriers are distributed at the interface with the thickness of the inversion layer. The total trap charge density Q_{trap} is thus written as

$$Q_{\mathrm{trap}} = qN_{\mathrm{t}} \tag{3.8}$$

For calculating the potential distribution under applied bias conditions, Equation (3.2) is solved together with the Gauss law. Here it is assumed that AlGaN layer is highly resistive and causes a linearly decreasing potential drop. With this definition, the surface potential ϕ_{s} is calculated. The boundary condition at the gate oxide and the AlGaN surface is derived under the approximation that the potential drop, induced by creating the inversion charge, is negligible in comparison to that occurring within the non-doped AlGaN layer.

$$\frac{V_{\mathrm{gs}} - V_{\mathrm{fb}} - \phi_{\mathrm{s}}}{T_{\mathrm{ox}}}\varepsilon_{\mathrm{ox}} = \frac{\phi_{\mathrm{s}} - \phi_{\mathrm{gan}}}{T_{\mathrm{algan}}}\varepsilon_{\mathrm{algan}} \tag{3.9}$$

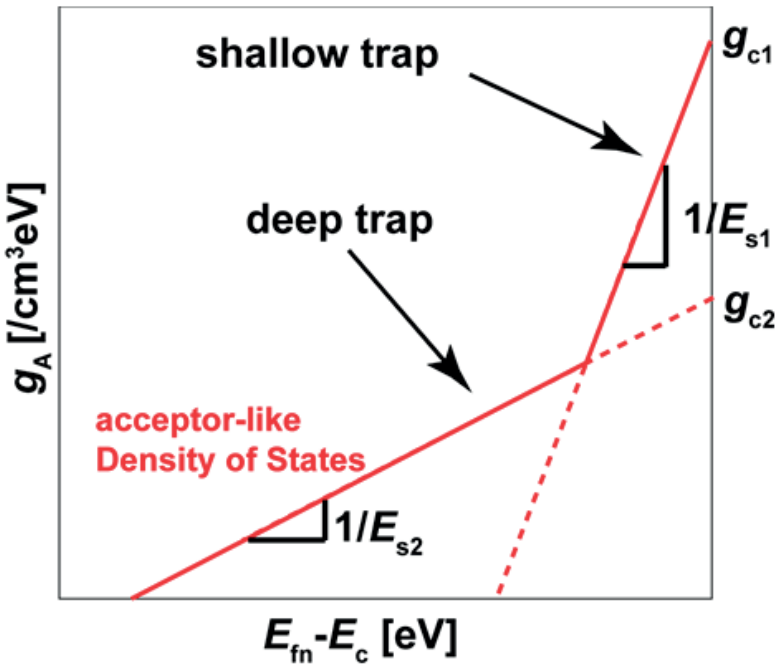


Figure 3.4: Schematic of the trap density-of-states distribution, where E_{fn} is the quasi-Fermi level for electrons. Two independent density-of-states are depicted.

where V_{fb} is the flat band voltage, T_{ox} is the gate oxide thickness, T_{algan} is the AlGaN layer thickness, and $\varepsilon_{\mathrm{algan}}$ is the permittivity of the AlGaN layer, respectively.

In the region Ⅲ, additional inversion charge Q_{algan} induced at the AlGaN surface must be considered, which is a function of the surface potential ϕ_{s} and ϕ_{gan}

$$Q_{\mathrm{algan}} = \sqrt{\frac{2q\varepsilon_{\mathrm{algan}} n_{\mathrm{i,algan}}}{\beta}} \{\exp(\beta\phi_{\mathrm{s}}) - \exp(\beta\phi_{\mathrm{gan}})\}^{1/2} \tag{3.10}$$

where $n_{\mathrm{i,algan}}$ is the intrinsic carrier density in the AlGaN layer. The calculation results are depicted together with the 2D simulation results in the Figs. 3.3a and 3.3b. In the Poisson equation, carrier traps are also induced to simulate the corresponding effects in a self-consistent way, which result not only in a threshold voltage shift but also in a sub-threshold slope degradation as well as a mobility degradation. All these effects are a function of the carrier density.

In addition to the potential distribution differences, there are two further distinguished differences between the GaN-HEMT and a conventional MOSFET under normal operating conditions. One is that the 2DEG layer prevents the pinch-off condition and preserves the inversion layer at the GaN surface. The other difference is that the Schottky contacts are forcing the consumption of all potential biases applied between source and drain contacts within the semiconductor. These differences of the GaN-HEMT can be captured automatically in the compact model by solving the Poisson equation with the quasi-fermi level under the gradual channel approximation.

3.3 Model Evaluation and Discussion

3.3.1 Drain Current Modeling and Extraction of the Trap Density

Figure 3.5 shows a schematic of the studied GaN-HEMT structure. The device has an MIS structure with a SiN layer between the AlGaN and the gate electronode

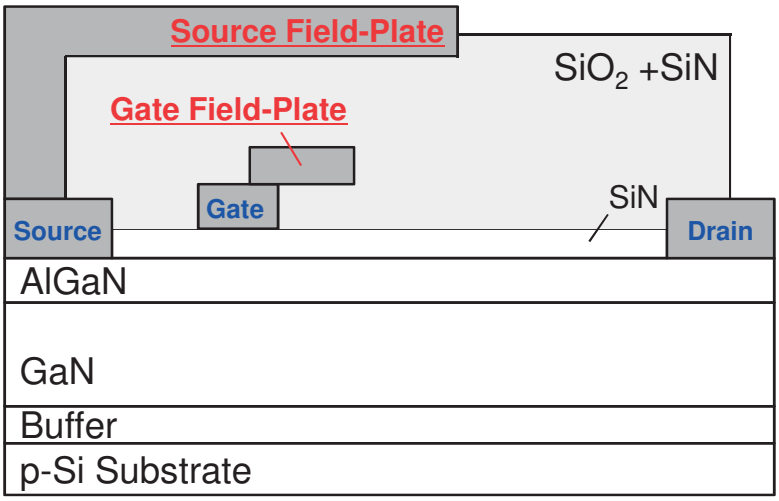


Figure 3.5: Cross-sectional schematic of the studied GaN-HEMT structure with dual-FP technique at the gate and the source electrodes.

as the insulator. In order to relax the electric field induced below the gate edge of the 2DEG region at the AlGaN/GaN interface, a structure with dual field plates on the gate and the source elactronodes has been developed.

The developed GaN-HEMT compact model equations are added to the industry-standard model HiSIM_HV for power MOSFETs to additionally solve the resistance effect consistently by introduction of internal nodes [17, 18]. HiSIM_HV solves the potential distribution along the surface by solving the Poisson equation iteratively. The HiSIM compact model determines the complete potential distribution along the device including the surface potential at the source side ϕ_{s0}, the potential at the pinch-off point ϕ_{sl}, and additionally at the internal node within the resistive drift region [42]. In the GaN-HEMT compact model, the gradual-channel approximation together with approximations of an idealized gate structure are used. Then the equation for the drain current I_{ds} can be written as shown in Equation (3.11) to Equation (3.14).

$$I_{\rm ds} = \frac{W_{\rm gate}}{L_{\rm gate}} \mu \frac{I_{\rm dd}}{\beta} \tag{3.11}$$

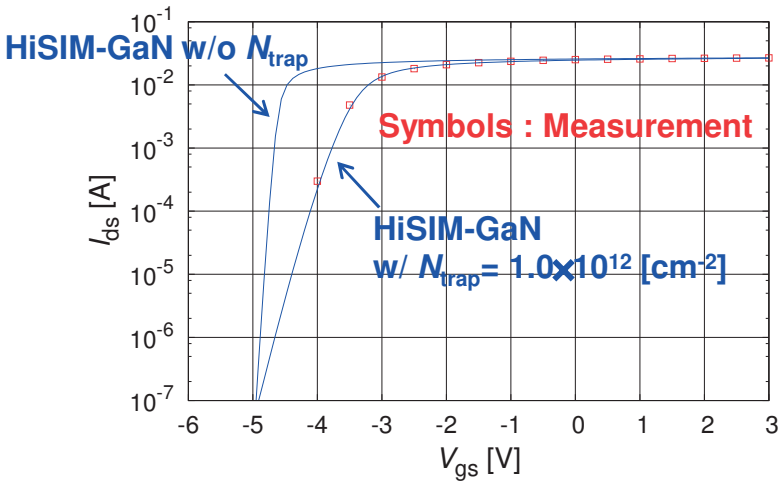
$$I_{\rm dd} = (Q_{\rm l} - Q_0) - \frac{\beta}{2}(Q_{\rm l} + Q_0)(\phi_{\rm ganl} - \phi_{\rm gan}) \tag{3.12}$$

$$Q_0 = \sqrt{\frac{2q\varepsilon_{\rm gan} n_{\rm i,gan}}{\beta}} \{\exp(\beta\phi_{\rm gan}) - 1\}^{1/2} \tag{3.13}$$

$$Q_{\rm l} = \sqrt{\frac{2q\varepsilon_{\rm gan} n_{\rm i,gan}}{\beta}} \{\exp(\beta(\phi_{\rm ganl} - V_{\rm ds})) - 1\}^{1/2} \tag{3.14}$$

where $W_{\rm gate}$ and $L_{\rm gate}$ are the gate width and the gate length, Q_0 and $Q_{\rm l}$ are the charge densities at the source side and the drain side, respectively. The carrier mobility μ considers both high and low electric field.

Furthermore, the trap density is extracted to reproduce the measured $I_{\rm ds}$-$V_{\rm gs}$ characteristics. In general, device degradation is caused by carrier-trapping effects. Especially, the threshold voltage and the subthreshold slope is determined only by the device parameter values such as the impurity concentration. In developed compact model HiSIM-GaN, the trapping event is assumed to be a long-term event. Figures 3.6a and 3.6b shows the comparison of measured and simulated $I_{\rm ds}$-$V_{\rm gs}$ characteristics with and without extracted trap density. Symbols are measurements, dashed line is HiSIM-GaN simulation results without the trap density, and solid line is HiSIM-GaN simulation results with extracted trap density. It is shown that the trap density is clearly influenced on the $I_{\rm ds}$-$V_{\rm gs}$ characteristic. The trap density is extracted to reproduce the measured $I_{\rm ds}$-$V_{\rm gs}$ characteristics. The subthreshold slope is determined only by the device parameter values such as the impurity concentration. The trap density of the HiSIM-GaN model is extracted as static trap density mostly from the subthreshold slope of measured $I_{\rm ds}$-$V_{\rm gs}$ characteristics, because trap charge $N_{\rm t}$ also degrades the subthreshold slope [38]. The extracted trap density of $1.0\times10^{12}{\rm cm}^{-2}$ is about ten times larger than that for silicon power devices [46, 47].

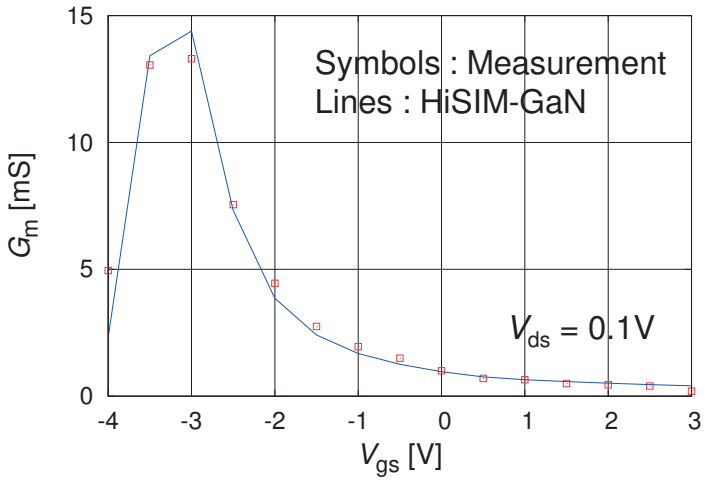


(b) Logarithmic scale

Figure 3.6: Comparison of measured and simulated I_{ds}-V_{gs} characteristics with fixed V_{ds} of 0.1V with and without extracted trap density.

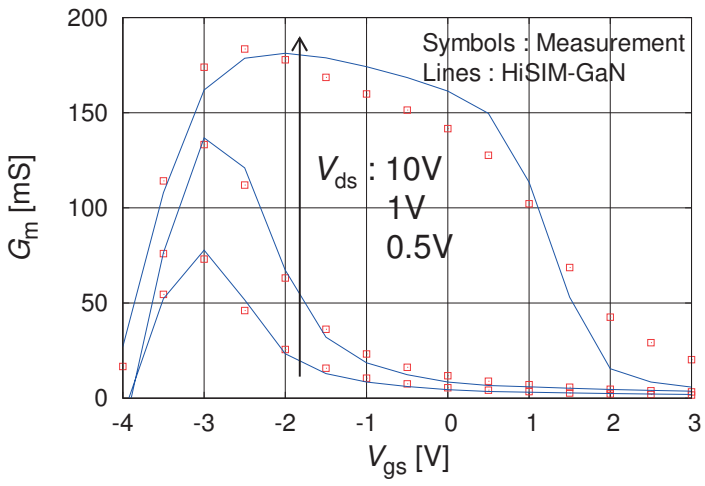
3.3.2 Parameter Extraction Results

In order to investigate GaN-HEMT-based circuit simulation, the model parameter extraction for HiSIM-GaN was performed. Figures 3.7, 3.8, and 3.9 show parameter extraction results for reproducing the I-V characteristics at the room temperature. Symbols are measurements, and solid line is HiSIM-GaN simulation results. As shown in Figs. 3.7 and 3.8, the studied GaN-HEMT device is the normally-on device. In general, it is essential to be a normally-off device in the case of using as the switching device for power electronics. In resent years, high



(c) Transconductance

Figure 3.7: I_{ds}-V_{gs} and G_m-V_{gs} characteristics at the room temperature with fixed V_{ds} of 0.1V. Symbols are measurements and lines are simulation results.



(c) Transconductance

Figure 3.8: I_{ds}-V_{gs} and G_m-V_{gs} characteristics at the room temperature with V_{ds}=0.5, 1, and 10V. Symbols are measurements and lines are simulation results.

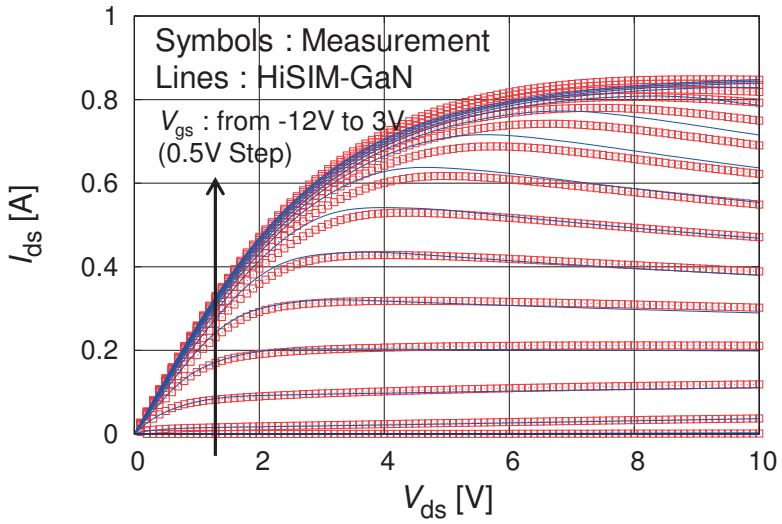


Figure 3.9: I_{ds}-V_{ds} characteristics at the room temperature from V_{gs}=-12 to 3 V. Symbols are measurements and lines are simulation results.

voltage normally-off GaN-HEMT devices are widely used in series connected with low voltage Si-MOSFETs for normally-off Cascode structure [59]. In the G_m-V_{gs} characteristic with V_{ds}=10V shown in Figure 3.8c, different slope are observed above threshold voltage. Self-heating effect can accurately predict the first slope and the second slope is mainly governed by the velocity saturation model. It is seen that HiSIM-GaN results are in good agreement with measurements.

3.4 Summary

This chapter presented the modeling for DC characteristics. Since specific features of GaN-HEMTs cannot be expressed by existing bulk-MOSFET models, in this thesis, a newly developed compact model HiSIM-GaN, based on the Poisson equation including trap density and all charges induced within the studied device, have been presented. All other possible phenomena in case of high-voltage applications, such as the resistance and the self-heating effect have been modeled in the same way as in HiSIM_HV. For characterizing GaN-HEMT's features, surface potential values at AlGaN and GaN surfaces are important. HiSIM-GaN model was successful to the reproduction of the potential distribution calculated by 2D

device simulation. It have been demonstrated the validity of the developed model by performing the parameter extraction of the measured GaN-HEMT's characteristics. It was demonstrated that measured DC characteristics of this GaN-HEMT technology are well reproduced.

Furthermore, in HiSIM-GaN trapping model, shallow and deep trap densities are approximated by exponential functions of energy. Influence of trapped carriers is consistently considered not only on the potential distribution but also on the other characteristics such as the mobility, which is determined by charge densities calculated from the potential distribution. In developed HiSIM-GaN model, trap density N_{trap} is extracted from the measured sub-threshold slope. Where the trapping event is assumed to be a long-term event in HiSIM-GaN. Trap density extracted from measured I_{ds}-V_{gs} characteristics is considered as static trap density. This static trap density means that time constant for trapping cannot be considered yet in the current HiSIM-GaN model.

Chapter 4

Modeling of Field Plates

4.1 Introduction

Power semiconductor devices are the key components of various inverter and converter circuits for high power applications. These high power devices determine the circuit-switching characteristics in applications such as voltage conversion or motor control. In circuit design, a compact model that accurately describes the device characteristics is a prerequisite in order to predict the power efficiency accurately [35,43,48]. Such high power efficiency of circuits is an important requirement for saving energy. It is well known that capacitances play important roles for the circuit switching performances, because charging/discharging according to the bias change depends on the capacitance characteristics of the devices. Therefore, in order to predict power efficiency accurately in circuit simulation, accurate modeling of capacitance characteristics is a key task. In this chapter, therefore, the new capacitance model of the field-plate (FP) effect is presented.

4.2 Analysis of Field-Plate Capacitance using 2D Device Simulation

To analyze in detail field-plate effects physically, two-dimensional simulations are performed using Sentaurus-TCAD device simulator [49]. Device simulators solve numerically the basic device equations given in Eqs. (2.1)-(2.3) is inherently solved. Figure 4.1 shows the 2D device simulation result for the electron density in a cross

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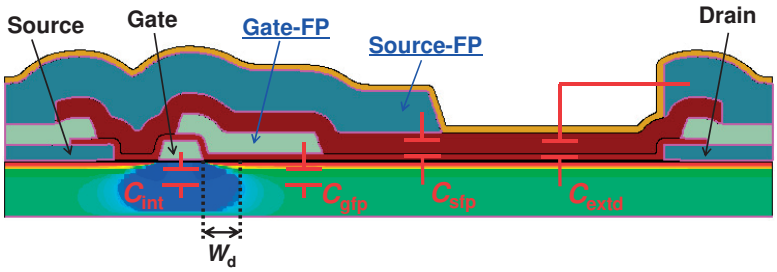

Figure 4.1: Sentaurus-TCAD simulation result for the electron density in a cross section of the fabricated GaN-HEMT with fixed gate-source voltage (V_{gs}= -20V) and drain-source voltage (V_{ds}= 0V). C_{int}, C_{gfp}, C_{sfp}, C_{extd} and W_d are the intrinsic gate capacitance, gate field-plate capacitance, source field-plate capacitance, extrinsic drain capacitance and depletion layer width, respectively.

C_{iss} ($= C_{gs} + C_{gd}$), C_{oss} ($= C_{ds} + C_{gd}$), and C_{rss} ($= C_{gd}$) are input capacitance, output capacitance and reverse transfer capacitance, respectively. These capacitances determine the applicable frequency and switching speed when the power device is utilized for switching operations. It is important for understanding the figure of merits as the switching device for input and output electrical signal. Therefore, in this thesis, capacitance analysis is performed using $C_{iss}/C_{oss}/C_{rss}$ capacitances. Figure 4.2 shows device simulation results for C_{iss} as a function of V_{gs} at fixed V_{ds} of 0V, with and without gate-FP and source-FP effects. Please notice that the FPs are responsible for a shoulder in C_{iss}, and that the gate-FP contribution dominates the C_{iss}-V_{gs} characteristic. This is because the insulator thickness under the gate-FP is thin compared with that under the source-FP.

Figure 4.3 shows the C_{rss} as a function of V_{ds} with fixed V_{gs} of -15V with the

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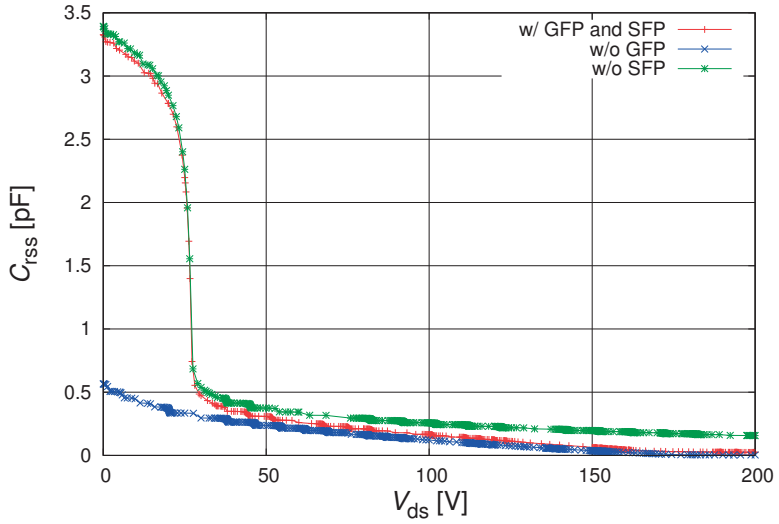


Figure 4.3: $C_{\rm rss}$-$V_{\rm ds}$ characteristic at the room temperature with fixed $V_{\rm gs}$ of -15V with the gate-FP and the source-FP simulated by TCAD.

gate and the source field-plate contribution simulated by TCAD. It is seen that the $C_{\rm rss}$ is mostly due to the FP and it reduces abruptly without this contribution. As well as for $C_{\rm iss}$ in Fig. 4.2, the gate-FP effect is also dominant for the $C_{\rm rss}$-$V_{\rm ds}$ characteristic. As $V_{\rm ds}$ increases, the depletion layer extends further from gate edge towards drain side. When the depletion extension reaches the edge of gate-FP and source-FP, $C_{\rm gfp}$ and $C_{\rm sfp}$ are reduced. This results in an abrupt capacitance reduction of $C_{\rm iss}$ and $C_{\rm rss}$.

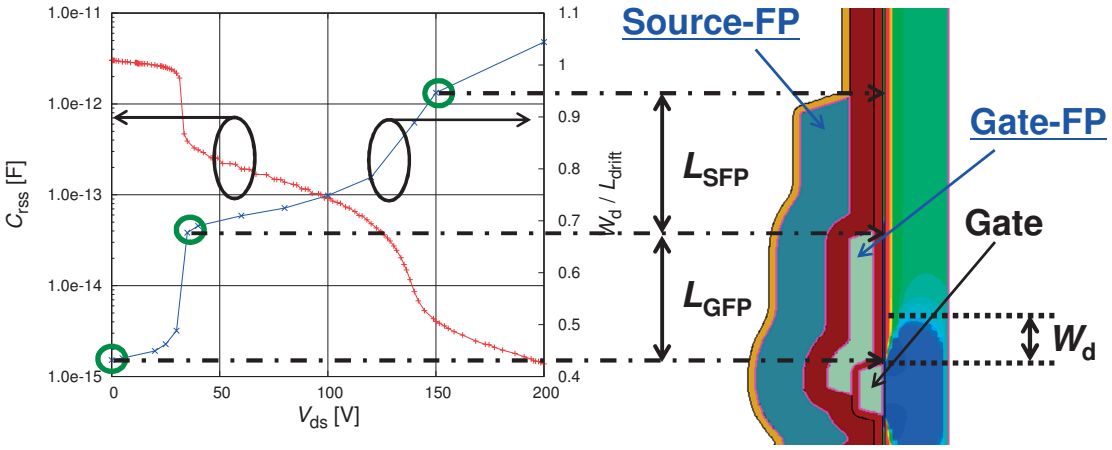


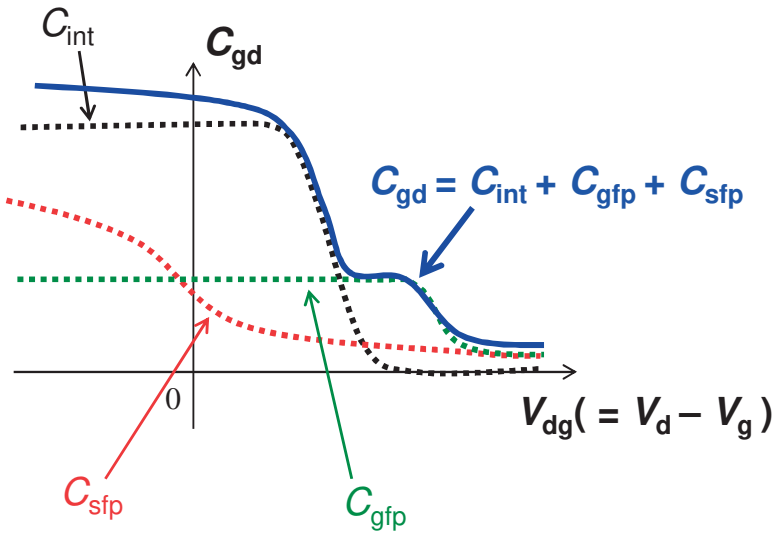
Figure 4.4: The relationship for the reverse transfer capacitance C_{rss} and the depletion layer width W_{d} as a function of V_{ds}. L_{GFP} and L_{SFP} are the gate-FP length and the source-FP length, respectively.

Figure 4.4 shows the C_{rss} characteristic at fixed V_{gs} of -15V and the depletion width (W_{d}) extension from the gate edge as a function of V_{ds}, as simulated by TCAD, where C_{rss} is plotted in logarithmic scale. The W_{d} value is extracted from TCAD device simulation results of the electron density and is $1.0\times10^{10}\mathrm{cm}^{-3}$, which is selected to achieve stable W_{d} extraction for any V_{ds} values. It is seen that the depletion width characteristic as a function of V_{ds} coincides with that of C_{rss}. Therefore, it is concluded that there is a strong correlation between the extension of the depletion width and the capacitance characteristics for the studied device. Consequently, for the accurate modeling of FP capacitances, it is important to accurately describe this extension of the depletion width in the compact model formulation.

4.3 Modeling of Field-Plate Effects

4.3.1 Empirical Modeling of Field-Plate Capacitances

Figure 4.5a shows a schematic of the studied GaN-HEMT with dual-FP technique at the gate and the source electrodes. The device uses a Metal-Insulator-Semiconductor (MIS) concept where a SiN layer is located between the AlGaN layer and the gate metal. In order to relax the electric field induced below the



(b) Capacitance modeling concept with gate and source FP effects.

Figure 4.5: Capacitance modeling concept with gate and source FP effects. C_{int}, C_{gfp} and C_{sfp} are the intrinsic gate capacitance, the gate FP capacitance and the source FP capacitance, respectively.

gate edge of the 2DEG region at the AlGaN/GaN interface, a structure with dual-FPs on the gate and the source electrodes has been developed [12, 13, 50]. Though the FP relaxes the electric-field peak induced at the electrode edge, it acts as an additional origin of the charge accumulation, namely creation of additional capacitance. It is known that capacitances usually play important roles concerning the switching characteristic. Therefore to predict the switching characteristic accurately for accurate prediction of circuit performances, it is necessary to predict capacitance characteristics accurately a well [35]. In a normally-on device, the FP effect is dominant under the depletion condition, where intrinsic capacitances remain small. Figure 4.5b depicts different contributions to C_{gd} [35]. It is seen that the total capacitance of GaN-HEMTs with dual-FPs is formed by three major components: the intrinsic gate capacitance C_{int}, the gate-FP induced capacitance

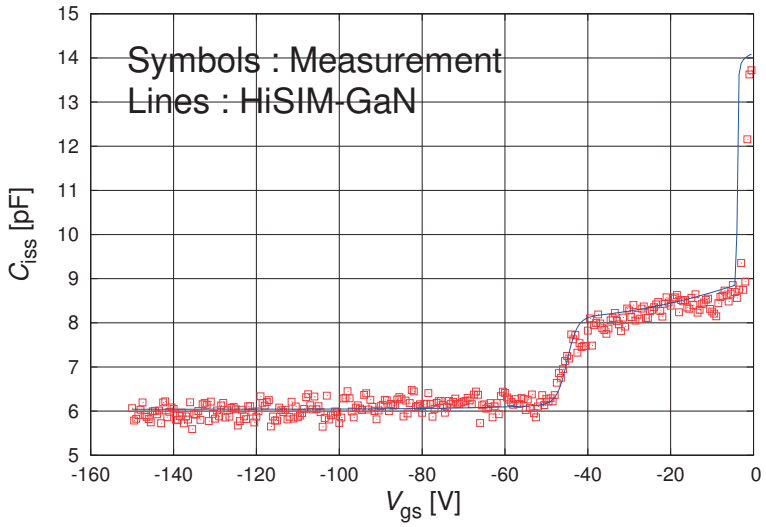


Figure 4.6: Comparison of measured and simulated C_{iss}-V_{gs} characteristic at room temperature with fixed V_{ds} of 0V.

C_{gfp} and the source-FP induced capacitance C_{sfp}. The total capacitances formed by these three components by using three different non-linear *tanh* functions as follows.

$$C_{\mathrm{int}} = C_1 \cdot tanh(C_2 \cdot V_{\mathrm{dg}} - C_3) + C_4 \tag{4.1}$$

$$C_{\mathrm{gfp}} = C_5 \cdot tanh(-C_6 \cdot V_{\mathrm{dg}}) + C_7 \tag{4.2}$$

$$C_{\mathrm{sfp}} = C_8 \cdot tanh(C_9(V_{\mathrm{ds}} - C_{10})) + C_{11} \tag{4.3}$$

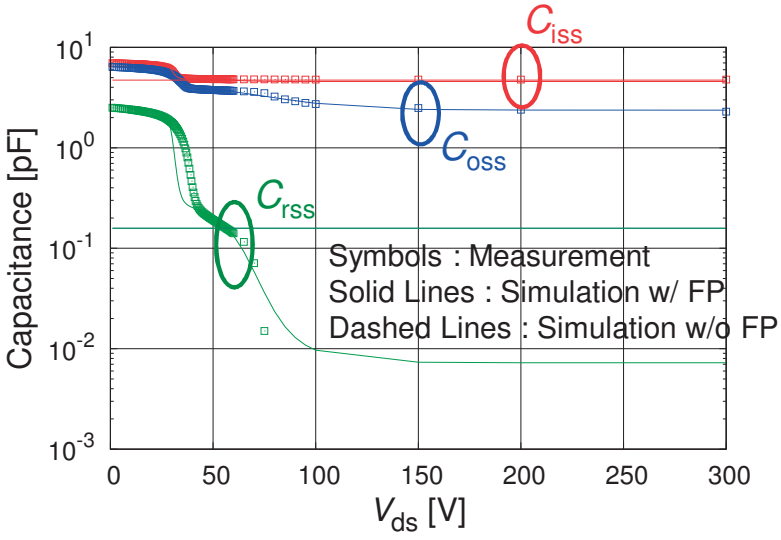
where C_1-C_{11} are model parameters for measured capacitance characteristics. For reproducing the V_{dg} (=V_{ds}-V_{gs}) dependence of the capacitance C_{gd}, influence of the depletion width extended from the drain contact must be considered. This depletion width extension diminishes the capacitor length, namely, the FP length. This intrinsic part can be calculated simply from the potential values ϕ_{s} and ϕ_{gan} [43]. All other possible phenomena in the case of high-voltage applications, such as the resistance and the self-heating effect have been modeled in the same way as in HiSIM_HV, an industry-standard compact model for power MOSFETs [17,18,29]. Figure 4.6 shows the C_{iss}-V_{gs} at V_{ds}=0 V characteristic, where the abrupt reduction at the subthreshold region is caused by the gate depletion. The depletion width

extension from the gate reaches the gate-FP edge by decreasing V_{gs} (V_{gs} < -50 V), and C_{iss} is further reduced.

Figure 4.7a shows the $C_{iss}/C_{oss}/C_{rss}$-V_{ds} characteristic at room temperature with fixed V_{gs}=-15 V. Symbols show the measurement data, dashed lines show the HiSIM-GaN simulation result without both the gate and the source FP effects, and solid lines show HiSIM-GaN simulation result with both the gate and the source FP effects. For the same reason, the reverse transfer capacitance C_{rss} shown in Figure 4.7a decreases beyond a certain V_{ds} value. Namely, the depletion width under the gate is extended to the gate FP edge by increasing V_{ds}. Figure 4.7b shows the $C_{iss}/C_{oss}/C_{rss}$-V_{ds} characteristic with logarithmic scale. The first abrupt reduction of C_{rss} observed at V_{ds}=50 V is caused by the extension of the depletion width to the gate-FP edge. By increasing V_{ds} further, the depletion width under the gate is extended to the source-FP edge, and the 2nd abrupt reduction of the C_{rss} is caused at V_{ds}=80 V. As a result, empirical FP capacitances model of HiSIM-GaN reproduces measured C-V characteristics by considering field-plate effects. Furthermore, as shown in Figs 4.7a and 4.7b, this model can represents that capacitance of the low V_{ds} are increased by considering field-plate effects.

4.3.2 Physics-based Modeling of Field-Plate Capacitances

Figure 4.8 schematically shows the depletion extension into the 2DEG region by applying V_{ds} on drain contact [51]. The potential distribution along the device surface is described by surface potential values, ϕ_{s0}, ϕ_{sL}, V_{ddp}, and V_{ds}+ϕ_{s0}. These values are solution of HiSIM-GaN solved iteratively. Due to the 2DEG charge distributed at the surface, the resistance effect along the drift region is negligible, and thus the potential difference between V_{ddp} and V_{ds}+ϕ_{s0} is negligible. Following the conventional modeling approach, it is derived an equation for the relationship between the electric-field in the depletion layer (E_y) and the total charge induced in the extended depletion layer (Q_{2DEG}) by applying the Gauss law [52].



(b) Logarithmic scale

Figure 4.7: Comparison of the modeled $C_{\mathrm{iss}}/C_{\mathrm{oss}}/C_{\mathrm{rss}}$-$V_{\mathrm{ds}}$ with measurements at fixed V_{gs} of -15 V and room temperature. Symbols are measurements and lines are simulation results.

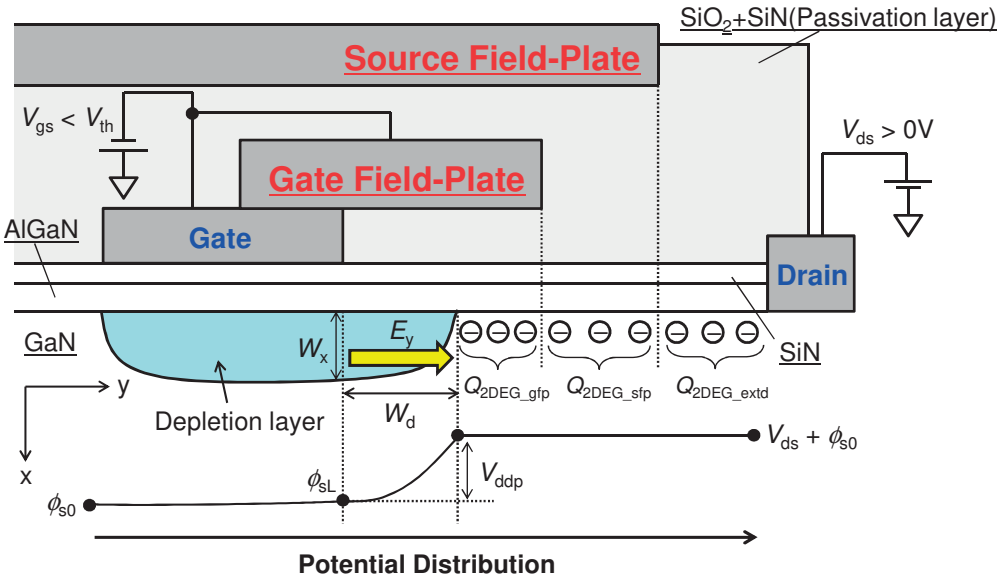


Figure 4.8: Schematic diagram of the depletion extension and the surface potential distribution in the 2DEG channel region.

$$W_{\mathrm{x}} \cdot \frac{dE_{\mathrm{y}}}{dy} = \frac{Q_{\mathrm{2DEG}}}{\epsilon_{\mathrm{gan}}} \tag{4.4}$$

where W_{x} and ϵ_{gan} are the thickness of the depletion region and the permittivity of GaN, where a linearly increasing potential distribution is approximated along the y direction (see Fig. 4.8). Eq. (4.4) describes the field strength, which is required to induce depletion condition to compensate Q_{2DEG}. The depletion width W_{x} is a function of the surface potential with negligible V_{ds} contribution [53].

$$W_{\mathrm{x}} = \left(\frac{2 \cdot \epsilon_{\mathrm{gan}} \cdot \phi_{\mathrm{s}}}{q \cdot N_{\mathrm{gan}}} \right)^{\frac{1}{2}} \tag{4.5}$$

Namely, ϕ_{s} is approximated to ϕ_{s0}. Here q and N_{gan} are the electron charge and the impurity concentration in the GaN layer. Since, the GaN layer is non-doped, N_{gan} is equal to the intrinsic carrier density of GaN, which is of the order of $10^{-10}\mathrm{cm}^{-3}$ This means that the depletion layer thickness fulfills nearly always whole the GaN layer. Therefore, it is assumed that W_{x} is equal to the thickness of the GaN layer thickness T_{GAN} under the strong inversion condition.

The assumption of a quadratic surface potential increase in the depletion layer leads to following description of the electric-field E_{y}.

$$E_{\mathrm{y}} = \frac{2 \cdot V_{\mathrm{ds}}}{W_{\mathrm{d}}^2} \cdot y \tag{4.6}$$

The depletion width (W_{d}) extends from the gate edge into the drain-contact direction and is calculated with Eq. (4.4) and Eq. (4.6)

$$W_{\mathrm{d}} = \left(\frac{W_{\mathrm{x}} \cdot 2 \cdot V_{\mathrm{ds}} \cdot \epsilon_{\mathrm{gan}}}{Q_{\mathrm{2DEG}}} \right)^{\frac{1}{2}} \tag{4.7}$$

The AlGaN layer, the insulator layer, and the passivation layer capacitances are connected in series. Thus, the gate-FP, the source-FP and the extrinsic drain capacitances per unit area under unbiased conditions are calculated by the following equations.

$$C_{\mathrm{gfp0}} = \frac{1}{\frac{T_{\mathrm{ALGAN}}}{\epsilon_0 \epsilon_{\mathrm{ALGAN}}} + \frac{T_{\mathrm{SIN}}}{\epsilon_0 \epsilon_{\mathrm{SIN}}} + \frac{T_{\mathrm{GFP}}}{\epsilon_0 \epsilon_{\mathrm{PAS}}}} \tag{4.8}$$

$$C_{\mathrm{sfp0}} = \frac{1}{\frac{T_{\mathrm{ALGAN}}}{\epsilon_0 \epsilon_{\mathrm{ALGAN}}} + \frac{T_{\mathrm{SIN}}}{\epsilon_0 \epsilon_{\mathrm{SIN}}} + \frac{T_{\mathrm{SFP}}}{\epsilon_0 \epsilon_{\mathrm{PAS}}}} \tag{4.9}$$

$$C_{\mathrm{extd0}} = \frac{1}{\frac{T_{\mathrm{ALGAN}}}{\epsilon_0 \epsilon_{\mathrm{ALGAN}}} + \frac{T_{\mathrm{SIN}}}{\epsilon_0 \epsilon_{\mathrm{SIN}}} + \frac{T_{\mathrm{EXTD}}}{\epsilon_0 \epsilon_{\mathrm{PAS}}}} \tag{4.10}$$

As shown in Figure 4.9, T_{ALGAN}, T_{SIN}, T_{GFP}, T_{SFP}, and T_{EXTD} are the thicknesses of the AlGaN layer, the SiN insulator, the insulator under the gate-FP, the insulator under the source-FP, and the passivation layer, respectively. Furthermore, ϵ_0, $\epsilon_{\mathrm{ALGAN}}$, ϵ_{SIN}, and ϵ_{PAS} are the permittivities of the vacuum, the AlGaN layer, the SiN layer, and the passivation layer, respectively. Using FP capacitances defined by Eqs. (4.8)-(4.10), the total charge per unit area of the gate-FP in the 2DEG region ($Q_{\mathrm{2DEG\_gfp}}$) and that of the source-FP in the 2DEG region ($Q_{\mathrm{2DEG\_sfp}}$) are modeled by following equations.

$$Q_{\mathrm{2DEG\_gfp}} = C_{\mathrm{gfp0}} \cdot \{-(V_{\mathrm{gs}} - V_{\mathrm{bs}}) + V_{\mathrm{FBGFP}} - \phi_{\mathrm{sover}}\} \tag{4.11}$$

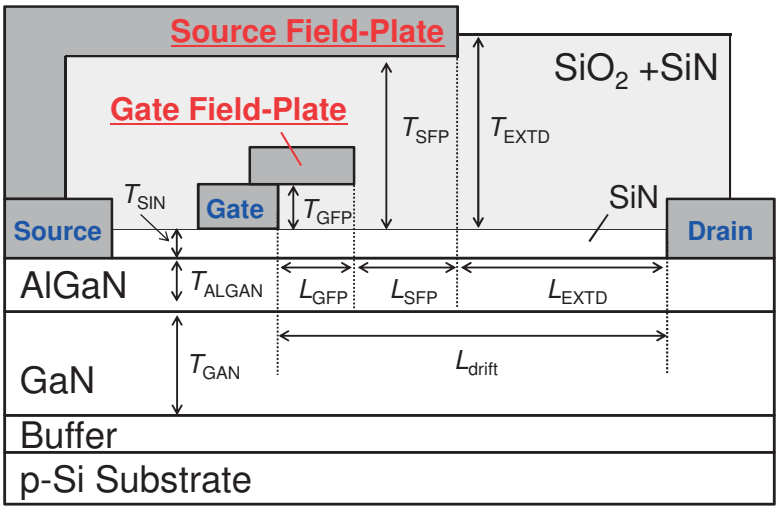


Figure 4.9: Cross-sectional schematic of the GaN-HEMT with the dual-field-plate (FP) (the gate field-plate and the source field-plate) technique.

$$Q_{\mathrm{2DEG\_sfp}} = C_{\mathrm{sfp0}} \cdot \{-(V_{\mathrm{gs}} - V_{\mathrm{bs}}) + V_{\mathrm{FBSFP}} - \phi_{\mathrm{sover}}\} \tag{4.12}$$

where V_{FBGFP} and V_{FBSFP} are model parameters for the flat-band voltage of the gate-FP and the flat-band voltage of the source-FP, respectively. These flat-band voltages are in principle determined by the impurity concentrations and the interface conditions. However, their exact values are mostly not known. Therefore, we keep them as model parameters. The surface potential ϕ_{sover} in Eqs. (4.11) and (4.12) is calculated by solving the Poisson equation for the gate field-plate and the source field-plate individually. Similarly, the extrinsic drain charge in the 2DEG region ($Q_{\mathrm{2DEG\_extd}}$) is modeled by following equation.

$$Q_{\mathrm{2DEG\_extd}} = C_{\mathrm{extd0}} \cdot \{-(V_{\mathrm{gs}} - V_{\mathrm{bs}}) + V_{\mathrm{FBEXTD}} - \phi_{\mathrm{sover}}\} \tag{4.13}$$

where V_{FBEXTD} is the flat-band voltage of the extrinsic drain side. Due to expansion of the depletion layer under the gate field-plate to the y direction, the total charge in the 2DEG region, as defined by Eqs. (4.11)-(4.13), is reduced. Using the depletion layer width (W_{d}) of Eq. (4.7) and Eqs. (4.11)-(4.13), effective charges in the 2DEG region Q_{ovd} are calculated by Eqs. (4.14)-(4.16).

i) L_{GFP} - $W_{\mathrm{d}} \geq 0$

$$Q_{\mathrm{ovd\_gfp}} = W_{\mathrm{eff}} \cdot (L_{\mathrm{GFP}} - W_{\mathrm{d}}) \cdot Q_{\mathrm{2DEG\_gfp}} \tag{4.14}$$

ii) $(L_{\mathrm{GFP}} + L_{\mathrm{SFP}})$ - $W_{\mathrm{d}} \geq 0$

$$Q_{\mathrm{ovd\_sfp}} = W_{\mathrm{eff}} \cdot (L_{\mathrm{SFP}} - (W_{\mathrm{d}} - L_{\mathrm{GFP}})) \cdot Q_{\mathrm{2DEG\_sfp}} \tag{4.15}$$

iii) $(L_{\mathrm{GFP}} + L_{\mathrm{SFP}} + L_{\mathrm{EXTD}})$ - $W_{\mathrm{d}} \geq 0$

$$Q_{\mathrm{ovd\_extd}} = W_{\mathrm{eff}} \cdot (L_{\mathrm{EXTD}} - (W_{\mathrm{d}} - (L_{\mathrm{GFP}} + L_{\mathrm{SFP}}))) \cdot Q_{\mathrm{2DEG\_extd}} \tag{4.16}$$

Here W_{eff}, L_{GFP}, L_{SFP} and L_{EXTD} are the effective channel width, the gate-FP length, the source-FP length and the length from the edge of the drain electrode to the edge of the source FP, respectively. By differentiating the modeled charges in the region Q_{ovd} with respect to the drain-source voltage V_{ds}, the gate-FP capacitance (C_{gfp}), the source-FP capacitance (C_{sfp}) and the extrinsic drain capacitance (C_{extd}) are finally obtained by following equations.

$$C_{\mathrm{gfp}} = \frac{dQ_{\mathrm{ovd\_gfp}}}{dV_{\mathrm{ds}}} \tag{4.17}$$

$$C_{\mathrm{sfp}} = \frac{dQ_{\mathrm{ovd\_sfp}}}{dV_{\mathrm{ds}}} \tag{4.18}$$

$$C_{\mathrm{extd}} = \frac{dQ_{\mathrm{ovd\_extd}}}{dV_{\mathrm{ds}}} \tag{4.19}$$

Together with the field-plate induced capacitance, total capacitance components are described as

$$C_{\mathrm{iss}} = C_{\mathrm{iss\_int}} + C_{\mathrm{gfp}} + C_{\mathrm{sfp}} \tag{4.20}$$

$$C_{\mathrm{oss}} = C_{\mathrm{oss\_int}} + C_{\mathrm{gfp}} + C_{\mathrm{sfp}} + C_{\mathrm{extd}} \tag{4.21}$$

where $C_{\mathrm{iss\_in}}$

respectively.

4.4 Cc
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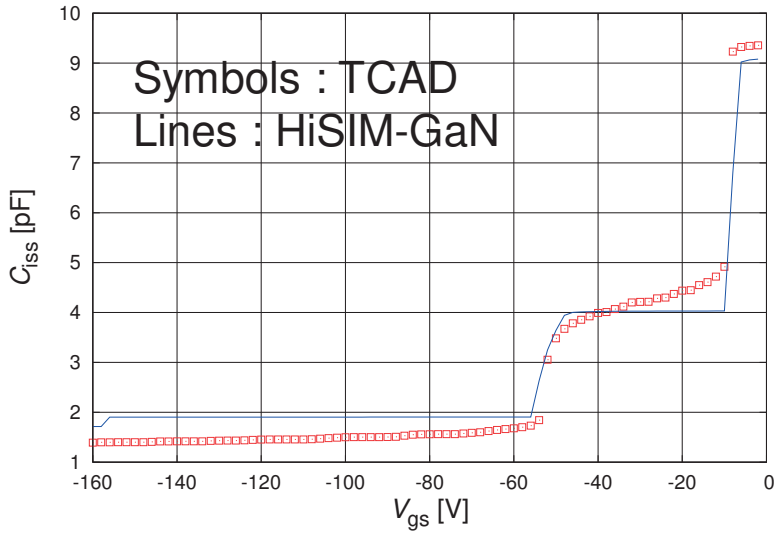

Figure 4.10: HiSIM-GaN calculated input capacitance C_{iss} as a function of V_{gs} compared with TCAD device simulation.

Figure 4.10 compares simulated C_{iss}-V_{gs} characteristics by TCAD with those of the developed model with circuit simulator HSPICE [54]. It is seen that the 1$^{\mathrm{st}}$ abrupt capacitance reduction by applying larger V_{gs} than the threshold voltage (V_{th}) and the 2$^{\mathrm{nd}}$ abrupt capacitance reduction, caused by the depletion layer reaching the edge of the gate-FP, are well reproduced by adopting the developed capacitance model. Figure 4.11 compares simulated C_{iss}, C_{oss} and C_{rss} characteristics as a function of V_{ds} by TCAD to those calculated by using the developed model. As V_{ds} increases, the depletion layer reaches the edge of the gate-FP and the 1$^{\mathrm{st}}$ abrupt capacitance reduction is caused by the decreasing gate-FP capacitance. By applying still larger V_{ds}, a 2$^{\mathrm{nd}}$ abrupt capacitance reduction occurs due

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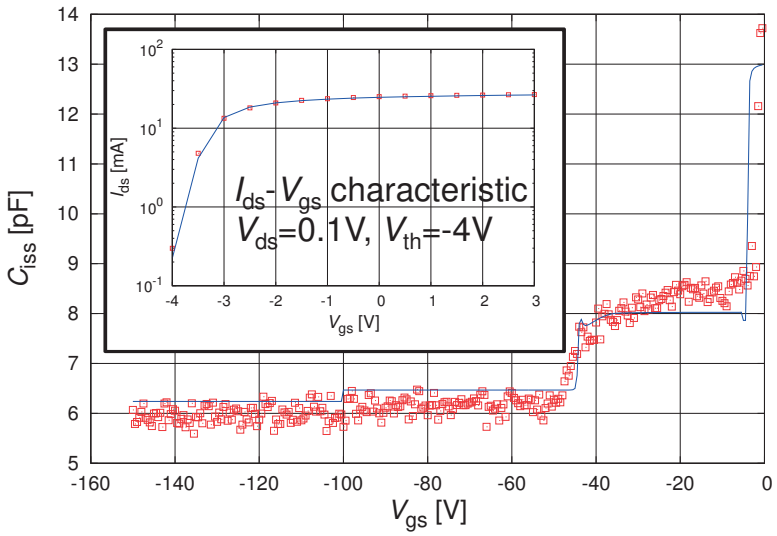

Figure 4.12: Measured and simulated I_{ds}-V_{gs} characteristics at V_{ds}=0.1V (inset). Comparison of modeled C_{iss}-V_{gs} with measurements at room temperature and fixed V_{ds} of 0V. Symbols are measurements and lines are HiSIM-GaN simulation results. The threshold voltage (V_{th}) for the studied GaN-HEMT is about -4.0V.

Figure 4.12 shows the comparison of the modeled C_{iss} as a function of V_{gs} with measurements at room temperature and fixed V_{ds} of 0V, to test the practical valid-

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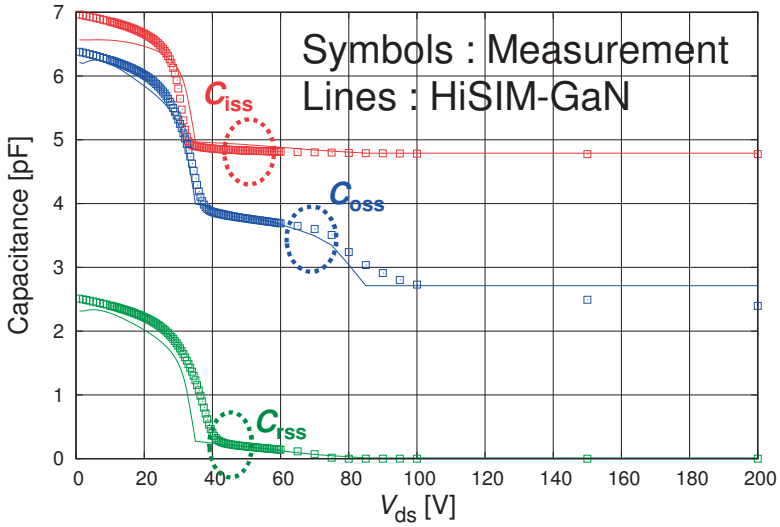

Figure 4.13: Comparison of the modeled $C_{\mathrm{iss}}/C_{\mathrm{oss}}/C_{\mathrm{rss}}$-$V_{\mathrm{ds}}$ with measurements at room temperature and fixed V_{gs} of -15V.

4.5 Summary

This chapter presented the analysis of the field-plate capacitance by 2D device simulation. In the studied GaN-HEMT device with dual FPs above the gate and the source electrodes, abrupt capacitance reduction of C_{iss} and C_{rss} caused by the depletion extension reaches the edge of gate-FP and source-FP. As a result of the analysis of 2D device simulation, there is a strong correlation between the C_{rss} and the depletion layer width. Hence, for the accurate modeling of field-plate capacitances, it is important to accurately describe the extension of the depletion width.

This chapter also presented two new capacitance modeling approaches for field-plates relaxing the electric field induced below the gate edge of the 2DEG region at the AlGaN/GaN interface. As the first approach, an empirical capacitance model is developed. In the developed empirical model, the total capacitance, which is formed by three major components; the intrinsic gate capacitance C_{int}, the gate field-plate capacitance C_{gfp}, and the source field-plate capacitance C_{sfp}, is modeled by using three different non-linear tanh functions. The empirical model reproduces the measured capacitance characteristics. As the second approach, the physics-based capacitance model is proposed. The proposed physics-based model is based on the surface potential calculated from the Poisson equation and successfully reproduces the simulated capacitance characteristics by TCAD device simulation and also the experimental measurement results.

Chapter 5

Analysis of Circuit Performance

5.1 Introduction

The compact model is a powerful tool for the power electronics design. Although some previous models were proposed, the power efficiency prediction has not been well analyzed. In circuit design, the power efficiency is an important concern for high power applications. In fact, devices based on GaN material can realize lower power loss in certain application types because their on-resistance is lower than for corresponding Si-based devices. For accurate analysis, the compact model must be constructed with not only the intrinsic GaN-HEMT part but also its parasitic components. In particular, in high frequency power-electronics applications over 1 MHz, these parasitic capacitances and inductances of pF and nH order, respectively, cannot be ignored for accurate efficiency prediction and switching-noise analysis [55].

This chapter indicates the newly developed compact model HiSIM-GaN, which includes a capacitance model of FP structures. The analysis results quantify the parasitic component influence upon power efficiency and voltage/current oscillations during switching.

5.2 Boost Converter Circuit

The boost converter circuit is a main DC/DC converter circuit and employed to the power-factor-correlation (PFC) circuit in the AC/DC converter for the per-

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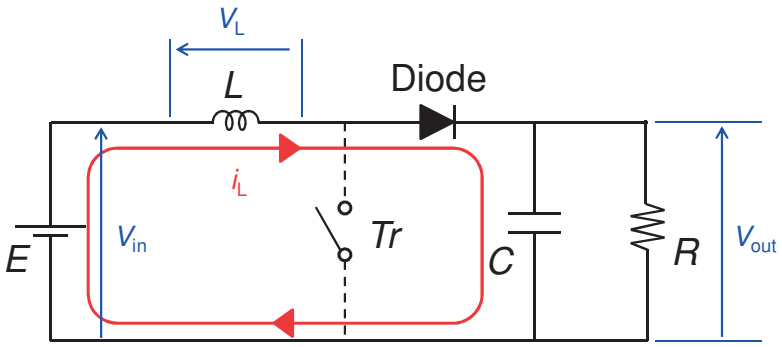

(b) Switch OFF

Figure 5.1: Circuit diagram of the simplified boost converter circuit

Figure 5.2 shows the typical waveforms of the current flowing through the inductor in the simplified boost converter circuit. When the switch is ON state as shown Fig 5.1a, the inductor voltage V_L is given by

$$V_L = L\frac{di_L}{dt} \tag{5.1}$$

where i_L is the current flowing through the inductor. During the ON state, the inductor voltage (V_L) is equal to the input voltage (V_{in}). Therefore, the increase

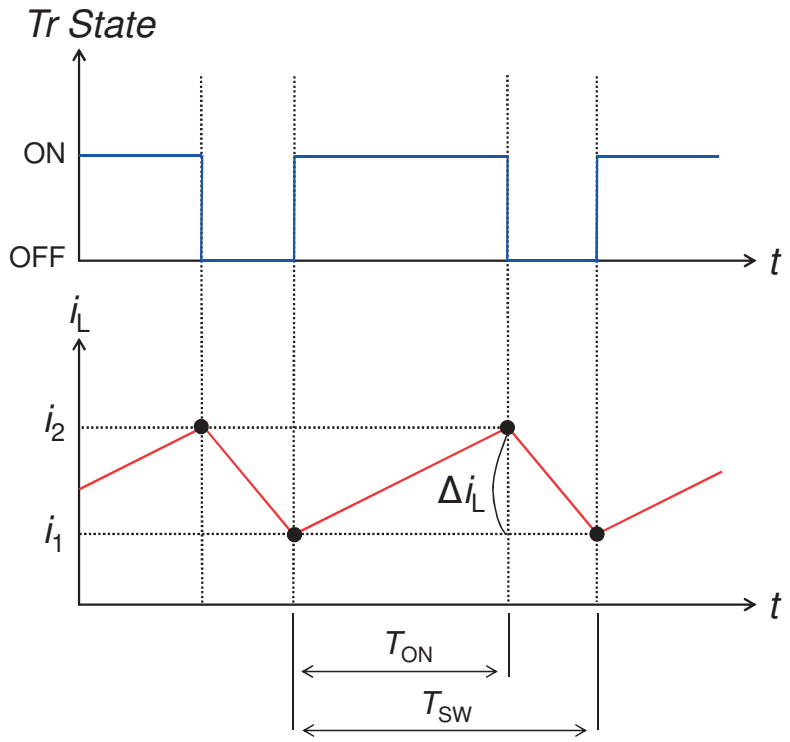

Figure 5.2: Example of the current flowing through the inductor in the simplified boost converter circuit as shown in Figs 5.1a and 5.1b.

of the current flowing the inductor ($\Delta i_{\mathrm{L\_on}}$) is

$$\begin{aligned} \Delta i_{\mathrm{L\_on}} &= i_2 - i_1 \qquad (5.2) \\ &= \frac{1}{L}\int_0^{\delta T_{\mathrm{SW}}} V_{\mathrm{L}} dt \\ &= \frac{1}{L} V_{\mathrm{in}} \delta T_{\mathrm{SW}} \qquad (5.3) \end{aligned}$$

where T_{SW} and T_{ON}, δ are the time period, the time during the on-state, and the duty ratio ($T_{\mathrm{ON}}/T_{\mathrm{SW}}$), respectively.

On the other hand, when the switch is OFF state as shown Fig 5.1b, the inductor current flows through the load. By assuming the voltage drop is zero in the diode and a capacitor C is large enough for the its voltage to remain constant, the inductor voltage V_{L} is given by

$$V_{\mathrm{L}} = V_{\mathrm{out}} - V_{\mathrm{in}} = L\frac{di_{\mathrm{L}}}{dt} \qquad (5.4)$$

During the OFF state, the inductor current is reduced as the impedance is higher. Therefore, the decrease of the current flowing the inductor ($\Delta i_{\mathrm{L\_on}}$) is

$$\begin{aligned}\Delta i_{\mathrm{L\_off}} &= i_2 - i_1 \qquad (5.5)\\ &= \frac{1}{L}\int_{\delta T_{\mathrm{SW}}}^{T_{\mathrm{SW}}} V_{\mathrm{L}} dt \\ &= \frac{1}{L}(V_{\mathrm{out}} - V_{\mathrm{in}})(1-\delta)T_{\mathrm{SW}} \qquad (5.6)\end{aligned}$$

In the steady state condition as the current through the inductor does not change abruptly, the current at the end of switch on state and the current at the end of switch off state should be equal. Also the currents at the start of switch off state should be equal to current at the end of switch on state. From Eqs. 5.3 and 5.6, the relationship between the output voltage (V_{out}) and the input voltage (V_{in}) are calculated as follows.

$$V_{\mathrm{out}} = \frac{1}{1-\delta} V_{\mathrm{in}} \qquad (5.7)$$

Equation 5.7 shows that the output voltage (V_{out}) is always higher than the the input voltage (V_{in}), and that it increases with the duty ratio δ, theoretically to infinity as δ approaches 1.

5.3 Circuit Analysis and Discussion

Table 5.1: Measurement conditions for the studied boost converter circuit.

	V_{in}	50 V
	R_{g}	20 Ω
V_{gs} (pulse)	High (on)	0 V
	Low (off)	-12 V
	Frequency	1MHz
	Duty Ratio	50 %

Figure 5.3:
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a switching

Figure 5.4: Pict

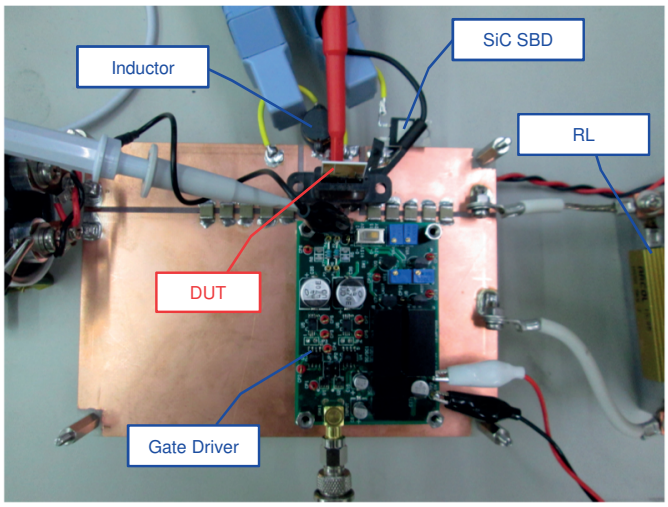


Figure 5.5: Picture of the measured boost converter.

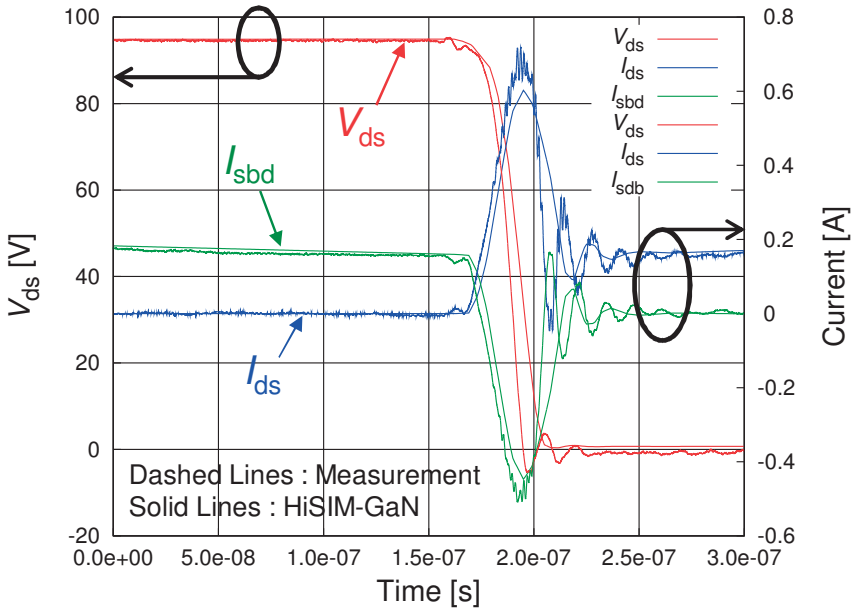
Figure 5.3 shows the circuit diagram of the studied boost converter circuit. To analyze the switching characteristics, parasitic elements induced in the measurement setup are considered explicitly. Since the measurements include additional parasitic effects in the circuit as depicted in Fig. 5.3, all these parasitic values were separately extracted and included in the simulation as well. Two parasitic inductances of 20 nH are added to both the drain and the source side of the GaN-HEMT. Additionally, a parasitic inductance of 7 nH is added to the anode side of the SiC-based Schottky-Barrier-Diode (SBD). A parasitic capacitance of 10 pF is considered between the drain and the source. These values of the parasitic elements are slightly adjusted from their nominal values to reproduce measured switching-on characteristics. Other element values within the circuit are fixed to their nominal values. Figure 5.4 is shown the picture of the measurement system for switching characteristics. Switching characteristics, such as waveforms, the rise time and the fall time, are able to be measured with an oscilloscope. And Figure 5.5 is shown the picture of the measured boost converter circuit. The gate driver provides the gate input signal (V_{gs}) to the studied GaN-HEMT as the Device-Under-Test (DUT).

5.3.1 Contribution of Trap Density Effects

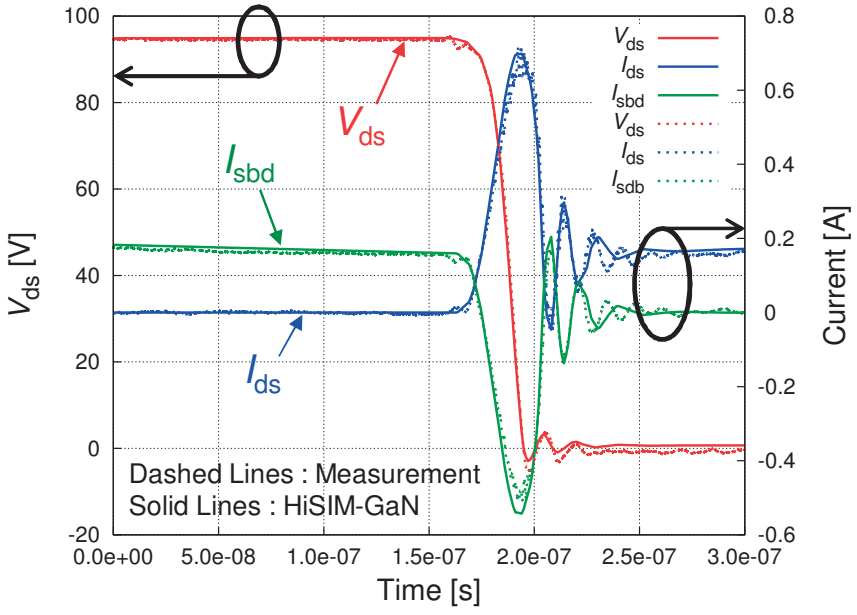
In this subsection, the trap density in the device was studied to clarify the influence of the current collapse phenomena upon the power efficiency. Figures 5.6a and 5.6b show a comparison of the measured and simulated switching-on waveform of the studied circuit shown in Fig. 5.3. Dotted lines show measurement data, and solid lines show HiSIM-GaN simulation results with trap density extracted from DC and transient measurement, respectively. It is seen that the trap density strongly affects the turn-on switching waveform and the measured turn-on waveform is well reproduced by considering one half of the trap density extracted by the measured I-V characteristics.

The trapped carrier inclusion in HiSIM-GaN leads to good reproduction of the

corresponding



(a) The trap density N_{trap}=1.0×10^{12}cm^{-2} extracted from DC measurement.



(b) The trap density N_{trap}=0.5×10^{12}cm^{-2} extracted from transient measurement.

Figure 5.6: Comparison of the measured and the simulated turn-on switching waveforms of the studied boost converter circuit (see Fig. 5.3).

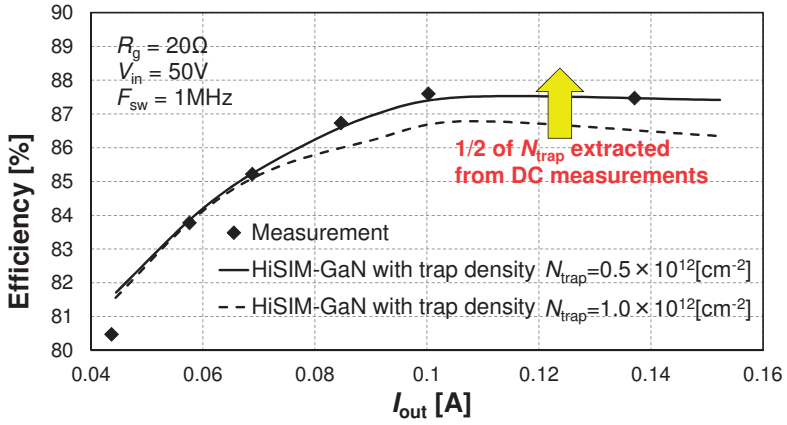


Figure 5.7: Measured and simulated power efficiency of the studied GaN-based boost converter circuit (see Fig. 5.3) with a gate resistance of R_g=20 Ω.

where P_{in} and P_{out} are the input power consumption and the output power consumption. As shown in Eq. (5.8), P_{in} is calculated by the integration of the product between the input current I_{in} and the input voltage V_{in} (see Fig. 5.3). Similarly, P_{out} is calculated by the integration of the product between the output current I_{out} and the output voltage V_{out} (see also Fig. 5.3).

Figure 5.7 shows a comparison of measured and simulated power efficiency of the studied circuit for different trap densities. Symbols are measurements, the dashed line is dashed line is HiSIM-GaN simulation result with trap density extracted from DC measurement, and the solid line is HiSIM-GaN simulation result with trap density extracted from transient measurement. The extracted trap density of the used device was $0.5\times10^{12}\text{cm}^{-2}$. It corresponds to 5% of the 2DEG density, which is approximately $1.0\times10^{13}\text{cm}^{-2}$. The power efficiency under heavy ($I_{out} \geq 0.1$A) load current condition decreases remarkably for higher trap density, due to the increased conduction loss induced by the current-collapse phenomenon, which substantially degrades the power efficiency. It is seen that, by considering half of trap density extracted from DC measurements, the measured power efficiency is well reproduced. The trap density shifts the threshold voltage to higher values, resulting in the reduction of the conductivity. The conductivity loss leads to the efficiency reduction. An interesting observation is that the trap

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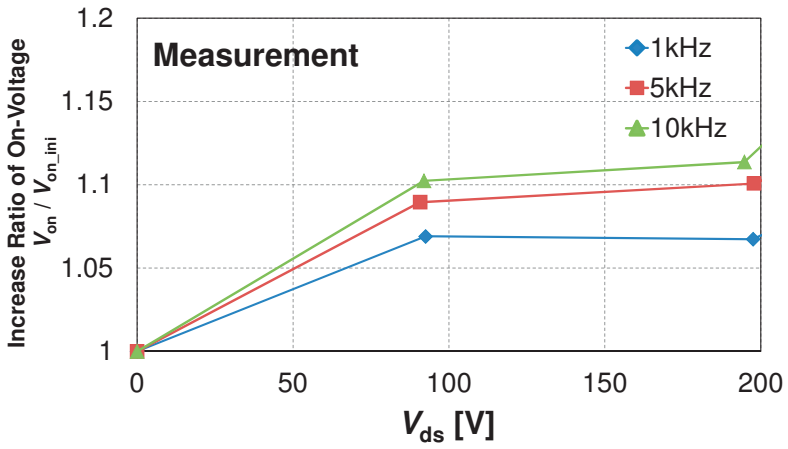

Figure 5.8: Measured increase ratio of on-voltage as a function of V_{ds} for different switching frequencies.

The trapping event contribution to the circuit performance is discussed as follows. Figure 5.8 shows the measured increase ratio of on-voltage as a function of V_{ds} for different switching frequencies. The measured on-resistance increase ratio is about 5% in the specified range of operation conditions for the studied circuit. This result suggests that the dynamically active trap density is different from the trap density under the DC condition. Therefore, re-extraction of N_{trap} was required for transient simulations. It is known that the trap event requires time to accomplish, namely, the time constant. If the time constant is longer than the switching speed, only a small amount of carriers can be trapped. This effect must be included.

5.3.2 Contribution of Field-Plate Effects

Furthermore, the contribution of the field-plate capacitance upon the circuit performance was studied. Figure 5.9 shows a contribution of field-plate effects upon the power efficiency in the studied circuit shown as Fig. 5.3. Symbols are measurements, the dashed line is HiSIM-GaN simulation result without the gate and the

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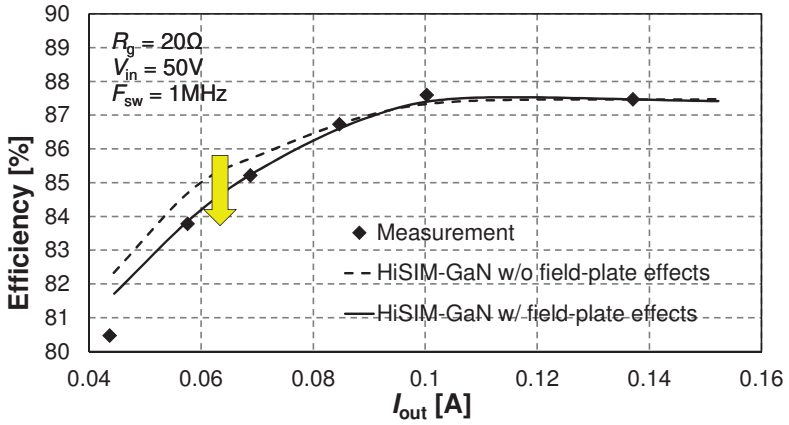

Figure 5.9: Contribution of field-plate effects upon the power efficiency in the studied circuit shown in Fig. 5.3.

Under light-load-current condition of $I_{\rm out} < 0.1$A, the switching loss dominates in the total loss because the switching time is determined by the charging of the output capacitance $C_{\rm oss}$ with the small drain-source current $I_{\rm ds}$ of the GaN-HEMT as the DUT. Since $I_{\rm ds}$ is small, charging of output capacitance $C_{\rm oss}$ becomes slow. Therefore the FP structure affects $C_{\rm oss}$, power efficiency under light-load-current condition is clearly influenced. On the other hand, under heavy-load-current condition of $I_{\rm out} \geq 0.1$A, the conduction loss is dominant for the total loss. Since the FP structure does not modulate the on-resistance, the influence of the FP length upon the efficiency is small as shown in Fig. 5.9. The HiSIM-GaN model achieved reproduction the measured power efficiency by considering parasitic components and the FP capacitance accurately.

Figure 5.10a depicts the measured power efficiency of the studied circuit with the gate resistance $R_{\rm g}$ of 20 Ω. It is seen that the peak value of the measured power efficiency is at the output load current $I_{\rm out}$ of 0.1A. Therefore, it have been defined $I_{\rm out} < 0.1$A to be the low-load-current condition and $I_{\rm out} \geq$0.1A to be the high-load-current condition. In order to confirm the effect of field-plate (FP) capacitances for power efficiency, it was simulated two different $R_{\rm load}$ conditions ($R_{\rm load}$=660 Ω and

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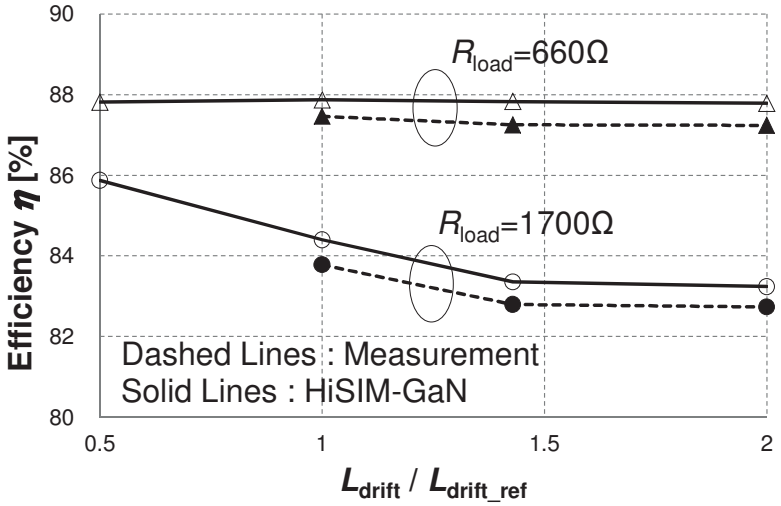


(b) The drift region length L_{drift} dependency of the power efficiency

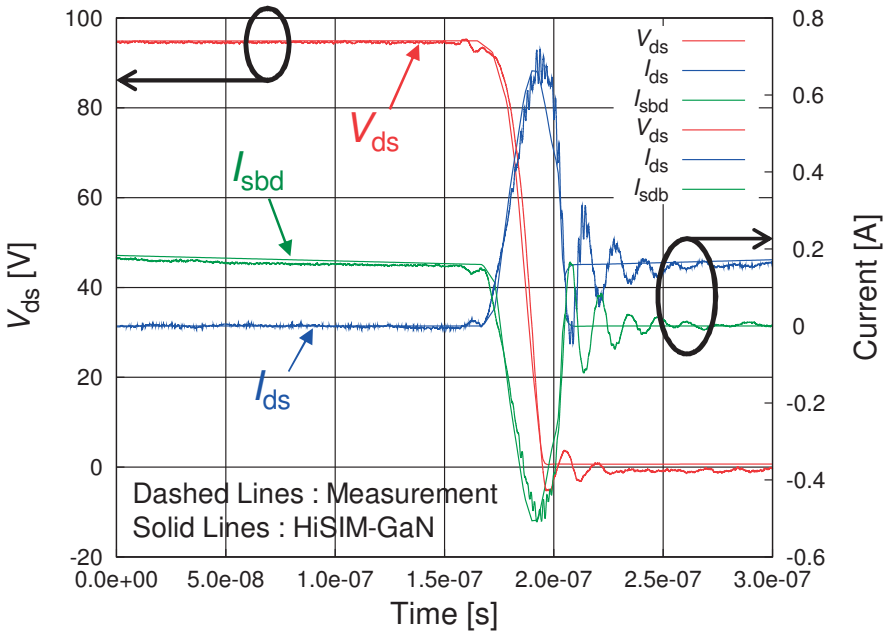
Figure 5.10: (a) Measured power efficiency of the studied GaN-based boost converter circuit (see Fig. 5.3) with a gate resistance R_{g} of 20Ω, (b) Comparison of measured and simulated power efficiency of the studied circuit by considering the ratio of the drift region length L_{drift} to the reference drift region length $L_{\mathrm{drift\_ref}}$ under high-load-current condition with R_{load} of 660Ω and low-load-current condition with R_{load} of 1700Ω.

total loss, because the switching time is determined by the charging of the output capacitance C_{oss}, which becomes longer due to the smaller drain-source current I_{ds} of the DUT in the studied circuit. Therefore, the FP structure affects C_{oss} and the power efficiency. As shown in Fig. 5.10b, the HiSIM-GaN simulation result with R_{load} of 1700 Ω verifies that the efficiency remarkably depends on L_{drift} in the low-load-current condition because C_{oss} increases with the FP length. On the other hand, under high-load-current condition, the conduction loss is dominant for the total loss. Since the FP structure does not modulate the on-resistance, the influence of the FP length upon the efficiency is small as shown in Fig. 5.10b for HiSIM-GaN simulation result with R_{load} of 660 Ω. From these obtained results, the validity of our developed compact HiSIM-GaN model was successfully confirmed.

5.3.3 Contribution of Parasitic Circuit Components

Finally, the influence of parasitic components upon the switching waveforms and the power efficiency was studied. Figures 5.11a and 5.11b show the contribution of considerable parasitic components upon the turn-on switching characteristic shown as Fig. 5.3. Dotted lines show measurement data, and solid lines show HiSIM-GaN simulation results with and without parasitic components, respectively. It is seen that the simulated turn-on switching waveform reproduces the measured waveform well by considering these capacitive and inductive parasitic components as shown in Fig. 5.11a. The trap density N_{trap} was held constant ($0.5\times10^{12}\mathrm{cm}^{-2}$) during the simulations to clearly see the influence of the parasitic components. In order to verify the capacitive and inductive parasitic components, the turn-on switching characteristics were simulated without parasitic components as shown in Fig. 5.11b. In the simulation result, the ringing during the switching disappeared due to the removed parasitic components. Therefore, these parasitic components must be considered to reproduce the switching waveform and to analyze the Electro Magnetic Interference (EMI) switching-noise.

The influence of parasitic components for the power efficiency is discussed as



(b) Without parasitic components

Figure 5.11: Contribution of considered parasitic components upon the turn-on switching characteristic. Gate resistance R_g=110 Ω and load resistance R_{load}=1120 Ω are applied.

follows. As shown in Figure 5.12, under light (I_{out} < 0.1A) and heavy (I_{out} ≥ 0.1A) load-current conditions, parasitic component contributions for the power efficiency are observed clearly. As a result, in order to predict the power efficiency

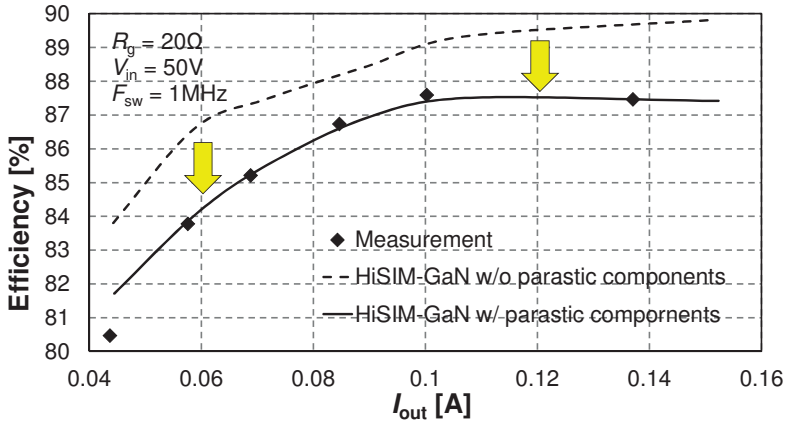


Figure 5.12: Contribution of considered parasitic components upon the power efficiency in the studied circuit.

accurately, the estimation and inclusion of parasitic components is necessary for accurate simulation.

5.4 Summary

In this chapter, in order to test the accuracy of the developed compact model for the prediction of circuit characteristics, the circuit simulation analysis of a boost converter circuit has been performed. The circuit simulation results are in good agreement with the measurement results by considering all necessary effects, such as the trap density, the field-plate capacitance and circuit parasitic components. Furthermore, the quantitative contributions of device and circuit parasitic components upon switching characteristics and power efficiency have been investigated.

- Trapping density effects
  - Power efficiency at Heavy load current condition
- Field-plate effects
  - Power efficiency at Light load current condition
- Parasitic components

- Power efficiency and switching noise at both Heavy and Light load current conditions

Consequently, the extraction and the modeling of field-plate effects, parasitic components and carrier-trapping effects in the GaN-HEMT device are essential for predicting the switching waveform and the power efficiency of GaN-HEMT circuits accurately.

Chapter 6

Conclusions and Future works

In this thesis, a newly developed compact model HiSIM-GaN has been developed. The developed model have adopts the HiSIM_HV mobility model for modeling of the DC operation for GaN-HEMTs. However, specific features of GaN-HEMTs cannot be expressed by existing bulk-MOSFET models. Therefore, the developed model includes two specific features of GaN-HEMT to reproduce device characteristics of GaN-HEMTs. One is the two-dimensional electron gas induced at the AlGaN/GaN heterojunction interface. By considering all possible induced charges, the inherent 2DEG charge and the trapped charge density explicitly within the Poisson equation, the simulated GaN-HEMT characteristics by 2D device simulation can be well reproduced accurately. As a result of parameter extraction for reproducing the I-V characteristics, it was demonstrated that measured I-V characteristics of this GaN-HEMT technology are well reproduced.

The second feature is the field plate, which is introduced to delocalize the electric-field peak that occurs at the electrode edge. However, an additional parasitic capacitance is induced by existence of the field-plate. Therefore, in this thesis, the analysis of the field-plate effect is performed by 2D device simulation. As a result of the analysis of 2D device simulation, it is found to be important to accurately describe the extension of the depletion width. In order to describe the field-plate effect accurately, this thesis presented both an empirical and physics-based field-plate capacitance modeling. In the developed empirical capacitance

model, the total capacitance is modeled by using three different non-linear tanh functions. As a result of parameter extraction for reproducing the C-V characteristics, it was demonstrated that measured C-V characteristics are well reproduced. This thesis also presented a new physics-based capacitance model for field plates of GaN-HEMTs. The developed physics-based model is based on the surface potential calculated from the Poisson equation. As a result, the physics-based model successfully reproduces the simulated capacitance characteristics by 2D device simulation. By performing the parameter extraction of the measured GaN-HEMT's characteristics, the capacitance characteristics of the studied GaN-HEMT technology are well reproduced.

Finally, the switching characteristic of a boost converter circuit that is a basic element of DC-DC converters was investigated. In order to investigate the influence of various parasitic components, the switching waveform and the power efficiency have been analyzed. It was confirmed, that by including all necessary effects and parasitic components, measured turn-on switching characteristics and power efficiency of this boost converter circuit were well reproduced. Furthermore, the quantitative contributions of specific features of GaN-HEMTs, which are trap density effects, field-plate capacitance effects, and parasitic components, upon the switching waveform and the power efficiency have been verified.

In general, device degradation is caused by carrier-trapping effects. Especially, the threshold voltage and the subthreshold slope are determined only by the device parameter values such as the impurity concentration. In HiSIM-GaN, the trap density is extracted to reproduce the measured I_{ds}-V_{gs} characteristics. The trapping event is assumed to be a long-term event in HiSIM-GaN. Therefore, trap density extracted from measured DC characteristics is considered as static trap density. This static trap density means that the time constant for trapping is not considered in this work. In order to reproduce the measured switching waveform and the power efficiency, the trap density has been re-extracted and was found to have a value which is one half of the density extracted with measured DC characteristics.

This results suggests that the dynamically active trap density is different from the static trap density under the DC condition, and that the transient waveform is required to consider the time constant of the trap events.

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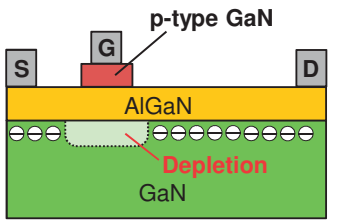
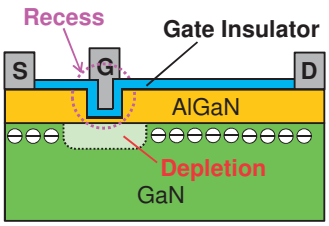
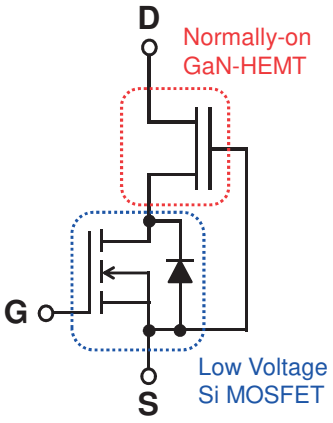


(a) *p*-type GaN gate structure



(b) Recess and MIS gate structure



(c) Cascode structure

Figure A.1: Various normally-off structures of the GaN-HEMT

A conventional GaN-HEMT as shown in Fig. 1.2 operates in the normally-on condition that means that the device does not shut down even when there is no gate voltage applied. The normally-on GaN requires negative voltage to switch to the off-state. With few options, manufacturers developed a countermeasure to transform the normally-on GaN transistors to normally-off in order to materialize the usage of GaN to power circuits. Figure A.1 shows various GaN-HEMT structures for the normally-off operation. To realize the normally-off operation in GaN-HEMTs, in general, two structural approaches and the circuit approach are utilized. The basic concept of the structural approach is the control of the 2DEG density under the gate electrode. As the 2DEG density is decreased between

the drain and the source, the on-resistance is increased. Therefore, by depleting only the 2DEG charge under the gate electrode, both the low-on-resistance and the normally-off operation are realized. The methodology of the deletion of the 2DEG charge under the gate electrode is distinguished in depleting by the pn junction which is the conventional approac

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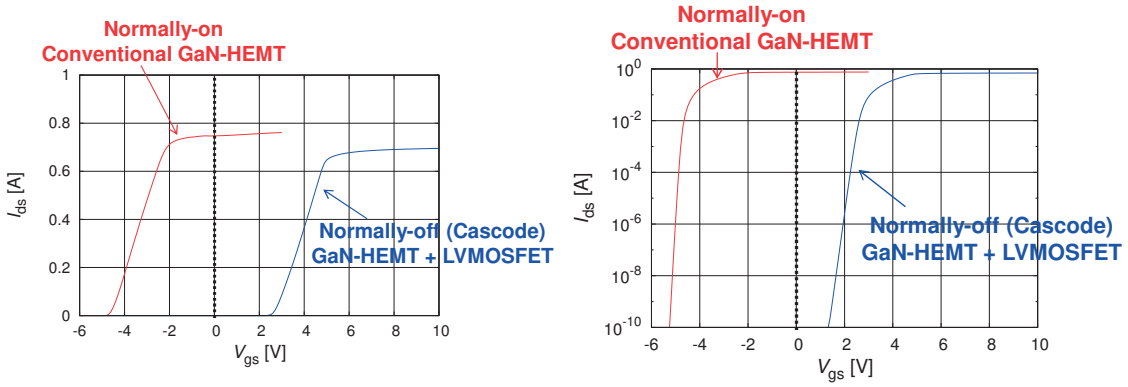

(a) Linear scale

(b) Logarithmic scale

Figure A.2: Comparison of the simulated I_{ds}-V_{gs} characteristics at V_{ds}=5V with the normally-on conventional GaN-HEMT and the cascode structure of the normally-on GaN-HEMT with LV-MOSFET for the normally-off operation.

On the other hand, the normally-on high voltage GaN-HEMTs are widely used in series connected with low voltage Si-MOSFETs for normally-off Cascode struc-

ture as shown in Fig. A.1c [59]. Figures A.2a and A.2b shows the comparison of the simulated I_{ds}-V_{gs} characteristics at V_{ds}=5V with the normally-on conventional GaN-HEMT and the cascode structure of the normally-on GaN-HEMT with low voltage Si-MOSFET for the normally-off operation. Since the low voltage Si-MOSFET is connected the normally-on GaN-HEMT in series, the threshold voltage of the pseudo-quasi normally-off GaN-HEMT is determined by the low voltage Si-MOSFET. On the other hand, the on-resistance of the low-voltage Si-MOSFET is much smaller than that of the normally-on GaN-HEMT, the total voltage drop is dominant by the normally-on GaN-HEMT.

Appendix B

Parameter Extraction Procedure

B.1 Flowchart of Parameter Extraction

Figure B.1 shows the flowchart of the HiSIM-GaN parameter extraction procedure for the main characteristics of the GaN-HEMT power device. First of all, target device characteristics are derived by the TCAD device simulation and measurements. At that time, the following items are listed as minimum necessary device characteristics.

1). I_{ds}-V_{gs} characteristics at the linear and the saturation regions (Including the temperature dependence).

2). I_{ds}-V_{ds} characteristics at the different V_{gs} (Including the temperature dependence).

3). C_{iss}-V_{gs} characteristic at fixed V_{ds} of 0V (only for the room temperature).

4). $C_{\mathrm{iss}}/C_{\mathrm{oss}}/C_{\mathrm{rss}}$-$V_{\mathrm{ds}}$ characteristics at fixed $V_{\mathrm{gs}} < V_{\mathrm{th}}$ (only for the room temperature).

As a flow of actual parameter extraction, the model parameters for the threshold voltage, the low-field mobility, the high-field mobility, the resistance effect at the drift region, the seld-heating effect, and the trapping event have been extracted, targeting the DC characteristics such as I_{ds}-V_{gs} characteristics and I_{ds}-V_{ds} characteristics. Next, structural parameters of target GaN-HEMT power device

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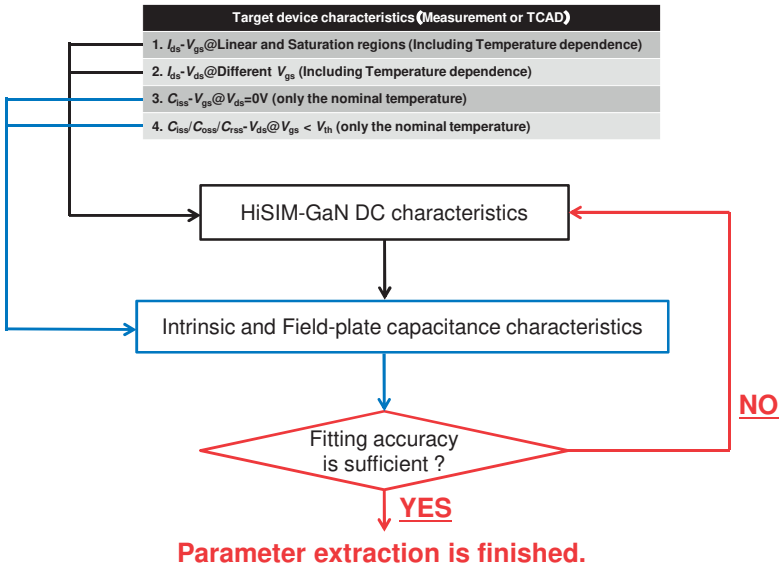

Figure B.1: Flowchart showing the parameter-extraction sequence of HiSIM-GaN model parameters.

B.2 Parameter Extraction for DC Characteristics

First, before carrying out the parameter extraction, the structural information that cannot be extracted from device characteristics is acquired as process parameters. The process parameters which are minimum necessary for extracting HiSIM-GaN model parameters are shown as follows.

L : Gate length

W : Device width

TOX : Gate insulator thickness (equal to **TSIN** as shown in Figures 4.9 and B.5)

In addition, structural parameters related to field plate such as field-plate length, inter-layer dielectric thickness etc. must be necessary for the capacitance

modeling.

Figure B.2a shows the extraction procedure of the threshold voltage and the trap density from subthreshold region. As a first step of the HiSIM-GaN model parameter extraction, the optimization of the subthreshold region is carried out using the I_{ds}-V_{gs} curve.

VFBC : To fit the threshold voltage
NSUBC : To fit the threshold voltage and the subthreshold slope
PTL : To fit the subthreshold slope

Two independent trap-density distributions are considered as schematically shown in Figure B.2b. One represents the shallow trap density distribution and the other represents the deep trap density distribution [44]. In HiSIM-GaN, trap density parameters are extracted from the targeted subthreshold slope. Where the trapping event is assumed to be a long-term event in HiSIM-GaN model. Therefore, extracted trap density is considered as static trap density. The static trap density means that time constant for trapping is not considered in this work.

GC1, E1 : Model parameters for the shallow trap
GC2, E2 : Model parameters for the deep trap

Figures B.3a and B.3b shows the extraction procedure of the low-field mobility from I_{ds}-V_{gs} curve and G_m-V_{gs} curve at the linear region. Some parameters to be extracted in this step are shown as follows.

MUECB0, MUECB1 : To fit the subthreshold slope
MUEPH0, MUEPH1 : To fit the maximum G_m value using the G_m-V_{gs} curve
MUESR0, MUESR1 : To fit the trend of the G_m value at the high V_{gs} region
RDRMUE : To fit the drain-source current I_{ds} value at the high V_{gs} region

Here, the parameter value of **MUEPH0** and **MUESR0** are adopted the default value, respectively.

MUEPH0

MUESR0

Figures I

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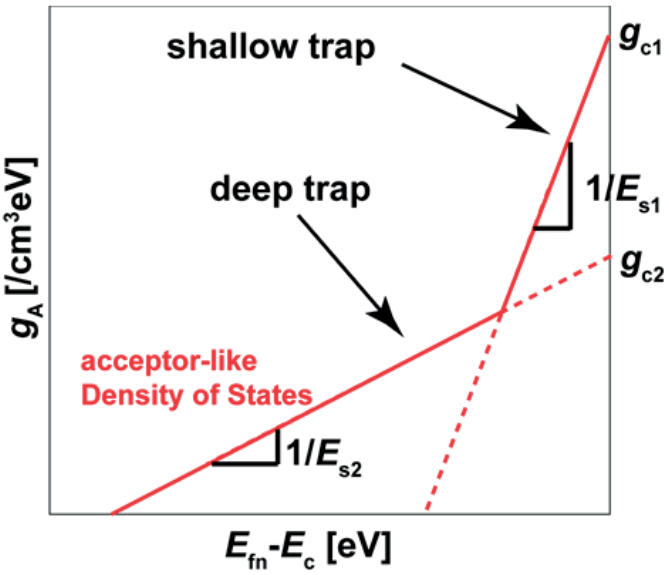
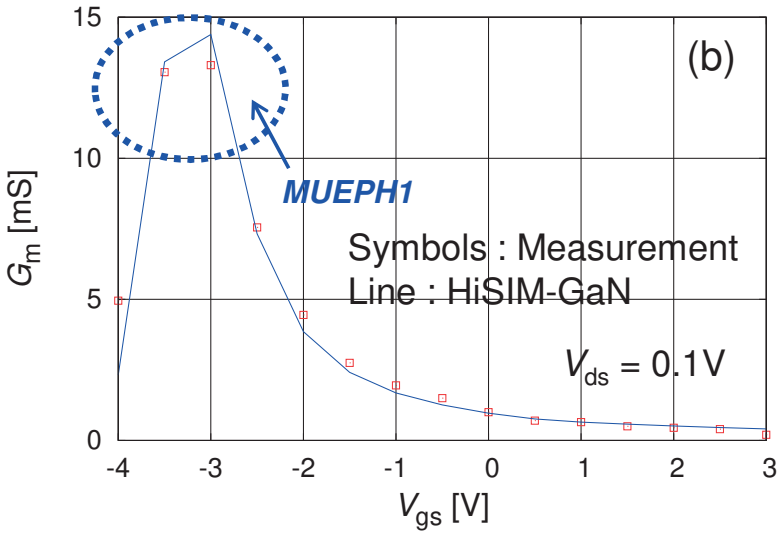
I_{ds} [mA]

(a) I_{ds}-



(b) Schematic of the trap density-of-states distribution, where E_{fn} is the quasi-Fermi level for electrons. Two independent density-of-states are depicted.

Figure B.2: Extraction of the threshold voltage and the trap density from sub-threshold region measurements.



(b) G_{m}-V_{gs} characteristic with fixed V_{ds} of 0.1V (linear scale).

Figure B.3: Extraction of low-field mobility parameters from I_{ds}-V_{gs} curve and G_{m}-V_{gs} curve in the linear region.

VMAX

: To fit the saturation current at $V_{\mathrm{gs}} \simeq V_{\mathrm{th}}$

RDRVMAX

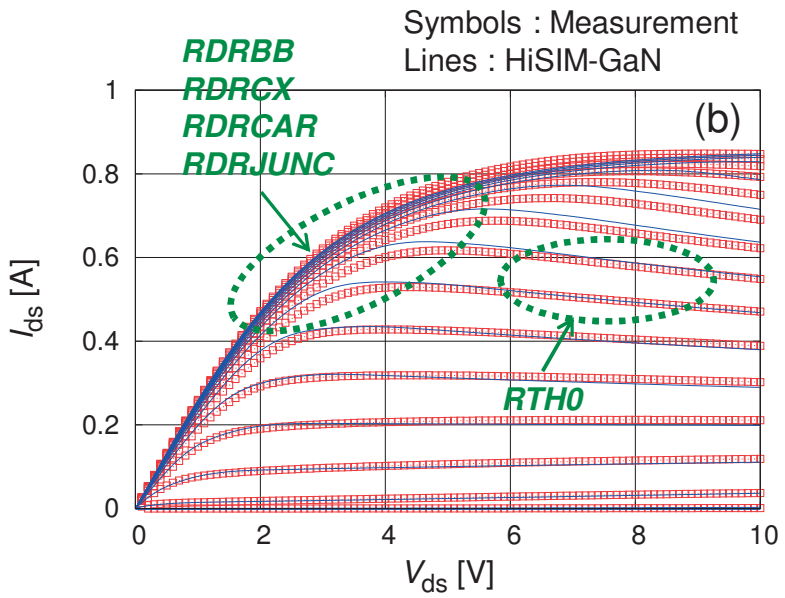
: To fit the drain-source current I_{ds} value at the high V_{gs} region

RDRBB, RDRCX, RDRCAR, RDRJUNC

: To fit the quasi-saturation region marked by dotted circles in Fig. B.4b

After the parameter extraction for DC characteristics at the room tempera-

(a



(b) I_{ds}-V_{ds} characteristics at the room temperature from V_{gs}=-12 to 3 V.

Figure B.4: Extraction of the high-field mobility, the resistance effect of the drift region, and the self-heating effect from from I_{ds}-V_{gs} curve in the saturation region and from I_{ds}-V_{ds} curve.

ture has been finished, temperature dependence parameters shown as follows are extracted by using the temperature dependence data.

BGTMP1, BGTMP2

: To fit the temperature dependence of the threshold voltage V_{th}

MUETMP

: To fit the temperature dependence of the maximum G_m value

RDRMUE

: To fi

VTMP

: To fi

RDRVTM

: To fi

B.3 P
ti

Figure B.5 s
reproduce tl
HEMT show

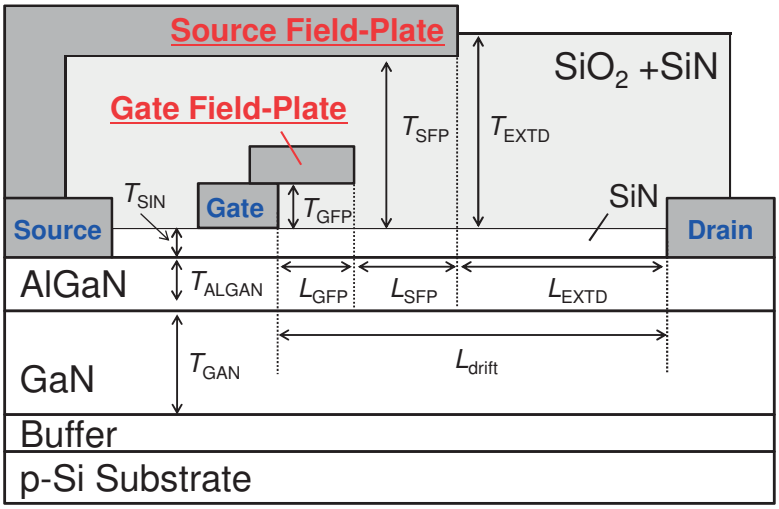
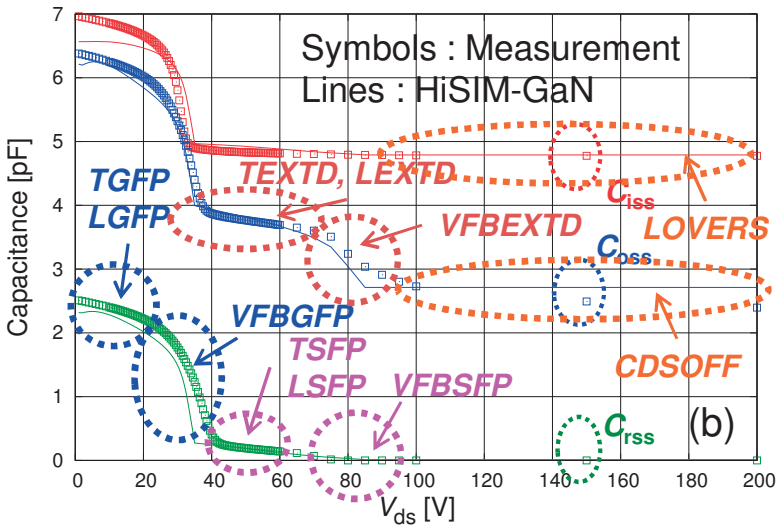


Figure B.5: Cross-sectional schematic of the GaN-HEMT with the dual-field-plate (FP) (the gate field-plate and the source field-plate) technique.

where T_{ALGAN}, T_{SIN} T_{GFP}, T_{SFP}, and T_{EXTD} are the thicknesses of the AlGaN layer, the SiN insulator, the insulator under the gate-FP, the insulator under the source-FP, and the passivation layer, respectively. Furthermore, L_{GFP}, L_{SFP}, and L_{EXTD} are the gate-FP length, the source-FP length and the length from the edge of the drain electrode to the edge of the source-FP, respectively.

In circuit
model that
to predict p
capacitance
teristics for

(a) Comparis
temperature



(b) Comparison of the modeled $C_{\mathrm{iss}}/C_{\mathrm{oss}}/C_{\mathrm{rss}}$-$V_{\mathrm{ds}}$ characteristic with measurements at room temperature and fixed V_{gs} of -15V.

Figure B.6: Extraction of structural parameters of field-plates for the target GaN-HEMT device from C_{iss}-V_{gs} curve and $C_{\mathrm{iss}}/C_{\mathrm{oss}}/C_{\mathrm{rss}}$-$V_{\mathrm{ds}}$ curve.

In order to reproduce the capacitance characteristics accurately, the following

parameters are adopted.

TGFP, LGFP

: To fit the C_{rss} value at the low V_{ds} region

VFBGFP

: To fit the 1^{st} abrupt C_{rss} reduction occurs V_{ds} value

TSFP, LSFP

: To fit the C_{rss} value after the 1^{st} abrupt C_{rss} reduction

VFBSFP

: To fit the 2^{nd} abrupt C_{rss} reduction occurs V_{ds} value

TEXTD, LEXTD

: To fit the C_{oss} value after the 1^{st} abrupt C_{oss} reduction

VFBEXTD

: To fit the 2^{nd} abrupt C_{oss} reduction occurs V_{ds} value

CDSOFF

: To fit the C_{oss} value at the high V_{ds} region

LOVERS

: To fit the C_{iss} value at the high V_{ds} region

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List of Publications

Refereed Journal Papers

i) **T. Mizoguchi**, T. Naka, Y. Tanimoto, Y. Okada, W. Saito, M. Miura-Mattausch, and H. J. Mattausch, "Analysis of GaN high electron mobility transistor switching characteristics for high-power applications with HiSIM-GaN compact model", *Japanese Journal of Applied Physics*, Vol. 55, 04EG03-1–5, 2016.

ii) **T. Mizoguchi**, T. Naka, Y. Tanimoto, Y. Okada, W. Saito, M. Miura-Mattausch, and H. J. Mattausch, "Modeling of Field-Plate Effect on Gallium-Nitride-based High Electron Mobility Transistors for High-Power Applications", *The Institute of Electronics, Information and Communication Engineers Transactions on Electronics*, Vol. E100-C, No. 3, pp. 321–328, 2017.

Refereed Conference Papers

i) **T. Mizoguchi**, T. Naito, Y. Kawaguchi, and W. Saito, "Compact Modeling of GaN-MISFET for Power Applications", *Proceedings of Simulation of Semiconductor Processes and Devices (SISPAD) Workshop on Compact Modeling*, pp. 74–77, 2014.

ii) Y. Okada, Y. Tanimoto, **T. Mizoguchi**, H. Zenitani, H. Kikuchihara, H. J. Mattausch, and M. Miura-Mattausch, "Compact Modeling of GaN HEMT Based on Device-Internal Potential Distribution", *Proceedings of Simulation of Semiconductor Processes and Devices (SISPAD)*, pp. 305–308, 2015.

iii) **T. Mizoguchi**, T. Naka, Y. Tanimoto, Y. Okada, W. Saito, M. Miura-Mattausch, and H. J. Mattausch, "Analysis of GaN-HEMT Switching Characteristics for High-Power Applications", *Proceedings of International Conference on Solid State Devices and Materials (SSDM)*, pp. 1066–1067, 2015.

iv) **T. Mizoguchi**, T. Naka, Y. Tanimoto, Y. Okada, W. Saito, M. Miura-Mattausch, and H. J. Mattausch, "Analysis of GaN-HEMTs Switching Characteristics for Power Applications with Compact Model Including Parasitic Contributions", *Proceedings of International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 267–270, 2016.

Related Papers

i) Q. Ngo, D. Navarro, **T. Mizoguchi**, S. Hosokawa, H. Ueno, M. Miura-Mattausch, and C. Y. Yang, "Gate Current Partitioning in MOSFET Models for Circuit Simulation", *Proceedings of Modeling and Simulation of Microsystems*, Vol. 2, pp. 322–325, 2003.

ii) **T. Mizoguchi**, H. J. Mattausch, H. Ueno, D. Kitamaru, K. Hisamitsu, M. Miura-Mattausch, S. Itoh, and K. Morikawa, "Extraction of Inter- and Intra-Chip Device-Parameter Variations with a Differential-Amplifier-Stage Test Circuit", *Proceedings of Synthesis And System Integration of Mixed Information technologies (SASIMI)*, pp. 76–82, 2003.

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iv) D. Navarro, **T. Mizoguchi**, M. Suetake, K. Hisamitsu, H. Ueno, M. Miura-Mattausch, H. J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "A Compact Model of the Pinch-off Region of 100nm MOSFETs Based on the Surface-Potential", *The Institute of Electronics, Information and Communication Engineers Transactions on Electronics*, Vol. E88-C, No. 5, pp. 1079–1086, 2005.