博士論文

Analysis and Modeling of Injection Enhanced Insulated Gate Bipolar Transistor for Power Electronic Circuit Simulation

（パワーエレクトロニクス回路シミュレーション用注入加速型IGBTの解析とモデル化）

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(3) Compact Modeling of Injection Enhanced Insulated Gate Bipolar Transistor Optimized Influence of Frequency Dependent.
Takao Yamamoto, Masataka Miyake, Uwe Feldmann, Hans Jürgen Mattausch, and Mitiko Miura-Mattausch
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主論文

ANALYSIS AND MODELING OF INJECTION ENHANCED INSULATED GATE BIPOLAR TRANSISTOR FOR POWER ELECTRONIC CIRCUIT SIMULATION

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF SEMICONDUCTOR
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preface

Power electronics are very frequently used in home electronics and automobile field High performance power devices are keys for advanced power electronic products. Required performances for the power device are low power loss as well as low noise. Here there are several types of power devices developed such as bipolar transistor, DMOS, super junction MOSFET and insulated-gate bipolar transistor (IGBT). Among them IGBT realizes the high current controllability together with the high breakdown voltage of over 500V. Even though IGBT is driven by applied voltage on the gate of the MOSFET part, the main part consists of a bipolar, and thus the low power consumption of the drive circuit can be realized.

Due to the advantage, IGBT has been widely applied for inverter circuits of power electronics. In order to further improve the performance, different IGBT structures have been developed according to different application purposes. The injection-enhanced insulated-gate bipolar transistor (IEGT) has been developed in order to reduce the on-state voltage, enabling a smooth switching waveform (soft switching) in comparison to the conventional IGBT. Abrupt switching (hard switching) causing destruction and noise of circuits is intended to avoid in the automotive application field Fig. 1 shows the schematic structure of IEGT, where one side of the p-base region is floated Therefore structure becomes asymmetric. It is known that this structure induces the injection enhancement effect.

Since IEGT has been utilized for applications where reduced voltage overshoot is required the soft switching of IEGT is well applicable. However, it causes at the same time large switching loss. To optimize the trade-off between the low overshoot and the low energy-loss, accurate circuit simulations valid for investigating the optimization of IEGT is inevitable.

Acknowledgement

This thesis is the result of my years of work in the Ultra Small Devices Engineering Laboratory and DENSO corporation whereby I am accompanied by many people who have shared their time, talent and friendship. I would like to express my deep appreciation to all of them.

To Prof. Mitiko Miura-Mattausch, my research adviser, for her care and guidance throughout the time of visiting to the laboratory and the question by e-mail. Her technical advice and constant encouragement have been very vital to the completion of this work. Miura-sensei gave me a lot of opportunities to participate in conferences and submit papers.

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To Mr. Hiromitsu Tanabe, and Mikimasa Suzuki at DENSO corporation, for their useful discussions about IEGT device structure and confirmatio of the material.

To Mr. Ryotaro Miura and Mr. Yasutaka Sennda who have provided the measurement data on IEGT device switching waveforms for circuit operation.

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Lastly, to my wife, my child Takuto and Hiromu for their moral support and care, to whom I dedicate this work.

I will do my best to reward all the graces and merits I am receiving.

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Chapter 1

Introduction

1.1 Backgrounds

Power electronics are very frequently used in home electronics and automobile field Automobile manufacturers are required to consider environmental problems and to reduce the fuel consumption of their products. The hybrid system(HV) and electric vehicles (EV) are expected as a way to solve the problem which is enabled by advanced development of power electronics product.

Nowadays, many power devices are used for achieving reliable, safe, as well as economic automobiles. High performance power devices are keys for advanced power electronic products. Required performances for the power device are low power loss as well as low noise. Here there are several types of power devices developed such as bipolar junction transistor(BJT) , metal-oxide-semiconductor field-e fect transistor (MOSFET), super junction MOSFET(SJ-MOS) and insulated-gate bipolar transistor (IGBT) as shown Fig. 1.1 and Fig. 1.2. Among them IGBT realizes the high current controllability together with the high breakdown voltage of over 600V [1]. Even though IGBT is driven by applied voltage on the gate of the MOSFET part, the main part consists of a bipolar, and thus the low power consumption of the drive circuit can be realized.

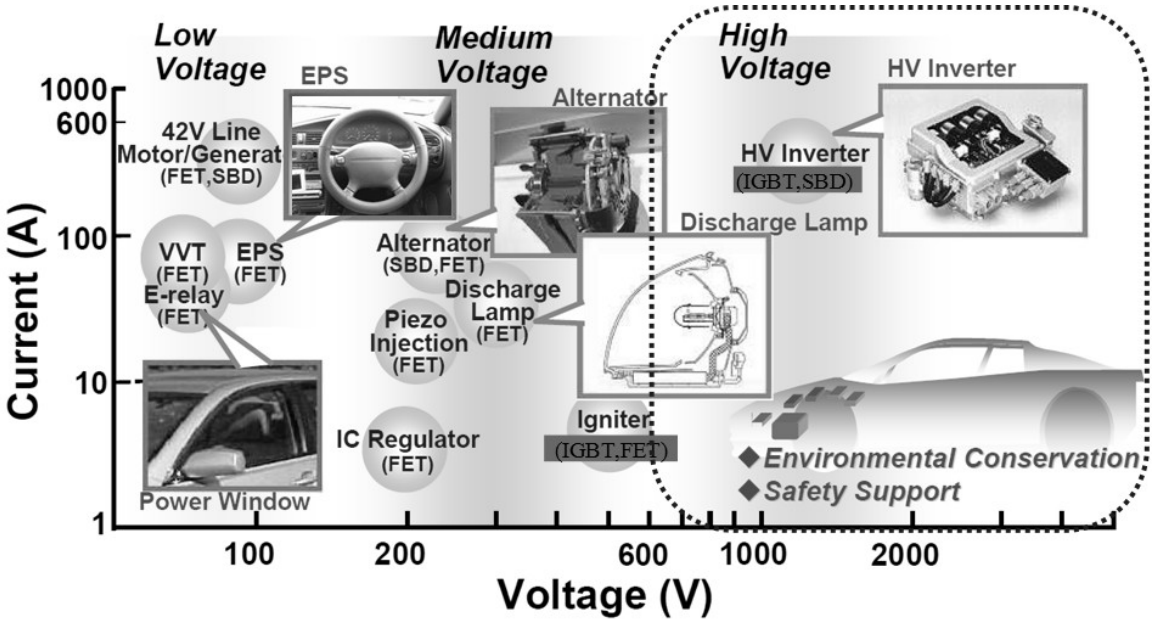

Figure 1.1: Device types and fields

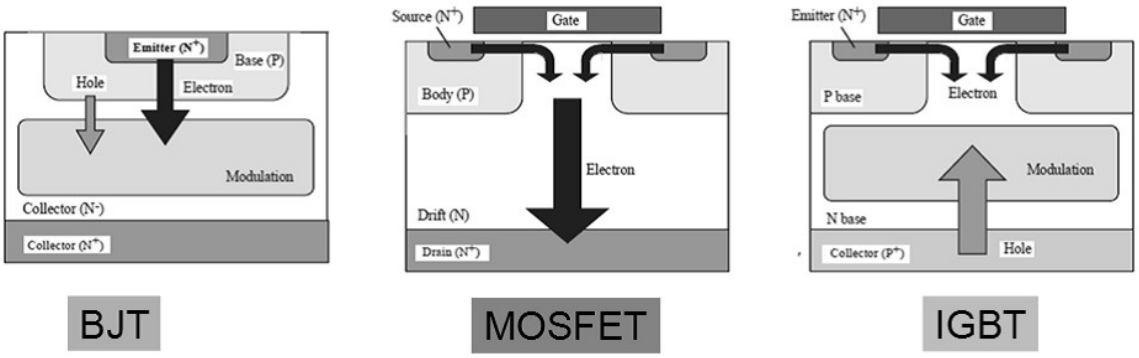

Figure 1.2: Transistor device structure.

Due to the advantage, IGBT has been widely applied for inverter circuits of power electronics [2, 3, 4]. In order to further improve the performance, different IGBT structures have been developed according to different application purposes [5, 6, 7, 8, 9, 10]. The injection-enhanced insulated-gate bipolar transistor (IEGT) has been developed in order to reduce the on-state voltage [11], enabling a smooth switching waveform (gradual slope switching) in comparison to the conventional IGBT [12, 13]. Abrupt switching (hard switching) causing destruction and noise of circuits is intended to avoid in the automotive application field In the automobile application field the noise which cause a bad influenc on other products is disliked. The feature of IEGT structure is having floatin p-base region. IGBT and IEGT have a structurally different portion. It is known that this structure difference induces the injection enhancement effect.

Since IEGT has been utilized for applications where reduced voltage overshoot is required the gradual slope switching of IEGT is well applicable. However, it causes at the same time large switching loss. To optimize the trade-off between the low overshoot and the low energy-loss, accurate circuit simulations valid for investigating the optimization of IEGT characteristics are necessary.

Satisfactory IGBT models are already used for various circuits [14, 15, 16]. However, they are not comprehensive physical models valid for practical circuit designs. Here we developed the compact model HiSIM-IEGT based on the conventional IGBT model HiSIM-IGBT for circuit operation. HiSIM-IGBT has been developed for simulating circuit performance [17, 18, 19], which solves the potential distribution within IGBT explicitly under fully dynamic load conditions, through the surface-potential-based modeling approach including the advanced MOSFET model HiSIM [20, 21, 22]. The main development of HiSIM-IEGT is modeling the hole accumulation in the floating-bas region, which is the origin of the injection enhancement [23]. Since the main advantage of IEGT is the soft switching, our focus is given on the transient characteristics of the hole accumulation phenomenon. For the purpose we analyzed capacitance characteristics in detail. Finally we verify the switching performance of the developed HiSIM-IEGT in comparison to measurements.

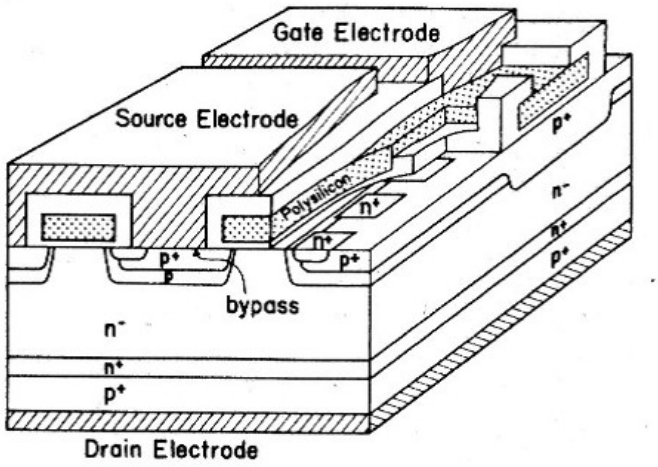

Figure 1.3: Cross section of IGBT structure.

1.2 IGBT Device description

The IGBT is a device which combines the advantages of the BJT and MOSFET. It has many advantageous such as a low on-state resistance, high voltage capability, and a high switching speed along with MOSFET gate controllability. And it has very wide safety operation area (SOA) [1]. These SOA's enable device protection from an abnormally large drain-current surge.

The IGBT has structure which added p-type layer to drain of n-type MOS FET currently used most widely as a power switching element. Gate structure of metal-oxide-semiconductor is common with the MOSFET. There are differences in electrical characteristics.

Figure 1.3 is cross section structure when IGBT is reported for the firs time [1]. The source layer is arranged periodically. It creating low-resistance bypasses for holes to reach the source electrode direct. It becomes unnecessary to bypass under source. And, it works as the shunting resistance for the parasitic n-p-n transistor.

Figure 1.4(a) shows the complicated IGBT structure witch combines a BJT with a MOSFET for base-current switching.

I will explain the switching operation easily. Turn-ON the MOSFET on the upper

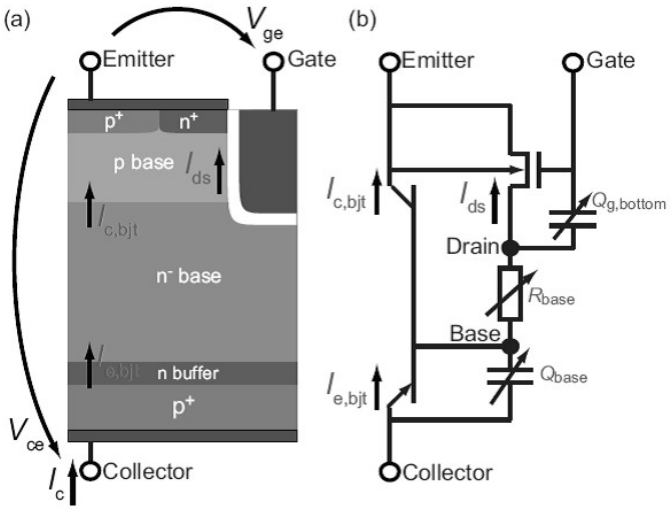

Figure 1.4: (a) Schematic cross-section of half cell unit of IGBT.(b) The conceptual model framework of HiSIM-IGBT.

surface when a positive voltage is applied between the emitter electrodes and the collector electrode, PN junction diode on the lower surface is forward biased, the n-base layer is modulated conductivity holes injected from the p+ layer. Because the hole exists in the n-base layer, it is necessary to discharge the carriers accumulated in the drift layer when the turn-off. The hole current continues to fl w even after the turn-off. It is called tail current and it is the characteristic of the device which carries out bipolar operation. Since it has PN junction in the collector side, ON voltage is certainly overlapped on junction potential (about 0.6V). For this reason, for those of a MOSFET I_{c} rises from $V_{\mathrm{d}} = 0V$ becomes advantageous in the area of low-voltage, IGBT is used in applications that require high breakdown voltage of over 600V.

1.3 Existing compact IGBT model

HiSIM-IGBT model was consists of two transistors, MOSFET and BJT. It was modeled for circuit simulations [e.g., 1.4(b)]. The MOSFET supplies the base current for the BJT part. A surface-potential-based model for high-voltage MOSFET HiSIM HV is applied

as the MOSFET part. HiSIM-IGBT's BJT part captures four specifi features. One is the trench-bottom MOSFET gate charge $Q_{\mathrm{g,bottom}}$ which forms a large Miller capacitance during switching operations. The second one is the base resistance R_{base} which determines the IGBT on-state voltage drop. Device-structural parameters, from which above features originate, are taken into account as summarized in Fig. 1.5.

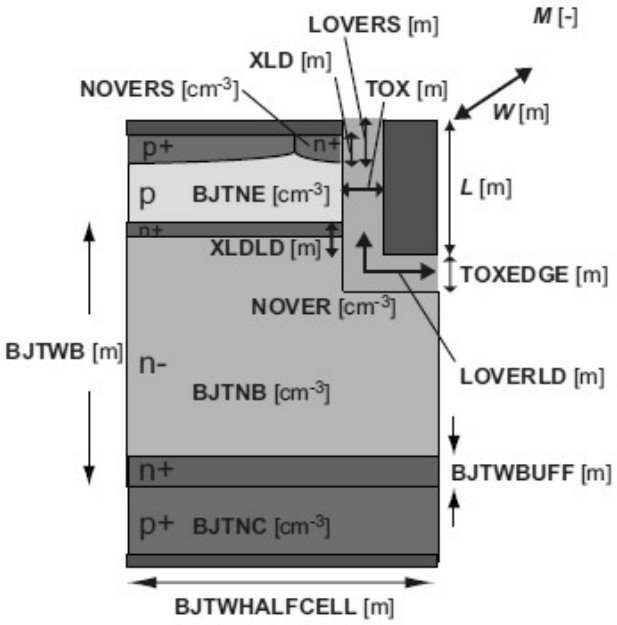

Figure 1.5: Parameter mapping of HiSIM-IGBT.

The normal IGBT structure has 3 terminals. The terminal ware called Collector, Emitter, and Gate. HiSIM-IGBT considers 4 terminals, Collector, Emitter, Gate, and Base(Fig. 1.6). The reason is that HiSIM-IGBT has been developed based-on the HiSIM's MOSFET-model framework. And combined the MOSFET model and BJT model. The circuit diagram of HiSIM-IGBT is shown in Fig. 1.7. In addition to the main 3 external terminals, four nodes (b, b', c', e') are considered to describe all important features of IGBT.

Figure 1.6: HiSIM-IGBT terminal.

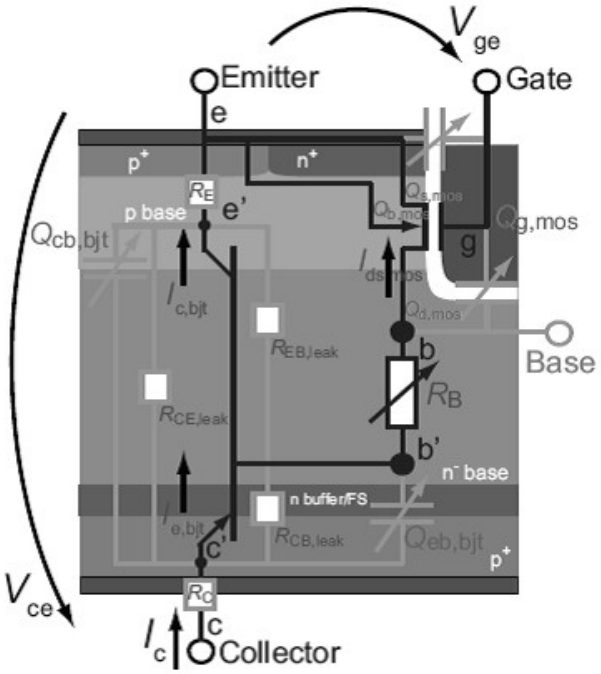

Figure 1.7: Circuit diagram inside the HiSIM-IGBT model.

1.3.1 MOS Part

There are many variety of MOS model [24, 25, 26, 27]. A surface-potential-based model for high-voltage MOSFET HiSIM-HV model is applied as the MOSFET part [28]. Its source and bulk terminals are connected together and are named as the emitter terminal. The drain terminal is connected to the base node within the IGBT framework. MOS part

is a trigger for IGBT operation. MOSFET part is compact model developed based on the drift-diffusion approximation. The important part in this model are the surface potential at the source and drain nodes. The surface potentials are calculated iteratively using Poisson equation as a function of applied voltage.

The MOSFET drain current I_{ds} as expressed in terms of the quasi-Fermi potential ϕ_S is given by

$$I_{\mathrm{ds}} = W q \mu_{\mathrm{eff}} n(y) \frac{d\phi_{\mathrm{f}}}{dy} \tag{1.1}$$

where μ_{eff} is effective carrier mobility, $n(y)$ is carrier density at position y along the channel. The Fermi potential expressed in surface potential ϕ_s is

$$\frac{d\phi_s}{dy} = \frac{d\phi_{\mathrm{s}}(y)}{dy} + \frac{1}{\beta} \frac{d \ln n(y)}{dy} \tag{1.2}$$

Substituting Eq. (1.1) to (1.2) gives a current equation which consists of two terms

$$I_{\mathrm{ds}} = W q \mu_{\mathrm{eff}} n(y) \left(\frac{d\phi_{\mathrm{s}}(y)}{dy} + \frac{1}{\beta} \frac{d \ln n(y)}{dy} \right) \tag{1.3}$$

The firs term denotes the drift current which is carrier fl w due to the electric fiel along the channel. The second term denotes the diffusion current which exists due to a difference in charge concentration gradients. Charge diffuse from regions of high charge concentration to low concentration giving rise to electric current.

The charge-sheet approximation assumes that the inversion charges are located at the Si surface like a sheet of charge and that there is no potential drop.The total charge density Q_{s} in the channel at position y is

$$Q_{\mathrm{s}}(y) = Q_{\mathrm{b}}(y) + Q_{\mathrm{i}}(y) \tag{1.4}$$

where $Q_{\mathrm{b}}(y)$ is bulk charge density and $Q_{\mathrm{i}}(y)$ is the inversion charge density.

By applying the Gauss law, the charge density induced in the substrate is derived from the Poisson equation

$$
\begin{aligned}
(Q_{\mathrm{b}}(y) + Q_{\mathrm{i}}(y)) &= C_{\mathrm{ox}}(V'_{\mathrm{G}} \quad \phi_{\mathrm{s}}(y)) \\
&= \sqrt{\frac{2\epsilon_{\mathrm{Si}} q N_{\mathrm{sub}}}{\beta}} \Big[\exp\big\{\beta(\phi_{\mathrm{s}}(y) \quad V_{\mathrm{bs}})) + \beta(\phi_{\mathrm{s}}(y) \quad V_{\mathrm{bs}}) \\
&\quad 1 + \frac{n_{\mathrm{p0}}}{p_{\mathrm{p0}}} (\exp(\beta(\phi_{\mathrm{s}}(y) \quad \phi_{\mathrm{f}}(y))) \\
&\quad \exp(\beta(V_{\mathrm{bs}} \quad \phi_{\mathrm{f}}(y))\big\}\Big]^{0.5}
\end{aligned}
\tag{1.5}
$$

$$
C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{T_{\mathrm{ox}}} \tag{1.6}
$$

$$
V'_{\mathrm{G}} = V_{\mathrm{gs}} \quad V_{\mathrm{fb}} + \Delta V_{\mathrm{th}} \tag{1.7}
$$

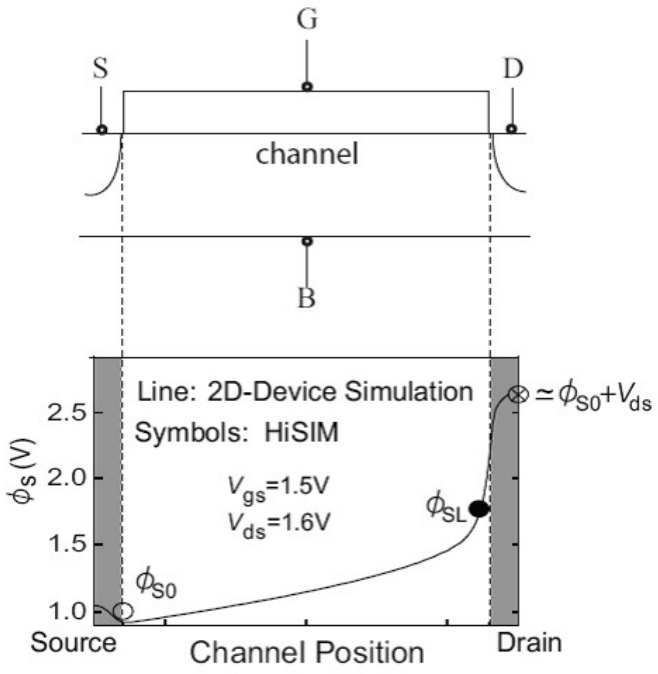

Figure 1.8: The surface potential distribution in the MOSFET channel.

$$\beta = \frac{q}{kT} \tag{1.8}$$

where Q_b(y) is the bulk charge density along the channel, Q_i(y) is the inversion charge density, and ϕ_f (y) takes a value between 0 and V_{ds}. V_{fb} is the flat-ban voltage, T_{ox} is the gate-oxide thickness, and ΔV_{th} is the threshold voltage shift due to the short-channel effect. ϵ_{Si} and N_{sub} are the silicon permittivity and the substrate impurity concentration, respectively. The electron charge is denoted by q. The Boltzmann constant and the lattice temperature in Kelvin are k and T, respectively.

HiSIM-IGBT describes the trench-bottom nonlinear MOS capacitance with the surface-potential-based approach.The trench-bottom gate-overlap charge equation is written with the calculated ϕ_S as

$$Q_{\mathrm{g,bottom}} = W_{\mathrm{eff}} \cdot L_{\mathrm{overLD}} \cdot \left(\sqrt{\frac{2\epsilon_{\mathrm{Si}} q N_{\mathrm{over}}}{\beta}} \sqrt{\beta(\phi_{\mathrm{S}} + V_{\mathrm{ds}} \quad 1} \right) \tag{1.9}$$

under the depletion and the accumulation conditions, and

$$Q_{\mathrm{g,bottom}} = W_{\mathrm{eff}} \cdot L_{\mathrm{overLD}} \cdot C_{\mathrm{ox,edge}} \; V_{\mathrm{gs}} \quad V_{\mathrm{fb,over}} \quad \phi_{\mathrm{S}} \big) \tag{1.10}$$

under the inversion condition, where $C_{ox,edge} = \epsilon_{ox}/T_{ox,edge}$. Here $T_{ox,edge}$ and L_{overLD} are the oxide thickness and the oxide length of the trench-bottom region, respectively. N_{over} and $V_{fb,over}$ are the base impurity concentration near the trench-bottom region and the flat band voltage for the overlap MOS structure, respectively.

The charge density is calculated by the Poison equation as

$$\frac{d^2\phi_{\mathrm{s}}(y)}{dy^2} = \quad \frac{q}{\epsilon_{\mathrm{Si}}} \big[p_{\mathrm{p0}} \; exp(\beta_{\phi \mathrm{f}} \quad 1) \big) \quad n_{\mathrm{p0}} \; exp(\beta_{\phi \mathrm{f}} \quad 1) \big) \big] \tag{1.11}$$

where p_{p0} is the density of holes and n_{p0} is the density of electrons in the p-region at thermal equilibrium.

The calculate result of Eq. (1.5) leads to electric fiel ε along the lateral direction

$$\begin{aligned}\varepsilon(y) &= \frac{d^2\phi_{\rm s}(y)}{dy^2} \\ &= \pm\frac{\sqrt{2}kt}{qL_{\rm D}}\Big[\ exp(\beta(\phi_{\rm s}(y) \quad V_{\rm bs})) + \beta(\phi_{\rm s}(y) \quad V_{\rm bs}) \quad 1\Big) \\ &+ \frac{p_{\rm p0}}{n_{\rm p0}}\ exp(\beta(\phi_{\rm s}(y) \quad \phi_{\rm f}(y))) + exp(\beta\phi_{\rm s}(y) \quad \phi_{\rm s}(y) \quad \phi_{\rm f}(y))\Big)\Big]^{0.5}\end{aligned} \tag{1.12}$$

Using Gauss'theorem, Q_s becomes

$$\begin{aligned}Q_{\rm s}(y) &= \epsilon_{\rm Si}\varepsilon_{\rm s} \\ &= qN_{\rm sub}L_{\rm D}\Big[\ exp(\quad \beta(\phi_{\rm s} \quad V_{\rm bs})) + \beta(\phi_{\rm s} \quad subVbs) \quad 1\Big) \\ &+ \frac{p_{\rm p0}}{n_{\rm p0}}\ exp(\beta(\phi_{\rm s}(y) \quad \phi_{\rm f}(y))) + exp(\beta\phi_{\rm s}(y) \quad \phi_{\rm s}(y) \quad \phi_{\rm f}(y))\Big)\Big]^{0.5}\end{aligned} \tag{1.13}$$

1.3.2 BJT Part

The BJT part is a point for determining a current characteristic of the IGBT. Voltage drop at the forward p/n junction $V_{eb,bjt}$ (the potential difference between the collector and base nodes, which are originally between the emitter and the base in BJT) is the most important physical variable in HiSIM-IGBT. $V_{eb,bjt}$ is calculated by a circuit simulator based on the circuit diagram inside the model shown in Fig. 1.7.

$$V_{\rm eb,bjt} = V(c', b') \tag{1.14}$$

$$V_{\rm cb,bjt} = V(e', b') \tag{1.15}$$

The BJT current equations in HiSIM-IGBT are modeled with the BJT junction potentials (V_{eb} and V_{cb}) [42]. Those junction potentials are iteratively calculated by the circuit simulator with the equivalent circuit shown in Fig. 1 1.4(b). Our specifi effort is given on calculating accurate potential values by modeling of the base resistance.

The base resistance plays an important role for the functionality of an IGBT [43]. Based on a simplifie carrier distribution approximated by an exponential function of the distance from the c/b junction, the base resistance in HiSIM-IGBT is modeled as

$$\begin{aligned} R_{\mathrm{base}} &= \frac{1}{qA(\mu_{\mathrm{BJT,n}}+\mu_{\mathrm{BJT,p}})}\int_0^{W_{\mathrm{base}}}\frac{1}{p_{\mathrm{base}}(y)}dy \\ &= \frac{1}{qA(\mu_{\mathrm{BJT,n}}+\mu_{\mathrm{BJT,p}})}\cdot\left[\frac{L_{\mathrm{dec}}}{p_{\mathrm{min}}}\cdot ln\ \ p_{\mathrm{inj}}+p_{\mathrm{min}}\cdot exp\ \ \frac{y}{L_{\mathrm{dec}}})\right)\right]_0^{W_{\mathrm{base}}} \\ &= \frac{1}{qA(\mu_{\mathrm{BJT,n}}+\mu_{\mathrm{BJT,p}})}\cdot\frac{L_{\mathrm{dec}}}{p_{\mathrm{min}}} \\ &\cdot\left\{ln\ \ p_{\mathrm{inj}}+p_{\mathrm{min}}\cdot exp\ \ \frac{W_{\mathrm{base}}}{L_{\mathrm{dec}}})\right) \quad ln(p_{\mathrm{inj}}+p_{\mathrm{min}})\right\} \end{aligned} \tag{1.16}$$

Here the hole density at the c/b junction ($y = 0\mu m$) is written as $p_{\mathrm{inj}} = p_{\mathrm{n0,b}}exp(\frac{qV_{\mathrm{cb}}}{kT})$. $\mu_{BJT,n}$ and $\mu_{BJT,p}$ are the electron and hole mobilities, respectively.

$$\mu_{BJT,n} = \mathrm{BJTMUEN}\Big(\frac{W_{\mathrm{qn}}}{\mathrm{BJTWB}}\Big)^{\mathrm{BJTMUEQN}} \tag{1.17}$$

$$\mu_{BJT,p} = \mathrm{BJTMUEP}\Big(\frac{W_{\mathrm{qn}}}{\mathrm{BJTWB}}\Big)^{\mathrm{BJTMUEQN}} \tag{1.18}$$

The base charge is also modeled as

$$\begin{aligned} Q_{\text{base}} = & \quad qA \int_0^{W_{\text{base}}} p_{\text{base}}(y)dy \\ = & \quad qA \left[\quad L_{\text{dec}} p_{\text{inj}} exp \quad \frac{y}{L_{\text{dec}}}) + p_{\text{min}} \cdot y \right]_0^{W_{\text{base}}} \\ = & \quad qA \left\{ \quad L_{\text{dec}} p_{\text{inj}} \cdot \left[exp \quad \frac{W_{\text{base}}}{L_{\text{dec}}}) \quad 1 \right] + p_{\text{min}} \cdot W_{\text{base}} \right\} \end{aligned} \tag{1.19}$$

Depletion charge in the base at the emitter side is modeled as

$$Q_{\text{dep}} = q \cdot N_{\text{base}} \cdot A \cdot W_{\text{dep}} \tag{1.20}$$

where W_{dep} is the depletion width measured from the e/b junction, which is a function of V_{eb}.

The carrier distribution model is introduced especially for better modeling capability of the punch-through type IGBT. Carrier distribution is separated into three regions, the depletion region, the quasi-neutral region and the buffer/FS region as shown Fig. 1.9.

$$f(x) = \begin{cases} p_{\min} \cdots (depletionregion) \\ p_{\text{inj}} \cdot exp\left(\dfrac{x}{L_{\text{dec}}} \right) + \text{BJTNB} \cdots (quasi \quad neutralregion) \\ p_{\text{inj,buff}} \cdot exp\left(\dfrac{x + \text{BJTWBUFF}}{L_{\text{buff}}} \right) \cdots (buffer/FSregion) \end{cases} \tag{1.21}$$

where

$$depletionregion : 0 \leq \text{BJTWB} \quad x \leq W_{\text{dep}} \tag{1.22}$$

$$quasi \quad neutralregion : W_{\text{dep}} < \text{BJTWB} \quad x < \text{BJTWB} \tag{1.23}$$

$$buffer/FSregion : \text{BJTWB} \leq \text{BJTWB} \quad x \leq \text{BJTWB} + \text{BJTWBUFF} \tag{1.24}$$

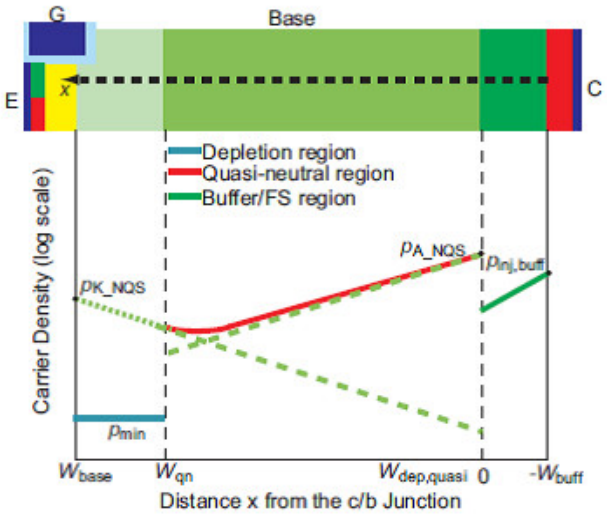

Figure 1.9: Schematic of the 1D excess-carrier distribution.

1.4 Purpose of This Research

The purpose of this study is analyze the characteristic of IEGT structure using 2D-device structure, and extending the HiSIM-IGBT model.
The novel proposals to approach the purpose are as follows.

1. The floating-bas effect is investigated by 2D-device simulations. To investigate the internal behavior by focusing on the capacitor characteristics.
2. To develop a model of the floating-bas structure that include capacitance and potential mechanism.
3. To implement the floating-bas model into HiSIM-IGBT model and verify the simulation result.
4. To investigate influenc of frequency dependence to total gate capacitance.
5. To verify the switching wave form by comparing with experimental result data and the simulation result using new develop model.

This thesis consists of 5 chapters.

Chapter 2 (Analysis of Floating-Base Structure) reviews the analysis result of the capacity characteristics which floating-bas structure causes. The potential change of the floating-bas part and the relation of hole accumulation is presented.

In **Chapter 3** (Floating-Base structure modeling (HiSIM-IEGT)) , the modeling of the floating-bas structure is described. The potential of floating-bas region is calculated by the relation between the collector current I_{c}. And, hole accumulation is expressed as a n-MOS capacitor.

Chapter 4 (HiSIM-IEGT Model Optimized Influenc of Frequency Dependence) presents influenc of frequency dependence for gate capacitance. And, the Non-Quasi-Static (NQS) effect model implement in new develop HiSIM-IEGT model based on the carrier transient delay.

Chapter 5 (Conclusion) summarizes of this thesis and the plans for further development.

Appendix A (NQS model formulation) gives the equivalence of the NQS charge formulation to a differential rate equation.

Chapter 2

Analysis of Floating-Base Structure

2.1 Motivation

Satisfactory IGBT models are already used for various circuits. However, they are not comprehensive physical models valid for practical circuit designs. HiSIM-IGBT has been developed for simulating circuit performance, which solves the potential distribution within IGBT explicitly under fully dynamic load conditions, through the surface-potential-based modeling approach including the advanced MOSFET model HiSIM. However, it considers the symmetrical trench-type IGBT structure, where both sides of the p-base are connected to the emitter.

Figure 2.1 shows the studied basic circuit with its element values. Measurements and results with HiSIM-IGBT developed for the symmetrical structure are compared in Fig. 2.2. The threshold voltage of the studied IGBT is 6.5 V, and the model parameter values of HiSIM-IGBT were extracted from the measured I_c.V_{ce} characteristics. It was observed that the measured waveform of the collector current I_c is not steep for IEGT, and soft switching is realized.

On the contrary, the model calculation result with HiSIM-IGBT shows no soft switching. Since the simulation result shows a clear deviation from the measured waveform, it appears that the loss calculation error is large, as shown in Fig. 2.3. It is not suitable for the switching prediction of the energy loss.The difference between the measured and

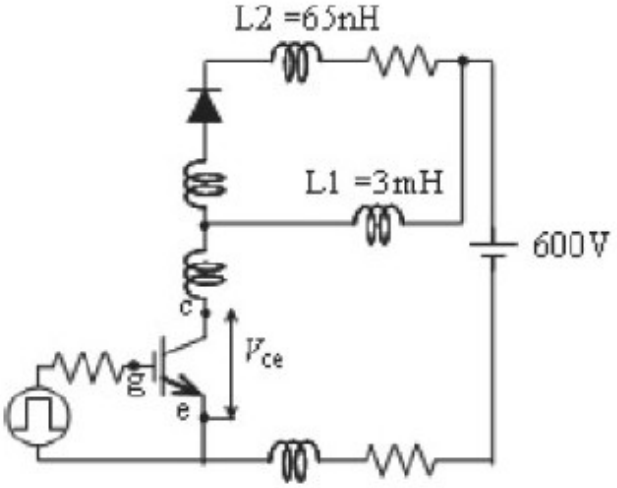

Figure 2.1: Studied basic circuit and its element values.

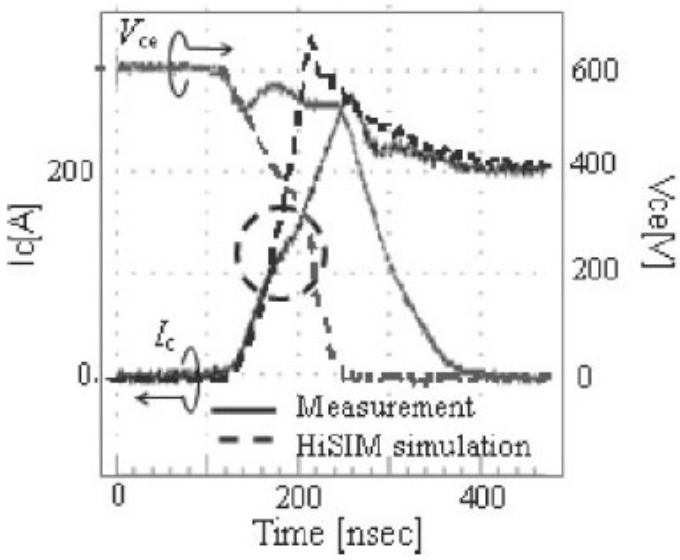

Figure 2.2: Measured transient characteristics in comparison with simulation results with original HiSIM-IGBT. (Wave form)

calculated waveforms is attributed to the floating-bas effect, which is not yet considered

in HiSIM-IGBT. The purpose of this investigation is to extend HiSIM-IGBT for the asymmetrical IEGT structure, where one side of the p-base is disconnected and floated For this purpose, we analyzed capacitance characteristics in detail.

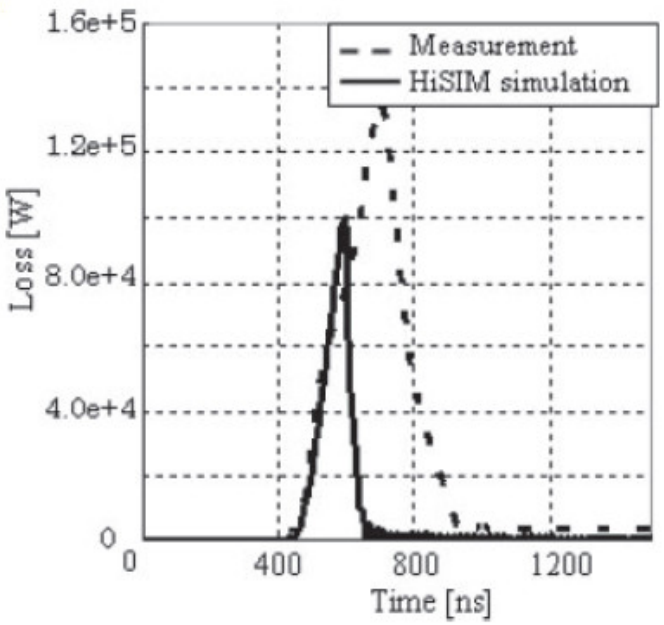

Figure 2.3: Measured transient characteristics in comparison with simulation results with original HiSIM-IGBT. (Switching loss)

2.2 IEGT structure

Figure 2.4 shows the symmetrical trench-type IGBT structure where both sides of the p-base are connected to the emitter and the asymmetrical trench-type IGBT structure.

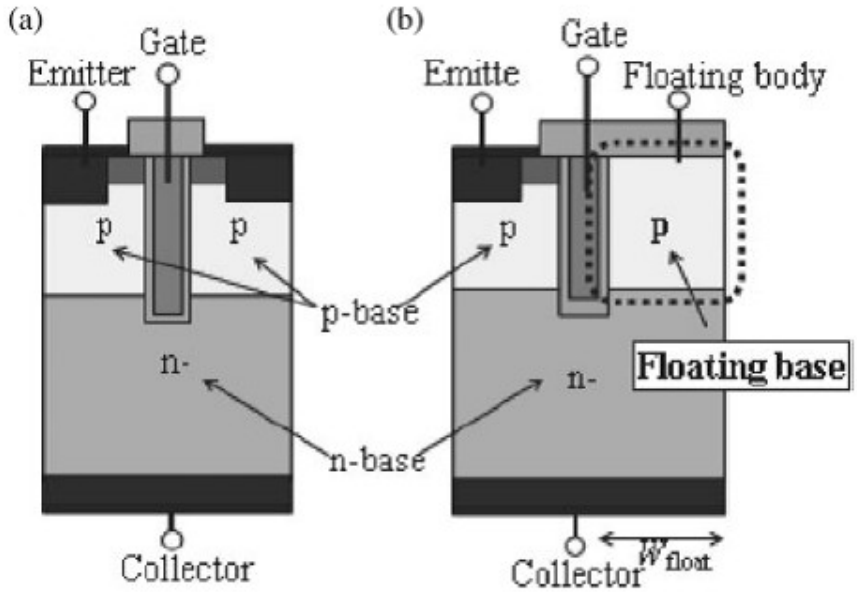

Figure 2.4: Comparison of two IGBT structures: (a) symmetrical IGBT and (b) asymmetrical IEGT.

2.3 Switching Wave Form IGBT and IEGT

It was observed that the measured waveform of the collector current I_c of the IEGT is not as steep as that of the IGBT, and thus a softer switching behavior is observed as shown by a dashed circle. However, the circuit simulation result with HiSIM-IGBT for the symmetrical structure shows no soft switching. The difference between the measured and calculated waveforms is attributed to the floating-bas effect, which is not yet considered in HiSIM-IGBT.

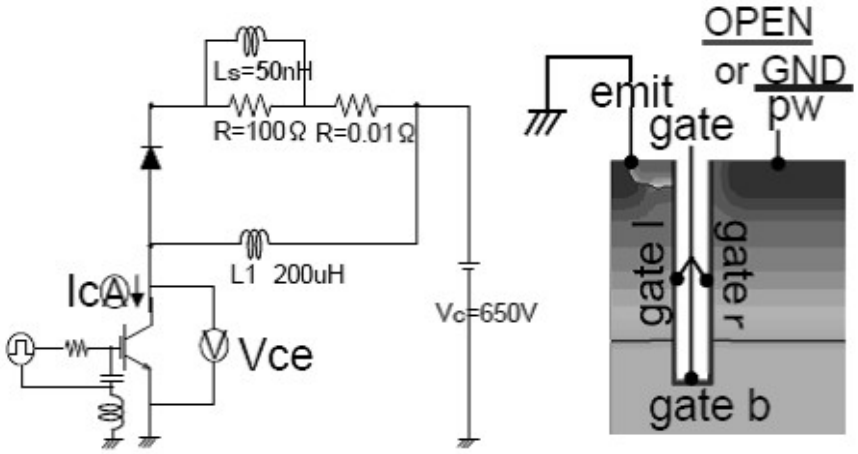

Figure 2.5: Simulation circuit and simulation structure

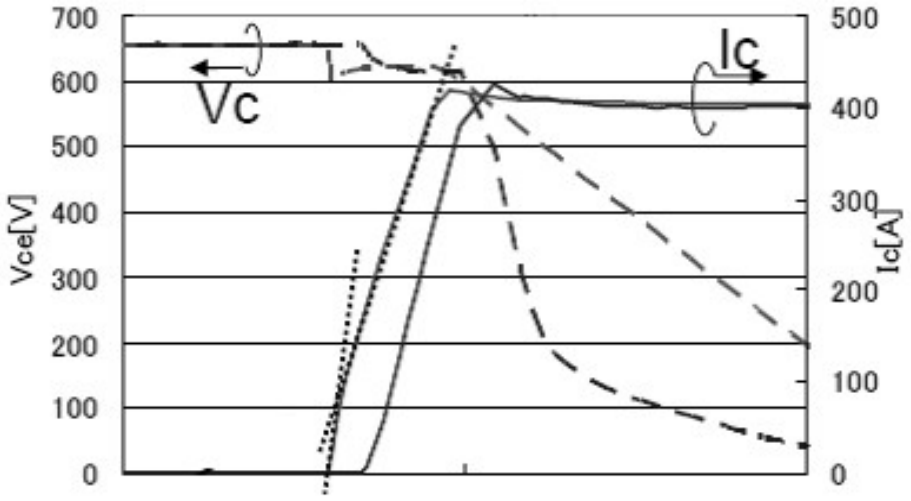

Figure 2.6: Comparison with open condition and short condition

2.4 2D Device Simulation Result

The floating-bas effect is investigated with 2D evice simulations [29]. Fig. 2.7 depicts separate contributions from different parts of the gate oxide to the total C_{gg}. The gate oxide divides into three parts, Namely, the gate oxides are divided into three parts, the emitter

side (Gate l), the bottom region (Gate b) and the floating-bas side (Gate r). Fig. 2.8 shows gate capacitance measurement circuit. It has measured on the conditions near static condition.

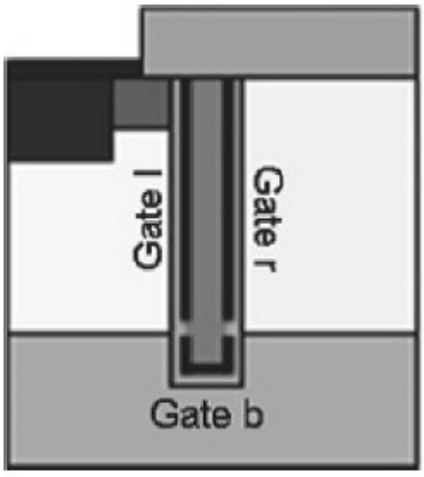

Figure 2.7: The gate contact is divided into different contributions.

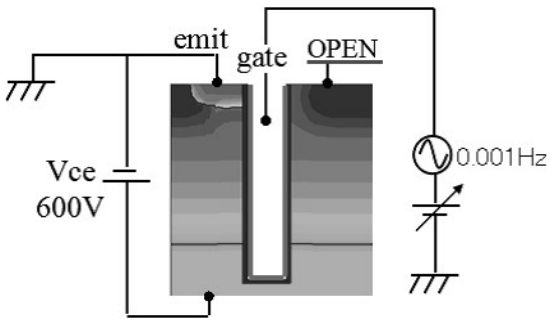

Figure 2.8: Capacitance measurement circuit.

Through the increase of V_{ge} induces the inversion condition, which causes the positive C_{gg} as shown in Fig. 2.10. It can be seen that the negative C_{gg} of the floatin base (Gate r) dominates the total C_{gg} [30, 31, 32] as shown in Fig. 2.9, and that the positive C_{gg} induced on Gate l is negligible.

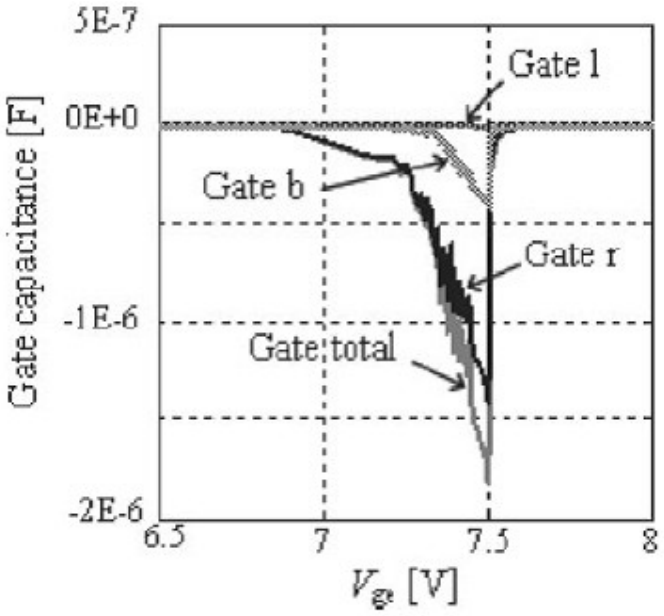

Figure 2.9: 2D device simulation result of gate capacitance for floating-bas structure at Vce = 600 V, frequency = 0:001 Hz, and V_{ge} sweep.

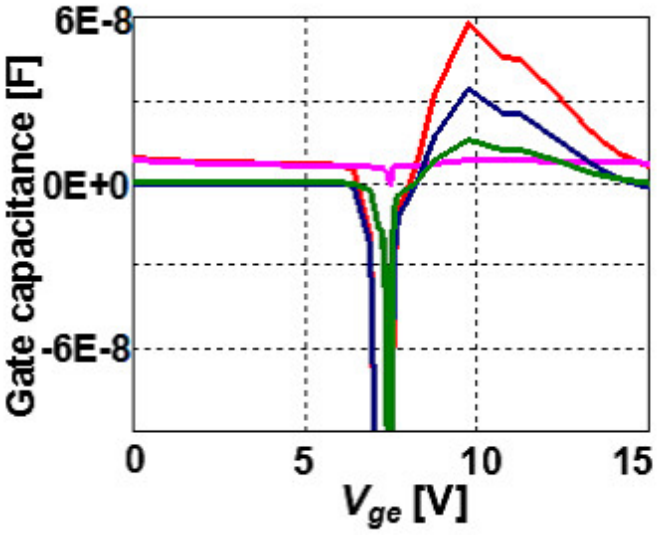

Figure 2.10: The expansion of C_{gg}.

Fig. 2.11 depicts 2D device simulation results of I_c and the gate current under the turn-on condition. For the gate current contributions from different parts are depicted separately. It is seen that the negative current fl ws in the floating-bas side (Gate r) at the beginning stage of the collector current fl w. This negative current is the origin of the negative capacitance of C_{gg}. By switching on the gate the collector current starts to fl w due to the electron injection from the emitter. This causes the positive C_{gg} at Gate l. The collector current fl w induces the hole accumulation underneath Gate r. This is the origin of the negative C_{gg}. Thus our focus is given on modeling the negative C_{gg}.

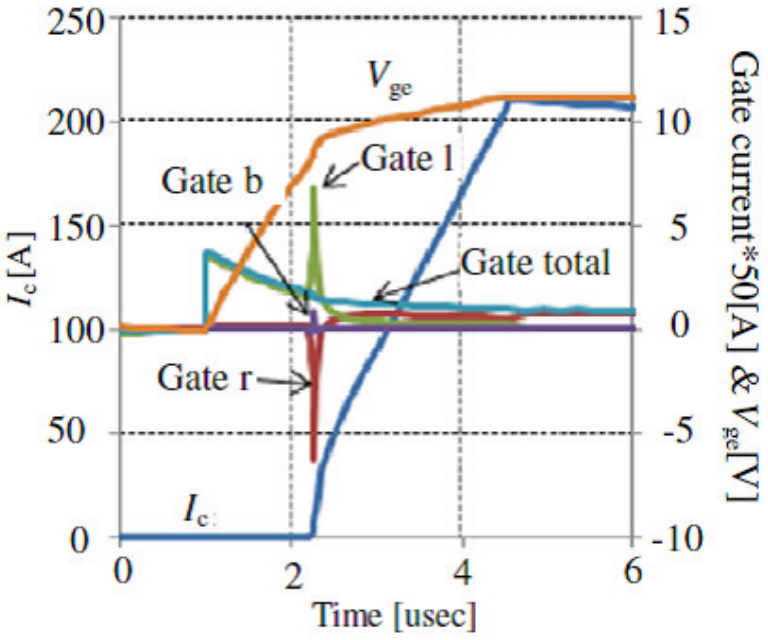

Figure 2.11: 2D device simulation result of I_c and different gate currents switch turn-on condition. (current rise rate:di/dt=82.5A/us)

2.4.1 Hole Accumulation

Figure 2.12 shows equi-hole-density contours. When V_{ge} reaches the threshold voltage (V_{ge} 6.5 V), the contacted p-base side forms the depletion layer as well as the inversion layer under the gate as can be seen from the low hole concentration. On the other hand,

the hole-density contours on the floating-bas side remain nearly unchanged, except in the depletion region at the n-/p-base junction, which is fille with holes injected from the collector for V_{ge} Vth. The potential distribution along the cross section shown by line A is depicted in Fig. 5. It is clearly seen that the contacted-base side forms the inversion layer and the non contacted side forms the accumulation layer.

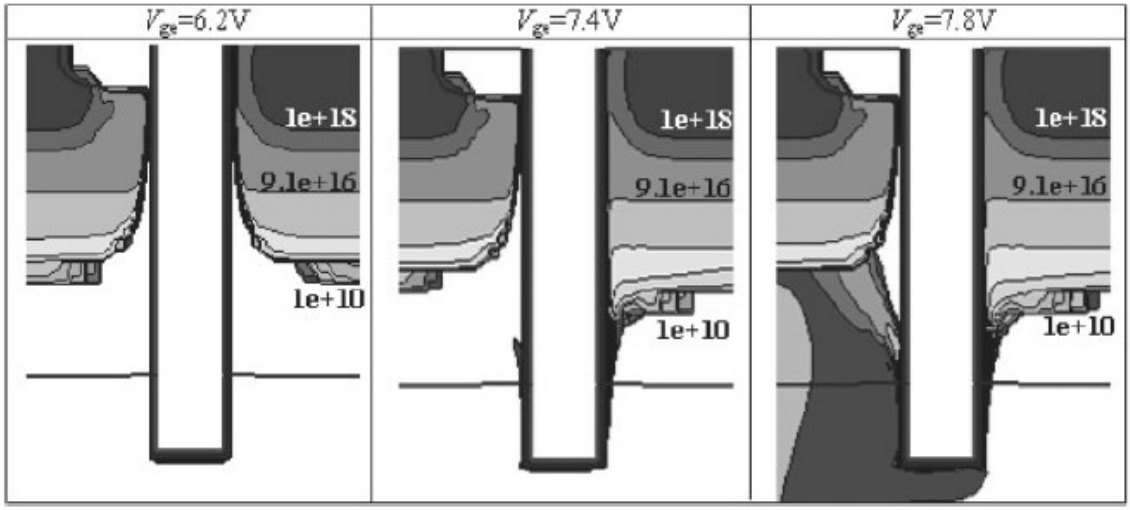

Figure 2.12: Simulated electrostatic potential around the gate (V) (V_{ce} = 600 V).

2.4.2 Potential Transition

The floating-bas effect is investigated by two-dimensional (2D) device simulations.16) Figure 2.13 shows electrostatic potential contours for different gate voltage V_{ge} values around the trench gate oxide for the same conditions as shown in Fig. 2.12. In the $V_{ge} \rangle$ Vth case, the potential distributions in the emitter-connected and floatin bases are nearly the same. However, the gate control becomes completely different between the two structures under the $V_{ge} \langle$ Vth condition when I_c begins to fl w. Under this condition, the potential value on the floating-bas side becomes even higher than V_{ge}. However, the potential value does not exceed 24.8V in the studied case, even with a further increase in V_{ge}.

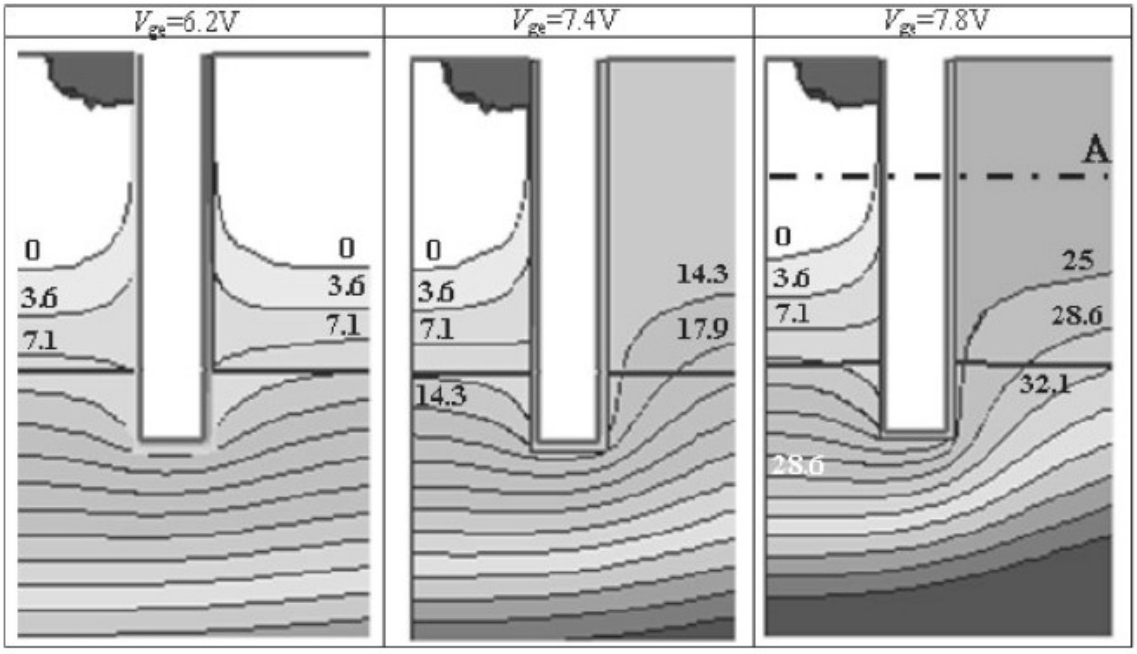

Figure 2.13: Simulated hole-density distributions around the gate (/cm3) (V_{ce} = 600 V).

2.4.3 Collector Current and Floating-Base Potential

The potential distribution along the cross section shown by line A(see Fig. 2.13) is depicted in Fig. 2.14. It is clearly seen that the contacted-base side forms the inversion layer and the non contacted side forms the accumulation layer. Beyond the threshold condition, the collector current fl ws into the floating-bas region as well and fill the entire region with holes. This hole injection into the floatin base is terminated after a certain number of holes occupy the region. It can be concluded that the floating-bas potential shown in Fig. 2.13 is determined by a balance created by carrier dynamics responding to the potential distribution within the entire IEGT. The carrier response to the potential change can be investigated with the capacitance.

Figure 2.15, 2.16 shows a comparison of the 2D numerical simulation results of C_{gg} for IEGT and IGBT. The humps around V_{ge} 10V observed for both structures are due to the resistive base effect under the on-current condition usually observed for power devices. A clear difference between the two structures is the sharp negative C_{gg}, which is observed only for the IEGT structure.

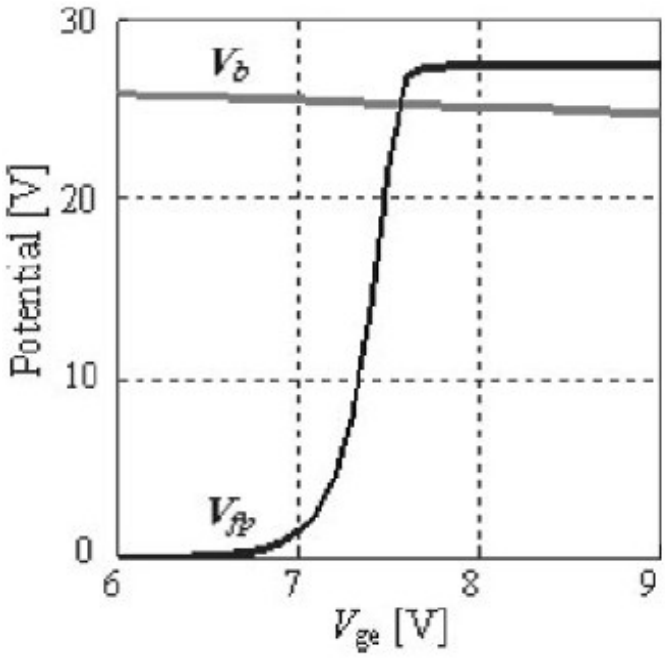

Figure 2.14: Potential distribution of line A.

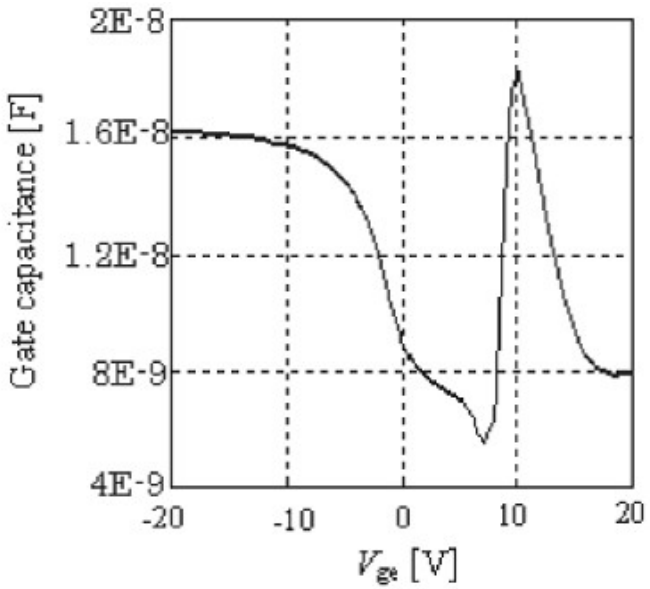

Figure 2.15: 2D device simulation of C_{gg}. The IGBT structure.

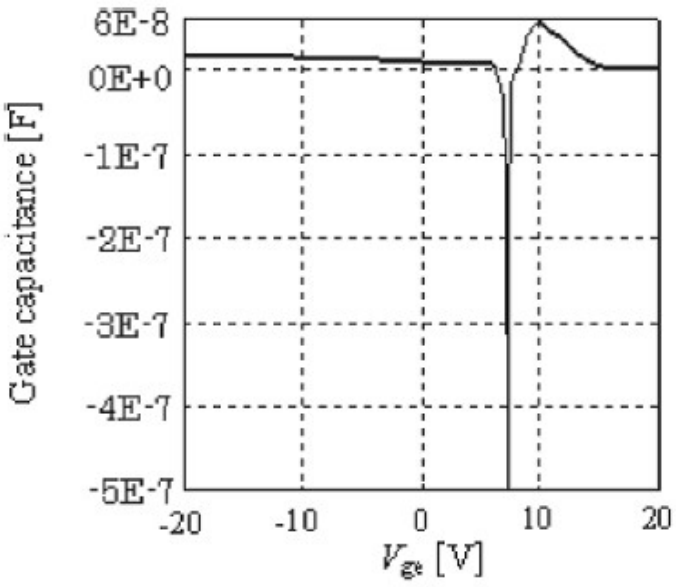

Figure 2.16: 2D device simulation of C_{gg}. The IEGT structure.

2.5 Influenc of Gate Capacitance

The origin of the ‘negative capacitance’ is attributed to the hole accumulation in the floatin base [30, 31, 32]. To model the charge distribution at Gate r, a potential node V_{fp} is investigated. The node is set at the surface of the floatin base as shown in Fig. 2.4. Figure 2.17 shows the relationship among different values as a function of $V_{\rm ge}$. Beyond $V_{\rm ge} \geq V_{\rm th}$, the collector current increases, accompanied by the reduction in C_{gg}. At $V_{\rm ge} \geq$ 7.5 V, C_{gg} increases abruptly, which coincides with the start of the saturation of the floating-bas potential V_{fp}. As can be seen in Fig. 2.14, the start of V_{fp} saturation is attributed to the condition where the potential in the floatin base becomes higher than the upside potential of the n-base region V_b. However, the increase is stopped when V_{fp} exceeds V_b. Figure 2.19 shows the width [W_{float}: see Fig. 2.18] dependence of C_{gg}. Although the increase in W_{float} does not affect C_{gg}, the W_{float} reduction results in the V_{ge} shift to higher values. The total number of injected holes into the floating-bas region is reduced with a reduced W_{float}. This requires the V_{ge} increase to realize V_{fp} larger than V_b.

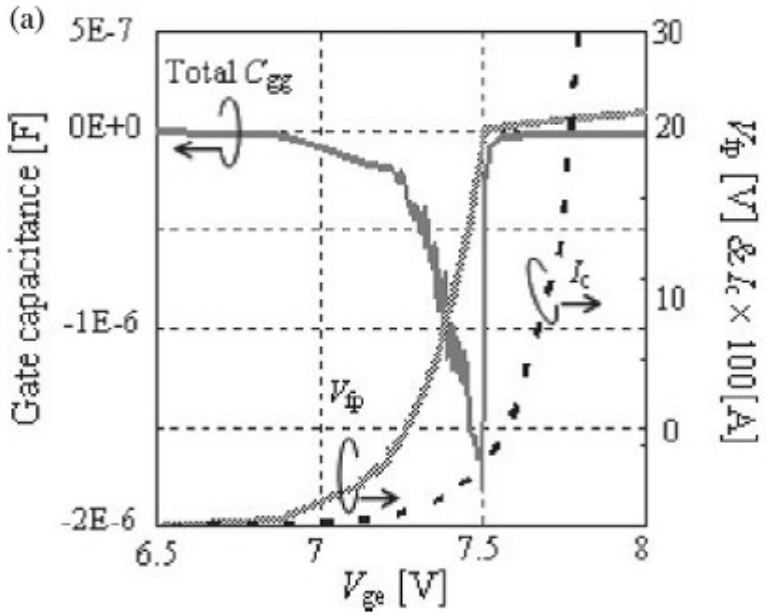

Figure 2.17: 2D device simulation results of $C_{\rm gg}$, floating-bas voltage, and Ic current for floating-bas structure.

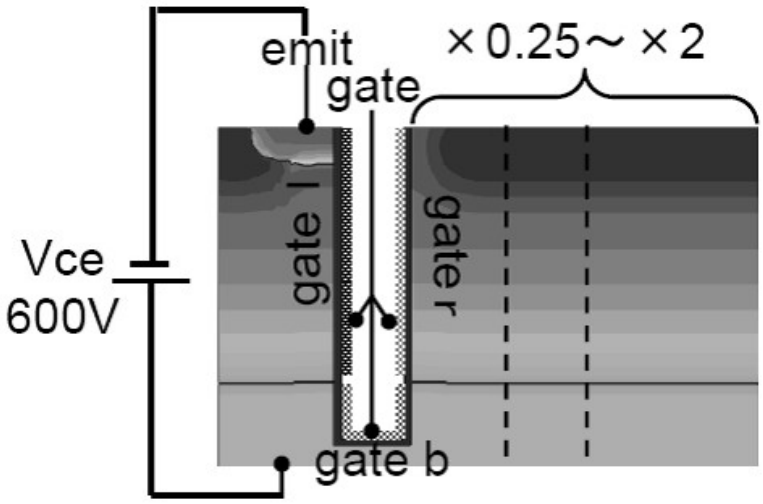

Figure 2.18: 2D device simulation model of width length difference.

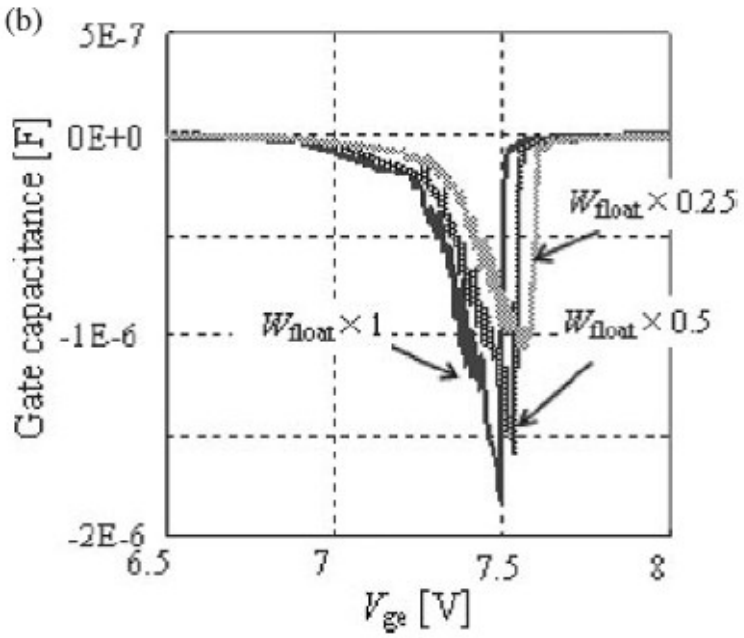

Figure 2.19: 2D device simulation result of the width (W_{float}) dependence of C_{gg}.

Chapter 3

Floating-base structure modeling (HiSIM-IEGT)

3.1 Concept of extend HiSIM-IGBT for HiSIM-IEGT

The conventional HiSIM-IGBT is formed by combining a surface-potential-based MOSFET-part and carrier-distribution-based bipolar junction (BJT) transistor part. Those two parts are connected by conductivity-modulated base resistance. The model considers the potential distribution from the MOSFET part to the BJT junction by solving some internal potential nodes self-consistently. The current value of MOSFET ($I_{\rm ds}$) is determined by "Drain" and "Emitter" and "Gate" nodes. By applying the Gauss law, the total charge density induced in the substrate is derived with the Poisson equation. The floating-bas effect is modeled by considering the charge accumulation within the region in addition to the HiSIM-IGBT, as shown in Figs. 3.1, where the node V_{fp} is introduced to model the accumulation charge explicitly.

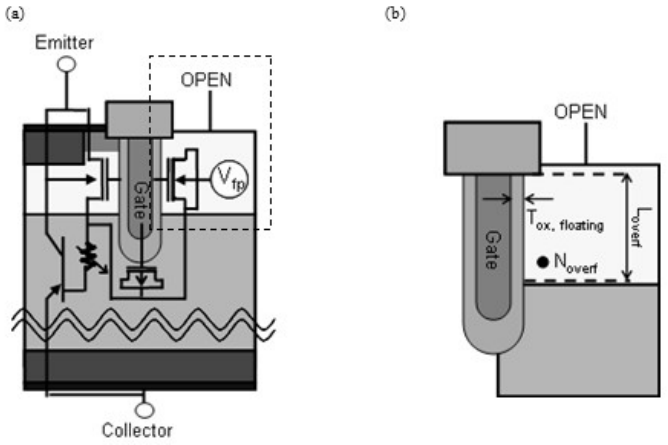

Figure 3.1: Equivalent circuit of the developed IEGT model. The parameter of floatin base region.

3.2 Model Development

3.2.1 Floating-Base Capacitance Model

When considering switching operation, it is one of important elements to take gate capacitance. Most of the IGBT capacitance consists of the MOSFET gate capacitance which includes the overlap parts with the n- base region at the bottom of the trench gate. HiSIM-IGBT describes this trench-bottom nonlinear MOS capacitance with the surface-potential-based approach. The floating-bas effect improved and produced the same model as the conventional HiSIM-IGBT trench-bottom MOS capacitor parts. Since original MOS capacitor was p-MOS, it was changed into n-MOS type, and it made various parameters correspond to floating-bas regions. The surface potential ϕ_s is calculated in the same manner as the MOSFET part. The floating-bas charge equation is written with the calculated ϕ_s as Eqs. (3.1) under the depletion and the accumulation conditions and inversion condition Eqs. (3.2), where $C_{\mathrm{ox,foating}} = T_{\mathrm{ox}} / T_{\mathrm{ox,floating}}$.

$$Q_{\mathrm{g,floating}} = W_{\mathrm{eff}} * L_{\mathrm{overLF}}((2\epsilon_{\mathrm{si}} q N_{\mathrm{over}}/\beta)^{0.5} * (\beta(\phi s + V_{\mathrm{fp}}) \quad 1)^{0.5}) \tag{3.1}$$

$$Q_{\mathrm{g,floating}} = W_{\mathrm{eff}} * L_{\mathrm{overLF}} * C_{\mathrm{ox,floating}}(V_{\mathrm{gs}} \quad V_{\mathrm{fb,floating}} \quad \phi s) \tag{3.2}$$

Here $T_{\mathrm{ox,floating}}$ and L_{overLF} are the oxide thickness and the oxide length of the floating base region, respectively. N_{overf} and $V_{\mathrm{fb,floating}}$ are the base impurity concentration at the floating-bas region and the flatban voltage for the IEGT structure, respectively.

It checked that negative capacitance is due to the capacity of floatin base region. Figure 3.2 shows calculation results of the C_{gg} to change the SiO_2 thickness. It shows a case of half and twice the oxide fil thickness. The Negative capacitance is decreasing oxide thickness is increased as shown Figure 3.3.

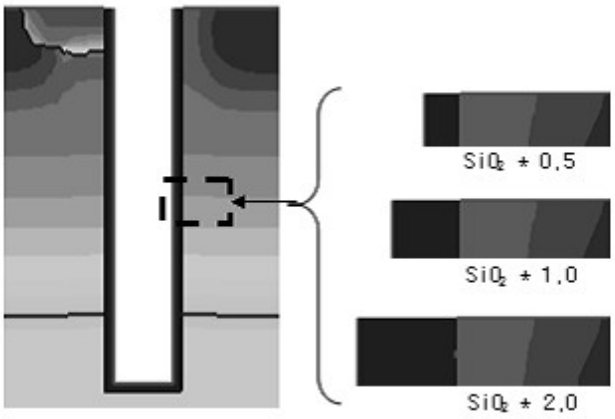

Figure 3.2: The picture of SiO_2 thickness change pattern.

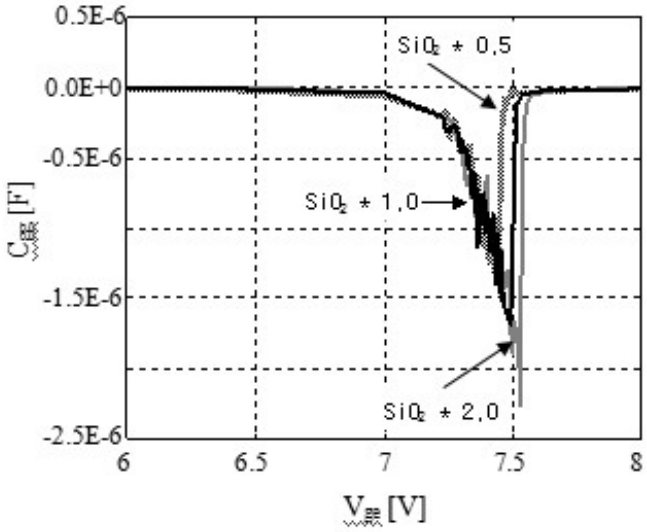

Figure 3.3: 2D-device simulation result of the SiO_2 thickness dependence of $C_{\rm gg}$.

Figure 3.4 a shows comparison of the simulated switching waveform simulated with the developed model with that obtained by the two-dimensional device simulation. Good agreement is obtained. From this result, it can be concluded that the gradual slope switching waveform depends on the floating-bas structure. The IEGT switching performance can be optimized using multiple options to achieve the required characteristics.

Figure 3.5 shows 2D-device simulation result of $C_{\rm gg}$, the concentration dependence of floatin base region. It turns out that the concentration of floatin base region also contributes to negative capacitance. Figure 3.6 shows the variation of $C_{\rm gg}$ when changing the lifetime of electrons and holes. Negative capacitance is small when lifetime is shortened. It considered the quantity of the hole is decreased which reaches to floatin base region. So that negative capacitance is changed by the life time, I found that the negative capacitance has occurred under the influenc of holes in from collector accumulates in floatin base region.

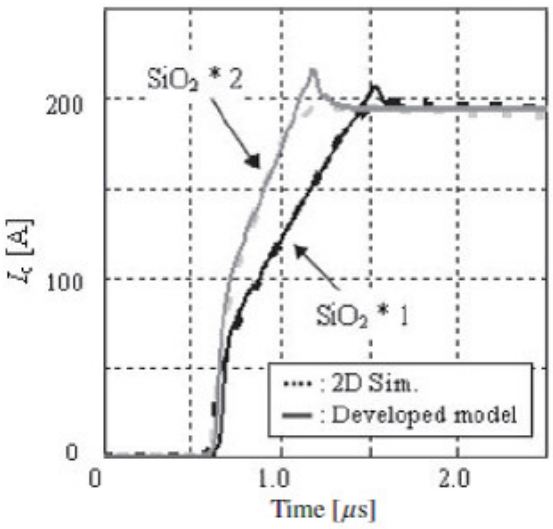

Figure 3.4: Switching waveform (I_c) comparison of a base model, the model which twice SiO_2 thickness, and the model which doubled the concentration of floating-base

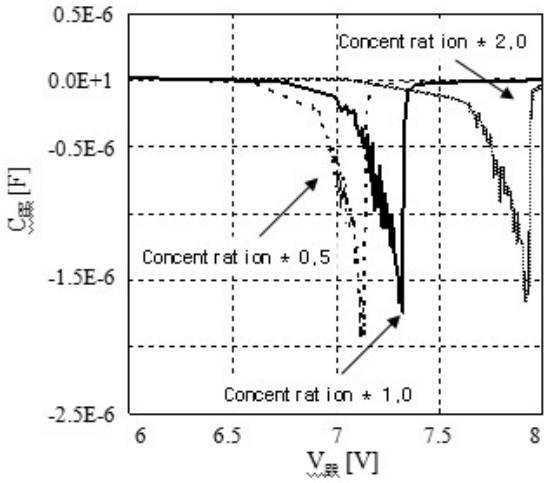

Figure 3.5: 2D-device SIM. result of the floatin base concentration dependence of C_{gg}.

3.2.2 Potential Node Model

Beyond the threshold voltage, the base current (the drain current of the MOSFET) fl ws, which induces the collector current. The hole injection into the floating-bas region as the

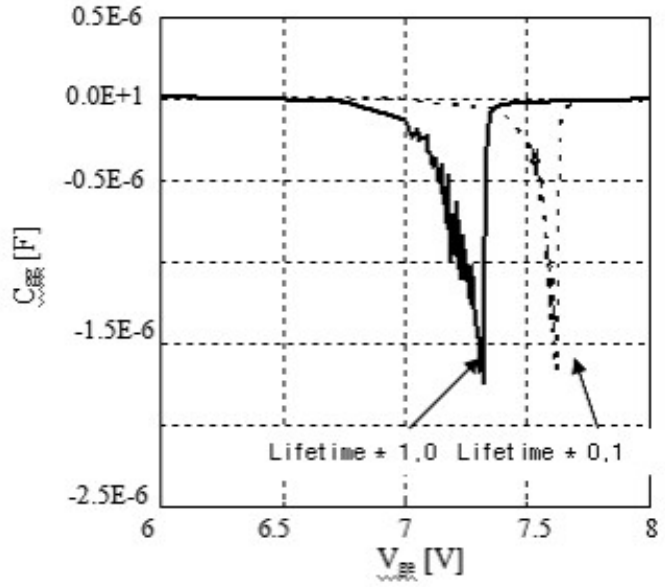

Figure 3.6: 2D-device simulation result of changing the lifetime of electrons and holes dependence of C_{gg}.

collector current causes the potential increase. So, the potential node V_{fp} are formulated in relation to the current.

3.2.3 Model Implementation

The floating-bas effect is modeled by considering an n-MOS capacitor in addition to HiSIM-IGBT as shown in Fig. 3.1. Figure 2.17 shows 2D device simulation result of C_{gg}, floating-bas voltage (V_{fp}), and collector current for IEGT structure.

The hole injection into the floating-bas region as the collector current causes the potential increase. Thus, the potential node V_{fp} introduced is connected to the current source to describe this mechanism. However, the collector current fl w into the floatin base is stopped, when V_{fp} becomes higher than the n-base potential V_b. This effect is described by the connected MOSFET, for which the electrodes are connected either to V_b. The hole injection even into the floating-bas region occurs, because the collector contact extends over the device width. The injected holes have no way of going out or recombining in the

p-Si base. Thus, they accumulate and increase V_{fb}. The balance between V_b and V_{fb} either continues or stops the hole injection.

It turns out that there is a relationship between V_{fp} and collector current. The potential node V_{fp} is calculated by the relationship of collector current. The bulk node of new modeled n-MOS capacitor is connected to the V_{fp}, the source node is connected to the V_{b}. The base node V_b as well as V_{fp} are calculated by solving the Kirchhoff law explicitly, namely, I_c+I_b+I_e=0. The additional equivalent circuit shown in Fig. 3.1 is included in the conventional HiSIM-IGBT and tested with a SPICE simulator. The negative C_{gg} is much larger than the positive C_{gg}. The total C_{gg} is dominated by the negative C_{gg} between 7V and 8V, when the hole accumulation occurs. An important task is to calculate the negative C_{gg} accurately as shown Fig. 3.7.

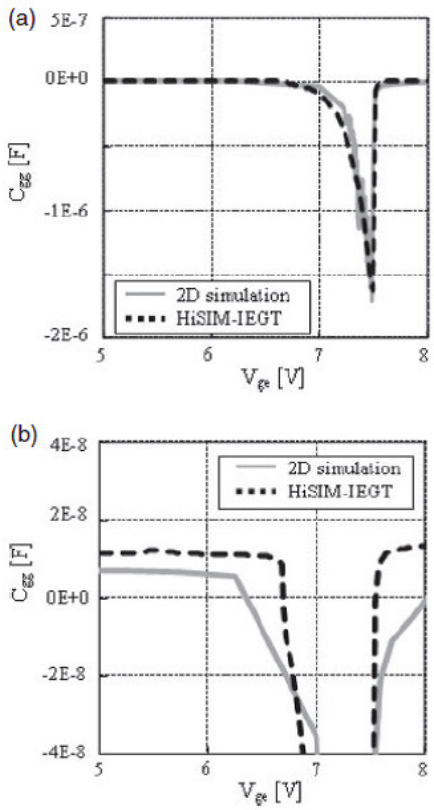

Figure 3.7: Gate cap. calculated with HiSIM-IEGT model and 2D device simulation result.

Figure 3.8 shows simulation condition (OPEN condition and GND condition) by simulated 2D device simulation. It found that the C_{gg} is increased over the negative capacitance range(V_{ge}) in OPEN condition as show Fig. 3.9. This is the effect from which the potential of the floating-bas part changes. The increase C_{gg} shows that switching speed becomes slow.

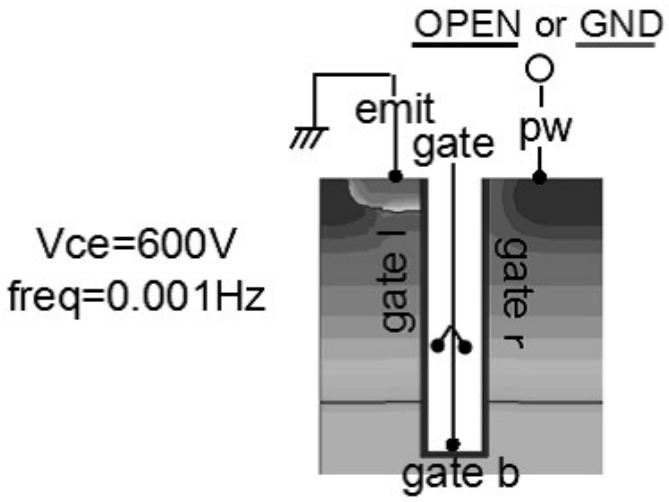

Figure 3.8: 2D-device simulation condition of the gate capacitance.

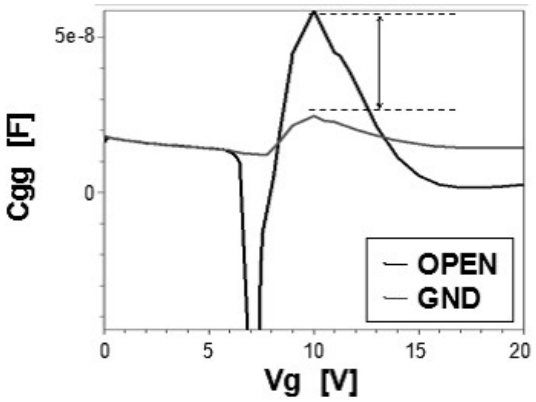

Figure 3.9: 2D-device simulation result of floating-bas OPEN and GND conditions.

Figure 3.10 shows simulation condition (OPEN condition and GND condition) by simulated new developed HiSIM-IEGT. The development HiSIM-IEGT model also shows the same result as 2D device simulator (Fig. 3.11).

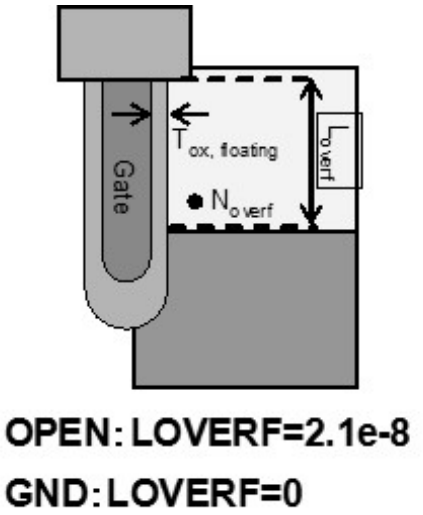

Figure 3.10: Simuration conditions.

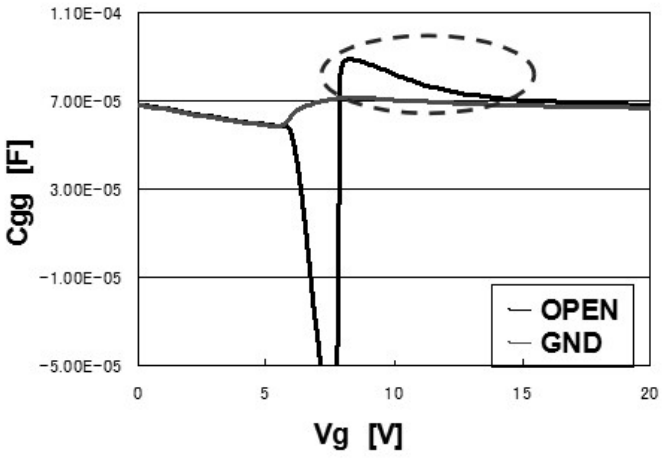

Figure 3.11: New HiSIM-IEGT simulation result of floating-bas OPEN and GND conditions.

3.3 Relation of Gate Capacitance and Switching Waveform

Figure 3.12 shows 2D numerical device simulation results of IEGT ' s gate capacitance. It becomes positive or negative depending on the value of gate voltage range. When the range of gate voltage is 0 to threshold voltage (range A), the gate capacitance shows positive value. However, negative capacitance is shown in the range of between threshold voltage and about 7.5V (ranges B). The gate voltage above about 7.5V (range C), gate capacitance becomes positive. Figure 3.13 shows 2D numerical device simulation results of I_c and V_{ge} waveform during switching turn-on timing. The I_c slope is changed in the middle of the waveform. The change is attributed to the negative-capacitance. The gate voltage state at the timing of switching turn-on is compared with the gate capacitance state. The range of gate voltage 0 to threshold at the time of switching, gate capacitance take a positive value corresponds to the gate capacitance range A. Next, in the range of between threshold voltage and about 7.5V, it is a range which shows negative capacity, same as range B of the gate capacitance. Gate voltage spikes under the influenc of negative capacitance. With the increase of the gate voltage, the collector current is also fl wing abruptly. Then, since gate voltage become higher than about 7.5V voltage which shows positive capacity again (range C), gate voltage buildup rate falls and slope of current also changes.

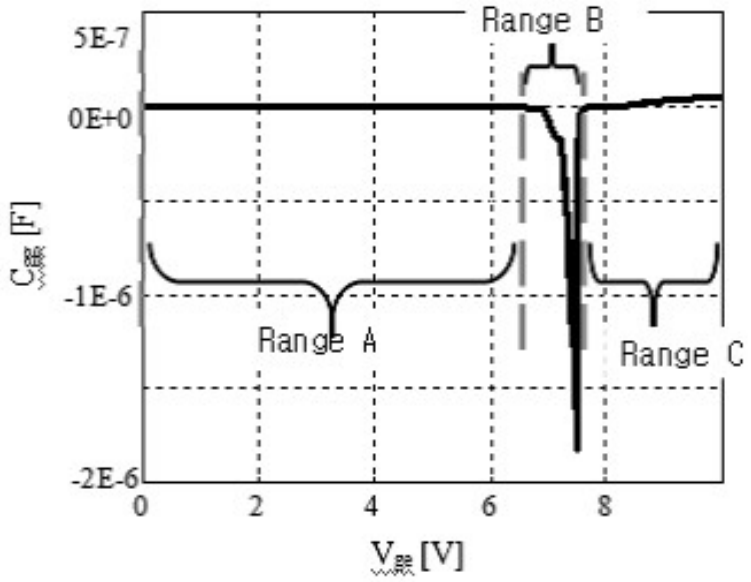

Figure 3.12: 2D-device simulation results of C_{gg}. Range A and C shows positive value. Range B shows negative value.

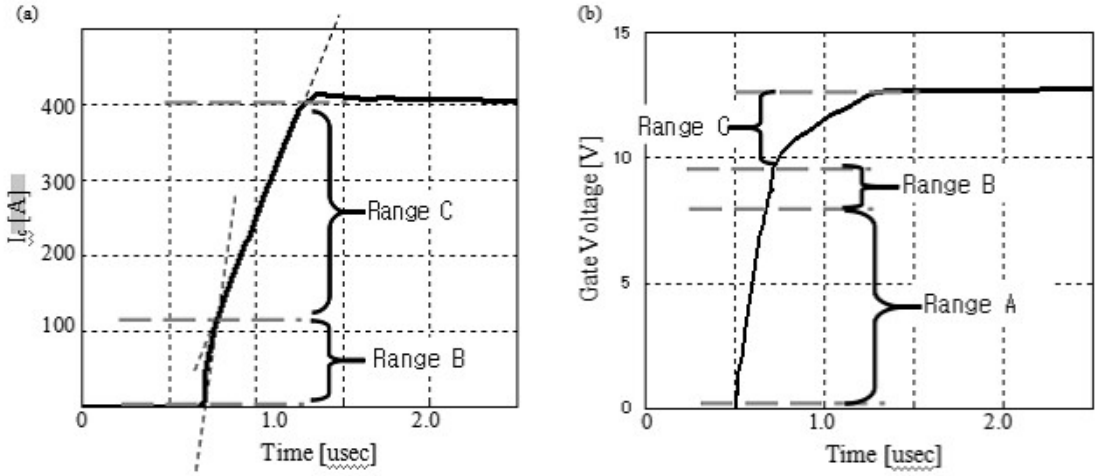

Fig. 5. 2D device simulation result of switching turn-on (a) Ic current. (b) gate voltage.

Figure 3.13: 2D device simulation result of switching turn-on (a) I_c current. (b) gate voltage.

Chapter 4

HiSIM-IEGT Model Optimized Influenc of Frequency dependence

4.1 Influenc of Carrier Delay

The static DC characteristics of IEGT is modeled using HiSIM-IGBT. The model parameter values of HiSIM-IGBT were extracted from the measured I_c-V_{ce} characteristic of IEGT. About static DC characteristic, it is expressed by HiSIM-IGBT. Fig. 4.1 shows the turn-off waveform of the circuit shown in Fig. 2.1. In comparison with the turn-on waveform, the waveform calculation result is well reproduced with the original HiSIM-IGBT under the turn-off condition. The small errors are found in the surge of V_{ce} and the slope of the I_c. The reason for the error can consider a lack of model accuracy or influenc of the inductance of the measurement environment. Thus it is concluded that the specifi effect observed in IEGT is pronounced only under the turn-on condition.

4.2 Frequency Dependence of Gate Capacitance

Fig. 4.3 shows 2D-device simulation results of frequency dependence of the total C_{gg} as a function of V_{ge}. It is seen that the magnitude of the negative C_{gg} is reduced with increased frequency. Fig. 4.4 depicts the frequency dependence of the minimum value of the total C_{gg}. It is seen that the minimum value remains constant for low frequency. However, it is

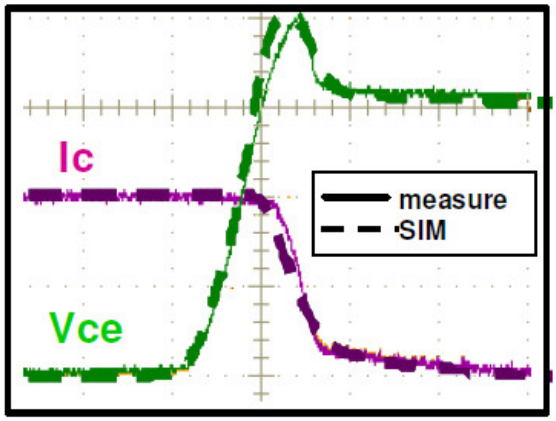

Figure 4.1: Measurement switching waveform in comparison to simulation results with conventional HiSIM-IGBT under turn-off condition.

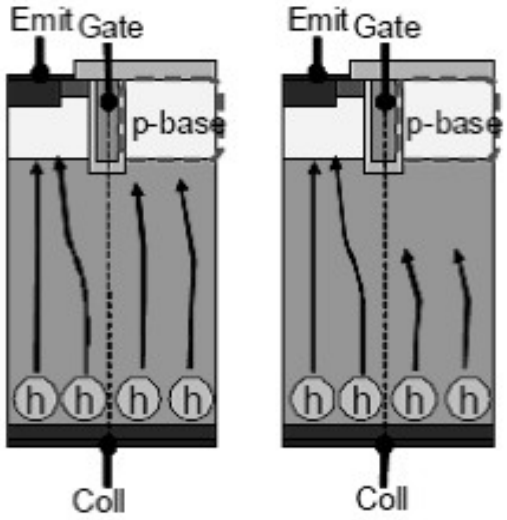

Figure 4.2: The image of carrier delay.

observed that the minimum diminishes rapidly for frequency faster than 1kHz. Beyond frequency = 100 kHz the negative C_{gg} disappears completely. This frequency dependence of C_{gg} is attributed to the hole transit delay injected from the collector and accumulated underneath Gate r (see Fig. 2.7). If V_{ge} is switched faster than the time for holes reaching

the floating-bas gate, C_{gg} remains zero. In actual circuit operations, turn-on and turn-off are repeated and thus the total C_{gg} is dependent on the switching speed. Therefore the negative C_{gg} under real circuit operation can never be large as observed under the DC condition. It needs to take delay of a career into consideration [33, 34, 35]. The carrier delay is derived from the effect of the Non-Quasi-Static(NQS) effect [36, 37, 38].

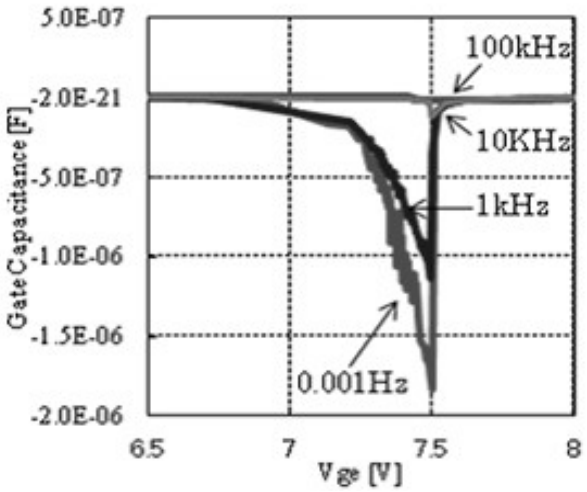

Figure 4.3: Total gate capacitance C_{gg} of 2D device simulation results as a function of the gate voltage V_{ge} at V_{ce}=600V. Frequencies applied for the simulation are depicted.

Fig. 4.5 shows the floating-bas width dependence of the minimum value of the total C_{gg}. The minimum value is changed as a function of the floating-bas width W_{fp} (see Fig.1). Thus, it is seen that the C_{gg} characteristic is strongly influence by the frequency and floating-bas structure. Fig. 4.6 summarizes the relationship between the floating-bas width W_{fp} and the current rise time di/dt. The reason for plotting as a function of di/dt is due to the present investigation of switching. The di/dt value corresponds approximately to the frequency of 10 kHz. The width W_{fp} is normalized by the total width W_{total}.

The “×” mark represents the condition that the negative gate current occurs. On the other hand, the “○” mark is the condition that the negative gate current disappears. When the ratio of W_{fp} to W_{total} becomes large, the negative C_{gg} is observed even at fast switching

speed. Thus it can be concluded that the resulting I_c waveform is very much dependent on the structure as well as switching speed. The line depicted in Fig. 4.6 matrix denotes the boundary for enabling the gradual slope switching.

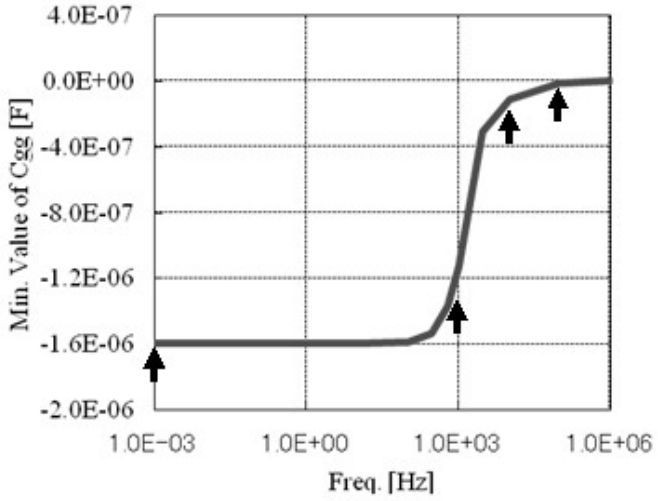

Figure 4.4: 2D device simulation result of the minimum C_{va} value as a function of the frequency applied at V_{ce}=600V.

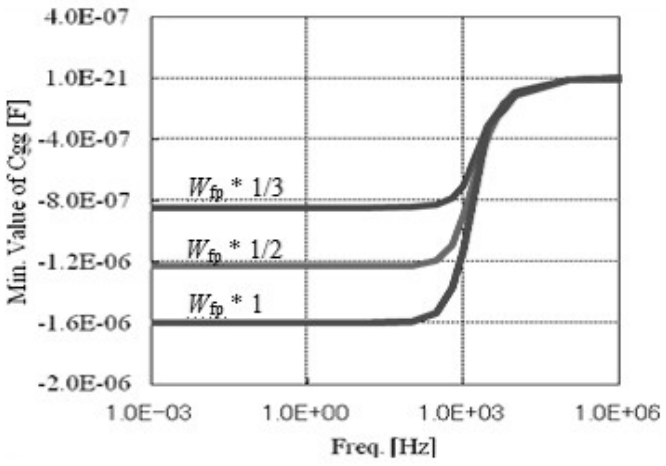

Figure 4.5: 2D device simulation result. The floating-bas width dependence of the minimum value of total C_{gg} at V_{ce}=600V..

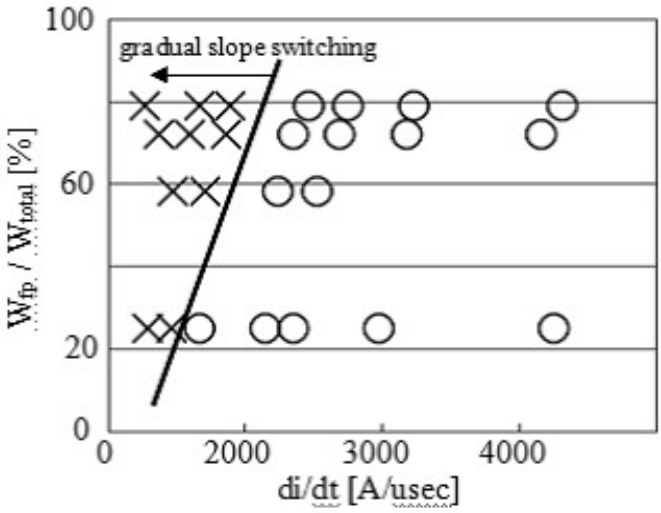

Figure 4.6: 2D device simulation result of the matrix of negative gate current appearance.

4.3 NQS Modeling for Floating-Base Structure

The NQS effect of HiSIM is modeled by introducing the carrier transit delay into the description of the charge formation. The carrier formation is modeled as

$$q_{\mathrm{n}}(y,t_{\mathrm{i}}) = q_{\mathrm{n}}(y,t_{\mathrm{i}-1}) + \frac{\Delta t}{\tau}(Q_{\mathrm{n}}(y,t_{\mathrm{i}}) \quad q_{\mathrm{n}}(y,t_{\mathrm{i}-1})) \tag{4.1}$$

where $q(t_{\mathrm{i}})$ and $Q(t_{\mathrm{i}})$ represent the non-quasi-static and the quasi-carrier density at time t_i, respectively, and $\Delta t = t_{\mathrm{i}} \quad t_{\mathrm{i}-1}$ is valid. The delay is determined by the carrier transit delay τ and the time interval in the circuit simulation Δt.

Two different τ mechanisms are distinguished in HiSIM, namely τ_{diff} and τ_{cond}. Before the front reaches to electric field the complete channel formation is modeled here by slow diffusive transit delay mechanism τ_{diff} given by

$$\tau_{\mathrm{diff}} = \frac{qL^2}{\mu kT} \tag{4.2}$$

Diffusion is fl w of carrier due to carrier concentration gradients. Carriers move randomly from region of higher concentration to lower concentration giving rise to electric circuit.

The conduction deelay τ_{cond} describes the average transit time for carriers to cross the completed MOSFET channel, which can be calculated as

$$\tau_{\mathrm{cond}} = \frac{|Q_i|}{I_{ds}} \tag{4.3}$$

where Q_i is the steady-state inversion layer charge and I_{ds} is the drain current. α is $HiSIM \quad QS$ function which take into account the drain voltage dependence. $V_{gs} \quad V_{th}$ is calculated in HiSIM as Q_{n0}/C_{ox}, where Q_{n0} is the charge at the source end and C_{ox} is the SiO_2 capacitance.

$$\tau_{\mathrm{cond}} = \mathrm{DLY2} \cdot \frac{L^2}{\mu(Q_{n0}/C_{ox}} \tag{4.4}$$

with the introduction of a constant factor DLY2 as a model parameter. Above variables are all represented in HiSIM's quasi-static formulation and thus no additional variables are necessary.
The two delay mechanism are combined using the Matthiessen rule as

$$\frac{1}{\tau} = \frac{1}{\tau_{diff}} + \frac{1}{\tau_{cond}} \tag{4.5}$$

4.4 Comparison of Measurement Switching Wave Form and Circuit Simulation Results

Fig. 4.7, 4.8 shows the switching waveform simulated with the developed IEGT model including the floating-bas effect in comparison to the measured data. Namely the reduction of the negative C_{gg} equivalent to the value at frequency = 100 kHz in Fig.10 is considered for the simulation. The circuit shown in Fig. 2 is investigated. The free wheel diode model

is used HiSIM-Diode model [39, 40, 41]. And the model parameter is adjusted in order to optimize the portion about the reverse recovery wave form. It is seen that the measured gradual slope switching behavior observed in the collector current I_c is accurately reproduced as shown Fig. 4.7. Furthermore, the collector voltage V_{ce} is also well reproduced with change of I_c waveform as shown Fig. 4.8. Fig. 4.9 shows calculated and measurement switching turn-on loss. The loss calculation result is also well reproduced, and thus the developed model is confirme to be applicable for accurate inverter circuit design. The HiSIM-IEGT model has been developed, which consider the floating-bas effect. The model can reproduce to the negative gate capacitance, witch is important feature of IEGT. This model has been implemented in a circuit simulator and verifie to be accurate. It has been shown that the frequency dependence of capacitance is shown to be an essence for characterizing the switching performance of IEGT. It has been shown that the observed gradual slope switching characteristic has been accurately reproduced with the developed model.

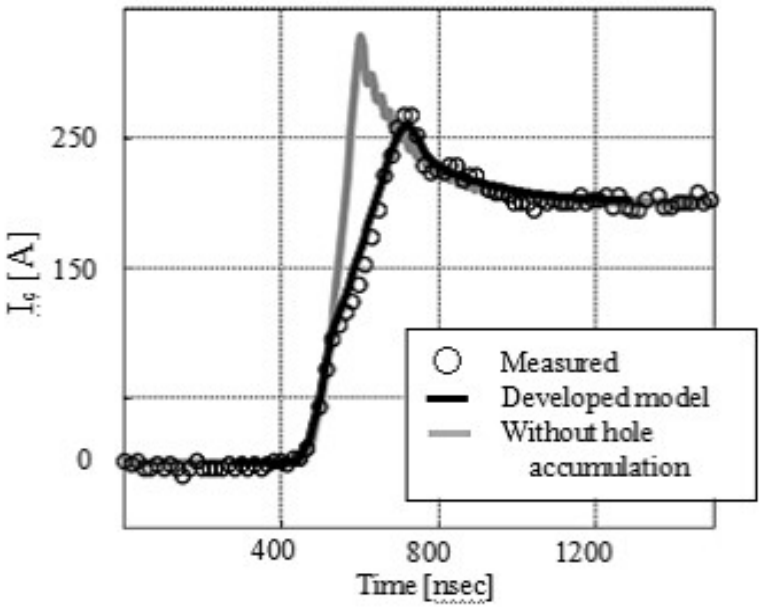

Figure 4.7: Comparison of calculated switching turn-on waveform with measurement results I_c waveform.

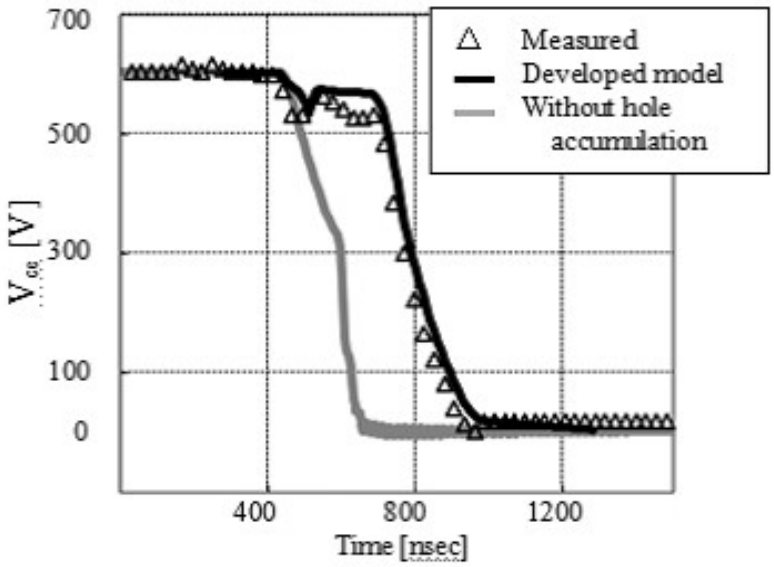

Figure 4.8: Comparison of calculated switching turn-on waveform with measurement results V_{ce} waveform.

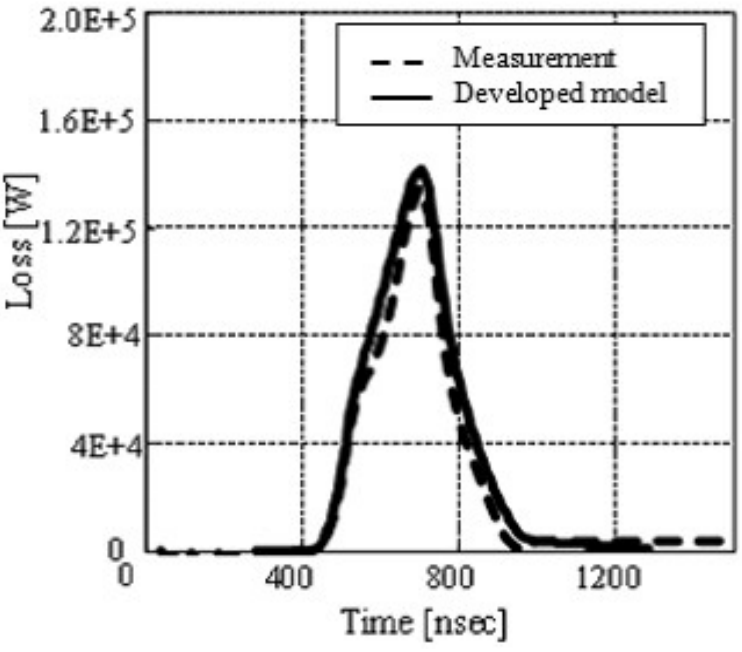

Figure 4.9: Comparison of calculated switching turn-on loss.

Chapter 5

Conclusion

5.1 Summary

The HiSIM-IEGT model has been developed, which consider the floating-bas effect. It was consider the hole accumulation effect in the floating-bas region, which is the origin of the injection enhancement and behavior of potential. Hole storage is expressed by n-type MOSFET capacitance model. And, potential of floating-bas region is modeled in relation with collector current I_c. The path of the hole current in IEGT device was expressed in implementation of a model. The negative gate capacitance simulation become possible by this modeling. The model can reproduce the negative gate capacitance, which is the important feature of IEGT. In addition, the analysis of the frequency dependence of C_{gg}. There is a frequency dependent on C_{gg}, the C_{gg} is changed by the switching speed on at the time of circuit operation. The NQS model is introduced into floating-bas model. Thereby, the model applied to transitional analysis. The developed model has been implemented in a circuit simulator and verifie the accuracy. It has been shown that the frequency dependence of the gate capacitance is shown to be an essence for characterizing the switching performance of IEGT. Switching simulation result reproduces measured I_{ce} and V_{ce} waveform as well as switching loss. It is verifie that the developed model can be utilized to optimize the ideal switching waveform, balancing the power loss and surge of I_{ce} and V_{ce}. The highly precise simulation will become possible.

5.2 Future Work

The model can be further utilized to optimize the switching speed for achieving appropriate circuit performance. For the purpose further verificatio of the carrier transit time within the device must be investigated. For the future ' s development, the developed model extend to the modeling of the influenc of temperature dependence. Further, it is possible to expand the other device with special gate structure that is not limited to the IGBT. For example, I want to apply to future devices such as SiC.

Appendix A

NQS model formulation

The HiSIM-NQS charge formulation model is formulated as

$$q(t_{\mathrm{i}}) = q(t_{\mathrm{i}-1}) + \frac{\Delta t}{\tau + \Delta t}\Big(Q_{\mathrm{i}}(t_{\mathrm{i}}) \quad q(t_{\mathrm{i}-1})\Big) \tag{A.1}$$

where q is the NQS charge, Q is the QS charge and τ is the carrier transit delay. t_{i} and $t_{\mathrm{i}-1}$ are the present and previous time points, respectively. Δt is the time interval given by $t_{\mathrm{i}} \quad t_{\mathrm{i}-1}$. Equation A.1 states that the increase of NQS carriers is given by the difference in QS and NQS carriers as delayed by the carrier transit delay.

Expanding Eq. A.1 gives

$$q(t_{\mathrm{i}}) = \frac{q(t_{\mathrm{i}-1})(\tau + \Delta t) + \Delta t\Big(Q_{\mathrm{i}}(t_{\mathrm{i}}) \quad q(t_{\mathrm{i}-1})\Big)}{\tau + \Delta t} \tag{A.2}$$

$$= \frac{\tau\, q(t_{\mathrm{i}-1}) + \Delta t\, Q_{\mathrm{i}}(t_{\mathrm{i}})}{\tau + \Delta t} \tag{A.3}$$

Multiplying the numerator and denominator by $1/\tau$ and then simplifying gives

$$q(t_{\mathrm{i}}) = \frac{\tau\, q(t_{\mathrm{i}-1}) + \frac{\Delta t}{\tau}\, Q_{\mathrm{i}}(t_{\mathrm{i}})}{1 + \frac{\Delta t}{\tau}} \tag{A.4}$$

$$= \frac{\Delta t}{\tau}\Big(q(t_{\mathrm{i}}) \quad Q_{\mathrm{i}}(t_{\mathrm{i}})\Big) + q(t_{\mathrm{i}-1}) \tag{A.5}$$

Rewriting Eq. A.5 gives

$$\frac{q(t_{\mathrm{i}}) \quad q(t_{\mathrm{i}-1})}{\Delta t} = \quad \frac{1}{\tau}\Big(q(t_{\mathrm{i}}) \quad Q(t_{\mathrm{i}})\Big). \tag{A.6}$$

Equation A.6 is a discretized equation of

$$\frac{dq}{dt} = \quad \frac{1}{\tau}\Big(q(t_{\mathrm{i}}) \quad Q(t_{\mathrm{i}})\Big), \tag{A.7}$$

which states that the time rate of change of the NQS carrier is equal to the difference between the QS and NQS charge as delayed by τ.

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Compact Modeling of Floating-Base Effect in Injection-Enhanced Insulated-Gate Bipolar Transistor Based on Potential Modification by Accumulated Charge

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We have developed a compact model of the injection-enhanced insulated-gate bipolar transistor (IGBT) applicable for circuit optimization. The main development is modeling the hole accumulation in the floating-base region. It is demonstrated that the observed negative gate capacitance is well reproduced with the developed model. © 2013 The Japan Society of Applied Physics

1. Introduction

Automobile manufacturers are required to consider environmental problems and to reduce the fuel consumption of their products. Hybrid and electric vehicles are expected as one of the solutions for realizing such a requirement. Nowadays, many power devices are used for achieving reliable, safe, as well as economic automobiles. Among the power devices, the insulated-gate bipolar transistor (IGBT) realizes a high current controllability together with a high breakdown voltage.[1)] Because of these advantages, IGBT has been widely applied for inverter circuits of power electronics.[2)] Therefore, many descendants of IGBT have been developed according to different application purposes. The injection-enhanced insulated-gate bipolar transistor (IEGT) has been developed in order to reduce the on-state voltage,[3,4)] and this structure exhibits a soft switching waveform in comparison with IGBT. Thus, IEGT has been applied to the area where reduced voltage overshoot is required.[5,6)] However, the soft switching waveform causes a large switching loss at the same time. To optimize the trade-off between the low overshoot and the low energy loss, an accurate circuit simulation for investigating the switching performance is inevitable.

Satisfactory IGBT models are already used for various circuits.[7–9)] However, they are not comprehensive physical models valid for practical circuit designs. HiSIM-IGBT has been developed for simulating circuit performance,[10,11)] which solves the potential distribution within IGBT explicitly under fully dynamic load conditions, through the surface-potential-based modeling approach including the advanced MOSFET model HiSIM.[12–15)] However, it considers the symmetrical trench-type IGBT structure [see Fig. 1(a)], where both sides of the p-base are connected to the emitter. The purpose of this investigation is to extend HiSIM-IGBT for the asymmetrical IEGT structure [see Fig. 1(b)], where one side of the p-base is disconnected and floated. For this purpose, we investigate the potential distribution in the floating-base region induced by applied voltages.

2. Switching Response of Floating Base

Figure 2(a) shows the studied basic circuit with its element values. Measurements and results with HiSIM-IGBT developed for the symmetrical structure are compared in Fig. 2(b). The threshold voltage of the studied IGBT is

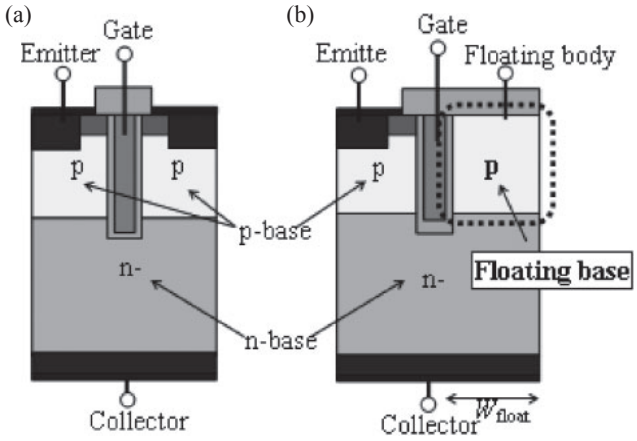

Fig. 1. Comparison of two IGBT structures: (a) symmetrical IGBT and (b) asymmetrical IEGT structures.

6.5 V, and the model parameter values of HiSIM-IGBT were extracted from the measured I_C–V_{CE} characteristics. It was observed that the measured waveform of the collector current I_c is not steep for IEGT, and soft switching is realized. On the contrary, the model calculation result with HiSIM-IGBT shows no soft switching. The difference between the measured and calculated waveforms is attributed to the floating-base effect, which is not yet considered in HiSIM-IGBT.

The floating-base effect is investigated by two-dimensional (2D) device simulations.[16)] Figure 3 shows electrostatic potential contours for different gate voltage V_{ge} values around the trench gate oxide. In the $V_{ge} < V_{th}$ case, the potential distributions in the emitter-connected and floating bases are nearly the same. However, the gate control becomes completely different between the two structures under the $V_{ge} \geq V_{th}$ condition when I_c begins to flow. Under this condition, the potential value on the floating-base side becomes even higher than V_{ge}. However, the potential value does not exceed 24.8 V in the studied case, even with a further increase in V_{ge}.

Figure 4 shows equi-hole-density contours for the same conditions as shown in Fig. 3. When V_{ge} reaches the threshold voltage ($V_{ge} = 6.5$ V), the contacted p-base side forms the depletion layer as well as the inversion layer under the gate as can be seen from the low hole concentration. On the other hand, the hole-density contours on the floating-base

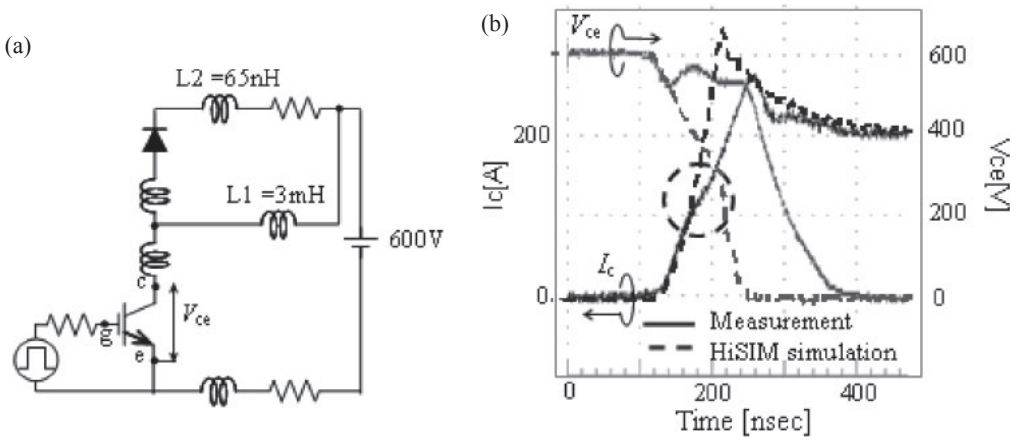

Fig. 2. (a) Studied basic circuit and its element values. (b) Measured transient characteristics in comparison with simulation results with original HiSIM-IGBT.

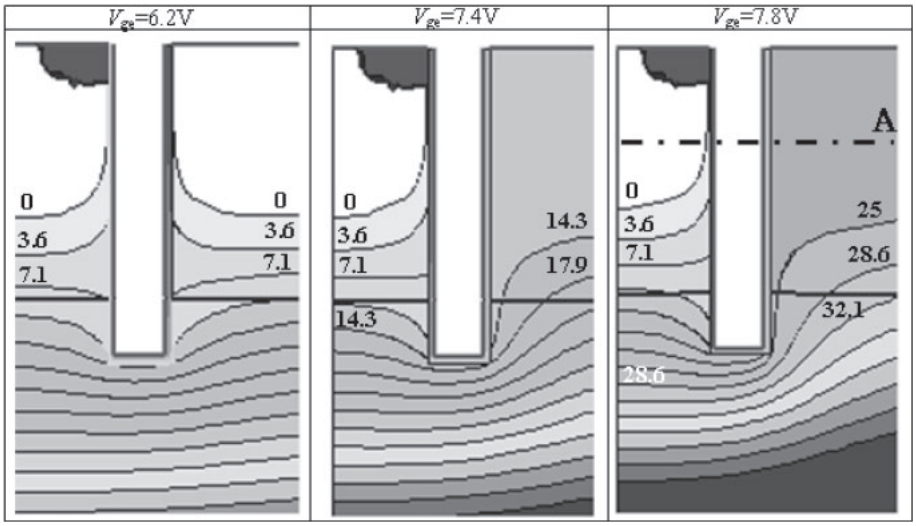

Fig. 3. Simulated electrostatic potential around the gate (V) ($V_{ce} = 600\,\mathrm{V}$).

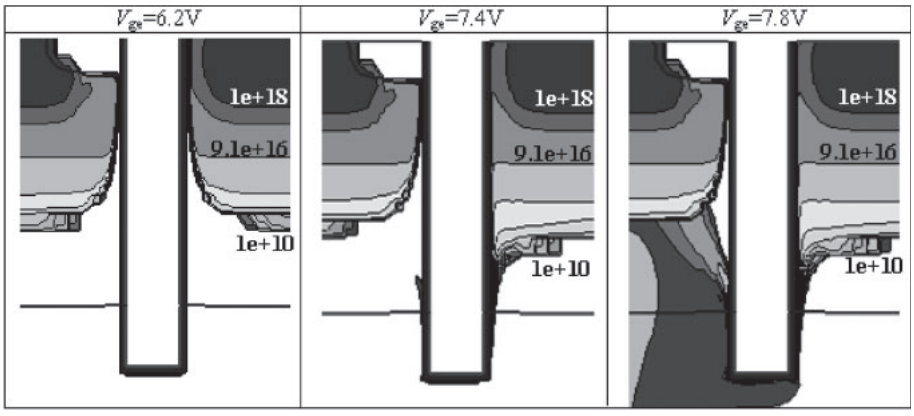

Fig. 4. Simulated hole-density distributions around the gate ($/\mathrm{cm}^3$) ($V_{ce} = 600\,\mathrm{V}$).

side remain nearly unchanged, except in the depletion region at the n-/p-base junction, which is filled with holes injected from the collector for $V_{ge} \geq V_{th}$. The potential distribution along the cross section shown by line A is depicted in Fig. 5. It is clearly seen that the contacted-base side forms the inversion layer and the non contacted side forms the accumulation layer. Beyond the threshold condition, the collector current flows into the floating-base region as well and fills the entire region with holes. This hole injection into the floating base is terminated after a certain number of holes occupy the region. Thus, it can be concluded that the floating-base potential shown in Fig. 3 is determined by

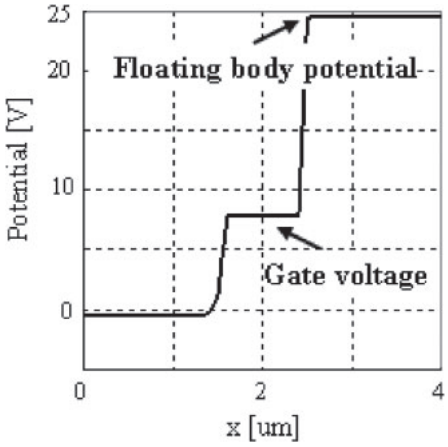

Fig. 5. Potential distribution of line A.

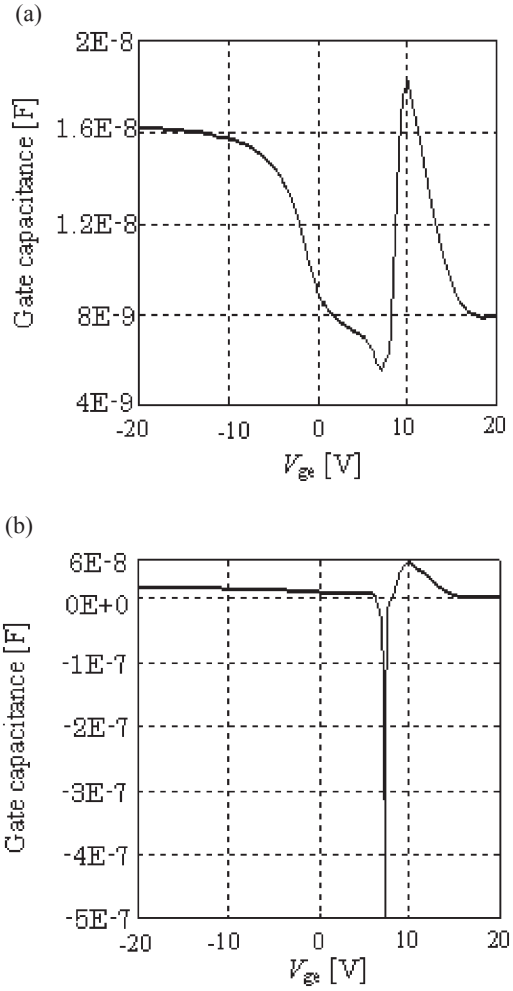

Fig. 6. 2D device simulation of C_{gg}. (a) IGBT structure. (b) IEGT structure.

a balance created by carrier dynamics responding to the potential distribution within the entire IEGT.

The carrier response to the potential change can be investigated with the capacitance. Figure 6 shows a comparison of the 2D numerical simulation results of C_{gg} for IEGT and IGBT. The humps around $V_{ge} = 10\,\mathrm{V}$ observed for both structures are due to the resistive base

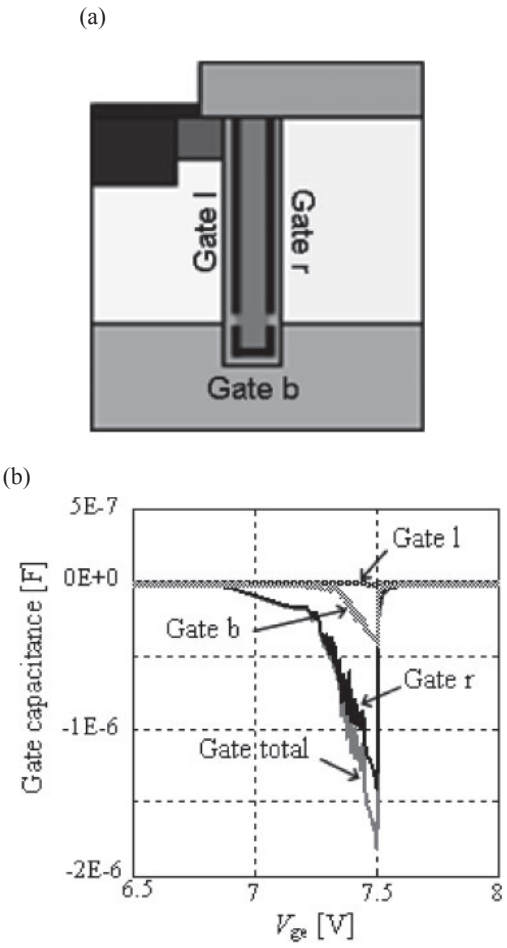

Fig. 7. (a) The gate contact is divided into different contributions. (b) 2D device simulation result of gate capacitance for floating-base structure at $V_{ce} = 600\,\mathrm{V}$, frequency $= 0.001\,\mathrm{Hz}$, and V_{ge} sweep.

effect under the on-current condition usually observed for power devices. A clear difference between the two structures is the sharp negative C_{gg}, which is observed only for the IEGT structure. Figure 7 depicts separate contributions from different parts of the gate oxide to the total negative C_{gg}. It is seen that the C_{gg} of the floating base (Gate r) dominates the total C_{gg}.

3. Modeling of Floating-Base Effect

The origin of the "negative capacitance"[17,18] is attributed to the hole accumulation in the floating base. To model the charge distribution at Gate r, a potential node V_{fp} is investigated. The node is set at the surface of the floating base as shown in Fig. 1(b). Figure 8(a) shows the relationship among different values as a function of V_{ge}. Beyond $V_{ge} = V_{th}$, the collector current increases, accompanied by the reduction in C_{gg}. At $V_{ge} = 7.5\,\mathrm{V}$, C_{gg} increases abruptly, which coincides with the start of the saturation of the floating-base potential V_{fp}. As can be seen in Fig. 9, the start of V_{fp} saturation is attributed to the condition where the potential in the floating base becomes higher than the upside potential of the n-base region V_b. However, the increase is stopped when V_{fp} exceeds V_b. Figure 8(b) shows the width [W_{float}: see Fig. 1(b)] dependence of C_{gg}. Although the increase in W_{float} does not affect C_{gg}, the W_{float} reduction results in the V_{ge} shift to higher values. The total number of

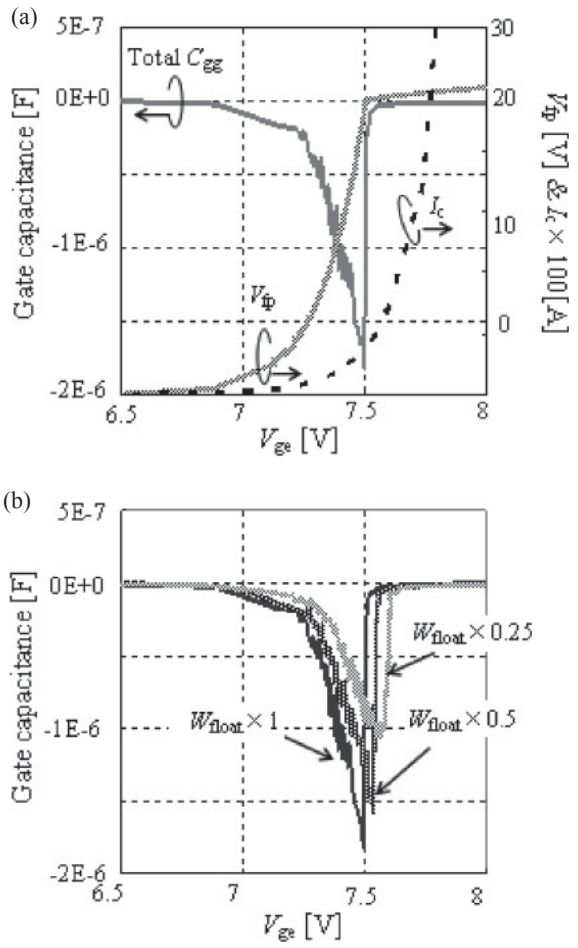

Fig. 8. (a) 2D device simulation results of C_{gg}, floating-base voltage, and I_c current for floating-base structure. (b) 2D device simulation result of the width (W_{float}) dependence of C_{gg}.

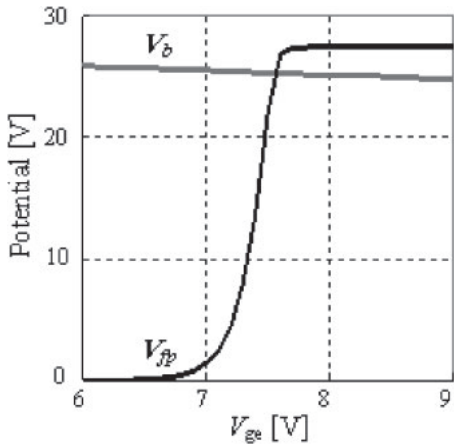

Fig. 9. Simulated results of the floating-base potential (V_{fp}) and the base potential (V_b).

injected holes into the floating-base region is reduced with a reduced W_{float}. This requires the V_{ge} increase to realize V_{fp} larger than V_b.

The floating-base effect is modeled by considering the n-MOS capacitor in addition to HiSIM-IGBT as shown Fig. 10. Beyond the threshold voltage, the base current (the drain current of the MOSFET) flows, which induces the

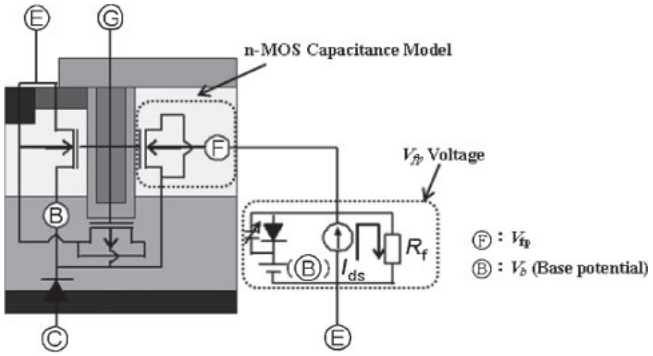

Fig. 10. Equivalent circuit of the developed model.

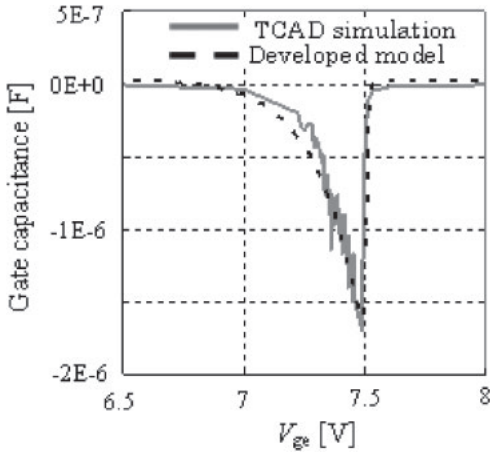

Fig. 11. Calculated gate capacitance with the developed model as a function of V_{ge} in comparison with 2D device simulation result.

collector current. The hole injection into the floating-base region as the collector current causes the potential increase. Thus, the potential node V_{fp} introduced is connected to the current source to describe this mechanism. However, the collector current flow into the floating base is stopped, when V_{fp} becomes higher than the n-base potential V_b. This effect is described by the connected MOSFET, for which the electrodes are connected either to V_b or V_{fb}. The hole injection even into the floating-base region occurs, because the collector contact extends over the device width. The injected holes have no way of going out or recombining in the p-Si base. Thus, they accumulate and increase V_{fb}. The balance between V_b and V_{fb} either continues or stops the hole injection. In HiSIM-IGBT, the base node V_b is calculated by solving the Kirchhoff law explicitly, namely, $I_c + I_b + I_e = 0$. Since the current flow from the floating base to the connected base beyond $V_{fb} > V_b$ is negligibly small in comparison with other current flows, the same Kirchhoff law is applied. Thus, all node potentials are precisely calculated, and the carrier movement within the device can be predicted consistently.

The developed equivalent circuit shown in Fig. 10 is written in the Verilog-A code and implemented with a commercial SPICE simulator. A calculation result of the negative C_{gg} due to the hole injection is shown in Fig. 11 in comparison with the 2D device simulation result. It is

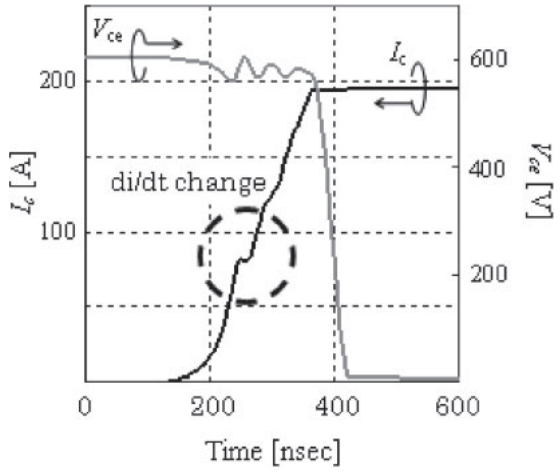

Fig. 12. Calculated switching turn-on waveform with developed model.

seen that the developed model reproduces the 2D device simulation result well. For better fitting, the resistance effect between the base potential and V_{fp} could be considered additionally. The neglected built-in potential between the floating base and the n-base could also play a role for better fitting.

4. Switching Simulation Results

Figure 12 shows the switching waveform simulated by using the newly developed model including the floating-base effect. At the early stage of switching-on, the gradient of I_c as a function of time t (di/dt) is early. Subsequently, di/dt changes in the second half, and the soft switching waveform is calculated. Such a phenomenon is simulated by considering the effect of the newly added model. Since positive and negative capacitances are intermingled, switching speed changes.

Moreover, the collector voltage becomes $V = -L \times di/dt$ as induced by the coil ingredient of a substrate.

5. Conclusions

We have developed the negative gate capacitance model observed in the IEGT structure based on the hole injection into the floating base. The model has been implemented in a circuit simulator and verified to be accurate. The characteristic switching waveform seen in the IEGT structure has also been considered in the circuit simulation.

Acknowledgements

The authors would like to thank Shuji Agatsuma, Hisato Kato, Hiromitsu Tanabe, and Mikimasa Suzuki for their useful discussions, and Ryotaro Miura for his help with measurements.

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Compact modeling of injection-enhanced insulated-gate bipolar transistor for accurate circuit switching prediction

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We have improved a compact model of an injection-enhanced insulated-gate bipolar transistor for accurate circuit switching prediction. The conventional model simulates the negative gate capacitance attributed to the floating-base effect. The relationship between the negative capacitance and the switching waveform is newly solved. The main development is concentrated on the floating-base region, the charge accumulation determined by the floating-base region structure, and the device model parameters. With the use of the model, it is demonstrated that the measured gradual slope switching performance of the studied device can be accurately predicted. It is shown that the gradual slope of I_c depends on the device parameters, which can be utilized for device optimization. © 2014 The Japan Society of Applied Physics

1. Introduction

In the development of automobiles, low fuel consumption and low pollution are crucial requirements. The hybrid system and electric vehicles are expected as a solution for such requirements. Power electronics are a driving force for development. High-performance power devices are keys for advanced power electronic products, where different power devices have been developed offering different application possibilities. Among them, the insulated-gate bipolar transistor (IGBT) realizes high current controllability together with a high breakdown voltage of over 500 V.[1)] The IGBT can be driven by voltage even though the main part consists of a bipolar part, and thus a low power consumption of the drive circuit can be realized. Owing to these advantages, the IGBT has been widely applied in inverter circuits of power electronics.[2,3)] Different IGBT structures have been developed according to application purpose.[4–10)] The injection-enhanced insulated-gate bipolar transistor (IEGT) has been developed in order to reduce the on-state voltage,[11,12)] enabling a smooth switching waveform (gradual slope switching) in comparison with the conventional IGBT. The difference between the two IGBT structures is that one is symmetrical and the other is asymmetrical, as shown in Fig. 1, where one side of the p-base region of IEGT is disconnected and floating. IEGT has been utilized for applications where reduced voltage overshoot is required.[13,14)] However, gradual slope switching leads to a large switching loss. To optimize the trade-off between the low overshoot and the low energy loss, accurate circuit simulations valid for investigating the optimization of IEGT are necessary.

We have developed the compact model HiSIM (Hiroshima-university STARC IGFET Modal)-IEGT based on the conventional IGBT model HiSIM-IGBT,[15–17)] on the basis of the surface-potential modeling approach, including the advanced MOSFET model HiSIM.[18–20)] The main development was modeling hole accumulation in the floating-base for C_{gg} calculations. We have introduced the potential node V_{fp} (see Fig. 1), which is solved together with other nodes under the Kirchhoff law. In this study, we have examined the application of switching simulation. With the use of the new improved HiSIM-IEGT model, we investigate here the switching performance of IEGT in comparison with measurements. The gradual slope switching mechanism and its device parameter dependence are demonstrated.

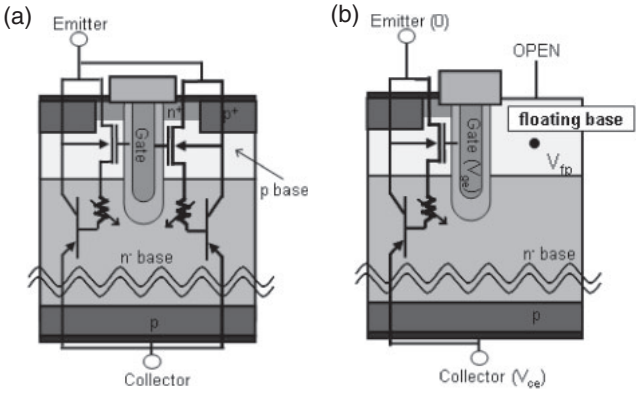

Fig. 1. Comparison of two IGBT structures: (a) symmetrical IGBT and (b) asymmetrical IEGT.

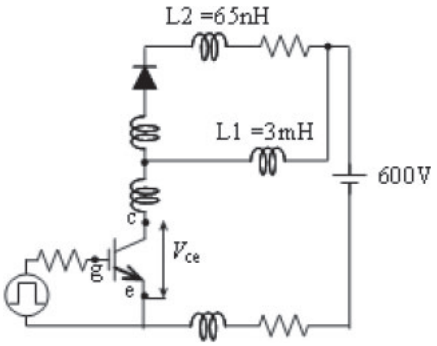

Fig. 2. Studied basic circuit and its element values.

2. Measurement and simulation results

Figure 2 shows the switching circuit studied, and Fig. 3(a) shows a comparison of the measured results with the results of the simulation with the original HiSIM-IGBT valid for the

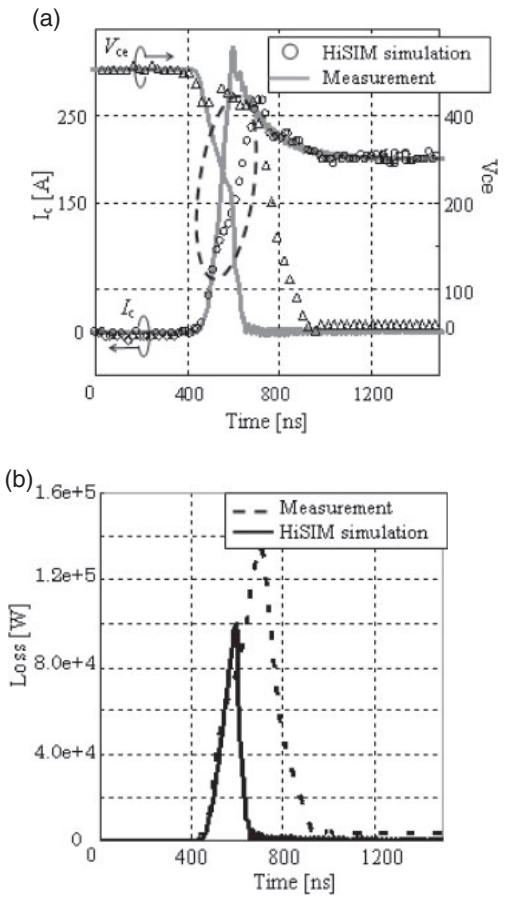

Fig. 3. Measured transient characteristics in comparison with simulation results obtained with HiSIM-IGBT without considering hole accumulation. (a) Switching wave form. (b) Switching loss.

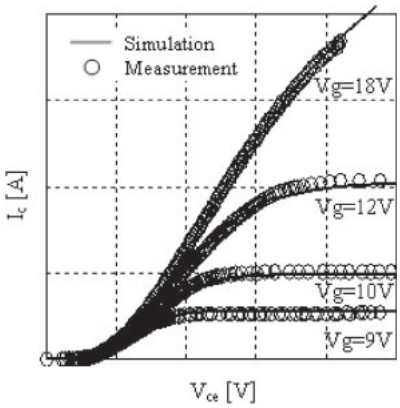

Fig. 4. Measured I_c–V_{ce} characteristics and simulation results of HiSIM-IGBT.

symmetrical structure. The model parameters of HiSIM-IGBT were determined from the measured I_c–V_{ce} characteristic, as shown in Fig. 4. The measured waveform of the collector current I_c slope (dI/dt) changes in the middle of the switching process, and a gradual slope switching behavior is realized. Since the simulation result shows a clear deviation from the measured waveform, it appears that the loss calculation error is large, as shown in Fig. 3(b). It is not suitable for the switching prediction of the energy loss. The

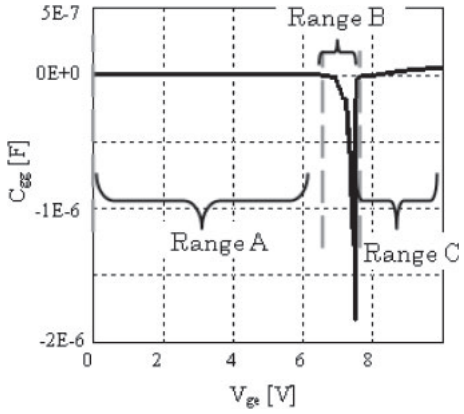

Fig. 5. Two-dimensional device simulation results of C_{gg}. Ranges A and C show positive values. Range B shows a negative value.

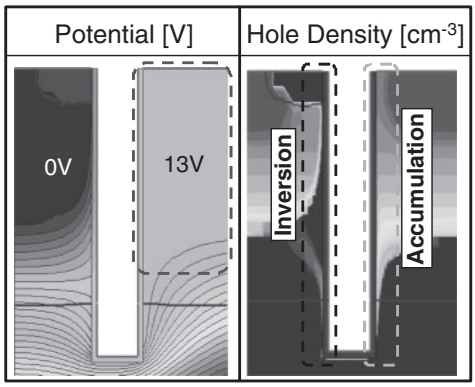

Fig. 6. Two-dimensional-device simulation results of electrostatic potential and hole-density distributions around the gate ($V_{ge} = 7.4$ V, $V_{ce} = 600$ V).

original HiSIM-IGBT does not consider the floating-base effect. The difference between the measured and calculated waveforms is attributed to the IGBT and IEGT structural differences.

3. Switching characteristics of IEGT structure

Figure 5 shows two-dimensional numerical device simulation results of the IEGT total gate capacitance,[21] which becomes positive or negative, depending on the range of the gate voltage.[22–25] When the gate voltage is varied from 0 to the threshold voltage (range A), the gate capacitance becomes positive. However, a negative capacitance is observed in the range between the threshold voltage and about 7.5 V (range B). At a gate voltage of over 7.5 V (range C), the gate capacitance becomes positive again. It has been demonstrated that the negative capacitance is induced by hole accumulation, as can be seen from the two-dimensional numerical device simulation result shown in Fig. 6. Figures 7(a) and 7(b) respectively show the simulation results of the I_c and V_{ge} waveforms during switching turn-on timing. It seems that the slope of I_c changes in the middle of the switching process. The change is attributed to the change in the capacitance sign. The gate voltage change at the time of switch turn-on is compared with the gate capacitance change. During the gate voltage change from 0 to the threshold voltage, the gate capacitance remains positive,

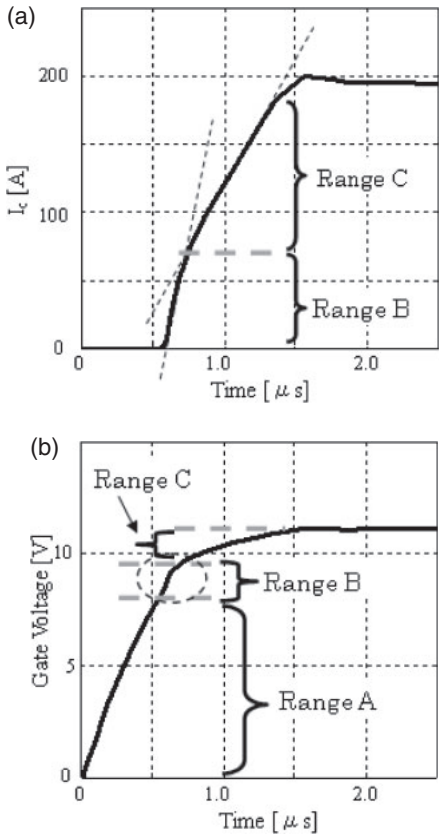

Fig. 7. Two-dimensional device simulation result of switch turn-on. (a) I_c current. (b) Gate voltage.

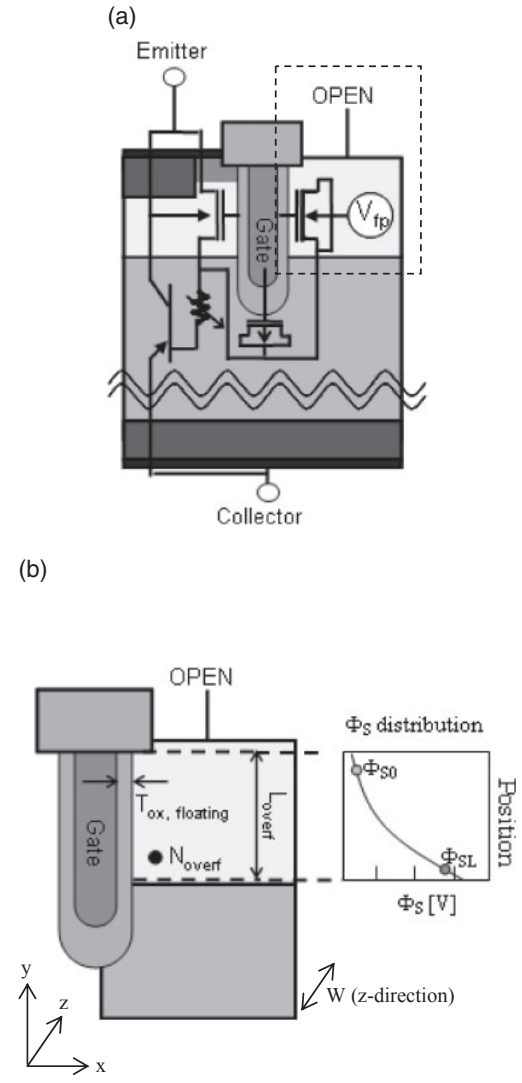

Fig. 8. (a) Equivalent circuit of the IEGT model developed. (b) Parameter of floating-base region.

indicating to range A of the gate capacitance. Next, the gate voltage change from the threshold voltage to about 7.5 V determines the range where the negative capacitance occurs. This indicates range B of the gate capacitance. The slope of the gate voltage increases under the influence of the negative capacitance. With increased gate voltage, the collector current starts to flow abruptly. When the gate voltage becomes higher than 7.5 V, the capacitance becomes positive again (range C), which results in a reduction in the gate voltage buildup rate as well as in a current increase. There is a strong relationship between the switching waveform and the negative capacitance and gate voltage range.

4. Floating-base region structure modeling and calculation result

The conventional HiSIM-IGBT is constructed by combining the surface-potential-based MOSFET part and the bipolar junction (BJT) transistor part, considering the carrier distribution within the base region explicitly.[14–16] Those two parts are connected by a conductivity-modulated base resistance, as schematically shown in Fig. 1(a). Thus, the model considers the potential distribution in the whole device by solving the introduced internal potential nodes self-consistently. All device characteristics are calculated with the node potentials.

An important element determining the switching performance of the IGBT is the gate capacitance. The MOSFET gate capacitance consists of the main IGBT capacitance. The overlap capacitance of the n-base region at the bottom of the trench gate must be considered as part of the MOSFET capacitance. The HiSIM-IGBT is used to calculate this trench-bottom nonlinear MOS capacitance as a function of the node potential explicitly together with the intrinsic MOSFET part.

The floating-base effect is modeled by considering the charge accumulation within the region in addition to the HiSIM-IGBT, as shown in Figs. 8(a) and 8(b), where the node V_{fp} is introduced to model the accumulation charge explicitly. Figure 9 shows the relationship among C_{gg}, the floating-base voltage V_{fp}, and the collector current for the IEGT structure. The node V_{fp} potential is determined by the amount of accumulated charges, $Q_{g,floating}$, which is also determined by the collector current. The collector current is determined by the base current, namely, the drain current of the MOSFET. To model the current flow from the floating-base region to the bipolar part after completing the charge accumulation for a given gate voltage, the bulk node of the new modeled n-MOS capacitor is connected to V_{fp}. The source node is connected to the upside potential of the emitter side n-base region, V_b. The base node V_b and V_{fp} are calculated by solving the Kirchhoff law explicitly, namely, $I_c + I_b + I_e = 0$. The additional equivalent circuit shown in

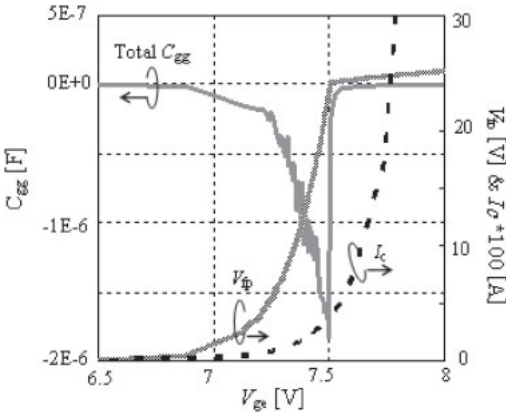

Fig. 9. Two-dimensional device simulation results of C_{gg}, V_{fp}, and I_c for floating-base structure.

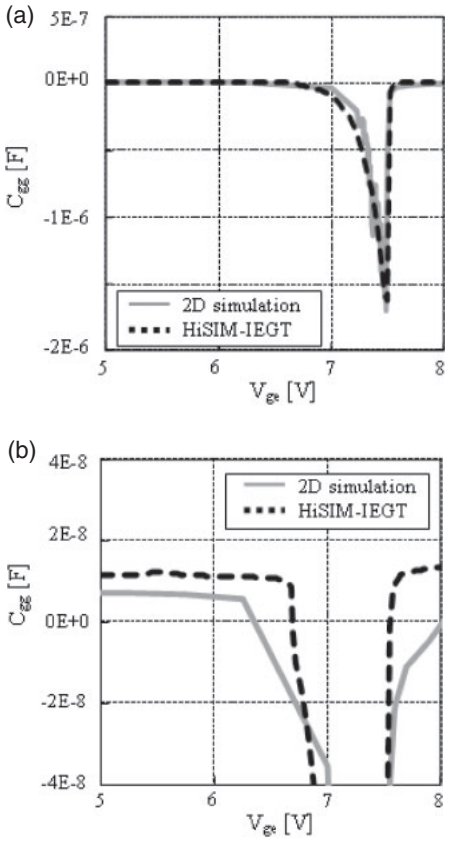

Fig. 10. Gate capacitance calculated with HiSIM-IEGT model and two-dimensional device simulation result.

Fig. 8 is added in the conventional HiSIM-IGBT and tested with a SPICE simulator. The negative C_{gg} is much larger than the positive C_{gg}, as shown in Fig. 10. The total C_{gg} is dominated by the negative C_{gg} between 7 and 8 V, during the hole accumulation.

The negative gate capacitance induced during switching is very important for simulating switching by considering the accumulation charge. The floating-base charge equation is written with the calculated Φ_S as Eq. (1) under the depletion and accumulation conditions, and under the inversion condition Eq. (2), where $C_{ox,foating} = T_{ox}/T_{ox,floating}$:

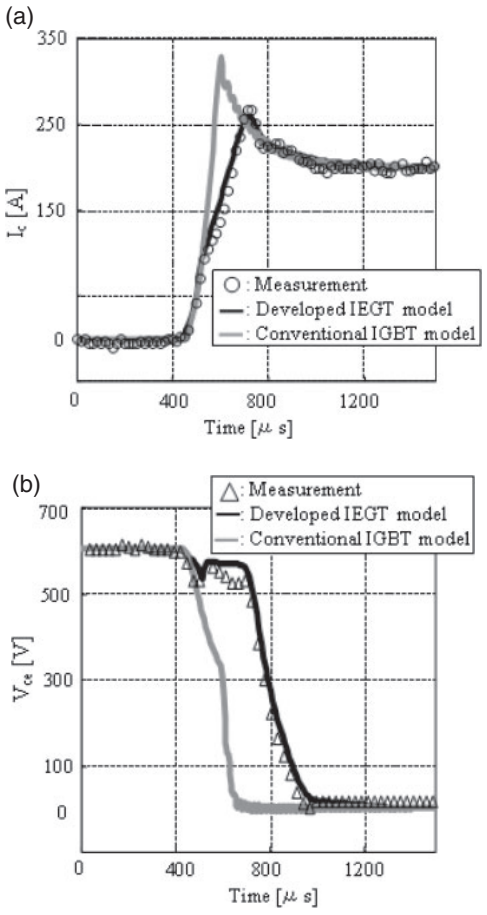

Fig. 11. Comparison of two calculated switching turn-on waveforms and measurement results. The IEGT model developed is modeled by the floating-base effect. (a) I_c and (b) V_{ce} waveforms.

$$Q_{g,floating} = W \times L_{overf}\{(2\varepsilon_{si}qN_{overf}/\beta)^{0.5} \times (\beta(\phi_S + V_{fp}) - 1)^{0.5}\}, \quad (1)$$

$$Q_{g,floating} = W \times L_{overf} \times C_{ox,floating}(V_{gs} - V_{fb,flating} - \phi_S), \quad (2)$$

where the surface potential Φ_S is calculated by solving the Poisson equation within the floating-base region. Here, $T_{ox,floating}$ and L_{overf} are the oxide thickness and oxide length of the floating-base region, respectively. The electron charge is defined by q. The Boltzmann constant and the lattice temperature in Kelvin are k and T, respectively. The inverse of the thermal voltage is written as $\beta = q/kT$. N_{overf} and $V_{fb,floating}$ are the base impurity concentration and the flatband voltage of the floating-base region respectively. By adjusting the parameter about the floating-base region, it can respond to different sizes of the IEGT structure.

Figure 11 shows the switching waveform simulated with the developed HiSIM-IEGT model in comparison with simulated results and measurement data obtained using the conventional HiSIM-IGBT model. The new HiSIM-IEGT developed models the floating-base effect. On the other hand, the conventional HiSIM-IGBT model does not model the floating-base effect. The circuit shown in Fig. 2 is investigated. It is seen that the measured gradual slope switching behavior observed in the collector current I_c is accurately reproduced. Furthermore, the collector voltage V_{ce} is also well reproduced with a change of the I_c waveform. Figure 12

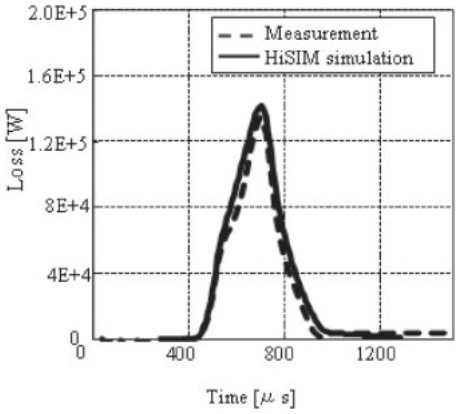

Fig. 12. Comparison of calculated switching turn-on losses.

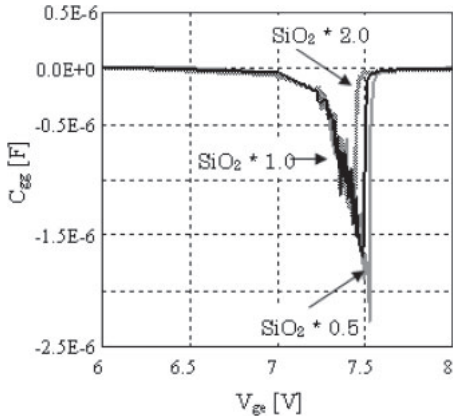

Fig. 14. Two-dimensional device simulation result of the SiO_2 thickness dependence of C_{gg}.

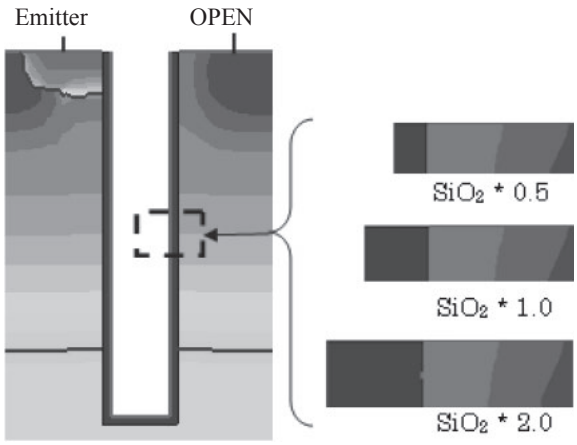

Fig. 13. Image of SiO_2 thickness change pattern.

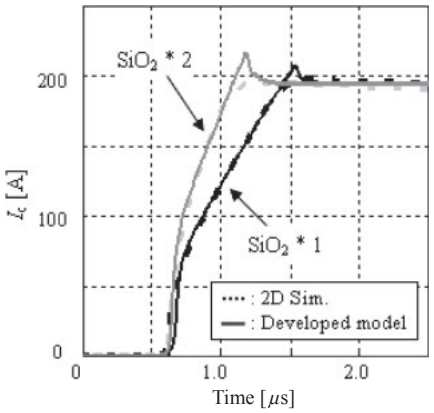

Fig. 15. Comparison of the switching waveform simulated with the model developed and that obtained by two-dimensional device simulation.

shows the calculated and measured switch turn-on losses. The loss calculation result is also well reproduced, verifying the applicability of the model to an inverter circuit design.

5. Discussion

The possible optimization of the device structure for switching waveforms with the use of the model developed is discussed. The negative capacitance changes with the floating-base structure and also affects switching waveform. Figure 13 shows two-dimensional device simulation results of C_{gg} with SiO_2 thickness variation. It is seen that the negative C_{gg} markedly decreases with increasing SiO_2 thickness, as shown Fig. 14. The reason for this is the decrease in $Q_{g,floating}$ owing to the $T_{ox,floating}$ increase. Figure 15 a shows comparison of the simulated switching waveform simulated with the developed model with that obtained by the two-dimensional device simulation. Good agreement is obtained. From this result, it can be concluded that the gradual slope switching waveform depends on the floating-base structure. The IEGT switching performance can be optimized using multiple options to achieve the required characteristics.

6. Conclusions

A new HiSIM-IEGT model has been developed, which considers the floating-base effect. This model has been implemented in a circuit simulator and verified to simulate the gradual slope switching characteristics accurately. It is verified that the switching waveform changes owing to the structural change of the floating-base region.

Acknowledgements

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PAPER

Compact Modeling of Injection Enhanced Insulated Gate Bipolar Transistor Optimized Influenc of Frequency Dependent

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Hans JÜRGEN MATTAUSCH[††], ***and*** **Mitiko MIURA-MATTAUSCH**[††], ***Members***

SUMMARY We have improved a compact model for the injection-enhancedinsulated-gate bipolar transistor for inverter circuit simulation. The holeaccumulation of floating-bas region and potential change are modeled. It turned out that negative capacitance which occurs by floating base region has the dependence of frequency. It is necessary to consider the frequency dependence of the total gate capacitance for transient simulation. We analyzed the relationship between negative gate capacitance and current rise rate at the switch turn-on timing and device structure. The development model simulation result is well reproduced I_c and V_{ce} of measurement data, and the switching loss calculation accuracy is improved.

key words: *IGBT, HiSIM, SPICE, compact model*

1. Introduction

Power electronics are very frequently used in home electronics and automobile field High performance power devices are keys for advanced power electronic products. Required performances for the power device are low power loss as well as low noise. Here there are several types of power devices developed such as bipolar transistor, DMOS, super junction MOSFET and insulated-gate bipolar transistor (IGBT). Among them IGBT realizes the high current controllability together with the high breakdown voltage of over 500 V [1]. Even though IGBT is driven by applied voltage on the gate of the MOSFET part, the main part consists of a bipolar transistor, and thus the low power consumption of the drive circuit can be realized. Due to the advantage, IGBT has been widely applied for inverter circuits of power electronics [2], [3]. In order to further improve the performance, different IGBT structures have been developed according to different application purposes [4]–[9]. The injection-enhanced insulated-gate bipolar transistor (IEGT) has been developed in order to reduce the on-state voltage [10], enabling a smooth switching waveform (gradual slope switching) in comparison to the conventional IGBT. Abrupt switching (hard switching) causing destruction and noise of circuits is intended to avoid in the automotive application field Figure 1 shows the schematic structure of IEGT, where one side of the p-base region is floated Therefore structure becomes asymmetric. It is known that this structure induces the injection enhancement effect [10]. Since IEGT has been utilized for applications where reduced voltage overshoot is required the gradual slope switching of IEGT is well applicable [11], [12]. However, it causes at the same time large switching loss. To optimize the trade-off between the low overshoot and the low energy-loss, accurate circuit simulations valid for investigating the optimization of IEGT is inevitable.

Here we developed the compact model HiSIM-IEGT based on the conventional IGBT model HiSIM-IGBT [13]–[15]. HiSIM-IGBT has been developed based on the surface-potential modeling approach including the advanced MOSFET model HiSIM [16]–[18]. The main development of HiSIM-IEGT is modeling the hole accumulation in the floating-bas region, which is the origin of the injection enhancement. We have introduced the potential node of the floating-bas potential V_{fp} (see Fig. 1), which is solved together with other nodes under the Kirchhoff law. Since the main advantage of IEGT is the gradual slope switching, our focus is given on the transient characteristics of the hole accumulation phenomenon. For the purpose we analyzed capacitance characteristics in detail. Finally we verify the switching performance of the developed HiSIM-IEGT in comparison to measurements.

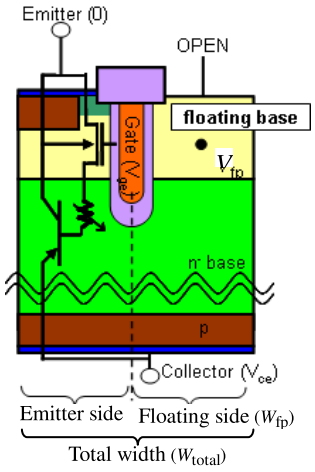

Fig. 1 Schematic of the asymmetric injection-enhanced insulated-gate bipolar (IEGT) structure.

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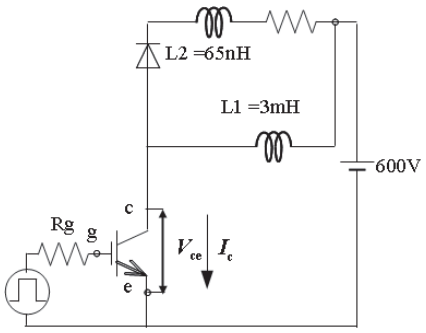

Fig. 2 Studied basic switching circuit.

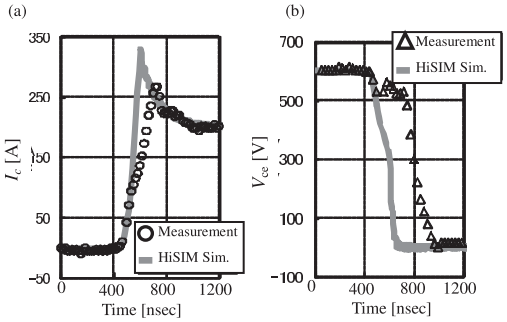

Fig. 3 Measured switching waveform in comparison to simulation results with HiSIM-IGBT without considering the hole accumulation under turn-on condition. (a) I_c, and (b) V_{ce} as a function of time.

2. Switching Response of Floating-base

Figure 2 shows the studied basic switching circuit that is assumed to handle only one phase of a three-phase motor control circuit. Figures 3(a) and (b) compare measured switching turn-on of the collector current I_c and the collector-emitter voltage V_{ce} waveform, respectively. For comparison simulation results of the original HiSIM-IGBT valid for the symmetrical structure are also depicted. The static DC characteristics of IEGT can be modeled using HiSIM-IGBT, where the model parameter values were extracted from the measured $I_c - V_{ce}$ characteristic of IEGT. As can be seen in Fig. 3(a), the transient characteristics of the IEGT structure cannot be reproduced by HiSIM-IGBT even though the DC characteristics are well reproduced. It is observed that the measured waveform of the collector current I_c of IEGT is not as steep as that of IGBT, and thus the softer switching behavior can be realized. Since the simulation result of the conventional symmetrical IGBT cannot capture the measured waveform, it is expected that the loss calculation error becomes large as can be seen in Fig. 4. The difference between the measured and calculated waveforms is attributed to the floating-bas effect, which is not considered in the original HiSIM-IGBT.

Figure 5 shows the turn-off waveform of the circuit shown in Fig. 2 under the same bias conditions as Fig. 3. The calculated turn-off waveform is well reproduced with the original HiSIM-IGBT. The small deviation observed in the surge of V_{ce} and the slope of the I_c could be attributed to external contributions of the measured system which are not accurately extracted. Thus it is concluded that the specifi effect observed in IEGT is pronounced only under the turn-on condition.

Figure 6 shows 2D numerical device simulation results of the total gate capacitance (C_{gg}) of an IEGT as a function of the gate voltage V_{ge} [19], [20]. It has been observed that the total capacitance can be negative for V_{ge} <7.5 V [21], [22]. The total C_{gg} consists of different parts of the gate oxide. Namely, the gate oxides are divided into three parts, the emitter side (Gate l), the bottom region (Gate b) and the floating-bas side (Gate r). It can be seen that the negative C_{gg} of the Gate r dominates the total C_{gg}. The value of 7.5 V is approximately the threshold voltage of the collector current.

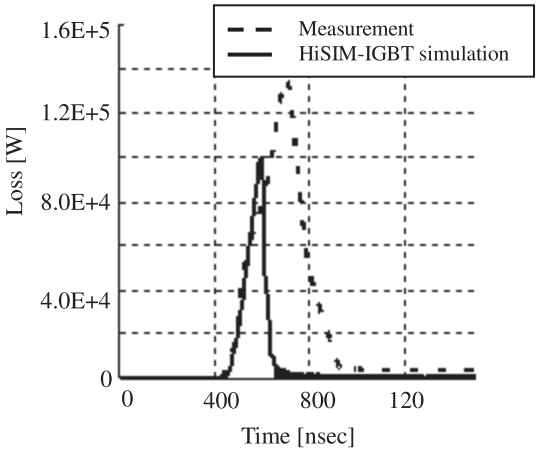

Fig. 4 Comparisons of measured switching loss in comparison to simulated loss with HiSIM-IGBT.

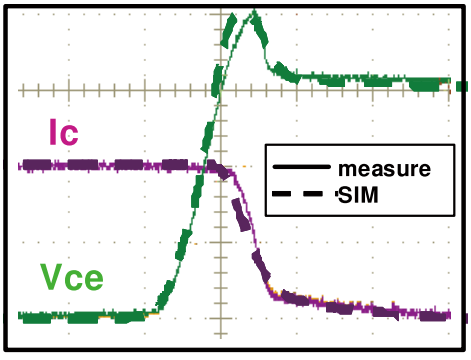

Fig. 5 Measured switching waveform in comparison to simulation results with HiSIM-IGBT under turn-off condition.

Figure 7 depicts 2D device simulation results of I_c and the gate current under the turn-on condition. For the gate current contributions from different parts are depicted separately. It is seen that the negative current fl ws in the floating-bas side (Gate r) at the beginning stage of the collector current fl w. This negative current is the origin of the negative capacitance of C_{gg}. By switching on the gate the collector current starts to fl w due to the electron injection from the emitter. This causes the positive C_{gg} at Gate l. The

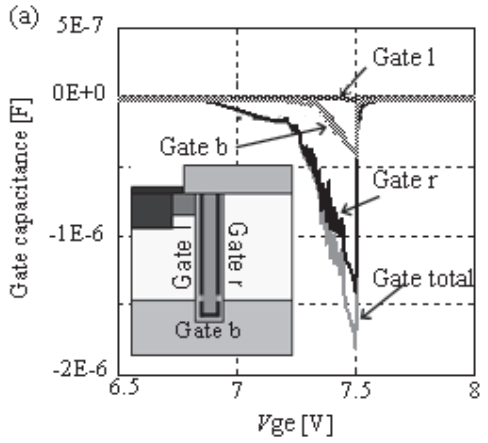

Fig. 6 2D device simulation result of IEGT gate capacitance for the floating-bas structure at V_{ce}=600 V, freq=0.001 Hz, as a function of V_{ge}.

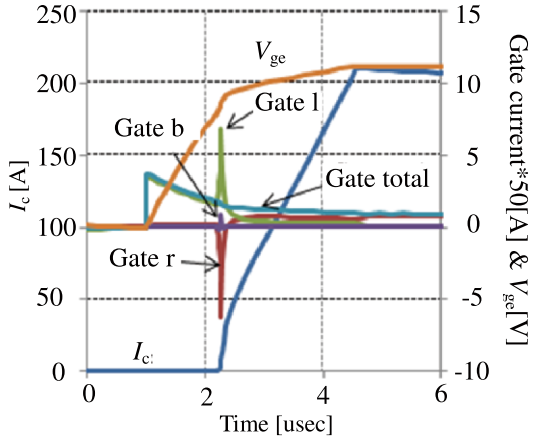

Fig. 7 2D device simulation result of I_c and different gate currents switch turn-on condition (current rise rate:di/dt=82.5 A/us).

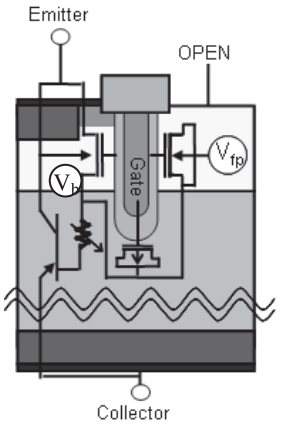

Fig. 8 Equivalent circuit of the developed IEGT model.

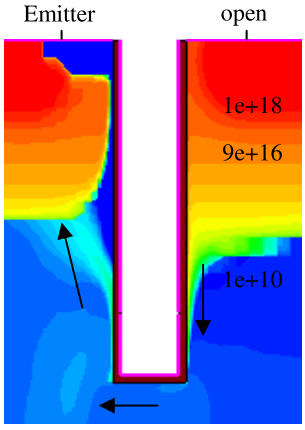

Fig. 9 Simulated hole-density distribution with a 2D device simulator at V_{ce} =600 V, and V_{ge} = 7.8 V.

collector current fl w induces the hole accumulation underneath Gate r. This is the origin of the negative C_{gg}. Thus our focus is given on modeling the negative C_{gg}.

3. Floating-base Model

The conventional HiSIM-IGBT is constructed by combining the surface-potential-based MOSFET part and the bipolar junction transistor (BJT) part, where the carrier distribution within the based region is explicitly considered [13]–[15]. Those two parts are connected by conductivity-modulated base resistance as schematically shown in Fig. 8. Thus the model considers the potential distribution within the whole device by solving the introduced internal potential node V_b self-consistently. All device characteristics are calculated with the node potential value together with those of the external nodes.

An important element determining the switching performance of IEGT is the gate-capacitance characteristics. The MOSFET gate capacitance (Gate l) consists of the main IGBT capacitance. The overlap capacitance of the n^- base region (Gate b) together with Gate l is explicitly calculated as a function of the node potentials V_{ge} and V_b.

Beyond the threshold condition of the MOSFET, the electron current begins to fl w from the emitter. The collector hole current fl ws toward the emitter as well as into the floating-bas region. The holes fl w into the floating-bas is accumulated, causing the potential value of the floating-bas side higher. When the floating-bas potential V_{fp} becomes higher than V_{ge}, the floating-bas side forms the accumulation condition. On the other hand, the inversion condition is formed underneath Gate l. These charge storages of different types (electrons underneath Gate l and holes underneath Gate r) cause different signs of the gate current.

The floating-bas effect is modeled by considering the charge accumulation within the region in addition to HiSIM-IGBT as shown in Fig. 8, where the node V_{fp} is introduced to calculate the stored charge explicitly.

Figure 9 shows hole density contours at V_{ge} = 7.8 V. Under the bias condition the amount of holes to be accumulated limits the further hole fl w into the floating-base Then holes are starts to fl w along gate into the emitter. Thus, the potential increase of floating-bas is stopped.

4. Frequency dependent of gate capacitance

Figure 10 shows 2D-device simulation results of frequency dependence of the total C_{gg} as a function of V_{ge}. It is seen that the magnitude of the negative C_{gg} is reduced with increased frequency. Figure 11 depicts the frequency dependence of the minimum value of the total C_{gg}. It is seen that the minimum value remains constant for low frequency. However, it is observed that the minimum diminishes rapidly for frequency faster than 1 kHz. Beyond frequency = 100 kHz the negative C_{gg} disappears completely. This frequency dependence of C_{gg} is attributed to the hole transit delay injected from the collector and accumulated underneath Gate r (see Fig. 6) [23], [24].

If V_{ge} is switched faster than the time for holes reaching the floating-bas gate, C_{gg} remains zero. In actual circuit operations, turn-on and turn-off are repeated and thus the total C_{gg} is dependent on the switching speed. Therefore the negative C_{gg} under real circuit operation can never be large sas observed under the DC condition.

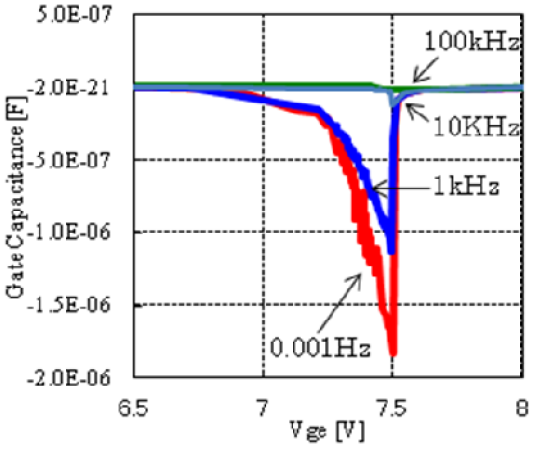

Fig. 10 Total gate capacitance C_{gg} of 2D device simulation results as a unction of the gate voltage V_{ge} at V_{ce} = 600 V. Frequencies applied for the simulation are depicted.

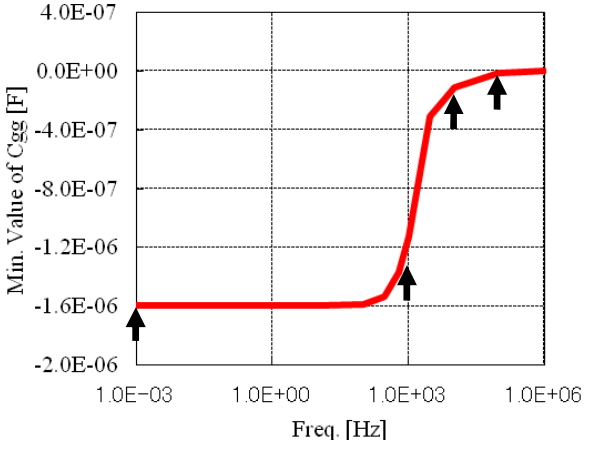

Fig. 11 2D device simulation result of the minimum C_{gg} value as a function of the frequency applied at V_{ce} = 600 V.

Figure 12 shows the floating-bas width dependence of the minimum value of the total C_{gg}. The minimum value is changed as a function of the floating-bas width W_{fp} (see Fig. 1). Thus, it is seen that the C_{gg} characteristic is strongly influence by the frequency and floating-bas structure.

Figure 13 summarizes the relationship between the floating-bas width W_{fp} and the current rise time di/dt. The reason for plotting as a function of di/dt is due to the present investigation of switching. The di/dt value studied in Fig. 7 corresponds approximately to the frequency of 10 kHz. The width W_{fp} is normalized by the total width W_{total} (see Fig. 1). The "×" mark represents the condition that the negative gate current occurs. On the other hand, the "○" mark is the condition that the negative gate current disappears. When the ratio of W_{fp} to W_{total} becomes large, the negative C_{gg} is observed even at fast switching speed. Thus it can be concluded that the resulting I_c waveform is very much dependent on the structure as well as switching speed. The line depicted in Fig. 13 denotes the boundary for enabling the gradual slope switching.

5. Simulation Result

Figure 14 shows the switching waveform simulated with the

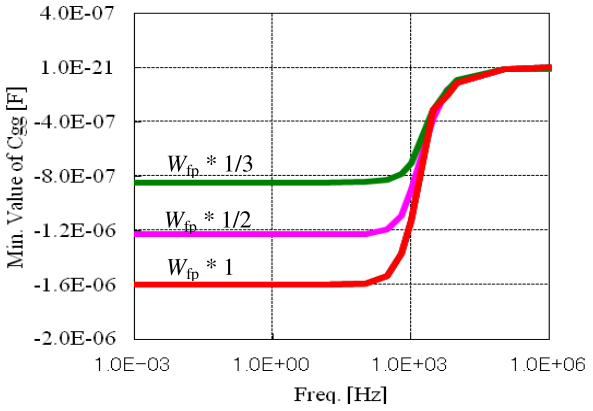

Fig. 12 2D device simulation result. The floating-bas width dependence of the minimum value of total C_{gg} at V_{ce} = 600 V.

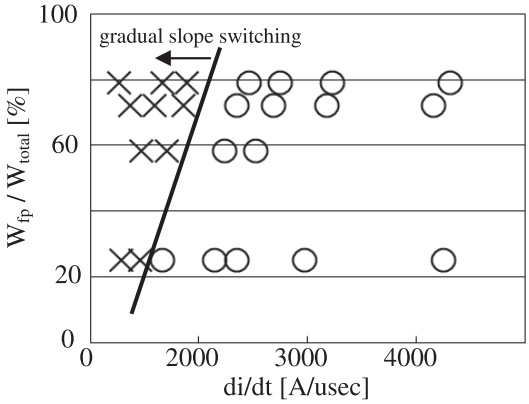

Fig. 13 2D device simulation result of the matrix of negative gate current appearance.

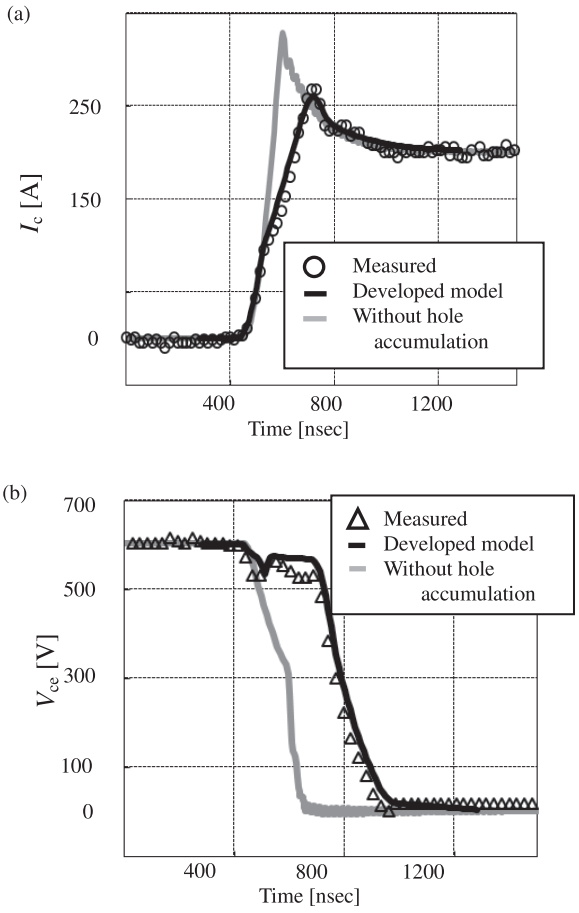

Fig. 14 Comparison of calculated switching turn-on waveform with measurement results (a) I_c waveform and (b) V_{ce} waveform.

developed IEGT model including the floating-bas effect in comparison to the measured data. Namely the reduction of the negative C_{gg} equivalent to the value at frequency = 100 kHz in Fig. 10 is considered for the simulation. The circuit shown in Fig. 2 is investigated. The free wheel diode model HiSIM-Diode model is applied [25]. The model parameters are extracted so that the reverse recovery wave form is accurately reproduced. It is seen that the measured gradual slope switching behavior observed in the collector current I_c is accurately reproduced. Furthermore, the collector voltage V_{ce} is also well reproduced with change of I_c waveform. Figure 15 shows calculated and measurement switching turn-on loss. The loss calculation result is also well reproduced, and thus the developed model is confirme to be applicable for accurate inverter circuit design.

6. Conclusions

The HiSIM-IEGT model has been developed, which consider the floating-bas effect. The model can reproduce the negative gate capacitance, which is the important feature of IEGT. The developed model has been implemented in a circuit simulator and verifie the accuracy. It has been shown that the frequency dependence of the gate capacitance is

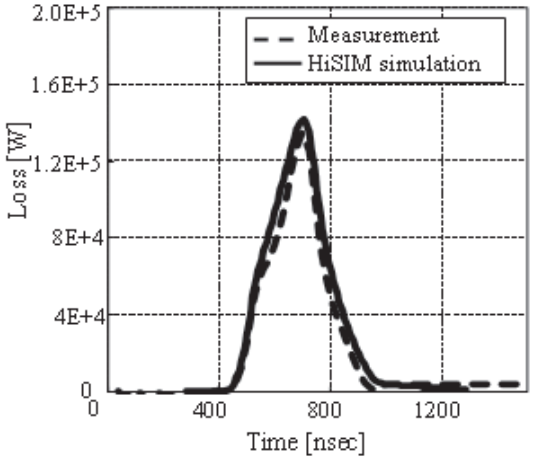

Fig. 15 Comparison of calculated switching turn-on loss.

shown to be an essence for characterizing the switching performance of IEGT. Switching simulation result reproduces measured I_{ce} and V_{ce} waveform as well as switching loss. It is verifie that the developed model can be utilized to optimize the ideal switching waveform, balancing the power loss and surge of I_{ce} and V_{ce}. The model can be further utilized to optimize the switching speed for achieving appropriate circuit performance. For the purpose further verificatio of the carrier transit time within the device must be investigated.

Acknowledgments

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学会発表

1. Compact Modeling of Floating-Base Effect in IGBT Based on Potential Modification by Accumulated Charge
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   International Conference on Solid State Devices and Materials (SSDM 2012), Kyoto, Japan (2012).

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3. Modeling of Injection Enhanced IGBT for Accurate Prediction of Switching Performance
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4. Role of Carrier Response Delay on Switching Performance of Injection-Enhanced IGBT
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   International Conference on Solid State Devices and Materials (SSDM 2013), Fukuoka, Japan (2013).

Compact Modeling of Floating-Base Effect in IGBT Based on Potential Modification by Accumulated Charge

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Abstract

We have developed a compact model of the Injection-Enhanced Insulated-Gate-Bipolar Transistor applicable for circuit optimization. The main development is modeling the hole accumulation in the floating-base region. It is demonstrated that observed negative gate capacitance is well reproduced with the developed model.

1. Introduction

The IGBT (Insulated-Gate-Bipolar Transistor) structure realizes the high current controllability together with the high breakdown voltage. Because of these advantages, the IGBT structure has been widely applied for inverter circuits of power electronics. Therefore many descendants of IGBT have been developed according to the different applications purposes. The IEGT (Injection-Enhanced Insulated-Gate-Bipolar Transistor) structure has been developed in order to reduce the on-state voltage [1], which results in the soft switching waveform in comparison to that of IGBT. Thus, IEGT has been applied to the area where reduced voltage overshoot is required. However, the soft waveform causes large switching loss at the same time. To optimize the trade-off between the low overshoot and the low energy-loss, accurate circuit simulation for investigating the switching performance is inevitable.

HiSIM-IGBT has been developed for simulating circuit performances, which solves the potential distribution within IGBT explicitly [2]. However, it considers the symmetrical IGBT structure. The purpose of this investigation is to extend HiSIM-IGBT for the asymmetrical IEGT structure (see Fig. 1). For the purpose we consider the accumulated charge induced in the floating- base region explicitly.

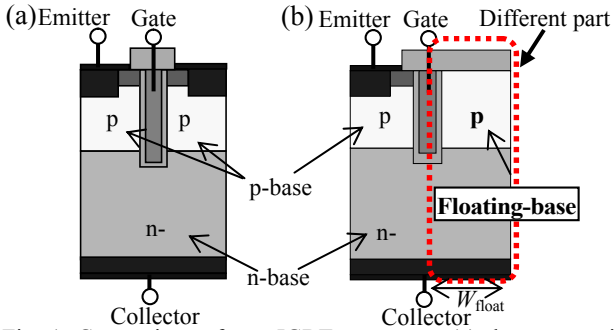

Fig. 1. Comparison of two IGBT structures, (a) the symmetrical IGBT structure, and (b) the asymmetrical IEGT structure.

2. Switching Response of Floating-Base

Fig. 2a shows the studied basic circuit with its element values. Measurements and results with HiSIM-IGBT for the asymmetrical structure are compared in Fig. 2b. The difference between the two waveforms denoted by a dashed circle is attributed to the floating-base effect.

The floating-base effect is investigated with 2D-device simulations [3]. Fig. 3 shows simulated gate capacitance C_{gg} divided into different contributions. Fig. 4 shows equi-hole-density contours around the gate oxide. The contacted p-base side forms the inversion layer, when V_{ge} reaches the threshold voltage (V_{ge}=7.4V). On the other hand, the floating-base side does not form the inversion layer at V_{ge}=7.4V. Beyond the threshold condition the collector current flows into the floating-base as well, and increases the potential drastically. This hole accumulation causes "negative capacitance [4, 5]".

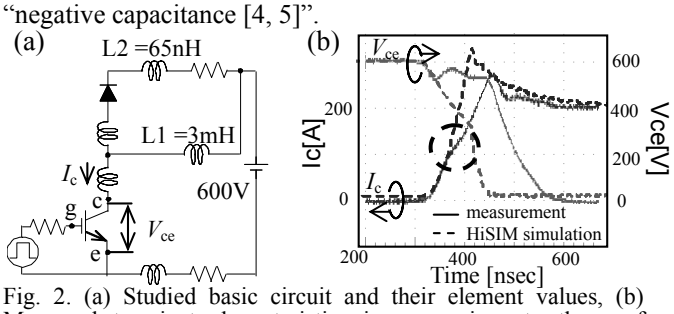

Fig. 2. (a) Studied basic circuit and their element values, (b) Measured transient characteristics in comparison to those of simulation results with original HiSIM-IGBT.

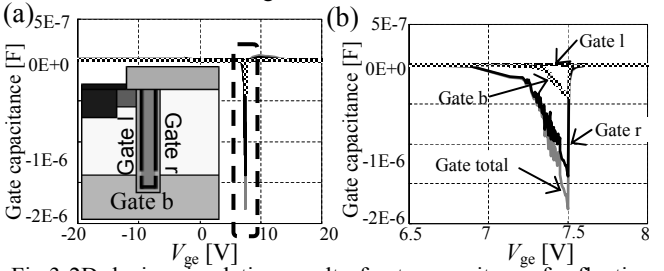

Fig.3 2D-device simulation result of gate capacitance for floating -base structure at V_{ce}=600V, freq=0.001Hz, V_{ge} sweep. (b) Zoomed result denoted by a dashed rectangle depicted in (a).

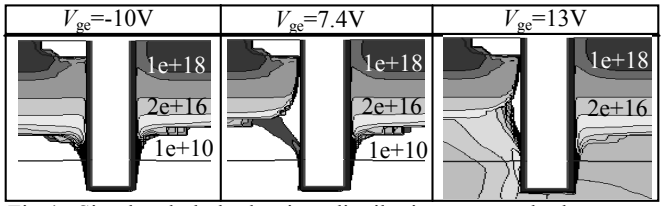

Fig.4 Simulated hole-density distributions around the gate. [/cm^3](V_{ce}=600V)

The negative capacitance reduces abruptly at V_{ge}=7.5V as shown Fig. 5a. This abrupt decrease of C_{gg} coincides with the saturation behavior of the floating-base potential V_{fp}. The hole accumulation charge changes the potential V_{fp}. Fig. 5b shows the width (W_{float}: see Fig. 1b) dependence of C_{gg}. Though the increase of W_{float} shows no influence, the decrease causes the delay of the switching from the accumulation to the depletion condition, because the total amount of the injected holes in the floating-base region is reduced with reduced W_{float}. Further increase of V_{ge} induces the inversion condition, which causes the positive C_{gg} as shown in Fig. 6.

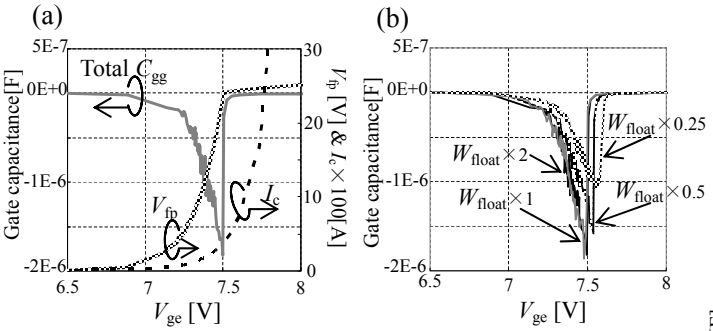

Fig. 5. (a) 2D-device simulation results of C_{gg}, floating-base voltage and I_c current for floating-base structure. (b) 2D-device simulation result of the width (W_{float}) dependence of C_{gg}.

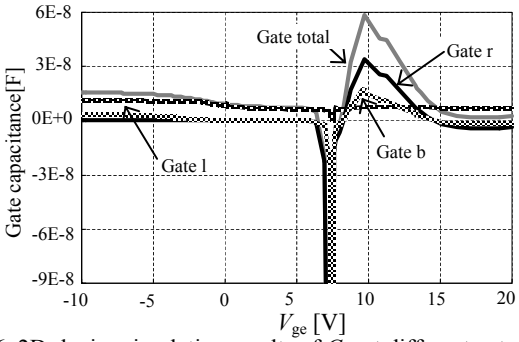

Fig. 6. 2D-device simulation results of C_{gg} at different gate parts.

3. Modeling of Floating-Base Effect

Modeling of the floating-base effect is done by considering the n-MOS capacitance as shown Fig.7, where V_{fp} is the node potential introduced to describe the floating-base effect induced by hole injection. The hole injection into the floating-base occurs because the base potential is higher than V_{fp} and continues until V_{fp} becomes larger than the internal base potential. In HiSIM-IGBT the base node is calculated by solving the Kirchhoff equation explicitly. Since all node potentials are precisely determined, the carrier movement within the device can be predicted in a consistent way. Once V_{ge} reaches the threshold condition and the collector current starts to flow, a large amount of the hole injection into the floating-base occurs and increase the V_{fp} potential drastically, resulting in the transition into the accumulation condition.

The developed equivalent circuit shown in Fig, 7 is written in the Verilog-A code and tested with a commercial SPICE simulator. A calculation result of the negative C_{gg} due to the hole injection is shown in Fig. 8 in comparison to the 2D-device simulation results. The model reproduces the 2D-device simulation result quite well. For better fitting, the resistance effect between the base potential and V_{fp} could be considered. The neglected built-in potential between the floating-base and the n-base could also play a role.

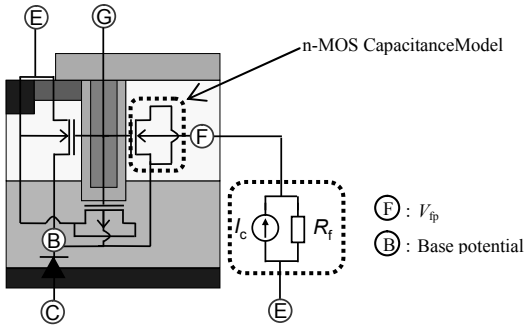

Fig. 7. Equivalent circuit of the developed model.

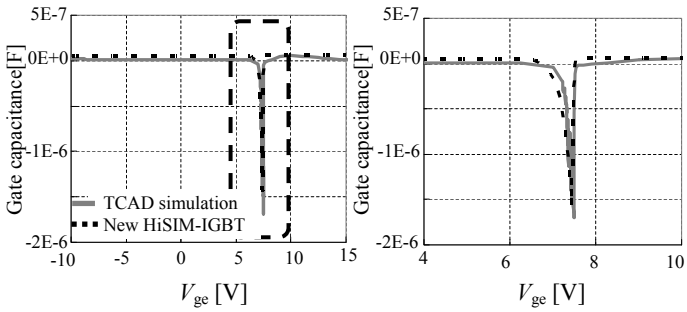

Fig. 8. Calculated gate capacitance with the developed model as a function of V_{ge} in comparison to 2D-device simulation result. (b) Zoomed result denoted by a dashed rectangle depicted in (a).

4. Conclusions

We have developed the negative gate capacitance model observed in the IEGT structure based on the hole injection into the floating-base. The model has been implemented into a circuit simulator and verified the accuracy.

5. Acknowledgements

The authors would like to thank Shuji Agatsuma, Hisato Kato, Hiromitsu Tanabe and Mikimasa Suzuki for their useful discussions, and Ryotaro Miura for his help with measurements.

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Floating-Base Effect Modeling for IGBT Structure Using Potential Modification

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The Injection-Enhanced Insulated-Gate-Bipolar Transistor developed for reducing the on-state voltage of the original Insulated-Gate-Bipolar Transistor is investigated. The main development is modeling the hole accumulation in the floating-base region which modifies the gate capacitance drastically. It is demonstrated that observed negative gate capacitance is well reproduced with the developed model.

I Introduction

Hybrid and Electric vehicles are attractive as an important solution for realizing the reduction of fuel consumption. Nowadays many power devices are used for better control for achieving reliable, safety, as well as economic automobiles. Among the power devices, the Insulated-Gate-Bipolar Transistor (IGBT) realizes the high current controllability together with the high breakdown voltage [1]. Because of these advantages, IGBT has been widely applied for inverter circuits of power electronics [2]. Therefore many descendants of IGBT have been developed according to different applications purposes. The Injection-Enhanced Insulated-Gate-Bipolar Transistor (IEGT) is one of the descendants and has been developed in order to reduce the on-state voltage [3, 4], and that structure also has the feature of the soft switching waveform in comparison to that of IGBT. Thus, IEGT has been applied to the area where reduced voltage overshoot is required [5, 6]. However, the soft waveform causes large switching loss at the same time. To optimize the trade-off between the low overshoot and the low energy-loss, accurate circuit simulation applicable for investigating the switching performance is inevitable.

Different IGBT models have been already developed and been used for various circuit designd [7, 8, 9]. However, the models are either lack of accuracy or not sufficient for stable circuit simulations. HiSIM-IGBT has been developed for simulating circuit performances [10, 11], which solves the potential distribution within IGBT explicitly under fully dynamic load conditions, through the surface-potential-based modeling approach including the advanced MOSFET model HiSIM [12, 13, 14, 15]. However, it considers the symmetrical trench-type IGBT structure (see Fig.1a), where both sides of the p-base are connected to the emitter. The purpose of this investigation is to extend HiSIM-IGBT for the asymmetrical IEGT structure (see Fig. 1b), where one side of the p-base is disconnected and floated. The purpose of this investigation is to model the IEGT characteristics based on the potential distribution in the floating-base region induced by applied voltages.

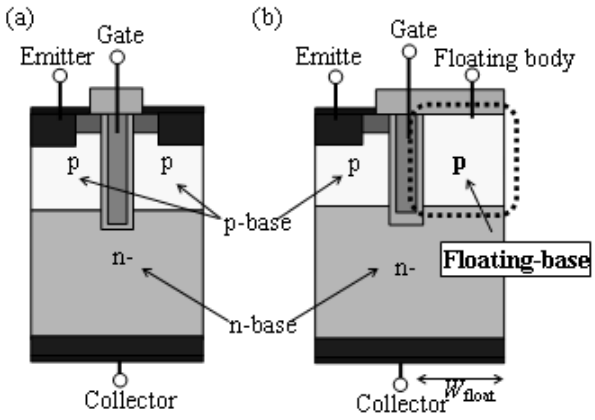

Fig. 1. Comparison of two IGBT structures, (a) the symmetrical IGBT structure, and (b) the asymmetrical IEGT structure.

Ⅱ. Switching Response of Floating-Base

Fig. 2a shows the studied basic circuit with its element values. Measurements and simulation results with the original HiSIM-IGBT for the symmetrical structure are compared in Fig. 2b. The threshold voltage of the studied IGBT is 6.5V, and the model parameter values of HiSIM-IGBT were extracted from measured I_c-V_{ce} characteristics. It is seen that the measured waveform of the collector current I_c is not steep for IEGT, and the soft switching is realized. On the contrary the model calculation result with HiSIM-IGBT shows no soft switching. The difference between the measured and calculated waveforms is attributed to the floating-base effect, which is not yet considered in HiSIM-IGBT.

The floating-base effect is investigated with 2D-device simulations [16]. Fig. 3 compares electrostatic potential contours for different gate voltages V_{ge} around the trench gate oxide. For the V_{ge}<Vth case the potential distribution in the emitter-connected base and the floating base are nearly the same. However, the gate control becomes completely different for two structures under the V_{ge}>=Vth condition when I_c begin to flow. Under the condition the potential value in the floating-base side becomes even higher than V_{ge}. However, the potential value does not exceed a certain value, namely 24.8V for the studied case, even with further increase of V_{ge}. Fig. 4 shows equi-hole-density contours for the same conditions as shown in Fig. 3. When V_{ge} reaches the threshold voltage (V_{ge} =6.5V), the contacted p-base side forms the depletion layer as well as the inversion layer under the gate as can be seen from the low hole concentration.

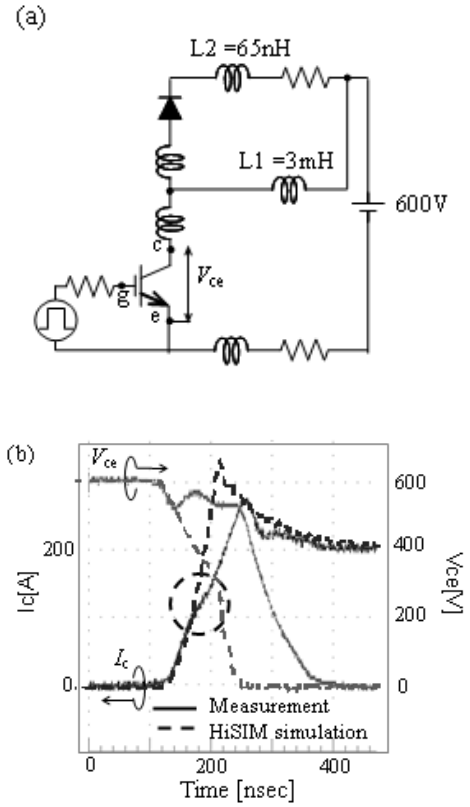

Fig. 2. (a) Studied basic circuit and their element values, (b) Measured transient characteristics in comparison to those of simulation results with original HiSIM-IGBT.

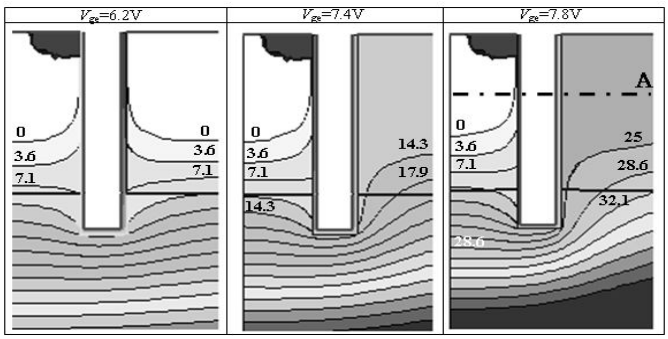

Fig. 3. Simulated electrostatic potential around the gate.

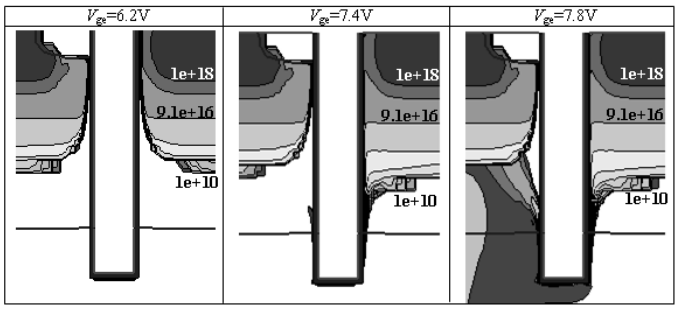

Fig. 4. Simulated hole-density distributions around the gate.

On the other hand, the hole-density contours in the floating-base side remain nearly unchanged. Except the depletion region at the n-base/p-base junction which is fulfilled by holes injected from the collector for V_{ge}>=Vth, and the contacted-base side forms the inversion layer and the non-contacted side forms the accumulation layer. Beyond the threshold condition the collector current flows into the floating-base region as well, and fulfills the whole region by holes. This hole injection into the floating base is stopped after a certain amount of holes occupy the region. Thus it can be concluded that the floating-base potential shown in Fig. 3 is determined by a balance created by carrier dynamics responding to the potential distribution within the whole IEGT.

The carrier response to the potential change can be investigated with the capacitance. Fig. 5 compares 2D numerical simulation results of C_{gg} for IEGT in comparison to that for IGBT. The humps around V_{ge}=10V observed for both structures are due to the resistive base effect under the on-current condition usually observed for power devices. A clear different between two structures is the sharp negative C_{gg}, which is observed only for the IEGT structure. Fig. 6 depicts separate contributions from different parts of the gate oxide to the total negative C_{gg}. It is seen that C_{gg} of the floating base (Gate r) dominates the total C_{gg}.

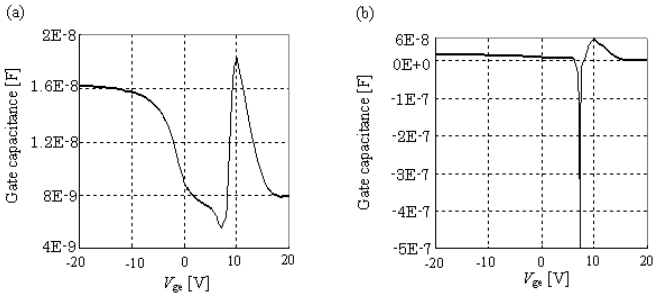

Fig. 5. 2D-device simulation of C_{gg}. (a) IGBT structure. (b) IEGT structure

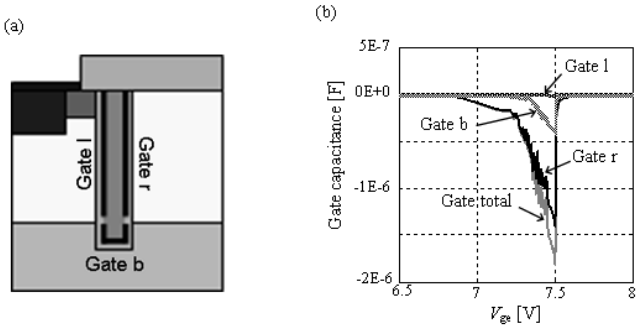

Fig. 6. (a) The gate contact is divided into different contributions. (b)2D-device simulation result of gate capacitance for floating -base structure at V_{ce}=600V, freq=0.001Hz, V_{ge} sweep.

Ⅲ. Modeling of Floating-Base Effect

Origin of the "negative capacitance [17, 18]" is attributed to the hole accumulation in the floating base. To model the charge distribution at Gate r, a potential node V_{fp} is investigated. The node is set at the surface of the floating base as shown in Fig.1b. Fig. 7a compares the relationship among different values as a function of V_{ge}. Beyond V_{ge}=Vth the collector current increases accompanied with the reduction of C_{gg}. At V_{ge}=7.5V C_{gg} increases abruptly, which coincides with entering the saturation condition of the floating-base potential V_{fp}.

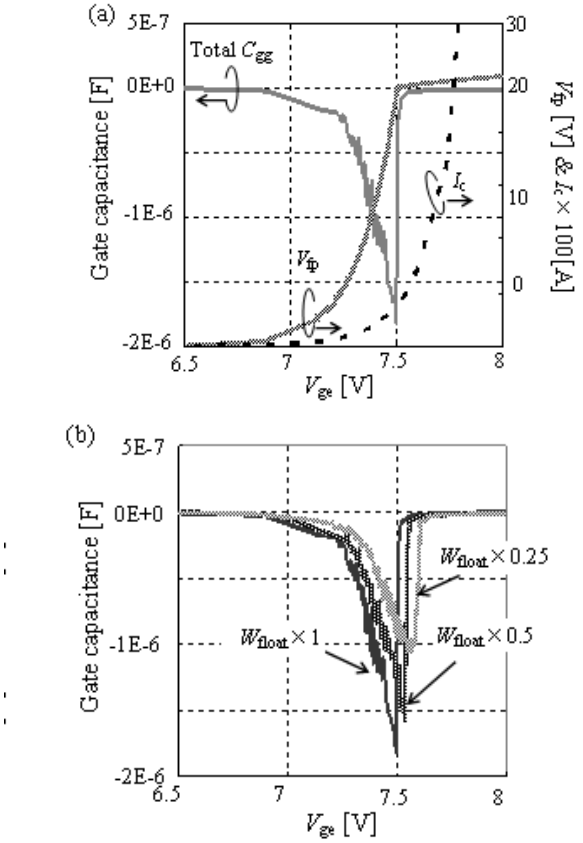

Fig. 7. (a) 2D-device simulation results of C_{gg}, floating-base voltage and I_c current for floating-base structure. (b) 2D-device simulation result of the width (W_{float}) dependence of C_{gg}.

As can be seen in Fig. 8 the starting of the V_{fp} saturation is attributed to the condition where the potential in the floating base becomes higher than the upside potential of n-base region V_b. However, the increase is stopped when V_{fp} exceeds V_b. Fig. 7b shows the width (W_{float}: see Fig. 1b) dependence of C_{gg}. Though the increase of W_{float} shows no influence on C_{gg}, the W_{float} reduction results in the V_{ge} shift to higher values. The total amount of the injected holes into the floating-base region is reduced with reduced W_{float}. This requires the V_{ge} increase to realize V_{fp} larger than V_b.

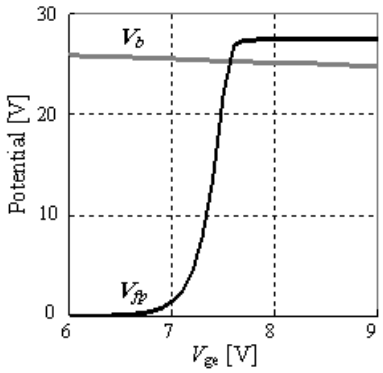

Fig. 8. Simulated results of the floating-base potential (V_{fp}) and the base potential (V_b).

Modeling of the floating-base effect is done by considering the n-MOS capacitor in addition to HiSIM-IGBT as shown Fig. 9. Beyond the threshold voltage the base current (the drain current of the MOSFET) flows, which induces the collector current. The hole injection into the floating-base region as the collector current causes the potential increase. Thus the potential node V_{fp} introduced is connected to the current source to describe this mechanism. However, the collector current flow into the floating base is stopped, when V_{fp} becomes higher than the n-base potential V_b. This effect is described by the connected MOSFET, for which the electrodes are connected either to V_b or V_{fb}. The hole injection even into the floating-base region occurs, because the collector contact extends over the device width. The injected holes don't have the way to go out or to be recombined in the p-Si base, they are accumulated and increases V_{fb}. The balance between V_b and V_{fb} controls the holes injection either to continue or to stop. In HiSIM-IGBT the base node V_b is calculated by solving the Kirchhoff law explicitly, namely $I_c+I_b+I_e=0$. Since the current flow from the floating base to the connected base beyond $V_{fb}>V_b$ is negligibly small in comparison to other currents, the same Kirchhoff law is applied. Thus all node potentials are precisely calculated, and the carrier movement within the device can be predicted in a consistent way.

The developed equivalent circuit shown in Fig. 9 is written in the Verilog-A code and implemented with a commercial SPICE simulator. A calculation result of the negative Cgg due to the hole injection is shown in Fig. 10 in comparison to the 2D-device simulation results. It is seen that the developed model reproduces the 2D-device simulation result well. For better fitting, the resistance effect between the base potential and V_{fp} could be considered additionally. The neglected built-in potential between the floating-base and the n-base could also play a role for better fittings.

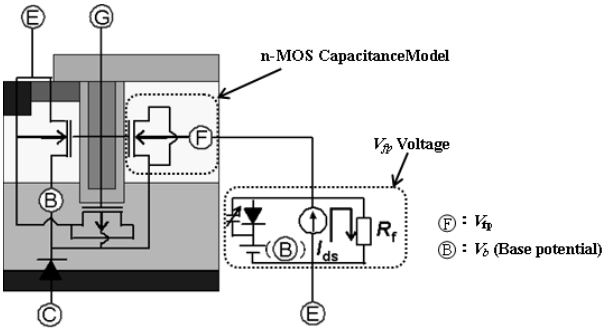

Fig. 9. Equivalent circuit of the developed model.

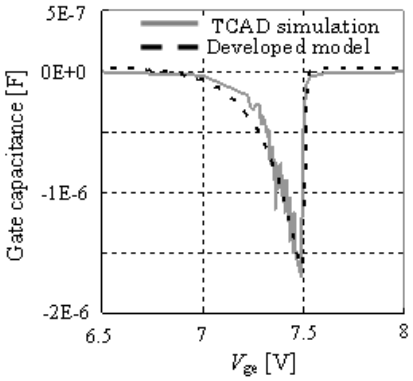

Fig. 10. Calculated gate capacitance with the developed model as a function of V_{ge} in comparison to 2D-device simulation result.

Ⅳ. Switching Simulation Results

Fig. 11 shows simulated switching waveform by using new developed model including the floating-base effect. At the early stage of switching-on, the gradient of I_c as a function of time t (di/dt) has become early. After that, di/dt changes in the second half, the soft switching waveform is calculated. Such phenomenon is simulated by the effect of the newly added model. Since plus capacitance and minus capacitance are intermingled, switching speed is changing.
Moreover, the collector voltage received change of V= -L*di/dt by the coil ingredient of a substrate.

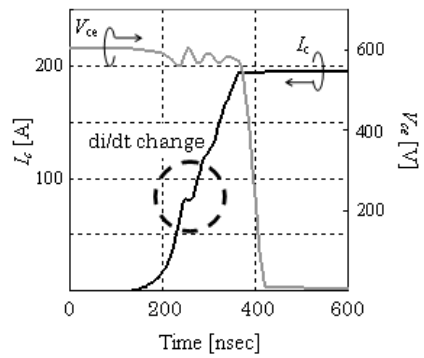

Fig. 11. Calculated switching turn-on waveform with developed model.

Ⅴ. Conclusion

We have developed the negative gate capacitance model observed in the IEGT based on the hole injection into the floating-base. The model has been verified the accuracy by the switching waveform.

Acknowledgements

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Modeling of Injection Enhanced IGBT for Accurate of Switching Performance

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***Abstract*—We have developed a compact model for the injection-enhanced insulated-gate bipolar transistor, which simulates switching performance accurately. The main development is to model the floating-base region, where charge accumulation occurs and influences strongly on the switching characteristics. It is demonstrated that the observed negative gate capacitance is well reproduced by considering the charge explicitly. Consequently, the measured soft switching performance of the studied device is accurately predicted with the developed model.**

I. INTRODUCTION

The insulated-gate bipolar transistor (IGBT) realizes high current controllability together with high breakdown voltage [1]. Because of these advantages, IGBTs are widely applied for inverter circuits of power electronics [2]. Furthermore, many descendants of the basic IGBT structure were developed due to differences in application purposes. The injection-enhanced insulated-gate bipolar transistor (IEGT) has been developed in order to reduce the on-state voltage [3], which realizes a smooth switching waveform in comparison to IGBT [4]. To optimize the trade-off between low overshoot and low energy loss, an accurate circuit simulation model is inevitable.

Compact IGBT models have been developed and are already used for circuit simulations [5, 6, 7]. Among them HiSIM-IGBT [8, 9, 10] solves the potential distribution within IGBT explicitly under fully dynamic load conditions, exploiting the modeling approach of the MOSFET model HiSIM [11] based on the full potential description. However, the present HiSIM-IGBT model considers only the symmetrical trench-type IGBT structure (see Fig. 1a), where both sides of the p-base regions are connected to the emitter. Consequently, the purpose of this contribution is to extend the HiSIM-IGBT model to the asymmetrical IEGT structure (see Fig. 1b), where one side of the p-base region is disconnected and floating, and to investigate the switching characteristics specific for the structure. For this purpose we have investigated device characteristics of the IEGT with a numerical 2D device simulator.

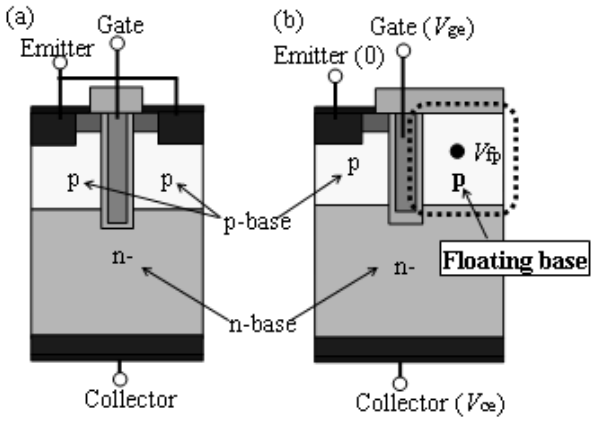


Figure 1. Comparison of two IGBT structures : (a)Symmetrical IGBT, and (b)Asymmetrical IEGT

II. MEASURED SWITCHING RESPONSE OF IEGT

Fig. 2(a) shows the studied basic circuit with its element values. Measurements and simulation results with HiSIM-IGBT, developed for the symmetrical structure, are compared in Fig. 2(b). The model parameter values of HiSIM-IGBT were extracted from the measured I_c-V_{ce} characteristics. It was observed that the measured waveform of the collector current I_c of the IEGT is not as steep as that of the IGBT, and thus a softer switching behavior is observed as shown by a dashed circle. However, the circuit simulation result with HiSIM-IGBT for the symmetrical structure shows no soft switching. The difference between the measured and calculated waveforms is attributed to the floating-base effect, which is not yet considered in HiSIM-IGBT.

The floating-base effect is investigated with 2D evice simulations. Fig. 3 depicts separate contributions from different parts of the gate oxide to the total C_{gg}. The gate oxide divides into three parts, Gate l, Gate b and Gate r. Through the increase of V_{ge} induces the inversion condition, which causes the positive C_{gg} as shown in Fig. 3(b). The humps around V_{ge}=10 V is due to the resistive base effect under the on-

current condition usually observed for power devices. It can be seen that the negative C_{gg} of the floating base (Gate r) dominates the total C_{gg}, and that the positive C_{gg} induced on Gate l is negligible.

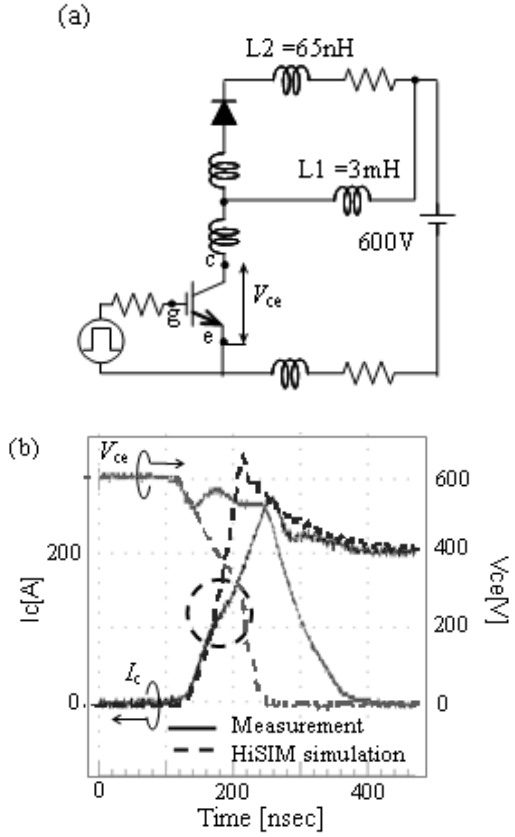
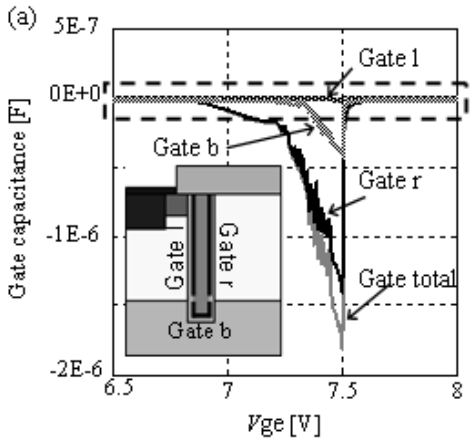


Figure 2. (a) Studied basic circuit with inductive element values (b) Measured transient characteristics in comparison to simulation results with the present HiSIM-IGBT model.



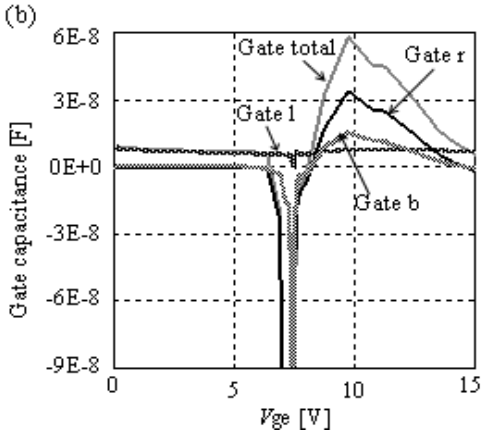


Figure 3. (a) 2D device simulation result of gate capacitance for floating-base structure at V_{ce}=600V, freq=0.001Hz, V_{ge} sweep. (b) Zoom into the dashed rectangle depicted in (a). [V_{ge} range is 0-15V]

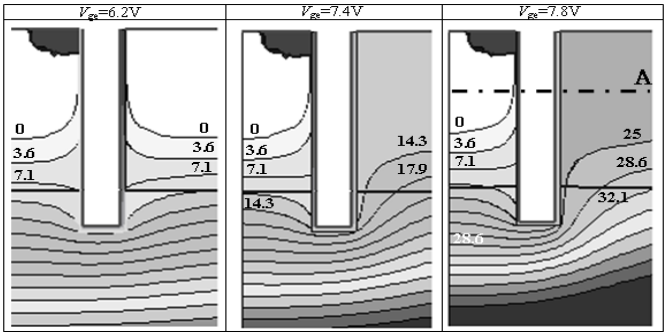


Figure 4. Simulated electrostatic potential around the gate. [/V] (V_{ce}=600V).

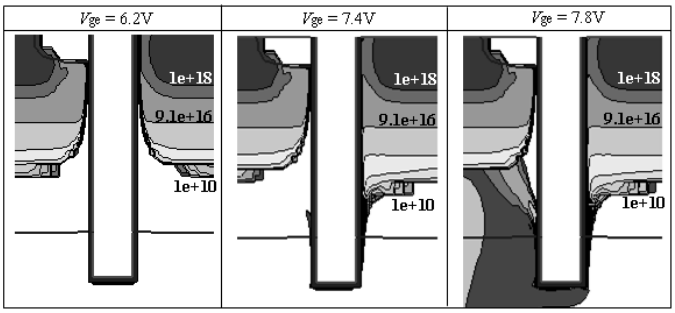


Figure 5. Simulated hole-density distributions around the gate. [/cm^3] (V_{ce}=600V).

III. Modeling of Floating-Base Effect

The origin of the "negative capacitance" [12, 13] is attributed to the hole accumulation in the floating base. The threshold voltage Vth of the studied IGBT is V_{ge}=6.5 V. Fig. 4 compares electrostatic potential contours for different gate voltages V_{ge} around the trench gate oxide. For the V_{ge}<Vth case the potential distribution in the emitter-connected base and the floating base are nearly the same. However, the gate control becomes completely different for two structures under the V_{ge}>=Vth condition when I_c begin to flow. Under the condition the potential value in the floating-base side becomes even higher than V_{ge}. However, the potential value does not exceed a certain value, namely 24.8V for the studied case,

even with further increase of V_{ge}. Fig. 5 shows equal-hole-density contours around the gate oxide at different gate voltages. To model the charge accumulation at Gate r, the potential node V_{fp} is introduced. The node is set near the surface of the floating base as shown in Fig. 1b. Fig. 5a shows 2D simulation results of C_{gg} and V_{fp} as a function of V_{ge}. Beyond V_{ge}=Vth, the collector current starts to increase which is accompanied with the reduction of C_{gg} (Figs. 6a and b). Beyond the threshold condition, the collector current flows into the floating-base region as well and fills the entire region with holes. At V_{ge}=7.5 V, C_{gg} increases abruptly, which coincides with the start of the saturation of the floating-base potential V_{fp}. This hole injection into the floating base is terminated after a certain number of holes occupy the region.

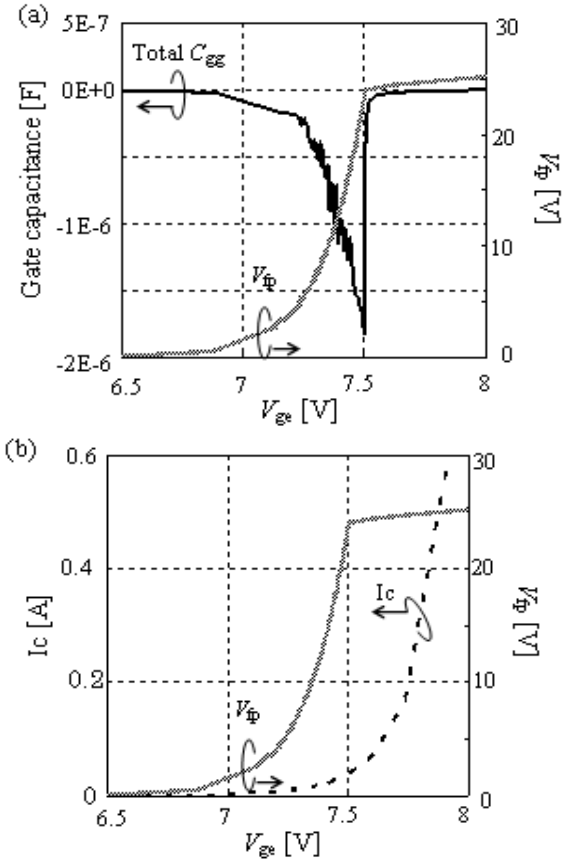


Figure 6. 2D device simulation results of floating-base potential V_{fp}, (a) total gate capacitance C_{gg}, and (b) I_c current for floating-base structure.

The floating-base effect is modeled by considering the n-MOS capacitor in addition to HiSIM-IGBT as shown in Fig. 6. Beyond the threshold voltage, the base current (the drain current of the MOSFET) flows, which induces the collector current. The hole injection into the floating-base region as the collector current causes the potential increase. Thus, the potential node V_{fp} introduced is connected to the current source to describe this mechanism. However, the collector current flow into the floating base is stopped, when V_{fp} becomes higher than the n-base potential V_b. This effect is described by the connected MOSFET, for which the electrodes are connected either to V_b or V_{fb}. The injected holes have no way of going out or recombining in the p-Si base. Thus, they accumulate and increase V_{fb}. The balance between V_b and V_{fb} either continues or stops the hole injection. In HiSIM-IGBT, the base node V_b is calculated by solving the Kirchhoff law explicitly, namely, $I_c+I_b+I_e=0$. Though the current flows from the floating base to the connected base beyond $V_{fp}>V_b$, the magnitude is negligibly small in comparison to other currents. Therefore the contribution is neglected in the Kirchhoff law.

IV. Modeling of MOSFET Model

The MOSFET part in the HiSIM-IGBT is made from surface-potential-based MOSFET model. By applying the Gauss law, the total charge density induced in the substrate is derived with the Poisson equation [11, 14].

$$-Q_S = C_{ox}(V'_G - \phi_S(y))$$

$$= (2\varepsilon_{si} q N_{sub}/\beta)^{0.5}[exp\{-\beta(\phi_S(y) - V_{bs}\} + \beta(\phi_S(y) - V_{bs}) - 1 + n_{p0}/p_{p0}\{exp(-\beta(\phi_S(y) - \phi_f(y))] - \exp(\beta(V_{bs} - \phi_f(y))\}]^{0.5} \quad (1)$$

$$C_{ox} = \varepsilon_{ox}/T_{ox} \quad (2)$$

$$V'_G = V_{gs} - V_{fb} + \Delta V_{th} \quad (3)$$

The Q_s is the bulk charge density along the channel, and $\phi_f(y)$ takes a value between zero and V_{ds}. V_{fb} is the flatband voltage, T_{ox} is the gate-oxide thickness, and ΔV_{th} is the threshold voltage shift due to the short-channel effect. ε_{Si} and N_{sub} are the silicon permittivity and the substrate impurity concentration, respectively. The electron charge is denoted by q. The Boltzmann constant and the lattice temperature in kelvins are k and T, respectively. The inverse of the thermal voltage is written as $\beta = q/kT$. HiSIM is an industry-standard surface-potential-based MOSFET model, which solves the aforementioned equations exactly.

When considering switching operation, it is one of important elements to take gate-collector capacitance. Most of the IGBT capacitance consists of the MOSFET gate capacitance which includes the overlap parts with the n− base region at the bottom of the trench gate [15]. HiSIM-IGBT describes this trench-bottom nonlinear MOS capacitance with the surface-potential-based approach. The surface potential ϕ_S is calculated in the same manner as in the channel region. The final trench-bottom gate-overlap charge equation is written with the calculated ϕ_S as (4) under the depletion and the accumulation conditions and inversion condition (5), where $C_{ox,edge} = \varepsilon_{ox} / T_{ox,edge}$.

$$Q_{g,\,bottom} = W_{eff} * L_{overLD}\{(2\varepsilon_{si} q N_{over}/\beta)^{0.5} * (\beta(\phi_S + V_{ds}) - 1)^{0.5}\} \quad (4)$$

$$Q_{g,\,bottom} = W_{eff} * L_{overLD} * C_{ox,edge}(V_{gs} - V_{fb,\,over} - \phi_S) \quad (5)$$

Here $T_{ox,edge}$ and L_{overLD} are the oxide thickness and the oxide

length of the trench-bottom region, respectively. N_{over} and $V_{fb,over}$ are the base impurity concentration near the trench-bottom region and the flatband voltage for the overlap MOS structure, respectively.

The additional equivalent circuit shown in Fig. 7 is included in HiSIM-IGBT and implemented into a commercial SPICE simulator. A calculation result of the negative C_{gg} due to the hole injection is shown in Fig. 8 in comparison to the 2D device simulation result. It is seen that the developed model for the IEGT reproduces the 2D device simulation result well.

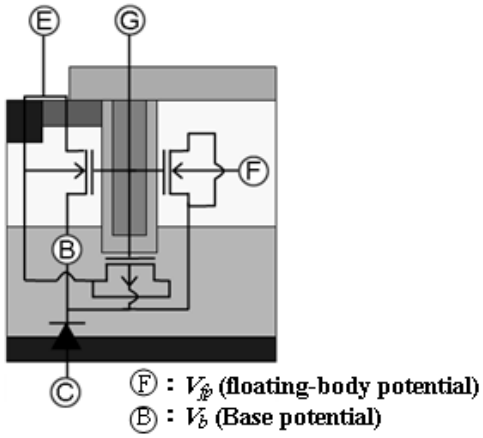


Figure 7. Equivalent circuit of the developed IEGT model.

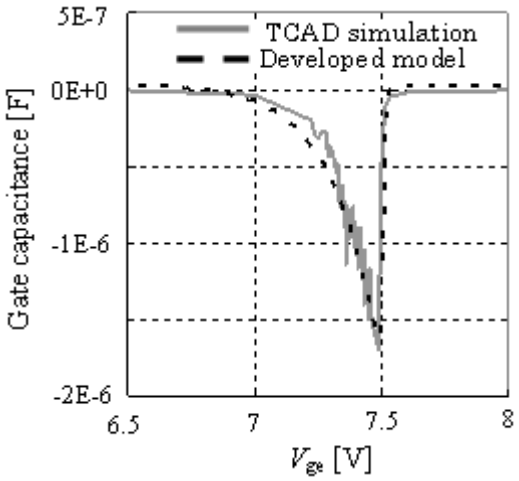


Figure 8. Calculated gate capacitance with the developed IEGT model as a function of V_{ge} in comparison with 2D device simulation result.

V. Switching Simulation Result

Fig. 9 shows the switching waveform simulated with the developed IEGT model including the negative C_{gg} in comparison to measurement data. The circuit shown in Fig. 2a is considered, handling only one phase of a three-phase motor control circuit. It is seen that the measured soft switching behavior observed in the collector current I_c is well reproduced.

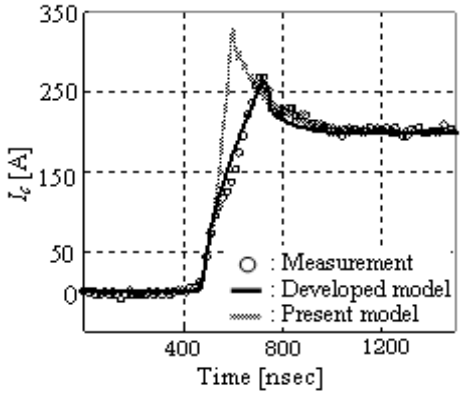


Figure 9. Calculated switching turn-on waveform with devedloped IEGT model..

VI. Conclutions

We have developed a compact model for the negative gate capacitance observed in the IEGT structure based on the hole injection into the floating base. This model has been implemented in a circuit simulator and verified to be accurate. The characteristic switching waveform seen for the IEGT structure has also been accurately reproduced in the circuit simulation.

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Role of Carrier Response Delay on Switching Performance of Injection-Enhanced IGBT

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Abstract

The Injection-Enhanced Insulated-Gate-Bipolar Transistor was invented to reduce the on-state voltage. We have successfully developed a compact model describing the hole accumulation in the floating-base region, which causes the negative gate capacitance, the origin of the reduction. This investigation reports that the hole response delay, suppressing the negative capacitance, plays an important role on switching performance for real circuits.

1. Introduction

The Injection-Enhanced Insulated-Gate-Bipolar Transistor (IEGT) structure has been developed in order to reduce the on-state voltage and achieving a smooth switching waveform (soft switching) [1] in comparison to the conventional Insulated-Gate-Bipolar transistor (IGBT). The difference of the two structures is either symmetrical or asymmetrical as depicted in Fig. 1, where one side of the p-base region of IEGT is disconnected and floating.

IEGT has been utilized for applications where reduced voltage overshoot is required. However, the smoothed waveform causes large switching loss. To optimize the trade-off between the low overshoot and the low energy-loss at the same time, accurate circuit simulations valid for investigating the switching performance of IEGT is inevitable.

We have developed the compact model HiSIM-IEGT [2] based on the conventional IGBT model HiSIM-IGBT [3,4]. The main development is modeling the hole accumulation in the floating base. For the purpose we have introduced the potential node V_{fp} (see Fig. 1), which is solved together with other nodes under the Kirchhoff law.

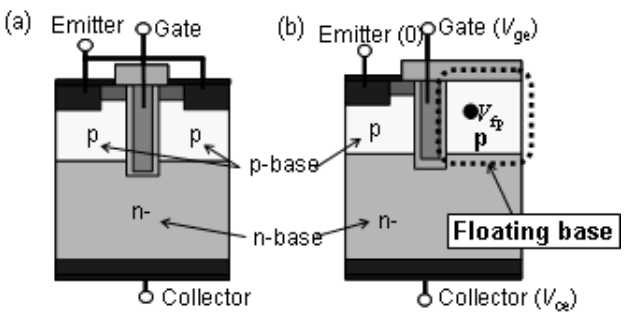

Fig. 1. (a) The symmetrical IGBT structure, and (b) the asymmetrical IEGT structure.

With use of the developed HiSIM-IEGT we investigate here the switching performance of IEGT in comparison to measurements.

2. Measured Switching Response of Floating Base

Fig. 2 (a) shows a switching circuit studied, and Fig. 2 (b) compares measured results to those of simulation with HiSIM-IGBT no inclusion of the hole accumulation effect in the floating base region. It is observed that the measured waveform of the collector current I_c is not as steep as that of IGBT, and thus softer switching behavior is realized.

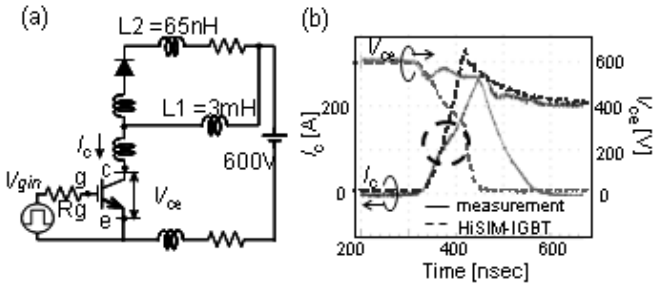

Fig. 2. (a) Studied basic circuit with inductive element values, (b) measured transient characteristics in comparison to simulation results with HiSIM-IGBT without considering the hole accumulation.

Fig. 3 depicts the gate oxide capacitance C_{gg} and the floating-base potential V_{fp} simulated with a 2D device simulator [5]. It can be seen that the large negative C_{gg} of the floating base induced at the floating base contact is the specific feature of IEGT [6, 7], and has been modeled in HiSIM-IEGT successfully [2] (see Fig. 5).

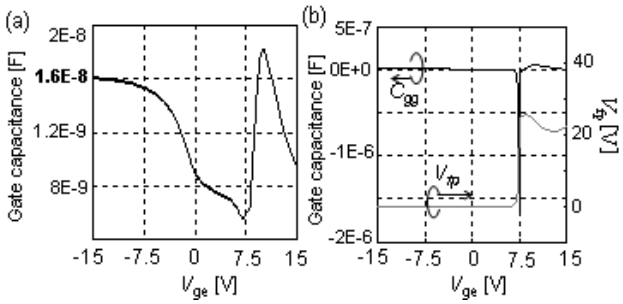

Fig. 3. 2D device simulation results of C_{gg} at V_{ce}=600V, freq=0.001Hz as a function of V_{ge} (a) for IGBT and (b) for IEGT. The floating-base potential V_{fp} is also depicted together.

3. Floating-Base Effect Model and Calculation Result

The floating-base effect is modeled by considering an n-MOS capacitor in addition to HiSIM-IGBT as shown in Fig. 4. The base node V_b as well as V_{fp} are calculated by solving the Kirchhoff law explicitly, namely, $I_c+I_b+I_e=0$ [3,4] The additional equivalent circuit shown in Fig.4 is included in the conventional HiSIM-IGBT and tested with a SPICE simulator. The negative C_{gg} is much larger than the positive C_{gg} as can be seen in Fig.5. The total C_{gg} is dominated by the negative C_{gg} between 7V and 8V, when the hole accumulation occurs. An important task is to calculate the negative C_{gg} accurately.

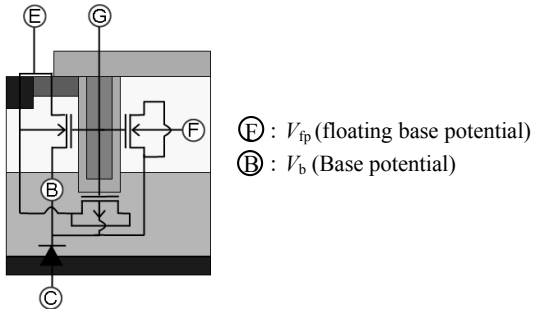

Fig. 4. Equivalent circuit of the developed IEGT model.

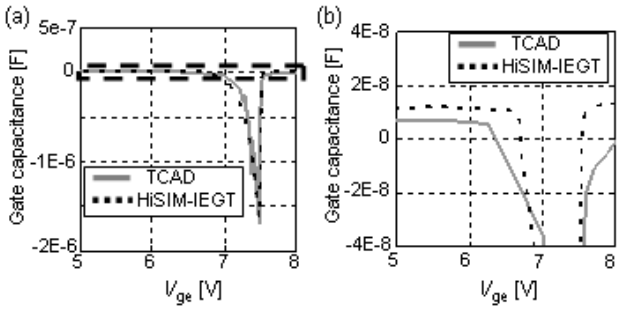

Fig. 5. Calculated gate capacitance with the HiSIM-IEGT model and TCAD simulation result.

Fig. 6 shows the switching waveform simulated with the developed IEGT model including the floating-base effect in comparison to measurement data. The circuit shown in Fig. 2(a) is investigated. It is seen that the measured soft switching behavior observed in the collector current I_c is accurately reproduced. Furthermore, the collector voltage V_{ce} is also well reproduced with change of I_c waveform. However, it has to be noticed that the negative C_{gg} predicted by 2D-device simulations is too large to reproduce the measured wave form (see Fig. 3(b)).

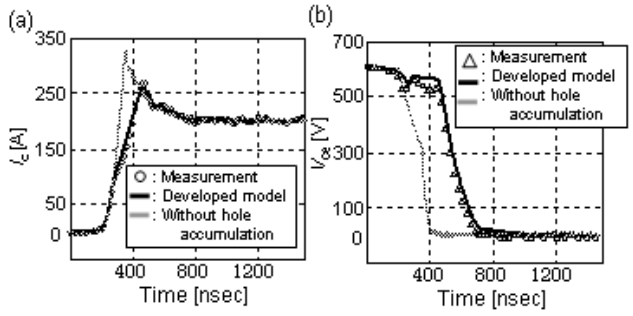

Fig. 6. Comparison of calculated switching turn-on waveform with measured results (a) I_c waveform and (b) V_{ce} waveform.

4. Discussion

Fig. 7 (a) shows frequency dependence of the total C_{gg} as a function of V_{ge}. It is seen that the negative C_{gg} is reduced at high frequency. Fig. 7 (b) shows frequency dependence of the minimum value of the total C_{gg}. The rapid reduction of the negative C_{gg} is observed beyond 1kHz. This frequency dependence of C_{gg} is attributed to the carrier transit delay, causing the device response delay to the switching speed. If the switching is faster than the carrier movement, reduction of C_{gg} is observed due suppressed amount of hole gathered. We have extracted the accumulated hole density of only about a few percents of the total expected hole density. This extracted drastically reduced accumulated hole density is exactly due to the carrier response delay.

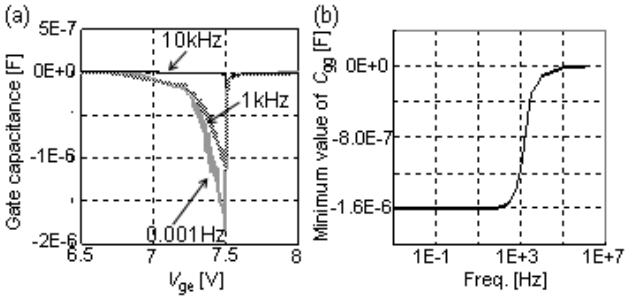

Fig. 7. 2D device simulation result. (a)The V_{ge} voltage dependence of total C_{gg} at V_{ce}=600V. (b) Frequency dependence of the minimum value of total C_{gg} at V_{ce}=600V.

5. Conclusions

A new HiSIM-IEBT model has been developed, which consider the floating-base effect. This model has been implemented in a circuit simulator and verified to be accurate. The characteristics switching waveform seen for the IEGT structure has also been accurately reproduced in the circuit simulation. It becomes clear that the negative capacitance has frequency dependent.

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