博士論文

Temperature Dependence of Threshold Voltage in Poly-Si/TiN Metal Gate Transistors

（Poly-Si/TiN 金属ゲートトランジスタの閾値電圧の温度依存性）

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２．公表論文

(1) Temperature Coefficient of Threshold Voltage in High-k Metal Gate Transistors with Various TiN and Capping Layer Thicknesses
Y. Nishida, K. Eikyu, A. Shimizu, T. Yamashita, H. Oda, Y. Inoue, and K. Shibahara
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(2) Mechanisms of Temperature Dependence of Threshold Voltage in High-k/Metal Gate Transistors with Different TiN Thicknesses
Y. Nishida and S. Yokoyama
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(1) Performance Enhancement in 45-nm Ni Fully-Silicided Gate/High-k CMIS using Substrate Ion Implantation
Y. Nishida, T. Yamashita, S. Yamanari, M. Higashi, K. Shiga, N. Murata, M. Mizutani, M. Inoue, S. Sakashita, K. Mori, J. Yugami, T. Hayashi, A. Shimizu, H. Oda, T. Eimori, and O. Tsuchiya
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主論文

Contents

1. Introduction

1.1. Background of this research

1.1.1. Technologies for breaking the scaling limit

In semiconductor technology, a trend of the transistor shrinkage has always continued [1-3]. The reason is because the transistor shrinkage based on scaling rule could achieve reduction in power consumption, improvement of reply speed and increase in the number of devices per the unit area at the same time [4, 5].

When the scaling was pushed forward more, however, the scaling limit approached and the transistor dimension entered the domain where a merit by the scaling is not provided enough. There are several factors in the scaling limit. One of the factors is that a further reduction of the gate oxide thickness became difficult because the gate leakage current extremely increases. In addition, it became difficult to decrease the effective gate oxide thickness due to the gate depletion layer in the polycrystalline silicon (poly-Si) gate electrode. Moreover there is also a factor that carrier mobility decreased because of the increase of the impurity concentration in the substrate. Therefore, although the scaling further advanced, it became basically necessary to add techniques for breaking the scaling limit in the technology of 65 nm node and beyond. These techniques are called "performance booster", which indicates for example techniques of "strained Si channel" or "high-k material", etc.

In the Symposium on VLSI 2007 (Kyoto), I reported "Advanced Poly-Si NMIS and Poly-Si/TiN PMIS Hybrid-Gate High-k CMIS using PVD/CVD-Stacked TiN and Local Strain Technique", in which the effects of performance boosters were explained concretely [6]. In this report, various performance booster technologies were indicated. Stress Memorization Technique (SMT), Dual Stress Liner (DSL), and disposable sidewall were applied as the methods which form a strained Si channel. These methods form tensile strain at channel region in n-MOSFET and compressive strain at channel region in p-MOSFET, which are the desirable strain for enhancement of carrier mobility, respectively. Moreover, as a new technology for the transistor shrinkage, Laser Annealing (LA) was applied to suppress diffusion of impurities. Due to the effects of above-mentioned performance boosters, etc., the value of drain current became large compared with that without performance boosters (56% up in n-MOSFET, 95% up in p-MOSFET). In addition, another important performance booster was an application of high-k/metal gate electrode, which is explained in the next section.

1.1.2. Necessity of metal gate transistor

As a performance booster, introduction of the new gate electrode structure of the high-k/metal stack was considered as mentioned in the former section. In fact, metal gate was originally older than poly-Si gate because old MOSFET used Al for gate electrode material. But, the use of the poly-Si gate became mainstream after a technique to use poly-Si for a gate electrode was reported in 1966. Because the heat resistance of Al is low, Al gate electrode must be formed after the formation of source/drain region which need high temperature process. On the other hand, because poly-Si has high thermal stability, a high temperature activation anneal for the source/drain region could be

performed after the formation of the poly-Si gate electrode. If source/drain region could be formed after gate electrode formation, source drain implantation became able to be performed as the self-aligned ion implantation using the gate electrode as an implantation mask. Because the mask overlap margin between the gate electrode region and the source drain implantation region became unnecessary in the poly-Si gate process, which is different from the Al gate process, poly-Si process was very favorable for shrinkage of MOSFET devices. Therefore a poly-Si gate kept being the mainstream for a long time.

As a result of advance of scaling, however, disadvantageous face emerged in the SiO_2 (or SiON)/poly-Si gate. As explained the former section, an increase in gate leakage current at thin gate oxide and an existence of gate depletion layer make it difficult to reduce the effective gate oxide thickness. Therefore high-k/metal gate stack structure became necessary, because it reduces gate leakage current by its thick physical thickness and reduces the effective gate oxide thickness by its high dielectric constant and by suppression of gate depletion.

1.1.3. Candidates of the metal gate process

In the mid-2000s, various companies and consortiums reported about the metal gate process development aiming at a mass production in international conferences such as VLSI technology symposium (VLSI) or International electron device meeting (IEDM). There were about three kinds of candidates for high-k metal gate process at that time. They were (1) Gate-First process (2) Gate-Last process (3) Fully Silicided (FUSI) process, which are explained below, respectively.

(1) Gate-First process

The metal layer in the gate electrode is formed before the activation anneal for source/drain region in the gate-first process. Metal Inserted Poly-Si Stacks (MIPS), which replaces poly-Si gate electrodes with poly-Si/metal gate electrodes, is substantially standard structure in the gate-first process [7]. Schematic diagram of MIPS transistor is indicated in Fig. 1.1. The gate-first process is relatively simpler than the gate-last process (described later) for fabricating metal gate MOSFETs because it is basically compatible with a conventional fabrication process flow using poly-Si gates.

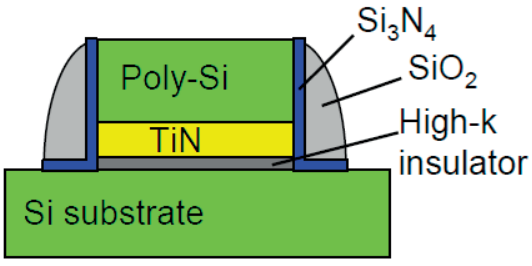

Fig. 1.1. Schematic diagram of the MIPS structure.

The important problem in the gate-first high-k/metal gate transistor is difficulty of the control of V_{th}. The effective work function tends to come to the mid gap of Si in the metal of gate electrode which have undergone some high temperature processes. This phenomenon, a change in the effective work function, is called Fermi Level Pinning (FLP), and it is explained at the later section 2.3.4 in detail. If the FLP occurs, V_{th} in both n-MOSFET and p-MOSFET become too high for usual CMOS circuits for high performance logic. Therefore, to achieve the proper V_{th}'s, the problem of FLP must be solved and the effective work function must be modified from mid gap to near the band edge. One solution is "capping process" in which capping layers are inserted before the gate metal layer deposition [7-9]. In an usual simple capping process, one kind of metal with effective work function around mid-gap is used for both n/p-MOSFET, and a capping material which decreases the effective work function like La_2O_3 is inserted in n-MOSFET gate stack, and a capping material which increases the effective work function like Al_2O_3 is inserted in p-MOSFET gate stack.

Also in above-mentioned our report at VLSI 2007 [6], we applied MIPS structure without capping layer for p-MOSFET (n-MOSFET had poly-Si gate) for suppression of gate depletion which is outstanding especially in poly-Si gate of p-MOSFET. The rate of increase in gate capacitance under the inversion condition between poly-Si gate and TiN MIPS gate in p-MOSFET was about 20%, as described in our previous report [10]. This result indicated that application of the TiN metal gate structure could suppress the gate depletion, and could become a very effective performance booster.

(2) Gate-Last process

In the gate-last process, the metal layer in the gate electrode is formed after the activation anneal for source/drain region [11, 12]. Therefore, the gate-last process is able to avoid the FLP which is serious problem in gate-first process. Since a work function near the band edge is achieved by choosing a suitable kind of metal, it is relatively easy to control the V_{th}. But, the gate-last process is quite different from the conventional poly-Si gate process. Usually after the formation of the source/drain region, the gate electrode is formed by damascene gate process (replacement gate process) [11]. In addition, different kind of metal is usually applied to obtain different effective work function in n-MOSFET and p-MOSFET. Therefore, in the gate-last process, there are some difficult processes for example metal deposition into narrow spaces or CMP for different kind of metals. Therefore fabrication of experimental samples was relatively difficult and reports at conferences were not many compared with other candidates.

(3) FUSI process

In FUSI process, the metal gate electrode is formed by complete silicidation of poly-Si gate electrode after the activation anneal [13]. Therefore, it does not need special processes which deal with pure metal. Although FIUSI process is classified into one kind of gate-last processes, its process flow is relatively closer to the conventional process flow and easier than usual "gate-last process" explained at (2).

In FUSI process, effective work function could be adjusted by phase control of silicide [14]. For example, the effective work function of NiSi is lower than that of Ni_3Si, although both of them consist of the same Ni and Si. And if necessary, FUSI process is able to use also the

capping process for control of V_{th} [15]. Also I reported "Performance Enhancement in 45-nm Ni Fully-Silicided Gate/High-k CMIS using Substrate Ion Implantation", in which result of the V_{th} control using the difference of work function between NiSi (for n-MOSFET) and Ni_2Si (for p-MOSFET) was demonstrated, in the Symposium on VLSI 2006 (Honolulu) [16].
There were many reports in international conferences about FUSI which was relatively easy to experiment, but it did not become the process for mass production after all. The reason of the abandonment of FUSI process is thought to be the difficulty of the phase control of Ni-silicide in actual small dimensions for the target technology node.

Figure 1.2 shows the classification of the content of report about metal gate MOSFET at VLSI symposium 2007, which was held in June 2007 at Kyoto in Japan. As shown in the figure, 8 of 14 cases chose gate-first MIPS structure. In addition, 5 of 8 cases of MIPS structure use the capping layer to control V_{th}. FUSI had 4 reports, but the number of reports of FUSI greatly decreased from 10 reports at 2006. On the other hand, gate-last process was not major topic at this conference. Under this situation, gate-first MIPS with capping seemed the most promising candidate. But, Intel reported the 45 nm node gate-last process at international electron device meeting (IEDM) in December, 2007 [12], and started mass production with the gate-last process. As a result, the gate-last process came to be considered to be the most realistic metal gate process. Actually, the instability of gate-first process against thermal processes or oxidation processes (remarkable especially at small size transistor) is a serious problem [17, 18]. Although drastic change in the fabrication process for gate-last process might be disadvantage, it is thought that to avoid the problems in gate-first process was more important.

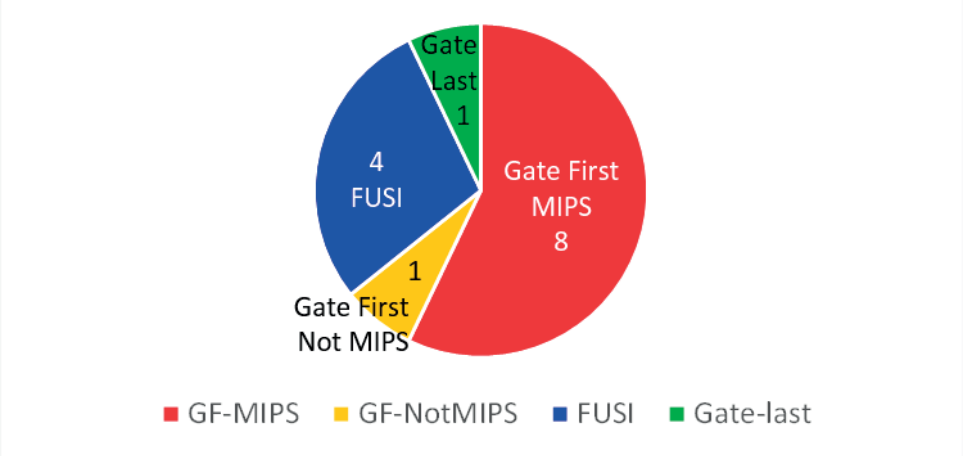

Fig. 1.2. Classification of the process of the metal gate reported at VLSI 2007.

However, gate-first process is easy to import the know-how of process from the similar conventional poly-Si gate process. Therefore, it is easy in gate-first process to make various experiment samples. It is an advantage in the case of experiment for a research of basic property. Because TiN is frequently used even in a conventional process and it has relatively high heat resistance, TiN MIPS structure with capping layer for control of V_{th} is thought to be most useful structure for basic experiment (especially transistor with large gate size is desirable for stability against thermal processes or oxidation processes).

Also we used this structure for our research, in which the basic characteristics of the metal gate transistor were analyzed.

1.1.4. Temperature coefficient of V_{th}

The threshold voltage (V_{th}) in a MOSFET is a very important parameter in circuit design. There is a possibility that the circuit does not operate normally if the V_{th} comes off from the range assumed at the time of the design. And, the value of V_{th} is changed by temperature, as shown in Fig. 1.3. Therefore, it is necessary for the circuit designer to consider the influence caused by the shift of the V_{th}.

There are parameters that reflect the temperature coefficient of V_{th} in the SPICE model. [19]. Usually, the circuit designer must check with the circuit model whether the circuit operates normally in the temperature range that the specifications of the product guarantee. Especially, low stand-by power devices often require stable operation under a wide temperature range without a special temperature management. For example, one assumed usage is very cold condition of outdoor in winter (less than −30°C), and other usage is very hot conditions where generated Joule heat is added to hot atmosphere in automobiles in summer (more than +100°C). Generally, if the temperature coefficient of V_{th} ($|dV_{th}/dT|$) is small, it is thought that the operation margin of the circuit becomes large, which is advantageous to enhancement of yield in mass production. The magnitude of the $|dV_{th}/dT|$ is an important parameter that might influence also the production efficiency of the products.

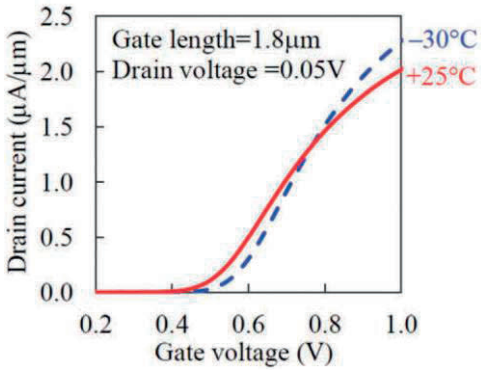

Fig. 1.3. Drain current-gate voltage (I-V) characteristics of a high-k/metal gate n-MOSFET at –30°C and +25°C. The structure of the gate electrode was high-k dielectric/TiN/poly-Si, and the gate length was 1.8 μm. The drain voltage was set at 0.05 V.

Although the reason why V_{th} changes depending on temperature will be explained in the next Chapter 2 in detail, the main cause is change of Fermi level in silicon. Therefore, by replacement of poly-Si gate with metal gate, $|dV_{th}/dT|$ of MOSFET is changed. Han *et al.* reported that $|dV_{th}/dT|$ in metal gate MOSFET became larger than that in poly-Si gate [20]. It is thought that this is not a favorable change as described above. It is very important to investigate the factor which decides the magnitude of $|dV_{th}/dT|$ in the metal gate MOSFET, and to find methods which are able to suppress the increased $|dV_{th}/dT|$.

1.2. Objectives and structure of this thesis

1.2.1 Objectives of this thesis

There were some reports that indicated $|dV_{th}/dT|$ in a metal gate MOSFET was larger than that in a poly-Si gate MOSFET [20, 21]. However, there are still few reports that consider how to suppress the increased $|dV_{th}/dT|$ in metal gate MOSFETs.

The aim of this thesis is to investigate the relation between the structure of the metal gate and the dV_{th}/dT in detail, and to clarify the factor that decides the dV_{th}/dT of metal gate MOSFETs. And, to consider methods which are able to suppress the increased $|dV_{th}/dT|$.

The conditions of metal gate samples in this study were based on the gate-first process and MIPS structure. Because the gate-first process was close to the conventional poly-Si gate process, it was relatively easy to make samples with different conditions. The TiN thickness dependence and the capping thickness dependence of dV_{th}/dT were measured with these samples.

1.2.2 The construction of this thesis

This thesis consists of six chapters.

In Chapter 1, the necessity of the metal gate process, the three kinds of metal gate process, and the importance of the temperature coefficient of V_{th} were demonstrated as a background of this thesis. And the objectives and constitution of this thesis were explained.

In Chapter 2, basic theories necessary to discuss the theme in this thesis were explained, and associated informations abstracted from past reports were explained. Theoretical equations, such as equations expressing the dV_{th}/dT in poly-Si gate or metal gate, etc. were indicated. In addition, the theory that a work function depended on crystallinity and the crystal orientation were explained. And the report that indicated the temperature dependence of those different work functions was shown.

In Chapter 3, the factors which affected dV_{th}/dT in the MIPS gate were investigated with measurement result of real MIPS gate samples. It was indicated that when thickness of TiN changed, the temperature coefficient of work function of TiN ($d\Phi_{TiN}/dT$) changed, and it became the change of temperature coefficient of the flat band voltage of the MOSFET (dV_{FB}/dT), which affected the dV_{th}/dT. On the other hand, it was also indicated that when *EOT* increased depending on the conditions of TiN thickness or capping thickness, the influence of the temperature coefficient of depletion charge became large and affected dV_{th}/dT. Because of the difference of the direction of

these two effects, when TiN thickness increased, the $|dV_{th}/dT|$ of n-MOSFET increased clearly and that of p-MOSFET did not change that much.

In Chapter 4, the mechanism which changed $d\Phi_{TiN}/dT$ when TiN thickness changed was investigated. It was indicated by physical analysis that when TiN thickness became larger, crystallinity of TiN became higher and Φ_{TiN} became higher at the same time. Because it was supposed that the difference of the Φ_{TiN} by difference of crystallinity became small in high temperature, it was thought that difference came to occur also in $d\Phi_{TiN}/dT$ (=slope of Φ_{TiN} - temperature plot).

In Chapter 5, I summarized the result of this study. With consideration of the result, the methods to control dV_{th}/dT in metal gate MOSFET were discussed.

In Chapter 6, the conclusions of this thesis were described briefly.

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2. Basic theories and previous reports

2.1. Theoretical equation of V_{th}

2.1.1. V_{th} in an ideal MOS structure

For sufficient comprehension of characteristics of threshold voltage (V_{th}) in MOS structures such as MOS capacitor or MOSFET, which is the subject of this thesis, an analytic equation which describes the value of V_{th} is very important. Then, I will explain the derivation process in detail here [1, 2]. Figure 2.1 represents band structures of an ideal MOS capacitor. I will explain about a change of the potential when voltage V_g is applied to this gate electrode which consists of metal. An ideal MOS capacitor, about which I will give more information in the next section, is a MOS capacitor in which there is no curve in its band structure at V_g=0 V. Figure 2.1(a) shows the band structure of V_g=0. The substrate is p-type semiconductor, and its accepter concentration is N_a.

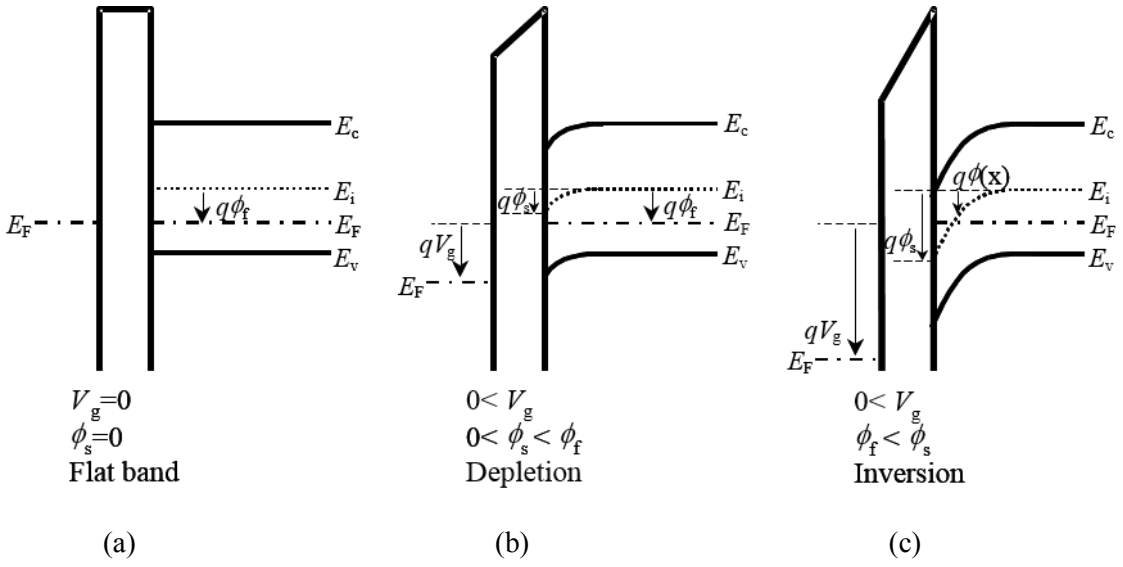

Fig. 2.1. Band structures of an ideal MOS capacitor with the state of (a) flat band, (b) depletion, and (c) inversion.

Figure 2.1(b) represents a state of the band structure when a gate voltage V_g, which is not very high, is applied. The Fermi level in the gate metal is lowered by qV_g. The lowered width qV_g is distributed into a slope of the oxide layer and a curve of the band structure of the silicon (q is the elementary charge). At this time, holes which are the majority-carrier in the substrate of p-type silicon are sent away near the oxide by field effect (depletion), and negative charge which is ionized acceptor atoms appears (depletion layer). It is assumed that the electric charge in the depletion layer is only these acceptor ions (depletion approximation). These acceptor ions become the cause which makes an electric potential and bends the band. Here, $\phi(x)$ is defined as the width of the potential change at the position x in the depletion layer. If the Poisson equation is applied to $\phi(x)$ in the depletion layer region,

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{qN_a}{\varepsilon_{Si}\varepsilon_0} \quad . \tag{2.1.1}$$

Here, ε_0 is the permittivity of vacuum. ε_{Si} is the dielectric constant of Si (= 11.7), ρ is the charge density. In addition, l_D is defined as the width of the depletion layer. Because the $\phi(l_D)$, which means the width of the potential change at $x=l_D$, is 0, and the rate of change of the $\phi(l_D)$ is also 0,

$$\phi(x) = \frac{qN_a}{2\varepsilon_{Si}\varepsilon_0}({l_D}^2 - 2xl_D + x^2) = \frac{qN_a}{2\varepsilon_{Si}\varepsilon_0}{l_D}^2(1-\frac{x}{l_D})^2 \quad (0 \le x \le l_D). \tag{2.1.2}$$

If the width of the potential change at the surface of p-type semiconductor substrate (x=0) is represented by ϕ_s, ϕ_s can be given by

$$\phi_s = \phi(0) = \frac{qN_a}{2\varepsilon_{Si}\varepsilon_0}{l_D}^2. \tag{2.1.3}$$

Next, the potential $\phi(x)$ in the gate oxide, the thickness of which is T_{ox}, is considered. The width of the depletion layer is l_D, and the relation between l_D and ϕ_s is expressed in (2.1.3). Therefore, the electric charge Q_D which has been generated in the Si substrate is given by

$$Q_D = -qN_a l_D = -\sqrt{2qN_a\varepsilon_{Si}\varepsilon_0\phi_s} \quad . \tag{2.1.4}$$

According to the Gauss' low, the electric field E_{ox} which this electric charge Q_D makes in the oxide layer is represented as

$$E_{OX} = \frac{Q_D}{\varepsilon_{OX}\varepsilon_0} \, . \tag{2.1.5}$$

ε_{ox} is the dielectric constant of the gate oxide. $\phi(x)$, which is the potential in the gate oxide, is integration of the electric field E_{ox} given by (2.1.5). If the boundary condition $\phi(0)=\phi_s$ is considered,

$$\phi(x) = E_{OX}x + c = \frac{Q_D}{\varepsilon_{OX}\varepsilon_0}x + c = \frac{Q_D}{\varepsilon_{OX}\varepsilon_0}x + \phi_s \quad (-T_{OX} \le x \le 0) \, . \tag{2.1.6}$$

At the position of $x= -T_{ox}$, which means the top edge of the gate oxide and the bottom edge of the metal electrode, $\phi(x)$ becomes equal to gate voltage V_g. Therefore, the relation,

$$V_g = \phi(-T_{OX}) = -\frac{Q_D T_{OX}}{\varepsilon_{OX}\varepsilon_0} + \phi_s = \phi_s - \frac{Q_D}{C_{OX}} \, , \tag{2.1.7}$$

is formed. C_{ox} is the capacitance of gate oxide, and it is expressed as

$$C_{OX} = \frac{\varepsilon_{OX}\varepsilon_0}{T_{OX}}. \tag{2.1.8}$$

If Q_D is represented by ϕ_s with (2.1.4), the equation (2.1.7) becomes

$$V_g = \phi_s + \frac{\sqrt{2qN_a\varepsilon_{Si}\varepsilon_0\phi_s}}{C_{OX}}. \tag{2.1.9}$$

In the previous explanation, I have considered the case in which a positive bias is applied to V_g in the MOS structure and the surface of the p-type silicon substrate becomes the depletion status. But, when V_g becomes higher and has exceeded a specific level, a generation of electric charge starts not only by the expansion of depletion layer width but also by formation of an inversion layer. Here, ϕ_F is defined as the potential difference between E_F which is the Fermi level at an inside position sufficiently separated from the surface, and E_i which is the Fermi level of an intrinsic semiconductor silicon. ϕ_F is decided by the substrate impurity concentration (here, N_a) and the intrinsic carrier concentration n_i, and it is expressed as

$$\phi_f = \frac{E_i - E_{F(p)}}{q} = \frac{kT}{q}\left(\ln\frac{N_a}{n_i}\right). \tag{2.1.10}$$

When ϕ_s is smaller than ϕ_F, negative charge is generated by depletion at the surface of p-type silicon substrate (Fig. 2.1(b)). When ϕ_s exceeds ϕ_F, negative charge in the inversion layer is added because the E_i which is bent by applying a positive voltage to V_g reaches lower than the level of E_F (Fig. 2.1(c)). But, if $\phi_F \leqq \phi_s < 2\phi_F$, this state is called weak inversion because the electron concentration in the inversion layer is still small. When the V_g becomes higher and the surface potential ϕ_s exceeds $2\phi_F$, the carrier concentration of the conduction electrons which was the minority carrier originally in the p-type silicon substrate, becomes larger than the original carrier concentration of the hole which was the majority carrier of p-type silicon substrate. This state, $\phi_s \geqq 2\phi_F$, is called strong inversion, where the amount of the electric charge which is formed by conduction electrons in the inversion layer remarkably varies depending on the level of ϕ_s.

The gate voltage when the status of strong inversion starts, is defined as the threshold voltage V_{th}. Therefore, V_{th} of an ideal MOS capacitor is given by

$$\begin{aligned} V_{th} &= 2\phi_f + \frac{\sqrt{4qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} \\ &= \frac{2kT}{q}\ln(N_a/n_i) + \frac{2\sqrt{N_a\varepsilon_{Si}\varepsilon_0\{kT\ln(N_a/n_i)\}}}{C_{OX}}. \end{aligned} \tag{2.1.11}$$

The 1st term of equation (2.1.11) means the voltage necessary to reach the strong inversion state by bending the band of p-type semiconductor substrate. This 1st term depends on the temperature and the acceptor impurity concentration in the substrate (the intrinsic carrier concentration n_i is also decided by the temperature). The 2nd term is the voltage which is generated by the electric field at the gate oxide layer, which is formed by the electric charge of acceptor ions in the depletion layer

(depletion charge) which was being increased until the attainment of the status of strong inversion. This 2nd term is influenced by the temperature, the acceptor impurity concentration in the substrate, and the capacitance of gate oxide.

2.1.2. V_{th} in a general MOS structure

The ideal MOS capacitor considered by the preceding section is defined as follows: (1)The only charges that can exist in the structure under any bias conditions are those in the semiconductor and those, with an equal but opposite sign, on the metal surface adjacent to the oxide. (2)There is no carrier transport through the oxide under dc bias conditions or the resistivity of the oxide is infinite [2]. The condition (1) means that there is no interface trap nor any kind of oxide charge and that the band doesn't have any curves without applying bias. Therefore, Fermi energy in the gate electrode metal agrees with that in the silicon substrate in a state of equilibrium. On the other hand, in the case of a general, not ideal MOS capacitor, electric charge can exist in the oxide layer, and the band is not straight at V_g=0 V. If the band which has a curve at V_g=0 becomes straight in a specific gate voltage, it is defined as the flat band voltage V_{FB}. V_{FB} is expressed as

$$V_{FB} = \varphi_{MS} - \frac{Q_{OX}}{C_{OX}}, \tag{2.1.12}$$

$$\varphi_{MS} \equiv \Phi_M - \Phi_{Si}. \tag{2.1.13}$$

Φ_M and Φ_{Si} is the work function (WF) of the metal gate and WF of a Si substrate respectively. Details about the work function are described at the section 2.3.

The 1st term φ_{MS} means a relative position of the Fermi level in the Si substrate measured from that in the metal gate (if it is described by the values of work function (Φ_M, Φ_{Si}), the sign becomes opposite to the case of using the values of Fermi level (E_F)). In equilibrium state where there is no applied voltage, if there is a Fermi level difference between the Si substrate and the metal gate, the band forms a bend and the oxide between metal and Si substrate forms a potential slope in order to make the Fermi level difference become 0. Therefore, for eliminating the bend of band and the potential slope in the oxide, a voltage φ_{MS} is needed to be applied at the gate electrode.

On the other hand, the 2nd term means influence of an electric charge in the gate oxide. When positive electric charges such as positive ions exist in the gate oxide layer, a certain negative voltage is needed for the gate electrode to compensate the effect of positive charge. Here, the effect of electric charge formed by positive ions in a gate oxide layer (the thickness is T_{OX}) is considered. If $\rho(x)$ represents the area density of electric charge at the distance x from the end of the gate oxide at the metal side, the electric potential at x=0 generated by the charge is $x\rho(x)/\varepsilon_{Si}\varepsilon_0$. Since $\Delta V=\Delta x$ $x\rho(x)/\varepsilon_{Si}\varepsilon_0$ is needed for compensation of this electric potential, the voltage V which compensates the effect of all ions in the oxide layer is expressed as

$$V = -\int_0^{T_{OX}} \frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} x dx = -\frac{1}{C_{OX}} \int_0^{T_{OX}} \frac{x}{T_{OX}} \rho(x) dx. \tag{2.1.14}$$

Here, $\varepsilon_{Si}\varepsilon_0$ was replaced by $C_{OX}T_{OX}$ using the relation of (2.1.8). If Q_{OX}, which is defined by

$$Q_{OX} = \int_0^{T_{OX}} \frac{x}{T_{OX}} \rho(x) dx \,, \tag{2.1.15}$$

is applied, (2.1.14) is expressed as

$$V = -\frac{Q_{OX}}{C_{OX}} \,. \tag{2.1.16}$$

Q_{OX} is the area density of electric charge which exists only at the interface between the gate insulator and the silicon substrate, and forms the same effect which is made by the electric charge distributed in the gate insulator. It means that if the effect of the electric charge in the gate insulator is represented by the effective electric charge density Q_{OX}, V_{FB} becomes higher by $-Q_{OX}/C_{OX}$ to compensate the effect of electric charge. This is the 2nd term in equation (2.1.12).

As a result, V_{th} of a general n-MOS capacitor is described as follows:

$$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{4qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} \tag{2.1.17}$$

$$= \Phi_M - \Phi_{Si} - \frac{Q_{OX}}{C_{OX}} + 2\phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} \tag{2.1.18}$$

$$= \Phi_M - (\chi_{Si} + \frac{E_g}{2q} + \phi_f) - \frac{Q_{OX}}{C_{OX}} + 2\phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}}$$

$$= \Phi_M - (\chi_{Si} + \frac{E_g}{2q}) - \frac{Q_{OX}}{C_{OX}} + \phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} \tag{2.1.19}$$

$$= \Phi_M - (\chi_{Si} + \frac{E_g}{2q}) - \frac{Q_{OX}}{C_{OX}} + \frac{kT}{q}\ln(N_a/n_i) + \frac{2\sqrt{N_a\varepsilon_{Si}\varepsilon_0\{kT\ln(N_a/n_i)\}}}{C_{OX}} \tag{2.1.20}$$

As the equation (2.1.17) indicates, V_{th} becomes higher when V_{FB} is higher. V_{FB} is expressed with three terms, from the 1st term to the 3rd term in (2.1.18). These equations mean that V_{FB} becomes high, if a material which has high work function is used for the gate electrode, or if the work function of Si is low (acceptor concentration is high or donor concentration is low), or if the density of negative charge in the gate insulator is high. In addition, the effect of negative charge in the gate insulator is enlarged if the gate capacitance is small (gate insulator thickness is thick).

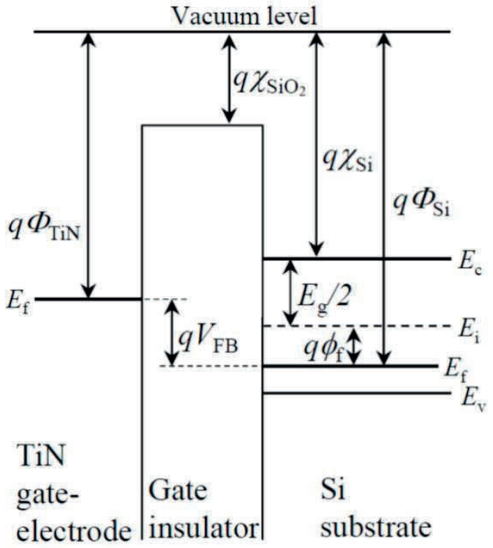

Fig. 2.2. Energy-band diagram at flat-band (gate voltage $=V_{FB}$) with the n-MOSFET used in this study. q is an elementary charge, χ_{Si} is the electron affinity of silicon, and E_g is the energy gap of Si. E_c is the bottom edge of the conduction band, E_v is the top edge of the valence band, and E_i is the intrinsic Fermi level. Φ_{TiN} and Φ_{Si} are the work functions of the TiN and Si substrates, and ϕ_f is the potential difference between the Fermi level and E_i.

Furthermore, the equation (2.1.20) is obtained by expressing Φ_{Si} in V_{FB} by $\chi_{Si}+E_g/2+\phi_f$, as indicated in Fig. 2.2 (χ_{Si} is the electron affinity of silicon, E_g is the energy gap of Si). The 1st term of (2.1.20) indicates that V_{th} becomes high, if a material which has high work function is applied for the gate electrode. And, the 4th term in (2.1.20) indicates that V_{th} becomes high, if the density of negative charge in the gate insulator is high (the effect becomes larger in a thicker gate insulator). The 5th term is the ϕ_f defined in the equation (2.1.10), which means a difference between the Fermi level in the semiconductor substrate and that in an intrinsic semiconductor. If the acceptor concentration is high, or if the carrier density of the intrinsic semiconductor is small (low temperature), the 5th term becomes large and V_{th} becomes high. Exactly speaking, if the acceptor concentration becomes higher, because the work function of Silicon substrate becomes higher, V_{FB} becomes smaller. A decrease in V_{FB} is regarded as factor of decrease in V_{th}. Concurrently, however, the increase in the acceptor concentration increases the potential change that the Si substrate needs for inversion state. This is regarded as factor of increase in V_{th}. The effect of latter is $-\phi_f$, and the effect of former is $+2\phi_f$. As a result, when the acceptor concentration in silicon substrate becomes higher, V_{th} becomes higher. The 6th term means the effect of the depletion charge. The effect of the 6th term also increases the V_{th}, if the acceptor concentration becomes higher, or if the carrier density of the intrinsic semiconductor becomes smaller (lower temperature). The effect of the 6th term is varied in inverse proportion to C_{ox} (in proportion to gate oxide thickness).

Furthermore, when there exist interface states between the gate oxide and the silicon substrate, we have to add the effect of electric charges which is generated by the interface states. If the interface states density is D_{it}, an additional new term is $+qD_{it}/C_{ox}$, and the equations for V_{th}, (2.1.17) ～(2.1.20) change to

$$V_{th} = V_{FB} + 2\phi_f + \frac{\sqrt{4qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} + \frac{qD_{it}}{C_{OX}} \tag{2.1.21}$$

$$= \Phi_M - (\chi_{Si} + \frac{E_g}{2q}) - \frac{Q_{OX}}{C_{OX}} + \phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} + \frac{qD_{it}}{C_{OX}} \tag{2.1.22}$$

$$= \Phi_M - (\chi_{Si} + \frac{E_g}{2q}) - \frac{Q_{OX}}{C_{OX}} + \frac{kT}{q}\ln(N_a/n_i) + \frac{2\sqrt{N_a\varepsilon_{Si}\varepsilon_0\{kT\ln(N_a/n_i)\}}}{C_{OX}} + \frac{qD_{it}}{C_{OX}}. \tag{2.1.23}$$

In the case of the discussion with consideration of the existence of the interface state, we must use (2.1.21)～(2.1.23) for the theoretical equation of V_{th}.

2.1.3. V_{th} in MOS device with a poly-Si gate

Until the previous section, MOS device was regarded as a literal Metal-Oxide-Semiconductor structure using complete metal for the gate electrode. However, the actually mass-produced MOS device usually applies poly-Si for gate electrode to which high-concentrated dopant (about 10^{20} cm^{-3} level) was implanted. This is because poly-Si has a superior heat-resisting property and poly-Si is favorable for shrinkage of MOSFET devices and the processing is easy, compared with metal. The band structure of n-type MOS capacitor which uses n-type poly-Si gate is indicated in Fig. 2.3. The WF of n-type poly-Si is represented by $\chi_{Si}+E_g/2-\phi_g$. ϕ_g is a potential difference between the Fermi level in the poly-Si gate electrode and that in an intrinsic semiconductor, and depending on the donor concentration N_g in poly-Si. In addition, a depletion layer is formed also in the gate electrode, and the gate voltage V_g increases by the electric potential (ϕ_p) that the depletion layer makes [3].

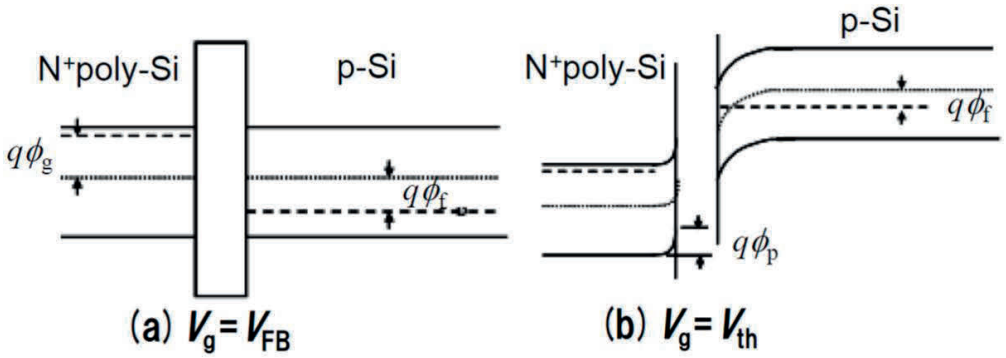

Fig. 2.3. Energy-band diagram of p-type $Si/SiO_2/N^+$poly-Si gate [3].
(a) Flat band voltage (b) Threshold voltage.

When a bend of the band in the silicon substrate has become $2\phi_f$ and V_g has reached V_{th}, the electric charge which exists in the substrate side is expressed in (2.1.4). Since the same electric charge exists also in the gate electrode side,

$$Q_D = -\sqrt{2qN_g\varepsilon_{Si}\varepsilon_0\phi_p} = -\sqrt{2qN_a\varepsilon_{Si}\varepsilon_0\phi_s} \ ,$$

$$\phi_p = \frac{N_a}{N_g}\phi_s = \frac{2N_a}{N_g}\phi_f \ . \tag{2.1.24}$$

Therefore, when poly-Si is applied for gate electrode, V_{th} is described based on (2.1.18) with

$$\begin{aligned} V_{th} &= \Phi_M - \Phi_{Si} - \frac{Q_{OX}}{C_{OX}} + 2\phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} + \phi_p \\ &= (\chi_{Si} + \frac{E_g}{2q} - \phi_g) - (\chi_{Si} + \frac{E_g}{2q} + \phi_f) - \frac{Q_{OX}}{C_{OX}} + 2\phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} + \frac{2N_a}{N_g}\phi_f \\ &= -\frac{Q_{OX}}{C_{OX}} - \phi_g + \left(1 + \frac{2N_a}{N_g}\right)\phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}} \qquad (2.1.25) \\ &= -\frac{Q_{OX}}{C_{OX}} + \frac{kT}{q}\left\{\ln\left(N_a/N_g\right) + \frac{2N_a}{N_g}\ln\left(N_a/n_i\right)\right\} + \frac{2\sqrt{N_a\varepsilon_{Si}\varepsilon_0\left\{kT\ln\left(N_a/n_i\right)\right\}}}{C_{OX}} \ . \qquad (2.1.26) \end{aligned}$$

Compared with the case of metal gate electrode (2.1.20), for example, the coefficient of $\ln(N_a/n_i)$ becomes $2N_a/N_g$ times. It means the amount of change of V_{th} caused by change of n_i is different from the case of metal gate. In the next section, I will show how temperature dependence of V_{th} changes by using a poly-Si gate instead of a metal gate.

2.2. Temperature dependence of V_{th}

2.2.1. Temperature coefficient of V_{th} in metal gate MOS device

Subject of this thesis is the temperature coefficient of V_{th} (dV_{th}/dT) in a metal gate transistor. Since theoretical equations of V_{th} have already been attained in the previous section 2.1, the equations are differentiated with temperature T. First, MOS device with metal gate electrode, which is expressed by simpler equation (2.1.19), is considered.

$$\begin{aligned} \frac{dV_{th}}{dT} &= \frac{d}{dT}\left[\Phi_M - (\chi_{Si} + \frac{E_g}{2q}) - \frac{Q_{OX}}{C_{OX}} + \phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}}\right] \\ &= \underbrace{\frac{d}{dT}\left(\Phi_M - \chi_{Si} - \frac{Q_{OX}}{C_{OX}}\right)}_{\text{1st ingredient}} + \underbrace{\frac{d}{dT}\left(-\frac{E_g}{2q}\right)}_{\text{2nd ingredient}} + \underbrace{\frac{d}{dT}\left(\phi_f + \frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}}\right)}_{\text{3rd ingredient}} \end{aligned} \tag{2.2.1}$$

Here, the differential coefficients are classified in three ingredients. The 1st ingredient, which contains metal work function Φ_M, electron affinity of Si χ_{Si}, the effective electric charge density in the gate insulator Q_{OX}, and the gate capacitance C_{OX}, is usually treated as negligible ingredient, because these parameters are considered not to have (or hardly to have) temperature dependence [3-5]. Because this section 2.2 is the explanation of basic theory, also here, I will describe dV_{th}/dT in degree of precision of the usual consideration and discuss with ignoring this 1st ingredient. But, the subject of this thesis is detailed consideration of dV_{th}/dT. Therefore, the influence of this 1st ingredient is discussed once again at the following section 2.3, and try to detect by measurement in the next Chapter 3.

Since E_g (bandgap of the silicon) becomes small at high temperature, Φ_{Si} (the work function of the silicon) decreases by a rise of temperature, because $\Phi_{Si} = \chi_{Si} + E_g/2q + \phi_f$ as shown in Fig. 2.2. The 2nd ingredient means an effect of increase in work function difference between the metal gate and the Si substrate (= increase in V_{FB}) which is caused by decrease in E_g at high temperature. Beye *et al.* reported that the temperature coefficient of $E_g/2q$ is −0.23 mV/K [6]. When temperature rises, the effect of the 2nd ingredient changes V_{FB} and V_{th} toward the positive direction by 0.23 mV/K.

The 3rd ingredient is the ingredient which collected the terms which contain ϕ_f which has large temperature dependence. It is considered that the 3rd ingredient substantially decides the approximate value of dV_{th}/dT.

This 3rd ingredient will be calculated. First, for the preparations, the differential coefficient of (2.1.10), which is $\phi_f = kT\{\ln(N_a/n_i)\}/q$, will be attained. Here, N_c and N_v means effective density of state in conduction band and valence band, respectively. Because both N_c and N_v are proportional to 1.5th power of T [7], their product is expressed as $N_cN_v = T^3 f(x)$. Therefore, $d(N_cN_v)/dT$ can be replaced by using $d(N_cN_v)/dT = 3T^2 f(x) = 3N_cN_v/T$, and $d\phi_f/dT$ is expressed as follows:

$$
\begin{aligned}
\frac{d\phi_f}{dT} &= \frac{d}{dT}\frac{kT}{q}\ln\left(N_a/n_i\right) = \frac{k}{q}\left\{T\frac{d}{dT}\ln\left(N_a/n_i\right) + \ln\left(N_a/n_i\right)\right\} \\
&= \frac{kT}{q}\frac{d}{dT}\ln\left\{N_a\left(N_cN_v\right)^{-1/2}\exp\left(\frac{E_g}{2kT}\right)\right\} + \frac{k}{q}\ln\left\{N_a\left(N_cN_v\right)^{-1/2}\exp\left(\frac{E_g}{2kT}\right)\right\} \\
&= \frac{kT}{q}\frac{d}{dT}\left\{\ln\left(N_a\right) - \frac{1}{2}\ln\left(N_cN_v\right) + \frac{E_g}{2kT}\right\} + \frac{k}{q}\ln\left\{N_a\left(N_cN_v\right)^{-1/2}\right\} + \frac{E_g}{2qT} \\
&= -\frac{kT}{2q}\frac{d\left(N_cN_v\right)}{dT}\frac{1}{N_cN_v} + \frac{T}{2q}\left(\frac{1}{T}\frac{dE_g}{dT} - \frac{E_g}{T^2}\right) + \frac{k}{q}\ln\left\{N_a\left(N_cN_v\right)^{-1/2}\right\} + \frac{E_g}{2qT} \\
&= -\frac{kT}{2q}\frac{3N_cN_v}{T}\frac{1}{N_cN_v} + \frac{1}{2q}\frac{dE_g}{dT} + \frac{k}{q}\ln\left\{N_a\left(N_cN_v\right)^{-1/2}\right\} \\
&= \frac{1}{2q}\frac{dE_g}{dT} - \frac{3k}{2q} - \frac{k}{q}\ln\left(\frac{\sqrt{N_cN_v}}{N_a}\right).
\end{aligned}
\tag{2.2.2}
$$

Therefore, the 3rd ingredient in equation (2.2.1) is given as

$$\frac{d}{dT}\left\{\phi_f+\frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}}\right\}=\frac{d\phi_f}{dT}+\frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0}}{C_{OX}}\frac{d}{dT}\sqrt{\phi_f}=\frac{d\phi_f}{dT}\left(1+\frac{\sqrt{qN_a\varepsilon_{Si}\varepsilon_0/\phi_f}}{C_{OX}}\right)$$

$$=\frac{1}{q}\left[\frac{1}{2}\frac{dE_g}{dT}-k\left\{\frac{3}{2}+\ln\left(\frac{\sqrt{N_cN_v}}{N_a}\right)\right\}\right]\left(1+\frac{\sqrt{qN_a\varepsilon_{Si}\varepsilon_0/\phi_f}}{C_{OX}}\right). \qquad (2.2.3)$$

As already mentioned, this 3rd ingredient in (2.2.1) is thought to be the prime factor which decides the value of dV_{th}/dT. For example, in the case of N_a=1x10^{17} cm^{-3}, EOT=2.0 nm, T=300 K, the calculated magnitude of the 3rd ingredient of (2.2.1) becomes −0.95 mV/K (The value of N_c, N_v was assumed 3.2x10^{19} cm^{-3}, 1.8x10^{19} cm^{-3}, respectively [8]).

Here, if EOT increases, the C_{OX} decreases, which cause an increase in the absolute value of the 3rd ingredient (<0). It means that the quantity of reduction of V_{th} due to a temperature rise becomes large. On the other hand, the change direction of the absolute value of the 3rd ingredient (<0) caused by an increase in N_a is not fixed. If EOT is thick, an increase in N_a causes an increase in the absolute value of the 3rd ingredient (the quantity of reduction of V_{th} due to a temperature rise becomes large). In the case of thin EOT, an increase in N_a causes a decrease in the absolute value of the 3rd ingredient (the quantity of reduction of V_{th} becomes small) [5].

As mentioned above, in "normal consideration" explained in this section 2.2, dV_{th}/dT is regarded as the sum of the 2nd and 3rd ingredients in equation (2.2.1) (the 1st ingredient is ignored). Although the 2nd ingredient is positive and the 3rd ingredient is negative, the 3rd ingredient usually has a larger absolute value. Therefore, when the temperature rises, V_{th} decreases by strong influence of the 3rd ingredient. The effect of the 2nd ingredient is making the influence of the 3rd ingredient dull. Under the condition mentioned above, dV_{th}/dT is calculated as

$$\frac{dV_{th}}{dT}=\frac{d}{dT}\left(-\frac{E_g}{2q}\right)+\frac{d}{dT}\left(\phi_f+\frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}}\right)=+0.23-0.95=-0.72\ \text{mV/K}. \qquad (2.2.4)$$

This result shows that V_{th} becomes lower by 72 mV when the temperature becomes higher by 100 K.

2.2.2. Temperature coefficient of V_{th} in poly-Si gate MOS device

In the case of poly-Si gate electrode, the temperature dependence is obtained from equation (2.1.25). The both sides of (2.1.25) were differentiated by temperature T. If ingredients which have no temperature dependence or which hardly have temperature dependence were ignored like the previous section, dV_{th}/dT was expressed as

$$\frac{dV_{th}}{dT}=\frac{d}{dT}\left(\frac{2N_a}{N_g}\phi_f-\phi_g\right)+\frac{d}{dT}\left(\phi_f+\frac{2\sqrt{qN_a\varepsilon_{Si}\varepsilon_0\phi_f}}{C_{OX}}\right). \qquad (2.2.5)$$

$\Delta dV_{th}/dT$, which is the increase from the case of metal gate expressed as equation (2.2.4), is given as

$$\Delta\frac{dV_{th}}{dT}=\frac{d}{dT}\left(\frac{E_g}{2q}-\phi_g+\frac{2N_a}{N_g}\phi_f\right)=\frac{1}{2q}\frac{dE_g}{dT}-\frac{d\phi_g}{dT}+\frac{2N_a}{N_g}\frac{d\phi_f}{dT} \tag{2.2.6}$$

$$=\frac{1}{2q}\frac{dE_g}{dT}-\frac{1}{2q}\left\{\frac{dE_g}{dT}-3k-2k\ln\left(\frac{\sqrt{N_cN_v}}{N_g}\right)\right\}+\frac{N_a}{qN_g}\left\{\frac{dE_g}{dT}-3k-2k\ln\left(\frac{\sqrt{N_cN_v}}{N_a}\right)\right\}$$

$$=\frac{k}{2q}\left\{3+2\ln\left(\frac{\sqrt{N_cN_v}}{N_g}\right)\right\}+\frac{N_a}{N_g}\left[\frac{1}{q}\frac{dE_g}{dT}-\frac{k}{q}\left\{3+2\ln\left(\frac{\sqrt{N_cN_v}}{N_a}\right)\right\}\right] \tag{2.2.7}$$

The 1st term and the 2nd term in (2.2.6) indicate the effect caused by the shift of Fermi level which moves depending on the temperature because the gate electrode is changed into an N-type poly-Si from a metal in which the Fermi level is regarded as fixed (a rise in temperature causes a drop in the gate Fermi level = an increase in the gate work function = an increase in the V_{th}). This effect corresponds to the 1st term in the equation (2.2.7). For example, the value of the 1st term becomes +0.11 mV/K if N_g is 3x10^{19} cm^{-3}. Since dV_{th}/dT in the metal gate has negative value (for example, (2.2.4) shows it is −0.72 mV/K under the condition of previous section), positive $\Delta dV_{th}/dT$ makes an effect which decreases $|dV_{th}/dT|$ (−0.72 + 0.11 = −0.61 mV/K). It means reduction of temperature coefficient of V_{th}. This effect becomes large when N_g (donor concentration in poly-Si gate electrode) becomes small.

The 3rd term in the equation (2.2.6) is caused by a change of the potential difference which is generated by a depletion layer in the gate electrode. In equation (2.2.7), the effect is equivalent to the 2nd term. When the effect is calculated under the condition of the previous section (N_a=1x10^{17} cm^{-3}, N_g=3x10^{19} cm^{-3}), it becomes −0.005 mV/K. Since dV_{th}/dT has negative value (for example, −0.72 mV/K), negative $\Delta dV_{th}/dT$ makes an effect which increases $|dV_{th}/dT|$. But, in this example, the effect is relatively small (|−0.005| < |−0.72|).

In this way, the changes generated by the application of a poly-Si gate electrode are "shift of the work function in the gate (caused by temperature change)" and "(temperature change of) depletion at the gate electrode". They have a reverse effect for $|dV_{th}/dT|$ each other. $|dV_{th}/dT|$ is decreased by the effect of the former, and increased by the effect of the latter. In both of them, the absolute values of the effect for $|dV_{th}/dT|$ become large when N_g (the donor concentration in the poly-Si gate) becomes small. But the former becomes superior in the range of the usual concentration for applying to poly-Si gate electrode. Therefore, it can be said that $|dV_{th}/dT|$ becomes smaller in the case of poly-Si gate than in the case of metal gate [3]. Actually, also in above-mentioned calculation example, the value of the former was +0.11 mV/K, and that of the latter was −0.005 mV/K, which illustrates that the former becomes sufficiently large. In conclusion, $|dV_{th}/dT|$ is increased by change to a metal gate from a poly-Si gate.

2.3. Work function and its temperature coefficient

2.3.1 Factors which decide the work function

As we saw in the foregoing section 2.1.2, the value of the work function of a silicon substrate and gate electrode material affects V_{th} directly. Here, "work function" is explained anew. The work

function (WF) is the minimum energy which is needed to remove an electron from a surface of a solid to an infinite distance point in the vacuum. WF is influenced by the energies of electrons and the property of the surface of the material (depending on crystal orientation or contamination). If it is assumed that electric charge is distributed as shown in Fig. 2.4 (a), and potential is distributed as shown in (b) around the surface of a material, the WF is given by the expression

$$\Phi = \Delta\varphi - \bar{\mu}. \tag{2.3.1}$$

Here, $\bar{\mu}$ is the chemical potential of the electrons in the bulk metal [9], which is determined by the kinetic energy and the exchange-correlation energy of the electron gas [10]. When the absolute temperature T=0 K, $\bar{\mu}$ becomes equal to Fermi level E_f, and the WF becomes the energy difference between the electrostatic potential in the vacuum nearby the surface and the Fermi level.

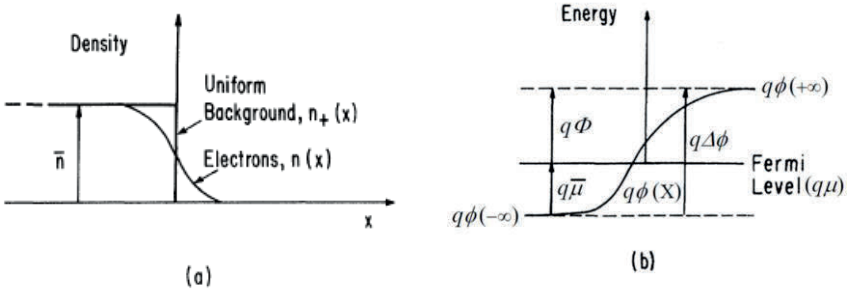

Fig. 2.4. Schematic representation of (a) charge density distributions at a metal surface and (b) various energies relevant to the definition of the WF [9].

Next, $\Delta\varphi$ is the change in electrostatic potential across the metal/vacuum interface. As shown in Fig. 2.4 (a), because there exists positive charge due to positive ions, "spilling out" of electrons at the surface makes positive charge inside the surface, and negative charge outside the surface. As a result, local dipole moments toward inside of the material are created and they influence the value of $\Delta\varphi$ [9-11]. The situation becomes more complicated in an actual crystal. Figure 2.5 indicates schematic diagrams which show the rearrangement of electric charge at a surface of a crystal. Smoluchowski explained about mechanism of the formation of double layer of electric charge at the surface as follows [12, 13]. With every atom one can associate a polyhedron with the atom at its center, such that it contains all points nearer to the atom under consideration than to any other atom. If the distribution of the electron density within these polyhedra of the surface atoms was the same as for the inside atoms then there would be no double layer on the surface. However, this is not the case since the total energy is lowered by a redistribution of the electron cloud on the surface. There are two effects: the first is a partial spread of the charge out of the polyhedra of the surface atoms (the dipole is directed toward inside of the material as shown in Fig. 2.5 (a)). The second is a tendency to smooth out the surface of the polyhedral (the dipole is directed toward outside as shown in Fig. 2.5 (b)). In consequence of the second effect the surfaces of equal charge density are more nearly plane than in the original picture. The first effect forms a negative dipole layer which

increases the work function, and the second effect forms a positive dipole layer which reduces the work function. The two effects have opposite influences and since they are comparable in magnitude, it is not possible to predict the sign of the total double layer without numerical computations. Thus, work functions become different depending on the crystal structure or the crystal orientation, even if it is the same material. Lang *et al*. acquired concrete work functions in various metals by a calculation using the pseudopotential which was formed by the positive ions which constitutes the crystal lattice [9]. Compared with the uniform-positive-background model, in which the lattice of positive ions are replaced by a uniform background charge, there were tendencies that the work function becomes higher in the face centered cubic (fcc) structure and becomes lower in the body centered cubic (bcc) structure (Fig. 2.6). This result implies that fcc structure, which is the structure of TiN which was used as a gate metal in this study, has a property that the dipole formed at its surface hinders a release of an electron from inside of it. When a metal is not single-crystal structure but polycrystal structure, the work function of the metal becomes the mean of the work function of each crystal orientation. This model could obtain a theoretical value that is close to the measured value to some extent, except some exceptions.

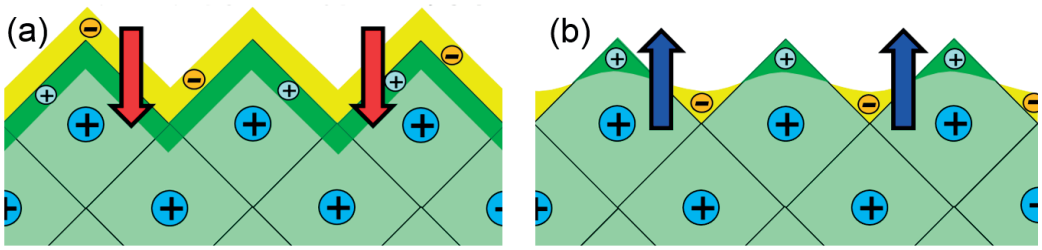

Fig. 2.5. Schematic diagrams which represent rearrangement of electric charge at a surface of a crystal. Yellow zones mean negative charged areas, and green zones mean positive charged areas.
(a) indicates a partial spread of the charge out of the polyhedra of the surface atoms.
(b) indicates effects of a tendency to smooth out the surface of the polyhedra. The arrows show a direction of the dipoles. [12].

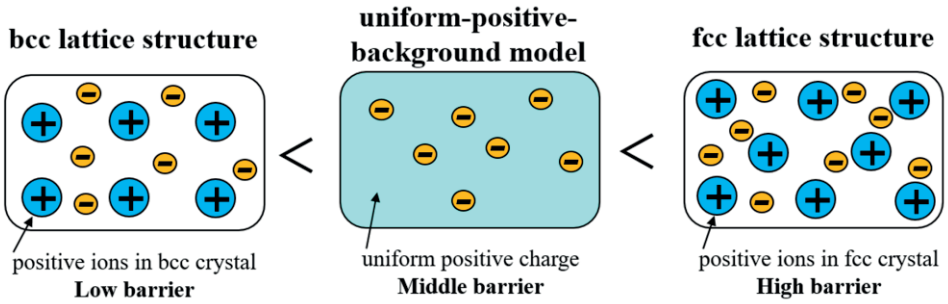

Fig. 2.6. Schematic diagram which indicates relationship between the distribution of the positive charge and the height of barrier for electrons caused by the effects of surface dipole.

2.3.2 Observation of the crystal orientation dependence of the work function

(1) Single crystal materials

The actual modulation of metal WF by dipole density was observed in the 1970s using photoelectrical measurements performed on different faces of the single crystal materials [10]. In the results of Cu, Al and Ag, there is a correlation between WF values and material surface atomic density, i.e. dipoles density, which shows that an increase in crystallographic face density implies an increase in the WF [12].

(2) Polycrystalline materials

In case of polycrystalline materials, a method of local WF measurement is needed. Gaillard *et al*. reported on WF measurements performed at deca-nanometer scale using Kelvin probe Force Microscope (KFM) [10]. The KFM technique permits both the surface topography and WF variations to be plotted with a spatial resolution in the order of 50 nm. The local WF at the surface of Cu polycrystalline was measured by KFM (Fig. 2.7 (b)), and crystallographic orientation was measured by Electron Back Scattered Diffraction (EBSD) with the same Cu sample (Fig. 2.7 (c)). By the comparison between EBSD analysis and WF mapping, they showed that the distribution of WF corresponds to the crystallographic orientation of each Cu grain. The WF values of high, medium and low are related to the <111>, <100> or <110> grain orientation. For fcc lattice systems such as Cu, Al and Ag, the denser faces are <111>, followed by <100> and <110>. It indicated that their observations with polycrystalline material were in agreement with both experimental results on single crystal materials and theoretical predictions which suggest that an increase in the density of the crystallographic face density leads to an increase in the WF.

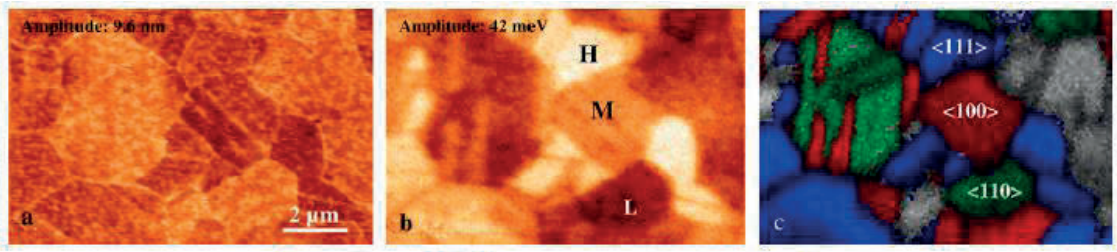

Fig. 2.7. Topography (a), Work function (b), Electron back scatter diffraction patterns (c) mapping of the same polished Cu area (12 µm x 8 µm) [10].

(3) TiN

The work function metal used in this study is TiN. TiN has a property which shows a trend to make columnar crystal grains in a longitudinal direction, and the size of the grain in a transverse direction is relatively small. The grain size in a transverse direction was about 10 nm in the samples we made, and it was 22 nm in a previous report [11]. Because the grain size of TiN is smaller than the spatial resolution of KFM (about 50 nm), a spatial distribution of local WF in TiN film has not been measured yet. The actual WF of TiN as a gate electrode of MOS structure is averaged according to the area rate of the crystallographic orientation [9, 11]. Dadgour *et al.* reported that under the gate size in the recent SRAM technology (deca-nanometer), the difference in local WF in

TiN metal gate (They calculated with a condition that the local WF of TiN is 4.6 eV at <200> and 4.4 eV at <111>) causes WF variation of the gate electrode [11]. Since the purpose of this study is basic research of behaviors of WF in TiN gate, we used MOS samples whose gate area is more than several μm^2, to avoid the problem of variability.

About TiN, however, not a WF of a small grain of single crystal but a WF of polycrystal, which was thought to be an averaged value of WF of small grains, was directly measured by Gaillard *et al*. [10]. They reported that a TiN layer which has clear crystal structures has higher WF than a TiN layer which has an amorphous-like structure. They compared the WF of 30-nm-thick TiN layers, which were formed by PVD on different substrates. The crystallinity of TiN is affected by the substrate, and XRD measurements indicated that TiN/Al has clearer crystal structure than TiN/SiO_2. The work function of each sample was measured by KFM, which showed that the WF of TiN/Al was 240 meV higher than that of TiN/SiO_2. This experimental result that TiN with higher crystallinity (i.e. more rigid fcc structure) has higher WF is thought to correspond with the results of theoretical calculation by Lang *et al*. [9] described in the section 2.3.1.

2.3.3 Temperature dependence of work function

As we saw in the section 2.2.1, temperature coefficients of WF of metal films are often regarded as very small value. In fact, a WF of metal film is changed according to the temperature. There are some factors which determine the temperature dependence of metal WF [14]. For example, a thermal expansion effect or an internal electrostatic effect of atomic vibrations, etc. Crowell *et al.* calculated those effects theoretically and compared the theoretical value of the temperature coefficients of WF with the experimental value [15]. There were some metals which have an experimental value which is close to the theoretical value, such as Ag (experimental value –0.134 mV/K, theoretical value –0.118 mV/K), K (experimental value –0.26 mV/K, theoretical value –0.28 mV/K), and Na (experimental value –0.51 mV/K, theoretical value –0.45 mV/K). However, difference between theoretical value and experimental value was relatively large in the case of Cu (experimental value –0.06 mV/K, theoretical value –0.143 mV/K). Their theoretical value didn't include influence of the temperature dependence of the effect of the surface dipole. Because the effect of the surface dipole is relatively large in Cu, it is thought that the difference from the experimental value became large. Because the theoretical prediction of temperature coefficient of metal WF including the effect of surface dipole requires more complicated analysis, it seems difficult to calculate a precise temperature coefficient of metal WF influenced by surface dipole.

As actual measurement of the influence of the surface dipole on the value of WF, Blevis *et al.* reported the case of Cu in wider range of temperature [16]. Diode retarding-field method was selected for their measurements. Although it did not lend itself to accurate determination of the absolute WF, it offered the advantage of a sensitive indication of small changes in the WF. Their measurements were made on (100), (110), (111), (211), and (221) faces of single crystals of high-purity copper. Temperature dependence of WF of Cu was shown in Fig. 2.8 by combining it with the absolute value of WF of Cu which other literature reported. WF of (100) and (111) decreases at a high temperature together, and it is expected that they become the same value at the melting point if they are extrapolated. If the WF of Cu becomes higher due to the effect of the dipole at the

surface of the fcc structure as described in section 2.3.1, this result implies that the effect of the surface dipole becomes small at the high temperature and the difference of WF depending on the crystal orientation also becomes small. In addition, they indicated that there is a possibility that the difference of WF of tungsten due to crystal orientation becomes small at high temperature and becomes same at the melting point, as well as the case of Cu. The reason why the difference of effect of the surface dipoles reduces at high temperature may be because the vibrations of the atomic lattice are increased by heat, and steepness of the potential distribution formed by positive ions is decreased, and the strength of the surface dipole effect is weakened. The phenomenon that the difference of WF depending on the crystal orientation is lost at the melting point is explained as follows from a point of view of thermodynamics [16]. Change from a liquid phase to a solid phase is a 1st order phase transition. In the case of the 1st order phase transition, although the Gibb's free energy (G) itself is equivalent before and behind the phase transition, which means the melting point here ($G_{Liquid}=G_{Solid}$), the 1st-order differential coefficient of G by the temperature becomes a discontinuous point at the phase transition. Work function Φ is expressed as $\Phi=\{(\partial G/\partial n)_{P,T}\}/q$. Since there is not the essential change even if n (the number of electrons in the crystal) increases under the same temperature and pressure, $\Phi_{Liquid}=\Phi_{Solid}$ is completed. On the other hand, because $\partial G/\partial T$ is discontinuous before and behind the melting point, the temperature coefficient of the work function Φ would be also permitted different values between before and behind the melting point. It means that at the melting point, all Φ becomes same regardless of the liquid phase or the solid phase, but at the temperature less than the melting point, Φ may become different values depending on the crystal orientation.

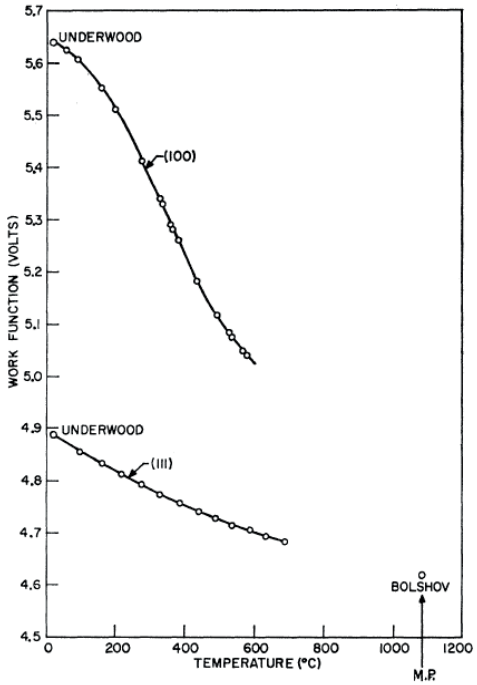

Fig. 2.8. The expected temperature dependence of work function of Cu (100), (111) [16].

2.3.4 Effective work function

V_{FB} of MOS depends on the work function difference between Si substrate and gate electrode and the effect of fixed electric charge, as expressed by equation (2.1.12). In the case of poly-Si gate electrode, the work function in gate electrode Φ_M is expressed as

$$\begin{aligned}\Phi_M &= \chi_{Si} + \frac{E_g}{2q} \mp \phi_g \\ &= \chi_{Si} + \frac{E_g}{2q} \mp \frac{kT}{q}\left\{\ln\left(N_g / n_i\right)\right\}. \end{aligned} \tag{2.3.2}$$

Here, ϕ_g is a potential difference between the Fermi level in the poly-Si gate electrode and that in an intrinsic semiconductor, and N_g is the impurity concentration in poly-Si. Usually, the upsides of the double signs are chosen for n-MOSFET (n-type poly-Si gate electrode), and the downsides of those are for p-MOSFET (p-type poly-Si gate electrode). Thus, in the case of conventional gate insulator which consists of SiO_2, Φ_M is decided by (2.3.2), and V_{FB} is decided by (2.1.12). When high-k material was used for gate insulator, however, examples which could not explain V_{FB} (could not explain V_{th} either) with these equations came to be reported [17]. On the other hand, also in the contrary case in which the gate electrode was metal and the gate insulator was SiO_2 (SiO_2/Metal structure), there were reports which indicated that observed WF became different from the original WF of the metal, if high temperature process was performed in its process.[18-20]. The Φ_M which is evaluated with real measurement of V_{FB} agrees with the Φ_M derived with the equation (2.3.2) in the conventional case of the SiO_2/poly-Si structure. In the case of other structure such as High-k/poly-Si or SiO_2/Metal, however, the Φ_M evaluated with observed V_{FB} does not agree with the Φ_M derived with the equation (2.3.2) or the original WF of the metal. In such cases, the work function calculated from the measured V_{FB} of a real MOS sample is called “effective work function” (eWF). "Fermi level pinning" and "capping" will be explained below as examples in which the effective work function must be considered.

(1) Fermi level pinning

Fermi level pinning is a phenomenon by which the effective work function of the gate electrode changes into a specific value different from the intrinsic work function of gate electrode according to combination of the gate insulator material and the gate electrode material. Two examples, "SiO_2 insulator/metal electrode" and "metal oxide insulator/poly-Si electrode" are explained as typical cases.

(1-A) SiO_2 insulator/metal electrode

In the structure of SiO_2 insulator/metal electrode, eWF of metal electrode shifts from its intrinsic position, especially if high temperature process such as activation anneal is performed (eWF is often located around midgap, the center of band gap). Yu *et al.* proposed a model that thermal process causes a reaction at SiO_2/metal interface, and interfacial bonding defects are generated, and extrinsic states are formed in the band gap of SiO_2 [18]. If extrinsic states are located at a specific energy height as shown in Fig. 2.9, electrons are captured by extrinsic

states when the Fermi level in metal is above the height. As a result, interface dipole where the SiO_2 side is the negative charge side is generated. Conversely, when the Fermi level in metal is lower than the extrinsic states, the interface dipole where the SiO_2 side becomes the positive charge side is generated. The effect of the interface dipoles changes the electric potential of the metal gate, which brings the result that the Fermi level is pinned to the position of extrinsic states. The location of FLP, which means the location of the extrinsic states, depends on the combination of the material of the gate electrode and that of the gate insulator. In a combination in which extrinsic states are not generated, FLP does not occur. In the case of HfO_2 insulator/metal gate (HfO_2 is typical high-k material), even if high temperature process is added, FLP is not as serious as above-mentioned SiO_2 insulator/metal gate [18]. SiO_2 chemically reacts with the metal which constitutes the electrode more easily than HfO_2, and SiO_2 is thought to generate extrinsic states more easily than HfO_2.

On the other hand, there is a model that the factors which make the difference between the effective WF and the original WF of the metal are the bonds such as Ti-Si or Ti-Hf at the interface of TiN and gate insulator [19, 20]. Since each atom has different electronegativity, a bond of different atoms forms a dipole. Because the difference of the electronegativities is changed according to the combination of the atoms, the difference between the effective WF and the original WF of the metal changes depending on the kind of the gate insulator (regarded as the difference of the strength of the FLP effect).

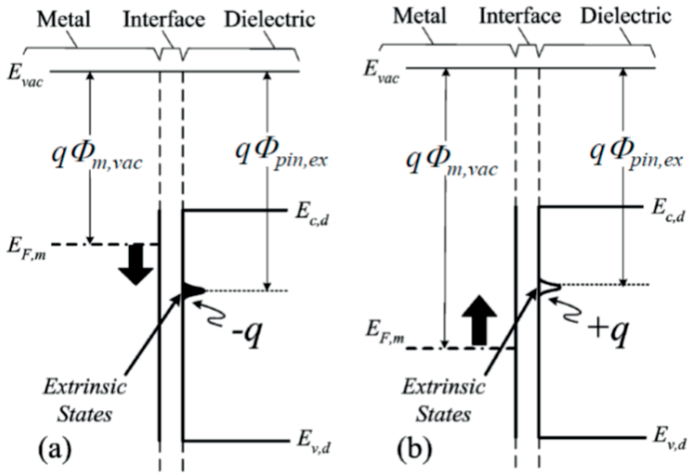

Fig. 2.9. Schematic energy band diagram for a metal gate on a dielectric, showing extrinsic states that pin the metal Fermi level. The energy level of the extrinsic states, i.e., pinning level, could be related to the interfacial bonding. (a) When the metal Fermi level is above the pinning level, a dipole is created that is charged negatively on the dielectric side. (b) When the metal Fermi level is below the extrinsic pinning level, a dipole is created that is charged positively on the dielectric side. For both cases, the interfacial dipole drives the metal Fermi level toward the pinning level. $E_{f,m}$ means metal Fermi level. $E_{c,d}$ and $E_{v,d}$ mean the conduction-band edge and valence-band edge of the dielectric, respectively. [18].

(1-B) metal oxide insulator/poly-Si electrode

FLP occurs also in the combination of high-k gate insulator and conventional poly-Si electrode. I will explain with an example of HfO_2/poly-Si gate electrode (although this structure was not used in this study). The conventional SiO_2/poly-Si structure can easily control the Φ_M (work function in the gate electrode) with the N_g (impurity concentration in the poly-Si) according to the equation (2.3.2). In order to make the surface channel type n-MOSFET and p-MOSFET, the difference of eWF is set around 1 V between n-MOSFET (n-type poly-Si) and p-MOSFET (p-type poly-Si) [17]. On the other hand, in the case of HfO_2/poly-Si, the Fermi level in p-type gate poly-Si with acceptors becomes a value close to that in n-type gate poly-Si without obeying the equation (2.3.2) [17]. The Fermi level is pinned near the E_c in both n-type poly-Si and p-type poly-Si. Therefore, with the HfO_2/poly-Si structure, the decrease in V_{th} at the p-type MOSFET is limited. For example, Hayashi *et al.* reported that in a MOSFET with HfSiON/poly-Si gate structure, V_{th} in n-channel was about 0.35 V and $|V_{th}|$ in p-channel was about 0.70 V [21]. To suppress such problem caused by FLP will be a serious issue at the introduction of high-k gate insulator.

The basic mechanism that causes FLP in high-k/poly-Si is thought to be a phenomenon that effective WF in poly-Si is changed by dipole generated in the High-k/poly-Si interface. But several opinions exist about the cause of the dipole generation.

Above-mentioned Hobbs explained that the movement of electron from Hf toward Si in Hf-Si bonds formed at HfO_2/poly-Si interface generated dipoles [17]. In this model, in the case of n-type poly-Si gate, there is no available levels in Si. But, in the case of p-type poly-Si gate, electrons occupy the acceptor states in Si, and E_F is raised toward midgap.

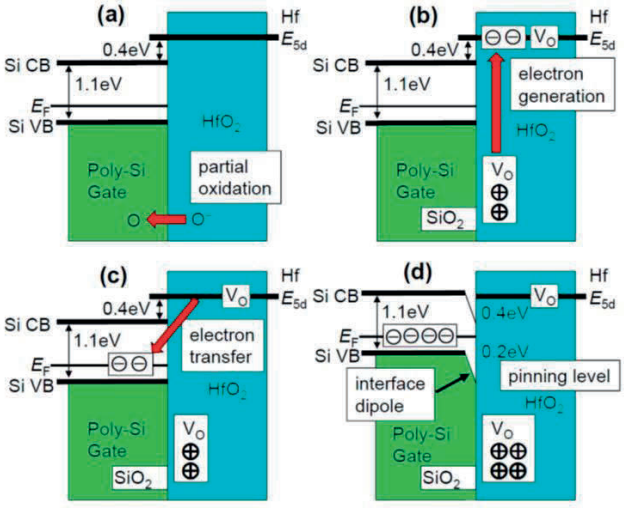

Fig. 2.10. Schematic diagram of electron transfer at poly-Si/HfO_2 interface. (a) An oxygen atom was pulled out of HfO_2 and the bulk Si of gate electrode was oxidized partially. (b) Two electrons were generated at HfO_2 region, and (c) the electrons transfer to the gate electrode. (d) Formation of interface dipole and the increase in Fermi level in the gate poly-Si [22, 23].

On the other hand, there is an opinion that vacancy (Vo) was generated at the position of oxygen in HfO_2 was the cause [22, 23].

The schematic diagrams are indicated in Fig. 2.10. (a)~(d). When poly-Si gate electrode came in contact with HfO_2, an oxygen atom was pulled out of HfO_2 and the bulk Si was oxidized partially, and a Vo was formed in HfO_2. HfO_2 is an ionic crystal and the state of oxygen atom in the crystal is O^{2-}. Therefore, when neutral O atom is pulled out of the crystal, two electrons which can move freely are left in the crystal. These electrons occupy the energy level of the Vo in HfO_2 at the position that is higher than E_c (Fig. 2.10 (b)). If HfO_2 comes in contact with poly-Si gate electrode, however, these electrons flow in the Si side where Fermi level is lower than the energy level of Vo in HfO_2 (Fig. 2.10 (c)). As a result, interface dipole is formed, and the Fermi level in the gate poly-Si increases (Fig. 2.10 (d)). Especially, in the case of p-type poly-Si gate electrode which has originally low Fermi level, many electrons move from HfO_2 to the poly-Si gate, and the Fermi level finally reaches the position which is about 0.2 eV lower than E_c (This is usually the position of Fermi level in n-type poly-Si gate). It is thought that FLP is unavoidable by above-mentioned mechanism in the case of combination of poly-Si gate electrode and HfO_2 which is an ionic crystal.

In conclusion, to reduce the effective gate oxide thickness of the MOSFET and to avoid asymmetric V_{th} of n- and p-MOSFET, it is necessary to choose suitable combination of materials of gate electrode metal and gate insulator high-k in consideration of FLP.

(2) Capping

A capping layer is deposited on high-k insulator, which has an effect to change the eWF. Representative materials are La_2O_3 and Al_2O_3 [24-28]. After forming a gate insulator, the deposition process of La_2O_3 or Al_2O_3 as a capping layer is inserted, then deposition of gate metal layer, for example TiN, is performed. The La has an effect of decreasing the eWF, and an effect of Al is increasing the eWF. These effects of capping are usually explained by the formation of the interface dipole [29, 30].

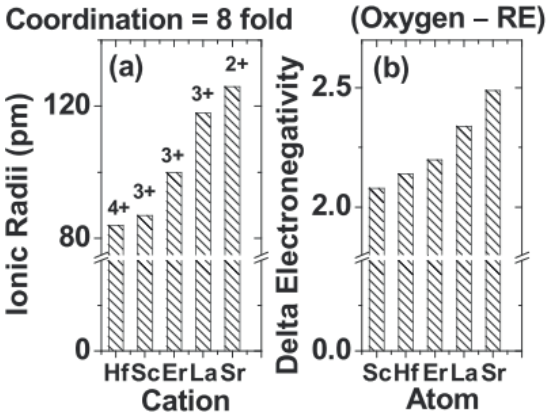

Fig. 2.11. (a) Dopant ionic radii and (b) ΔEN (O-RE) [29].

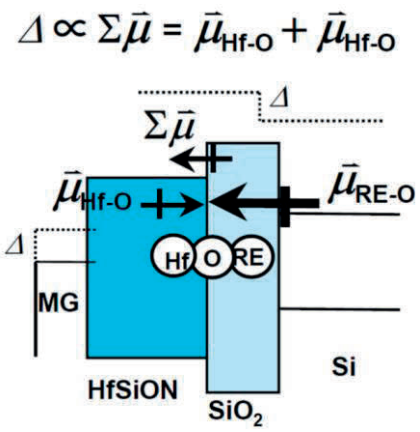

Fig. 2.12. Interface dipole moment model. Shift of eWF (Δ) proportional to net dipole moment including both Hf-O and RE-O dipole moments. [29].

In a model suggested by Sivasubramani *et al.* [29], about various kinds of rare earth elements applied as a capping for n-MOSFET (Sc, Er, La, Sr), the difference in the magnitude of V_{th} shift was explained by their dipole moment. As shown in Fig. 2.11 (b), in both of the Hf in high-k material and the atom of rare earth (RE) such as La which was introduced into the high-k insulator as capping, the electronegativity is lower than that of oxygen. Therefore they combine with oxygen, and a dipole is made at HfSiON/SiO_2 interface (its direction is from a metal atom to oxygen atom). Here, the Hf is located in the High-k side, and the RE, forming silicate, is located in the SiO_2 side. Therefore, the directions of dipoles are opposite each other, as shown in Fig. 2.12. The dipole moment is equal to the product of electric charge Q ($\Delta EN \propto Q$ in Fig. 2.11 (b)) and distance d (Ionic radii $\propto d$ in Fig. 2.11 (a)). The RE-O dipole moment ($\mu_{RE\text{-}O}$) is larger than the Hf-O dipole moment ($\mu_{Hf\text{-}O}$) because RE is less electronegative (larger q) and has larger cationic radius (larger d), as indicated in Fig. 2.11. Therefore, the dipole moment formed by RE-O such as La-O becomes dominant and changes the eWF. In addition, Sivasubramani *et al.* concluded that although the dipole moment with Sr is larger and the V_{th} shift by Sr capping is also larger than the case of La capping, La_2O_3 is the most desirable as capping for n-MOSFET with considering the deterioration of subthreshold swing or electron mobility etc.

Tatsumura *et al.* reported that the dipole formation mechanism is different by the kind of the capping material and also the influence on mobility is different [30]. Although the influence on mobility is small even if the quantity of La is increased, when quantity of Al is increased, remote Coulomb scattering (RCS) increases and mobility decreases. In their model, when quantity of capping is increased, distance d of the dipole increases in the case of La, but charge q increases in the case of Al.

Finally, I will summarize how to adjust the eWF in high-k gate insulator MOSFET with gate-first process. For shrinking the size of logic transistor, we have to realize n- and p-MOSFETs with

thin effective T_{ox} and symmetric V_{th}, with considering the influence of the abovementioned (1) FLP and (2) Capping. Therefore,

- There is no advantage in the poly-Si/High-k structure. An adjustment of the work function by impurity doping which is an advantage at the poly-Si gate does not function because of Fermi level pinning. Only the demerit that gate depletion occurs remains.
- Thus, a metal gate electrode is necessary, but eWF of the HfO_2/metal structure depends on the kind of the metal. One solution by which both n-/p-MOSFET become surface channel MOSFET with suitable V_{th} (for example $|V_{th}|< 0.4$ V) is "dual metal gate" structure which applies two kinds of metal which has appropriate work functions to n-/p-MOSFET, respectively [31].
- Another solution is "capping process". For example, one kind of metal is used and eWF is adjusted by adding proper capping layer. This is relatively easier process than “dual metal gate”, but the magnitude of V_{th} shift with capping process has a limit (smaller than ± several hundred mV).

In this study, "capping process" was adopted with considering ease of process to make experimental samples. TiN (its typical eWF was around 4.5 eV in our sample, which is near the Si mid-gap 4.61 eV [32]) was applied as common gate metal in n-/p-MOSFET, and eWF was adjusted by La_2O_3 in n-MOSFET, by Al_2O_3 in p-MOSFET [28].

In fact, however, more successful process is dual metal gate structure with the gate-last process [33]. Because the gate-last metal gate process is very different from a conventional poly-Si gate process, it is thought that generally the construction of the gate-last process is difficult. However, it is thought that the gate-last process is more advantageous because of the problem which appears in the gate-first process (for example characteristic instability depending on the transistor size [34, 35]). The details were explained in the section 1.1.3.

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3. Temperature dependence of V_{th} in metal gate transistors

3.1. Introduction

As explained in the section 1.1.4 "Temperature coefficient of V_{th}", the temperature coefficient of V_{th} is an important parameter for design of a semiconductor device, and the value generally becomes large by application of a metal gate structure. This is a change in which it becomes hard to design, and it is important to research a method for control of coefficient. For the purpose, it is necessary to clarify causes which affect the value of dV_{th}/dT of the metal gate.

In this chapter, temperature dependence of V_{th} in metal gate MOSFETs were analyzed with measurement of real MOSFET samples, and the factors which affected dV_{th}/dT in metal gate structure were investigated. MIPS structure was used as a metal gate sample [1-3]. The gate metal was TiN, and the capping material, which controls the work function of the gate electrode, was La_2O_3 or Al_2O_3. MOSFET samples were made with changing a specific process condition in this poly-Si/TiN/capping/high-k structure. Temperature coefficients of V_{th} and V_{FB} were measured with each sample, and the relations with the process condition were considered. The experiments were performed with three steps. The content and result of each step of the experiments was shown briefly.

Step (1) dV_{th}/dT in metal gate n-MOSFET (TiN or capping dependence)

[Experiment content] The MIPS type metal gate electrode consists of a stacked structure of poly-Si/TiN/capping. The factors which directly influence the value of V_{th} are regarded as properties of TiN layer and capping layer in this stack structure. In this "Step (1)", the influence on dV_{th}/dT caused by the difference in process conditions such as the thickness of TiN, La_2O_3, and Al_2O_3 was investigated with n-MOSFET sample.

[Experiment result] When TiN thickness becomes large, the temperature coefficient of V_{FB} (dV_{FB}/dT) changes, and $|dV_{th}/dT|$ becomes large. And, the increase in TiN thickness or Al_2O_3 thickness increases the *EOT*, which enlarges the influence on dV_{th}/dT from the temperature coefficient of depletion charge. As a result, $|dV_{th}/dT|$ becomes large [2].

Step (2) dV_{th}/dT in metal gate p-MOSFET (comparison of TiN dependence with n-MOSFET)

[Experiment content] The difference in influence on dV_{th}/dT of the TiN thickness was investigated with both samples of n-MOSFET and p-MOSFET.

[Experiment result] Although the dV_{FB}/dT changed according to the increase in TiN thickness also in p-MOSFET, it made the $|dV_{th}/dT|$ small contrary to the case of n-MOSFET (the quantity of change was same as that of n-MOSFET, but direction was opposite). On the other hand, the influence from the depletion charge made $|dV_{th}/dT|$ large as well as n-MOSFET. As a result, $|dV_{th}/dT|$ in n-MOSFET increases remarkably by the increase in TiN thickness, but $|dV_{th}/dT|$ in p-MOSFET does not so much depend on TiN thickness because the directions of two effects are opposite each other [3].

Step (3) Work function and its temperature coefficient in TiN metal gate

[Experiment content] Because the cause which changes dV_{FB}/dT depending on TiN thickness might be influence of the TiN/high-k interface, dV_{FB}/dT was compared with the sample which changed the gate insulator from HfON to SiON.

[Experiment result] The TiN thickness dependence of dV_{FB}/dT in SiON sample is not different from that in HfON sample. Therefore, the cause of the change of the temperature coefficient of V_{FB} is attributed to TiN itself, which is thought the change of the temperature coefficient of the work function of TiN [3].

In addition, some of fabrication process condition or measurement condition are different between the experiments of "Step(1)" and "Step(2),(3)". For example, (1) used HfSiON for high-k, but (2)(3) used HfON. However, these differences have no essential influence on the conclusions in the series of experiments.

Hereinafter, the detailed experiment method is indicated in the next section 3.2. After that, the results and interpretations are discussed in the section 3.3 for “Step (1)”, in the section 3.4 for “Step (2)”, and in the section 3.5 for “Step (3)”, respectively. Finally, the total consideration of this Chapter 3 is described in section 3.6.

3.2. Experimental method

3.2.1. The fundamental process flow for the sample fabrication

All the samples used in experiments in this chapter were the TiN metal gate transistors with MIPS structure, and they were fabricated with a "gate-first" process. The fundamental gate-first process flow, which was common for all samples, was shown in Fig. 3.1. If process conditions changed according to kinds of experiment, the conditions are anew explained in the later chapter in which the experiment is described. [2, 3]

Firstly, on a P-type silicon substrate (1), shallow trench isolation (STI) was formed for element isolation structure (2). P-well region was formed in the n-MOSFET area, and N-well region was formed in the p-MOSFET area (3). Next, Hf-based high-k dielectric layer was formed as a gate insulator (4). As described later, in the case that capping layers were applied for V_{th} control, capping layers were deposited after the formation of high-k layer. Then, TiN and poly-silicon were deposited (5)(6). TiN was deposited using one of two methods, chemical vapor deposition (CVD) or physical vapor deposition (PVD). The thickness of TiN (T_{TiN}) was from 4 to 15 nm, since using thicker TiN for gate electrode of MOSFET is difficult because of difficulty of gate etching. When samples which had thicker TiN were required, we had to use MOS capacitor samples, because their gate edges are on STI region and gate etching is easy. After patterning of gate electrodes (7), source/drain extension and halo implantations were performed (8), and side wall spacers were formed (9). The structure of side wall was SiO_2/Si_3N_4. After deep source/drain ion implantations (10), activation by spike rapid-thermal-anneal (RTA) was performed (11). Then, interlayer dielectric deposition and contact formation were performed (12). Metal interconnections were formed (13), and samples completed.

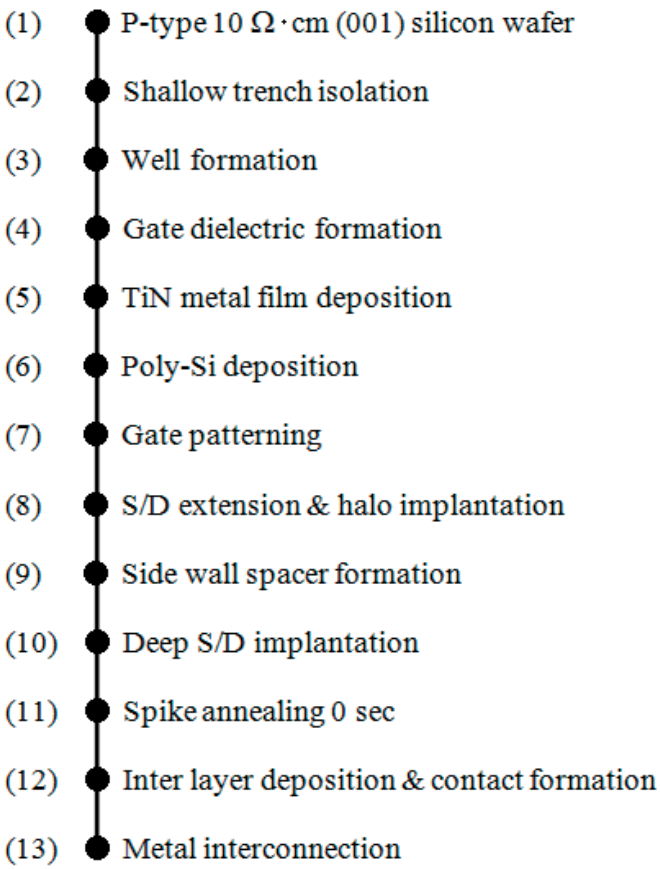

Fig. 3.1. Process flow for fabrication of samples in this study.

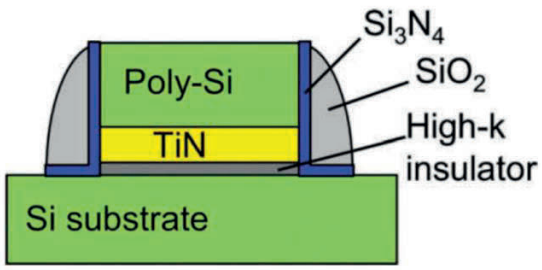

Fig. 3.2. Schematic diagram of the sample used in this study.

A schematic diagram of metal gate MOSFET fabricated using this process flow is shown in Fig. 3.2. In this thesis, we had a policy that comparison of the characteristics was performed only between the samples in which only capping conditions or TiN conditions were different each other. Process conditions other than capping layer and TiN layer were basically the same.

3.2.2. Measurement Method

(1) Sizes of samples

State-of-the-art high-k/metal gate MOSFETs technology usually uses short gate lengths and narrow gate widths which are much smaller than 1 μm. However, influences of short channel effects and narrow channel effects are inevitable in the high-k/metal gate MOSFETs with such small gates fabricated with gate-first process [4, 5]. Therefore, we researched fundamental temperature characteristics of poly-Si/TiN/high-k gate MOSFETs by using samples with large-sized gates. The concrete values of the sample sizes are mentioned later, since the values change by each experiment.

(2) Measurement of electric characteristics

Linear V_{th} was abstracted from the drain current-gate voltage (I_d-V_g) measurement data setting the absolute value of drain voltage ($|V_d|$) at 0.05 V.

V_{FB} was abstracted from the gate capacitance-gate voltage (C_g-V_g) characteristics. The C_g-V_g characteristics were also measured with the same transistors as former I_d-V_g characteristics. The equivalent gate oxide thickness (*EOT*) of a transistor was obtained with the method reported by Saito *et al*. [6]. V_{FB} was calculated according to the following method [7].

C_{min} (the minimum value in C_g-V_g curve of a MOSFET) and C_{FB} (C_g at the flat band voltage V_{FB}) are described as

$$C_{\min} = \frac{C_{OX}}{1+\dfrac{2\varepsilon_{OX}}{T_{OX}}\sqrt{\dfrac{\varepsilon_0\phi_f}{\varepsilon_{Si}qN_a}}} = \frac{\varepsilon_0\varepsilon_{OX}}{T_{OX}+2\varepsilon_{OX}\sqrt{\dfrac{\varepsilon_0\phi_f}{\varepsilon_{Si}qN_a}}} = \frac{\varepsilon_0\varepsilon_{OX}}{T_{OX}+2\varepsilon_{OX}\sqrt{\dfrac{\varepsilon_0 kT\ln\left(N_a/n_i\right)}{\varepsilon_{Si}q^2N_a}}} \tag{3.2.1}$$

$$C_{FB} = C_{OX}\left(1+\frac{\varepsilon_{OX}L_D}{T_{OX}\varepsilon_{Si}}\right)^{-1} = \left(\frac{T_{OX}}{\varepsilon_{OX}}+\frac{L_D}{\varepsilon_{Si}}\right)^{-1} \tag{3.2.2}$$

$$L_D = \sqrt{\frac{kT\varepsilon_{Si}\varepsilon_0}{q^2p_{p0}}} \cong \sqrt{\frac{kT\varepsilon_{Si}\varepsilon_0}{q^2N_a}} \tag{3.2.3}$$

Here, C_{ox} is the capacitance of gate oxide, ε_{Si} and ε_{ox} are relative permittivities of silicon and silicon oxide, respectively. T_{ox} is the thickness of gate oxide, which is replaced by *EOT* if gate insulator is a material other than silicon oxide. q is the elementary charge, k is the Boltzmann constant, N_a is the acceptor concentration of the silicon substrate, T is absolute temperature, p_{p0} is hole concentration ($\cong N_a$). L_D, which is defined in (3.2.3), is Debye length of hole. The value of C_{min} was determined by the measurement of C_g-V_g characteristics, and N_a was obtained. L_D was determined from (3.2.3), and C_{FB} was calculated. As a result, V_{FB} was obtained.

Electric characteristics of samples were measured at several temperature points. Actual examples of I_d-V_g characteristics and C_g-V_g characteristics are shown in Fig. 3.3 and Fig. 3.4. It was

confirmed that the V_{th} and V_{FB} changes with the temperature almost linearly in the range between -30°C and +80°C. The temperature coefficients of V_{th} and V_{FB} were obtained by calculation of a slope between two temperatures.

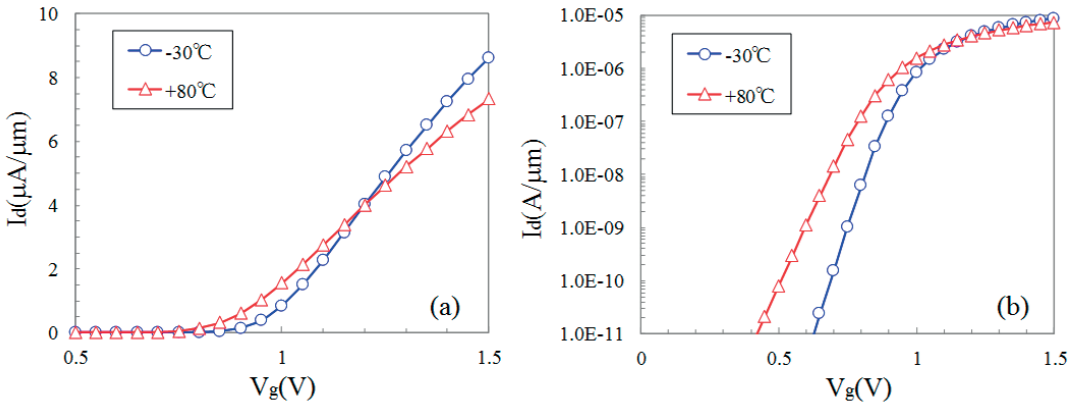

Fig. 3.3. I_d-V_g characteristics of a metal gate n-MOSFET with V_d=50 mV at −30°C and +80°C, (a) linear scale (b) logarithmic scale. Gate length=1 μm, Gate width=10 μm, TiN thickness=15 nm.

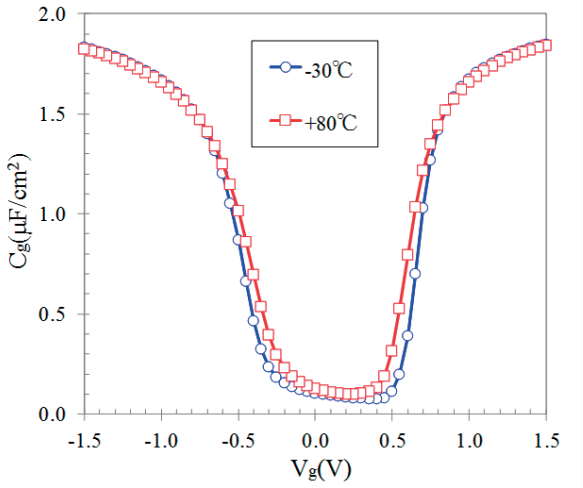

Fig. 3.4. C_g-V_g characteristics of a metal gate n-MOSFET with measurement frequency =100 kHz , at −30°C and +80°C.

3.3. dV_{th}/dT in metal gate n-MOSFET

Firstly, as the experiment of step (1) described in the section 3.1, the influence in dV_{th}/dT caused by changing of the several process conditions in metal gate n-MOSFET, such as TiN deposition method, TiN thickness (T_{TiN}), La_2O_3 capping thickness, and Al_2O_3 capping thickness, was investigated.

3.3.1 Condition of experiments

The process conditions of the devices used in this section and measurement conditions are summarized in Table 3.1.

In the process of n-MOSFET samples in this section, the well region was formed by boron implantation. The gate insulator consisted of several layers. The first layer was SiON as interlayer, and the second one was HfSiON by atomic layer deposition (ALD) as a high-k layer. The third one was capping layer for V_{th} control [2, 8-11]. La_2O_3 was used for lowering V_{th}, and Al_2O_3 was used for raising V_{th}. The thickness of capping layer was different among the samples. Next, TiN film for gate metal was deposited using one of two methods, chemical vapor deposition (CVD) or physical vapor deposition (PVD). The thicknesses of TiN were 4 nm or 15 nm. Phosphorus-doped poly-Si was deposited on TiN, and poly-Si/TiN gate electrode was patterned. A deep source / drain region for n-MOSFET was formed by As implantation, and activated by spike annealing (1050°C, 0 sec).

Table 3.1. The process conditions of the device samples and measurement conditions used in this section 3.3.

Process condition for sample fabrication

Number in Fig.3.1	process	condition
(3)	P-well	B implantation
(4)	Gate insulator	HfSiON (ALD) / SiON
	Capping for V_{th} control	La_2O_3 0.3-0.5nm
		Al_2O_3 0.1-0.7nm
(5)	TiN film	CVD or PVD 4, 15nm
(6)	poly-Si	Phosphorus-doped poly-Si 120nm
(10)	n^+ source/drain	As implantation
(11)	spike annealing	1050°C, 0 sec

Device sizes of measured samples

Gate length	1μm
Gate width	10μm

Temperature range for calculation of temperature coefficient

V_{th}	-30°C ~ +80°C
V_{FB}	-30°C ~ +80°C

The length of the gate electrode of n-MOSFET was 1 μm, and its width was 10 μm. Linear V_{th} with extrapolation method from I_d-V_g characteristics, and V_{FB} from C_g-V_g characteristics were extracted. Temperature coefficients of V_{th} and V_{FB} were calculated between −30°C and +80°C.

3.3.2 TiN condition dependence

Figure 3.5 indicates the *EOT* obtained by measuring the electrical characteristics of the fabricated n-MOSFETs. The relative shift of the *EOT* against the thinnest TiN is plotted in the figure, which shows that an increase in T_{TiN} resulted in an increase in *EOT* [12]. Although the increase in *EOT* was shown in both CVD-TiN and PVD-TiN, increase width was larger in CVD-TiN. The *EOT* increase possibly originated from oxygen contained in the TiN film.

Figure 3.6 shows the shift of effective work function (*eWF*) which was calculated with assuming that fixed oxide charge can be ignored. The *eWF* of 4-nm TiN was lower than that of 15-nm TiN [12, 13] in both CVD-TiN and PVD-TiN. The relation between T_{TiN} and *eWF* will be discussed in the section 3.5. The validity of ignoring fixed oxide charge is also shown there.

Figure 3.7 plots the dependence of dV_{th}/dT on T_{TiN}. Here, it should be noted that dV_{th}/dT is a negative value. And, if the magnitude of the V_{th} shift by temperature increases, the symbols are plotted on the lower part of the graph. Regardless of TiN deposition method, the thick TiN metal gate device had a large magnitude of $|dV_{th}/dT|$.

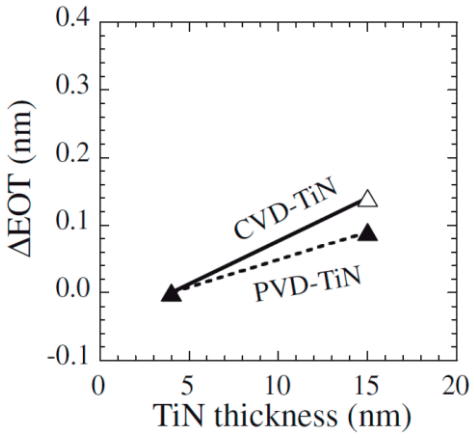

Fig. 3.5. Dependence of *EOT* on TiN thickness.

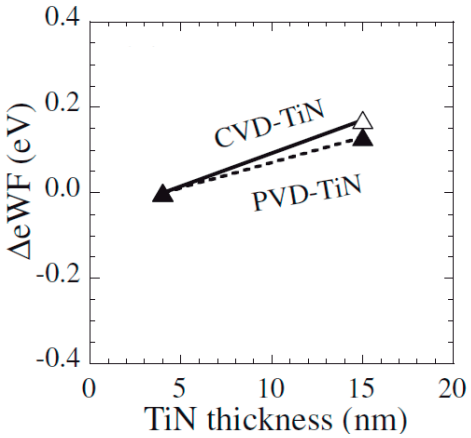

Fig. 3.6. Dependence of *eWF* on TiN thickness.

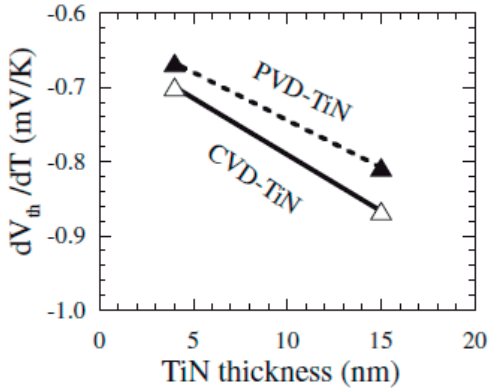

Fig. 3.7. Dependence of dV_{th}/dT on TiN thickness.

3.3.3 Capping condition dependence

Figure 3.8 plots the relation between the capping thickness and the *EOT*. The *EOT* changed with the Al_2O_3 thickness, as shown in Fig. 3.8. On the contrary, changes in La_2O_3 thickness resulted in only a very slight change in *EOT*. Although diffusion of La and Al increases the physical high-k insulator thickness, *EOT*, which is a function of film thickness and permittivity, does not always do so. In cases with La capping, an increase in permittivity is considered to compensate for changes in physical thickness.

The shift of *eWF* by capping layer is confirmed by Fig. 3.9. In this experiment, La_2O_3 capping was applied to the samples with 4-nm TiN and Al_2O_3 capping was applied to the samples with 15-nm TiN, for attaining larger range of *eWF*, respectively. As shown in the figure, 0.5-nm La_2O_3 lowers *eWF* by about 350 meV, and 0.7-nm Al_2O_3 raises *eWF* by about 200 meV.

Figure 3.10 plots the dependence of dV_{th}/dT on capping thickness. The magnitude of temperature coefficient increased with the Al_2O_3 thickness, and showed very little dependence on the La_2O_3 thickness.

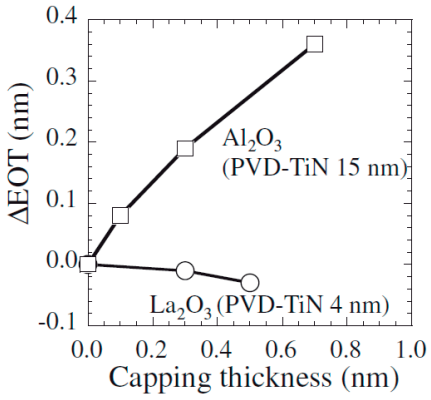

Fig. 3.8. Dependence of *EOT* on capping thickness.

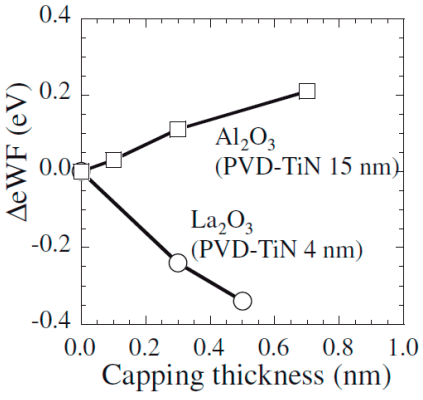

Fig. 3.9. Dependence of *eWF* on capping thickness.

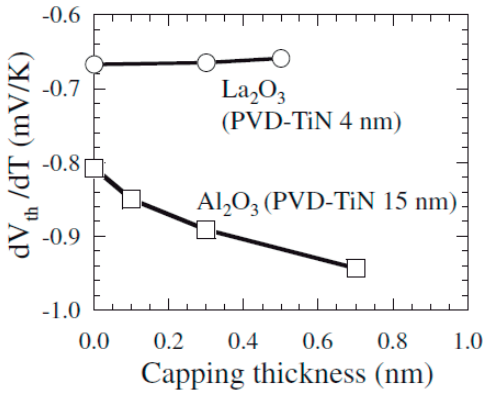

Fig. 3.10 Dependence of dV_{th}/dT on capping thickness.

3.3.4 Consideration of the interface state density

As explained in the section 2.1.2, if sufficient interface states exist, they influence on the V_{th} according to the 4th term in equation (2.1.21). Han *et al.* [14] estimated that the interface states density (D_{it}) of 10^{12} cm^{-2}•eV^{-1} increases $|dV_{th}/dT|$ by 0.03 mV/K for MOSFETs fabricated using 45-nm technology (our sample was also similar size node). As shown in Figs. 3.5 and 3.8, *EOT* increased when the TiN and capping thickness were increased. This implies the interface modification and D_{it} change because of diffusion of elements in the upper structures. Therefore, the influence of interface state density was evaluated. D_{it} was measured using the charge pumping method. As shown in Figs. 3.11 and 3.12, D_{it} did not exceed 10^{12} cm^{-2}•eV^{-1}. Considering the magnitude of the measured D_{it} and its influence estimated with the report of Han *et al.* [14], the 4th term of equation (2.1.21) and the influence of interface states can be ignored for our devices. Therefore, we can apply equation (2.1.17) without D_{it}.

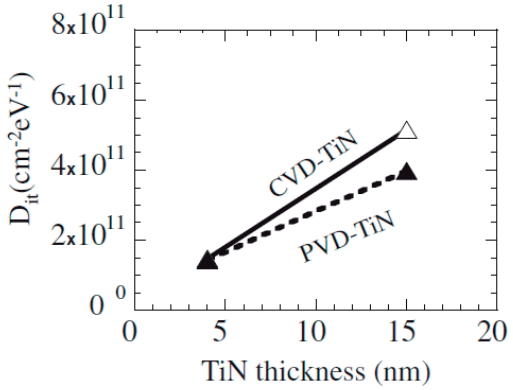

Fig. 3.11. Dependence of D_{it} on TiN thickness.

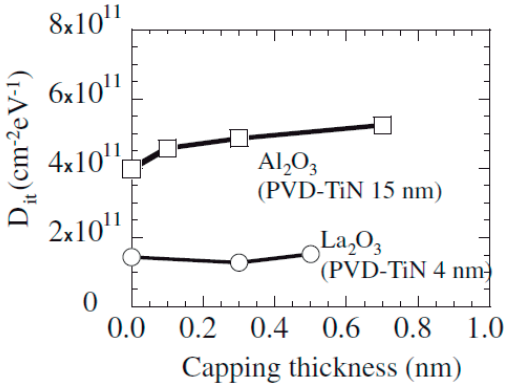

Fig. 3.12. Dependence of D_{it} on capping

3.3.5 Behavior of V_{FB} component

Here, analysis based on the theoretical equation (2.1.17) is considered. The dV_{th}/dT is obtained by differentiating both sides of equation (2.1.17)

$$\frac{dV_{th}}{dT} = \frac{dV_{FB}}{dT} + 2\frac{d\phi_f}{dT} + \frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4qN_a\varepsilon_{Si}\varepsilon_0\phi_f} \ . \qquad (3,3,1)$$

In this equation, it is considered which factors in the right hand are the causes of difference of the left hand (temperature coefficient of V_{th} among the nMOSFET samples). ϕ_f is described by equation (2.1.10), and it depends on T, N_a, and n_i. Because all samples have the same substrate doping concentration N_a, ϕ_f becomes the same value in all samples. Because q, ε_{Si}, and ε_0 are constants, also the value of depletion charge $\sqrt{4qN_a\varepsilon_{Si}\varepsilon_0\phi_f}$ is common to all samples. As a matter of course, also the values of $d\phi_f/dT$ and $d\sqrt{4qN_a\varepsilon_{Si}\varepsilon_0\phi_f}/dT$ become same in all samples. Therefore, the remaining candidates for the dominant factors are the 1st term dV_{FB}/dT, and the C_{ox} in the 3rd term in equation (3.3.1).

Then, dV_{FB}/dT was experimentally obtained to estimate the contribution of the 1st term. In Figs. 3.13 and 3.14, the relationships between dV_{FB}/dT and the TiN thickness or the capping thickness were plotted on the same scale as dV_{th}/dT shown in Figs. 3.7 and 3.10. Comparing Figs. 3.7, 3.10, 3.13, and 3.14, we can see that the reductions in dV_{FB}/dT and dV_{th}/dT caused by the increase in T_{TiN} are similar to each other. On the contrary, the change in dV_{FB}/dT caused by the influence of the capping layer, which is indicated in Fig. 3.14, seems to be relatively small compared with the T_{TiN} dependence in Fig. 3.13. This means that the change in T_{TiN} affected dV_{FB}/dT, the 1st term in equation (3.3.1), and it influenced the change in dV_{th}/dT. Assuming that the fixed oxide charge does not change with different temperatures, V_{FB} corresponds to the differences in work functions between the gate metal and the Si substrate. The interpretations of the T_{TiN} dependence of dV_{FB}/dT will be discussed in the section 3.5.

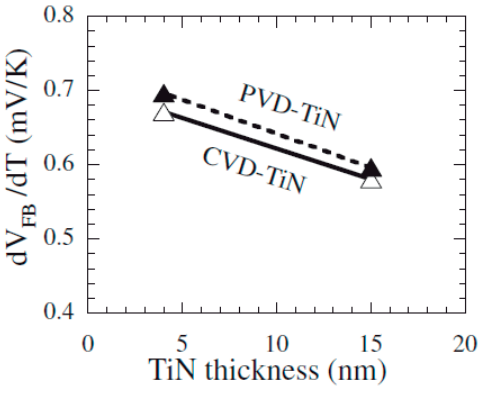

Fig. 3.13. Dependence of dV_{FB}/dT on TiN thickness.

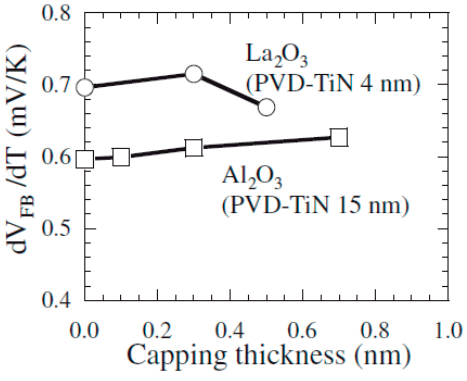

Fig. 3.14. Dependence of dV_{FB}/dT on capping thickness.

3.3.6 Contribution of the effect of depletion charge

Finally, the influence of the 3rd term (contains C_{ox}) in equation (3.3.1), which means the effect of temperature coefficient of depletion charge, is considered. But, since only V_{th} and V_{FB} can be measured directly, it is analyzed by calculation from the dV_{th}/dT and dV_{FB}/dT.

For this purpose, the 1st term dV_{FB}/dT is transposed to the left side of equation (3.3.1):

$$\frac{dV_{th}}{dT} - \frac{dV_{FB}}{dT} = \frac{d\phi_f}{dT} + \frac{1}{C_{ox}} \frac{d}{dT} \sqrt{4qN_a \varepsilon_{Si} \varepsilon_0 \phi_f} \tag{3.3.2}$$

$$= a + b \cdot (EOT) . \tag{3.3.3}$$

Here, a and b are constants that are common for all samples. Equation (3.3.2) corresponds to the case of an ideal MOS, which is an analytical MOS assuming V_{FB}=0. Equation (3.3.3) means that $dV_{th}/dT - dV_{FB}/dT$, which corresponds to the temperature coefficient of V_{th} in an ideal MOS, is proportional to EOT. To verify the validity of this equation, $dV_{th}/dT - dV_{FB}/dT$ was plotted against EOT, as shown in Fig. 3.15. This figure includes data from all of the samples in this section 3.3, and they are plotted with the same symbols used in the previous figures. As expected, linearity with EOT is clearly seen. This result means that one part of the temperature dependence of high-k/capping/metal gate MOSFET V_{th}, which is the component described as an ideal MOS, essentially obeys the traditional MOS theory. In our samples, one of the main causes of the change in dV_{th}/dT was attributable to the change in EOT induced by differences in the process conditions.

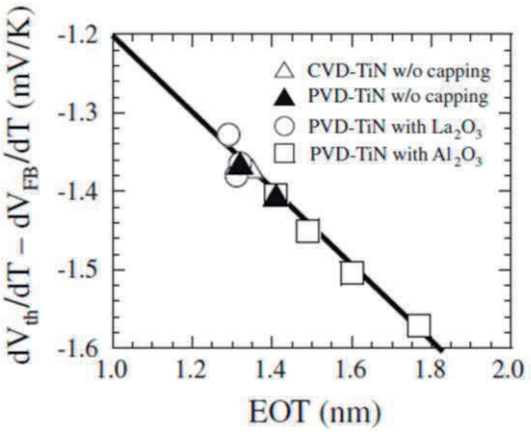

Fig. 3.15. Correlation between EOT and $dV_{th}/dT - dV_{FB}/dT$ for all samples in this section 3.3. As expected from the equation (3.3.2) and (3.3.3), $dV_{th}/dT - dV_{FB}/dT$ is determined by $1/C_{ox}$, and its absolute value decreases with the reduction in EOT.

3.3.7 Conclusion about dV_{th}/dT in metal gate n-MOSFET

The conclusion from the experimental result of step (1) described in the section 3.1 is indicated below:

The temperature dependence of V_{th} for high-k/TiN gate MOSFETs with capping was evaluated. The dV_{th}/dT was affected by the thickness of the TiN gate and the La_2O_3 or Al_2O_3 capping layer. However, by subtracting the temperature dependence of V_{FB} from that of V_{th}, the difference in the temperature coefficient of V_{th} was attributed to a change in *EOT* due to process condition differences, as shown in equation (3.3.3) and Fig. 3.15. This means that the ideal MOS model, which is a well-known analytical MOS assuming V_{FB}=0, is sufficient to explain the fundamental behavior of V_{th} of high-k/metal gate MOSFETs against temperature change.

The key characteristic of fabricated high-k/metal gate MOSFETs was that dV_{FB}/dT depended on T_{TiN} (Fig. 3.13) although dV_{FB}/dT was not affected by the capping layer thickness (Fig. 3.14). When T_{TiN} changes, *eWF* changes (therefore V_{FB} changes), and dV_{FB}/dT also changes. The origins of the T_{TiN} dependence of dV_{FB}/dT is discussed in the following section 3.5 with further experiments.

On the other hand, when the thickness of capping layer changes, although *eWF* changes (therefore V_{FB} also changes), dV_{FB}/dT does not change. It is thought that the change of *eWF* by capping is caused by the effect of the dipole formed by atoms introduced by capping process, as explained in the section 2.3.4. dV_{FB}/dT becomes the same value regardless of the kind of the capping element or the amount (including 0) of the capping. These experimental results indicate that the effect of the dipole is constant without depending on temperature.

Here, I will confirm the validity of the conclusion that "the effect of capping in dV_{FB}/dT does not have temperature dependence". As explained at section 2.3.4, the effect of capping in V_{FB} can be interpreted as the moment of dipole formed by the bond of the metal atom of the capping layer and the oxygen atom of the gate insulator [15]. And the dipole moment depends on the electronegativity and the cationic radius of metal element of capping material. For example, I will estimate the temperature dependence of the electronegativity and the ion radius of La. The electronegativity χ_{AR} defined by A. L. Allred and E. G. Rochow is described as

$$\chi_{AR} = 3590\frac{Z_{eff}}{r_{cov}^2} + 0.744. \tag{3.3.4}$$

Here, Z_{eff} is effective nuclear charge, and r_{cov} is covalent radius [16]. This equation is based on the hypothesis that the electronegativity is decided by the strength of the electric field at the atomic surface. Z_{eff} of La is about 9 [17], and r_{cov} is 207 pm [18]. Therefore, if *k* represents the relative ratio for the r_{cov}, the equation (3.3.4) becomes

$$\chi_{AR} = 0.744 + \frac{0.754}{k^2}. \tag{3.3.5}$$

As approximate calculation, temperature coefficients of both ion radius and covalent radius of La could be substituted by the linear expansion coefficient α_L, which is 4.03 x 10^{-6} K^{-1} in La [19]. As a result, the changes per 1K of the factors which influence the dipole moment which consists of La-O bond are expected as follows: the distance becomes $(1+\alpha_L)$ time and the electric charge becomes $0.744 + 0.754/(1+\alpha_L)^2$ times. Even though the temperature change reaches 100 K, the change of

the effect of dipole moment formed by capping material is less than 1%. This estimate approximately agrees with the experimental result that "the effect of capping in dV_{FB}/dT does not have temperature dependence".

To be exact, Iijima reported dV_{th}/dT of the metal gate transistors in [11], and showed that the existence of capping layers (La_2O_3 or Al_2O_3) does not influence the temperature coefficient. But, the capping thickness dependence was not confirmed in their report. Our experiment proved that even though the thickness of capping layer changes, the temperature coefficient is the same.

There is a possibility that the reason for the change of the dV_{th}/dT depending on T_{TiN} is because increase in T_{TiN} causes a strain in channel region by stress of TiN film. It is thought that a tensile strain toward channel direction is enhanced by the increase in T_{TiN}. But, in another experiment in which an evident strain was added with contact etch stop layer (CESL) in the channel region, a tendency that $|dV_{th}/dT|$ slightly decrease by tensile strain was observed in n-MOSFETs. This tendency does not correspond to the result of the case in which T_{TiN} increases ($|dV_{th}/dT|$ increases despite of tensile strain). Therefore, it is thought that the influence of the channel strain caused by the increase in T_{TiN} is negligible and not the cause of the increase in $|dV_{th}/dT|$.

3.4. dV_{th}/dT in metal gate p-MOSFET

Next, as the experiment of step (2) described in the section 3.1, the difference in the T_{TiN} dependence of dV_{th}/dT was investigated with metal gate transistor samples of n-MOSFET and p-MOSFET.

3.4.1 Condition of experiments

The process conditions of the devices and measurement conditions used in this section, which were for analysis of difference of characteristics between metal gate n-MOSFET and p-MOSFET, are summarized in Table 3.2. They were different from that in the previous section (Table 3.1), which were for analysis of difference of characteristics caused by TiN thickness or capping layer thickness dependence. Although there were some different points between the two experiments, the fundamental features of T_{TiN} dependences of V_{th} and dV_{th}/dT were almost the same as explained later. For the MOSFET samples in this section, the p-well region was formed by boron implantation and the n-well region was formed by phosphorus implantation. The gate high-k insulator was HfON by atomic layer deposition (ALD) without capping layer for V_{th} control. For a comparison, samples using SiON gate insulation in substitution for high-k were also fabricated. Next, TiN film for gate metal was deposited using physical vapor deposition (PVD). The thickness of TiN was different among the samples, which was 5 or 10 or 15 nm. Non-doped poly-Si was deposited on TiN, and poly-Si/TiN gate electrode was patterned. A deep source / drain region for n-MOSFET was formed by arsenic implantation, and that for p-MOSFET was boron implantation. After that, a spike annealing (1000°C, 0 sec) was performed for activation.

The length of the gate electrode of n-MOSFET was 1.8 μm, and its width was 2.7 μm. Linear V_{th} and V_{FB} were measured, and their temperature coefficients were calculated between −30°C and +25°C.

Table 3.2. The process conditions of the device samples and measurement conditions used in this section 3.4.

Process condition for sample fabrication

Number in Fig.3.1	process	condition
(3)	P-well	B implantation
	N-well	P implantation
(4)	Gate insulator	HfON (ALD)
	Capping for V_{th} control	Not used
(5)	TiN film	PVD 5, 10, 15nm
(6)	poly-Si	Non-doped poly-Si 50nm
(10)	p^+ source/drain	B implantation
	n^+ source/drain	As implantation
(11)	spike annealing	1000°C, 0 sec

Device sizes of measured samples

Gate length	1.8μm
Gate width	2.7μm

Temperature range for calculation of temperature coefficient

V_{th}	-30°C ~ +25°C
V_{FB}	-30°C ~ +25°C

3.4.2 Difference between n- and p-MOSFET in the TiN thickness dependence

First, T_{TiN} dependence of V_{FB} was confirmed [12, 13]. Figure 3.16 indicates shift of V_{FB} depending on T_{TiN} in n-MOSFET, and Fig. 3.17 indicates that in p-MOSFET. The value of V_{FB} is negative in n-MOSFET, and positive in p-MOSFET. When TiN becomes thick, V_{FB} shifts toward the positive direction with approximately the same quantity in both n-MOSFET and p-MOSFET.

Then, temperature coefficient of V_{th} (dV_{th}/dT) was measured, and the T_{TiN} dependence of dV_{th}/dT for n-MOSFET was indicated in Fig. 3.18 and that for p-MOSFET was indicated in Fig. 3.19. The value of dV_{th}/dT is negative in n-MOSFET, and positive in p-MOSFET. The T_{TiN} dependence of dV_{th}/dT is quite different between n-MOSFET and p-MOSFET. In n-MOSFET, dV_{th}/dT shifts to the negative direction by about 130 mV/K when T_{TiN} shifts from 5 nm to 15 nm. In contrast, the shift in p-MOSFET is only tens of millivolts. As a result, when T_{TiN} becomes large, the absolute value of dV_{th}/dT becomes large in n-MOSFET, and hardly changes in p-MOSFET.

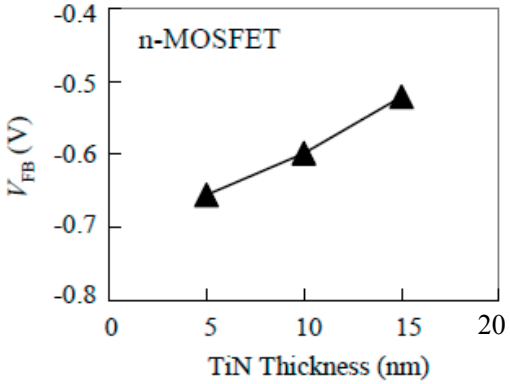

Fig. 3.16. Dependence of V_{FB} on the TiN thickness in n-MOSFETs.

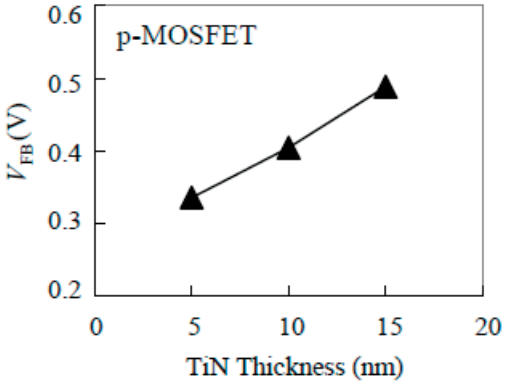

Fig. 3.17. Dependence of V_{FB} on the TiN thickness in p-MOSFETs.

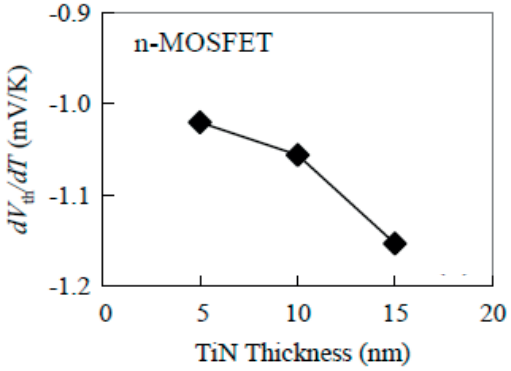

Fig. 3.18. Dependence of dV_{th}/dT on the TiN thickness in n-MOSFETs.

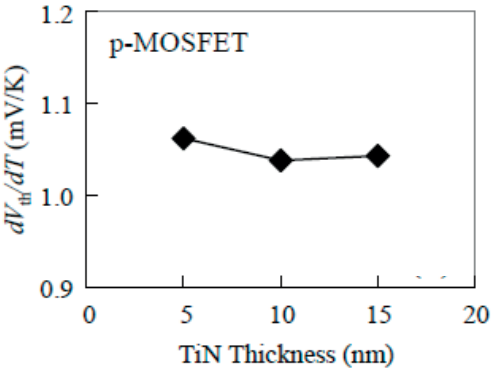

Fig. 3.19. Dependence of dV_{th}/dT on the TiN thickness in p-MOSFETs.

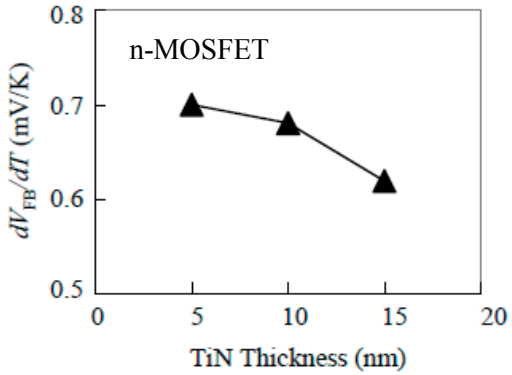

Fig. 3.20. Dependence of dV_{FB}/dT on the TiN thickness in n-MOSFETs.

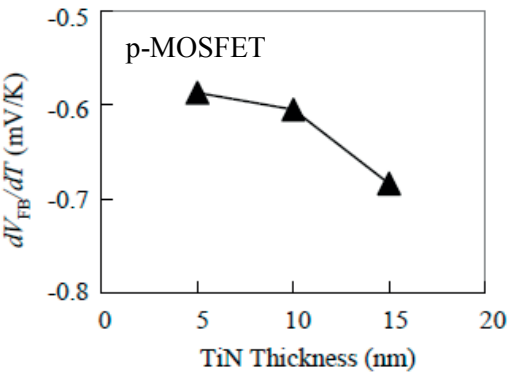

Fig. 3.21. Dependence of dV_{FB}/dT on the TiN thickness in p-MOSFETs.

Figures 3.20 and 3.21 indicate the relationships between dV_{FB}/dT and T_{TiN} for n-MOSFET and p-MOSFET, respectively. The value of dV_{FB}/dT is positive in n-MOSFET, and negative in p-MOSFET. But, these figures indicate that when TiN becomes thick, the behavior of dV_{FB}/dT is similar between n-MOSFET and p-MOSFET. The direction of shift is toward the negative direction, and the quantity of shift is approximately the same in both n-MOSFET and p-MOSFET. As a result, the absolute value of dV_{FB}/dT becomes small in n-MOSFET and becomes large in p-MOSFET when T_{TiN} becomes large.

3.4.3 Analysis of the experimental results

The behaviors of $|dV_{th}/dT|$ in TiN metal gate transistors are analyzed based on a theoretical equation. The theoretical equations (2.1.17) and (3.3.1) described in the previous sections express V_{th} and dV_{th}/dT in n-MOSFET, respectively. If these equations are modified for p-MOSFET, V_{th} and dV_{th}/dT are expressed as

$$V_{th} = V_{FB} \pm 2|\phi_f| \pm \frac{\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a|\phi_f|}}{C_{ox}}$$

$$\frac{dV_{th}}{dT} = \frac{dV_{FB}}{dT} \pm 2\frac{d|\phi_f|}{dT} \pm \frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a|\phi_f|}\,. \tag{3.4.1}$$

The upsides of the double signs (±) are chosen for n-MOSFET, and the downsides of those are for p-MOSFET [20].

As described in equation (3.4.1), dV_{th}/dT is influenced directly by dV_{FB}/dT. When T_{TiN} increases, the value of dV_{FB}/dT shifts to the negative direction both in Figs. 3.20 and 3.21. This direction means an increase in $|dV_{th}/dT|$ of n-MOSFETs and a decrease in $|dV_{th}/dT|$ of p-MOSFETs because dV_{th}/dT is negative in n-MOSFETs and positive in p-MOSFETs. In addition, an influence of the 3rd term in equation (3.4.1), which represents the temperature coefficient of the depletion charge in silicon substrate, is added. When T_{TiN} increases, the absolute value of the 3rd term in equation (3.4.1) becomes large due to a decrease in C_{ox}, which is caused by an increase in *EOT* [2, 12]. The sign of the 3rd term is negative in n-MOSFETs and positive in p-MOSFETs. Therefore, when T_{TiN} increases, both the 1st and 3rd terms in equation (3.4.1) shift to the negative direction in n-MOSFETs. On the contrary, the 3rd term shifts to the positive direction and the 1st term shifts towards the negative direction in p-MOSFETs. As a result, the amount of the decrease in $|dV_{th}/dT|$ in p-MOSFETs becomes smaller than that of the increase in $|dV_{th}/dT|$ in n-MOSFETs, as shown in Figs. 3.18 and 3.19.

The results of analysis of behaviors of $|dV_{th}/dT|$ in TiN metal gate transistors are summarized in Table 3.3. The change in the 3rd term, which means the change in the effect from depletion charge, is influenced by *EOT* of TiN metal gate transistors. This component essentially obeys the traditional MOS theory, as explained in the section 3.3. The change in the 1st term, which means the change of dV_{FB}/dT, is almost the same between n- and p-MOSFET. This is because dV_{FB}/dT is thought to be related to the temperature dependence of the work function of TiN. The detailed consideration about the origins of dV_{FB}/dT will be discussed in the next section 3.5.

I added, as a reference, schematic diagrams of the C_g-V_g curves in Fig.3.22, in which the quantities V_{FB}, $\pm\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a|\phi_f|}/C_{ox}$, and V_{th} are schematically shown by red, green, and blue arrows, respectively. Each of the temperature differential of them means "1st term", "3rd term", and "total value" in Table 3.3.

Table 3.3. Summary of analysis of the 1st and 3rd terms in equation (3.4.1), which influence on dV_{th}/dT when TiN thickness is changed. The sign (positive or negative) and the direction of change when the thickness of TiN becomes thicker (↓ means a shift toward negative direction, and ↑ means positive direction) are listed. For the 3rd term of p-MOSFET, the effect of "minus" before the term is also included.

		n-MOSFET		p-MOSFET	
	content	positive or negative	change in thicker TiN	positive or negative	change in thicker TiN
1st term	$\frac{dV_{FB}}{dT}$	positive	↓	negative	↓
3rd term	$\pm\frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a\lvert\phi_f\rvert}$	negative	↓	positive	↑
total value	$\frac{dV_{th}}{dT}$	negative	↓↓	positive	small ↓
absolute total value	$\left\lvert\frac{dV_{th}}{dT}\right\rvert$	-	↑↑	-	small ↓

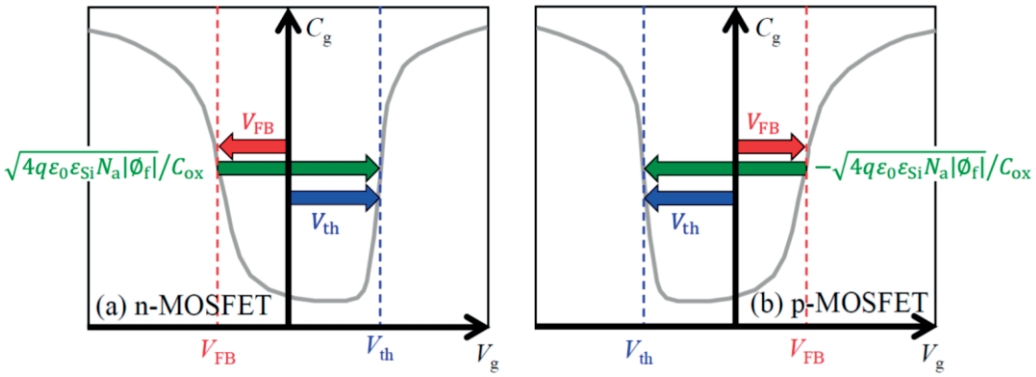

Fig. 3.22. Schematic diagrams of C_g-V_g curves of (a) n-MOSFET and (b) p-MOSFET for illustrating each item in Table 3.3. The red, green, and blue arrows indicate the quantities V_{FB}, $\pm\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a|\phi_f|}/C_{ox}$, and V_{th}, respectively. All arrows (red, green, and blue ones in both n-/p-MOSFET) reduce their own length at a high temperature. The temperature differential (rate of the reduction width) of red, green, and blue arrows indicates "1st term", "3rd term", and "total value" in Table 3.3. When T_{TiN} becomes large, the reduction width of the red arrow in n-MOSFET decreases. On the other hand, the reduction width of the red arrow of p-MOSFET increases. In both n- and p-MOSFET, the reduction widths of the green arrows increase when T_{TiN} becomes large. Therefore, when T_{TiN} increases, the reduction width of the blue arrow increases in n-MOSFET, and scarcely changes in p-MOSFET.

3.5. Work function and its temperature coefficient in TiN metal gate

Finally, as the experiment of step (3) described in the section 3.1, dV_{FB}/dT was compared between samples which have different kind of gate insulation and the cause which affect the T_{TiN} dependence of dV_{FB}/dT was considered. As a result, I attained a conclusion that the change of V_{FB} and the change of dV_{FB}/dT were caused by a change of Φ_{TiN} (work function of TiN) and $d\Phi_{TiN}/dT$. I will explain below the details of the discussion.

3.5.1 Condition of experiments

The process conditions of the devices and measurement conditions used in this section are basically the same as the previous section "3.4. dV_{th}/dT in metal gate p-MOSFET". But, samples with SiON gate insulator instead of HfON gate insulator were added for comparison.

3.5.2 Relation between flat band voltage and work function of TiN

As explained in further detail below, the mechanism of the shifts of V_{FB} and dV_{FB}/dT depending on T_{TiN} is attributed to the shift of Φ_{TiN} and $d\Phi_{TiN}/dT$. With modifying the equation (2.1.12) and (2,1,13), the relation between the actually measured flat-band voltage and work function in n-MOSFETs (p-type substrate) is expressed as

$$V_{FB} = \Phi_{TiN} - \Phi_{Si} - \frac{Q_{ox}}{C_{ox}} + S_{FLP} \,. \tag{3.5.1}$$

Here, Φ_{TiN} and Φ_{Si} are the original (not "effective" described in section 2.3.4) work functions of TiN and Si substrates, respectively, Q_{ox} is the equivalent oxide charge per unit area, and C_{ox} is the oxide capacitance [21]. S_{FLP}, which is a newly added term to the equation (2.1.12), represents an effect of Fermi Level Pinning (FLP) at the interface between TiN and the gate insulator [22, 23]. The distribution of the electric charge at the surface of metal is changed by whether or not the surface is in contact with other material [24]. Therefore, the effect of surface dipole, which is described in the section 2.3.1, will change and the effective value of V_{FB} will also change. Although this is a phenomenon which occurs at the interface not only between a metal and a high-k material but also between any other materials, the term of S_{FLP} actually includes also the effect of such phenomenon.

Because only T_{TiN} is changed in the samples in this study, Φ_{Si} is the same value in all samples. In order to check the influence of Q_{ox} or S_{FLP}, we measured the T_{TiN} dependence of V_{FB} in samples with SiON gate insulators for comparison to high-k gate insulators. As a result, the V_{FB} of high-k/TiN was higher than that of SiON/TiN in n-MOSFETs by approximately 0.12 V. The difference in V_{FB} between high-k/TiN and SiON/TiN is thought to be the difference in S_{FLP}. It means the difference of the amount of Ti-Si bonds at the TiN/gate-insulator interface [23] or the difference of the amount of extrinsic states generated at the interface [22]. However, the shifts of V_{FB} (ΔV_{FB}) caused by the increase by 10 nm or 11 nm in T_{TiN} were mostly in agreement among HfON, HfSiON and SiON, as shown in Fig. 3.23. The behaviors of ΔV_{FB} are almost the same regardless of n-/p-MOSFETs and HfON/HfSiON/SiON insulators, although the values of V_{FB} are different among samples.

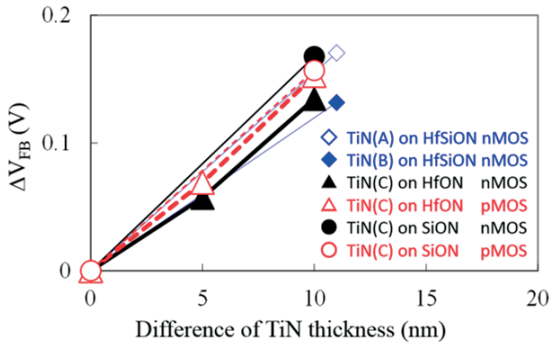

Fig. 3.23. Dependence of ΔV_{FB} on the increase in TiN thickness comparing six samples. There are three kind of gate insulator, HfON, HfSiON and SiON. The samples with HfON and SiON have both n- and p-MOSFETs. The data of HfSiON sample are the result of the previous measurement illustrated in the Fig. 3.6. TiN(A) on HfSiON was formed with CVD, and TiN(B) on HfSiON was formed with PVD process. Although TiN(C) on HfON or SiON was also formed with PVD, the process conditions were different from those of TiN(B). The real minimum thickness of TiN(A) and (B) was 4 nm, and that of TiN(C) was 5 nm.

Garros *et al*. [25] reported that nitrogen incorporated into the gate insulator from the TiN film increases when T_{TiN} increases. There is a possibility that Q_{ox} and S_{FLP} are influenced depending on the increase in nitrogen. However, in our experiments, the SiON sample and the high-k sample showed almost the same ΔV_{FB}, even though the C_{ox} of the HfON sample was more than 1.7 times larger than that of the SiON sample. Therefore, it is thought that the influence of the change in Q_{ox} in equation (3.5.1) is sufficiently small and negligible in our sample. In addition, even though the SiON insulator is a completely different material than the HfON and S_{FLP} is different between them [22, 23], there is almost no difference in ΔV_{FB} in Fig. 3.23. Therefore, the conclusion that the change in S_{FLP} in equation (3.5.1) is also sufficiently small and negligible in the case of the increase in T_{TiN} is thought to be reasonable. If it is assumed that Q_{ox}/C_{ox} and S_{FLP} scarcely change (they are practically constants) in equation (3.5.1) during the change in T_{TiN}, the shift of V_{FB} is essentially determined by only the shift of Φ_{TiN} ($\Delta\Phi_{TiN}$), i.e.,

$$\Delta V_{FB} = \Delta\Phi_{TiN} . \tag{3.5.2}$$

Consequently, Fig. 3.16 indicates that Φ_{TiN} increases by approximately 130 mV when T_{TiN} increases from 5 nm to 15 nm.

3.5.3 Estimate of temperature coefficient of work function of TiN

Next, $d\Phi_{TiN}/dT$ is discussed. If Q_{ox} does not have temperature dependence [26], the temperature differentiation of equation (3.5.1) is given by

$$\frac{dV_{FB}}{dT} = \frac{d\Phi_{TiN}}{dT} - \frac{d\Phi_{Si}}{dT} = \frac{d\Phi_{TiN}}{dT} - \frac{d}{dT}\left(\chi_{Si} + \frac{E_g}{2q} + |\phi_f|\right), \tag{3.5.3}$$

Here, χ_{Si} is the electron affinity of silicon, E_g is the energy gap of Si (see Fig. 2.2) [27]. ϕ_f was defined by the equation (2.1.10) which means the potential difference between the Fermi level at the

silicon substrate and the Fermi level of an intrinsic semiconductor silicon. The reason why dS_{FLP}/dT is omitted in equation (3.5.3) will be explained later.
Here, n_i (intrinsic carrier density) is expressed as

$$n_i^2 = N_c N_v \exp\left(\frac{-E_g}{kT}\right) \propto T^3 \exp\left(\frac{-E_g}{kT}\right), \tag{3.5.4}$$

where k is the Boltzmann's constant, N_c is an effective density of states in the conduction band, and N_v is that in the valence band (both of N_c and N_d are proportional to $T^{3/2}$)[26, 28, 29]. Therefore, ϕ_f in equation (2.1.10) also has a temperature dependence. Then, the value of $d|\phi_f|/dT$ calculated with equation (2.1.10) for the substrate concentration in our samples is –0.69 mV/K. The temperature dependences of χ_{Si} and E_g were measured by Beye *et al.* [30]. Temperature coefficients are presented in their report, with that of χ_{Si} being +0.16 mV/K and that of $E_g/2q$ being –0.23 mV/K. Because these values are common in all samples, they are substituted in equation (3.5.3). As a result, $d\Phi_{TiN}/dT$ becomes lower than the dV_{FB}/dT shown in Fig. 3.20 by 0.76 mV/K (= – 0.16 + 0.23 + 0.69 mV/K). The changes in $d\Phi_{TiN}/dT$ in n-MOSFETs and p-MOSFETs for high-k and SiON are thus calculated from dV_{FB}/dT and are shown in Fig. 3.24.

We can characterize the features of $d\Phi_{TiN}/dT$ as follows. First, $d\Phi_{TiN}/dT$ has a negative value, roughly –0.05 to –0.20 mV/K. Our experimental values of $d\Phi_{TiN}/dT$ in Fig. 3.24 are thought to be valid because published data indicate the same order of magnitude. As mentioned in the section 2.3.3 "Temperature dependence of work function", for example, –0.134 mV/K for Ag, –0.26 mV/K for K and –0.51 mV/K for Na [31]. Second, $d\Phi_{TiN}/dT$ shifts to the negative direction, and $|d\Phi_{TiN}/dT|$ becomes larger by approximately 0.1 mV/K when T_{TiN} increases from 5 nm to 15 nm for each of the 4 lines in Fig. 3.24. The reason for the change of $d\Phi_{TiN}/dT$ with the change in T_{TiN} is discussed in next Chapter 4.

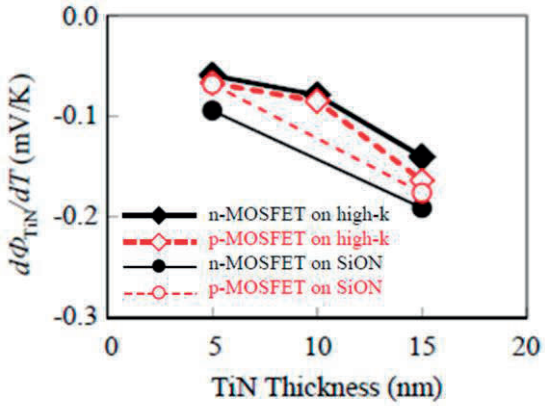

Fig. 3.24. Dependence of $d\Phi_{TiN}/dT$ on the TiN thickness in n-/p-MOSFETs with high-k/SiON gate insulator. The behaviors of $d\Phi_{TiN}/dT$ are almost the same regardless of n-/p-MOSFETs or TiN being on high-k/TiN or on SiON. $d\Phi_{TiN}/dT$ has a negative value. $d\Phi_{TiN}/dT$ shifts to the negative direction, and $|d\Phi_{TiN}/dT|$ becomes larger when the thickness of TiN increases.

The case of $d\Phi_{TiN}/dT$ in p-MOSFETs is also explained. In p-MOSFETs, the relation between $d\Phi_{TiN}/dT$ and dV_{FB}/dT is

$$\frac{dV_{FB}}{dT} = \frac{d\Phi_{TiN}}{dT} - \frac{d}{dT}\left(\chi_{Si} + \frac{E_g}{2q} - |\phi_f| \right), \tag{3.5.5}$$

and ϕ_f for p-MOSFET is given by

$$\phi_f = \frac{kT}{q} \ln\left(\frac{N_d}{n_i} \right). \tag{3.5.6}$$

Here, ϕ_f is the difference between the Fermi level and the intrinsic Fermi level, and N_d is the donor impurity concentration for a substrate. The value of $d|\phi_f|/dT$ at the donor concentration in our sample was calculated and found to be –0.59 mV/K. The other parameters in equation (3.5.5) have the same values as equation (3.5.3) for n-MOSFETs. As a result of the calculation via equation (3.5.5), $d\Phi_{TiN}/dT$ in p-MOSFETs becomes larger than the dV_{FB}/dT shown in Fig. 3.21 by 0.52 mV/K (= + 0.16 – 0.23 + 0.59 mV/K). The change in $d\Phi_{TiN}/dT$ in p-MOSFETs has already been plotted in Fig. 3.24. It is clear that the $d\Phi_{TiN}/dT$ obtained from n-MOSFETs and the $d\Phi_{TiN}/dT$ obtained from p-MOSFETs are almost the same. This indicates that the shifts of dV_{FB}/dT with increasing T_{TiN} in both n-MOSFETs and p-MOSFETs are caused by a single phenomenon, which is the change in $d\Phi_{TiN}/dT$ with increasing T_{TiN}. Furthermore, we also measured the metal gate n- and p-MOSFETs with the poly-Si/TiN/SiON (without high-k material) structure and calculated the values of $d\Phi_{TiN}/dT$ in the same manner. The results are also included in Fig. 3.24. If the dielectric constant of the high-k insulator changes or the interaction effect at the interface of TiN/high-k, such as FLP [22, 32], changes depending on temperature, the values of $d\Phi_{TiN}/dT$ on the high-k insulator become different from the values of $d\Phi_{TiN}/dT$ on SiON. However, it was confirmed that all samples have almost the same $d\Phi_{TiN}/dT$, regardless of whether TiN is on high-k or on SiON. These results suggest that the shifts of $d\Phi_{TiN}/dT$ depending on T_{TiN} are attributed to not a characteristic change in the high-k insulator or the TiN/high-k interface but a characteristic change in TiN itself. This is the reason why dS_{FLP}/dT is omitted in equation (3.5.3).

As reference, the relative shift of the $d\Phi_{TiN}/dT$ caused by the change of T_{TiN} is confirmed comparing various samples (comparisons of n-/p-MOSFETs or HfON/HfSiON/SiON insulators like Fig. 3.23). The result is shown in Fig. 3.25. The dispersion in vertical axis (absolute value of $d\Phi_{TiN}/dT$) in Fig. 3.24 is eliminated because constant errors, for example errors in the calculation of $d|\phi_f|/dT$, are ignored. It is confirmed clearly from Fig. 3.25 that when T_{TiN} increases by approximately 10 nm, the shift of $d\Phi_{TiN}/dT$ becomes almost the same quantity (about 0.1 mV/K) in all samples, even if the kinds of the insulator are different.

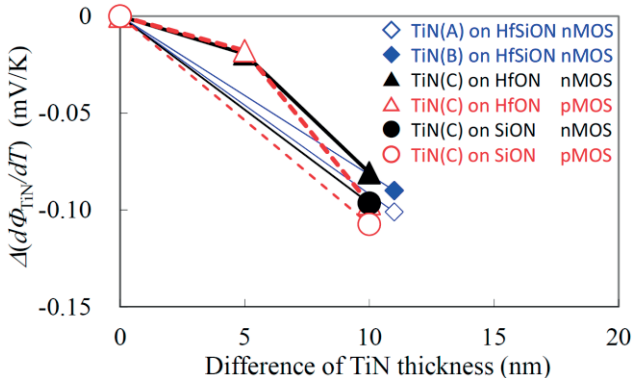

Fig. 3.25. Dependence of $\Delta(d\Phi_{TiN}/dT)$ on the increase in TiN thickness comparing six samples. The sample conditions and their symbols are the same as those of Fig. 3.23. There are three kind of gate insulator, HfON, HfSiON and SiON. The samples with HfON and SiON have both n- and p-MOSFETs.

3.6. Total consideration

3.6.1 Experimental results and considerations in Chapter 3

In this chapter, experiments were conducted to reveal temperature dependence of V_{th} in metal gate MOSFETs by three steps. The results in each step are as follows.

Step (1) dV_{th}/dT in metal gate n-MOSFET (TiN or capping dependence)

- The dV_{th}/dT is affected by the thickness of the TiN and the capping layer in gate electrode.
- There are two components in the mechanism which changes dV_{th}/dT. One is a change in the temperature coefficient of V_{FB} (dV_{FB}/dT). Another is a change in the temperature coefficient of the depletion charge.
- The dV_{FB}/dT is depended on TiN thickness (T_{TiN}). The condition of capping layer does not affect the dV_{FB}/dT.
- The *EOT* increases when the thickness of TiN or Al_2O_3 capping layer increases. The effect of temperature coefficient of the depletion charge is thought to be enlarged by the increase in *EOT*.

Step (2) dV_{th}/dT in metal gate p-MOSFET (comparison of TiN dependence with n-MOSFET)

- When the TiN layer becomes thick, $|dV_{th}/dT|$ of n-MOSFET becomes large, while $|dV_{th}/dT|$ of p-MOSFET is almost stable.
- When the TiN layer becomes thick, the dV_{FB}/dT of both n- and p-MOSFETs shifts to the negative direction, which causes an increase in the $|dV_{th}/dT|$ of an n-MOSFET and a decrease in the $|dV_{th}/dT|$ of a p-MOSFET.

・When the TiN layer becomes thick, *EOT* also becomes thick. As a result, the influence of the temperature coefficient of the depletion charge additively affects (a shift toward negative direction) the dV_{FB}/dT of an n-MOSFET, while it oppositely affects (a shift toward positive direction) the dV_{FB}/dT of a p-MOSFET.

Step (3) Work function and its temperature coefficient in TiN metal gate

・The shifts of V_{FB} and dV_{FB}/dT depending on the T_{TiN} in a TiN metal gate MOSFET are almost the same, regardless of the kind of the gate insulator (HfON or HfSiON or SiON) or the type of the MOSFET (n- or p-MOSFET).

・The cause of the shifts of V_{FB} and dV_{FB}/dT is attributed to the shift of work function of TiN (Φ_{TiN}) and shift of its temperature coefficient ($d\Phi_{TiN}/dT$) depending on the T_{TiN}.

・The value of $d\Phi_{TiN}/dT$ is about –0.05 to –0.20 mV/K. When the T_{TiN} increases from 5 nm to 15 nm, $d\Phi_{TiN}/dT$ shifts to the negative direction, and $|d\Phi_{TiN}/dT|$ becomes larger by approximately 0.1 mV/K.

From the above mentioned results, changes in the temperature coefficient of V_{th} in High-k/TiN/poly-Si metal gate transistors were analyzed into the ingredients indicated at Table 3.4, which is based on the equation (3.4.1) shown again below.

$$\frac{dV_{th}}{dT} = \frac{dV_{FB}}{dT} \pm 2\frac{d|\phi_f|}{dT} \pm \frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a|\phi_f|}\,. \tag{3.4.1}$$

According to Table 3.4, I will explain once again sequentially.

[The 1st row: $d\Phi_{TiN}/dT$] By changing T_{TiN}, both Φ_{TiN} and $d\Phi_{TiN}/dT$ change. $d\Phi_{TiN}/dT$ is a negative value. When TiN becomes thicker, $d\Phi_{TiN}/dT$ shifts to the negative direction (the absolute value becomes larger).

[The 2nd row: dV_{FB}/dT] The value of the dV_{FB}/dT, is positive in n-MOSFET, and negative in p-MOSFET. In both n-MOSFET and p-MOSFET, however, when T_{TiN} becomes large, the shifts of dV_{FB}/dT are almost the same (the same negative direction and almost the same quantity). This "negative direction" means an increase in $|dV_{th}/dT|$ in n-MOSFET, and a decrease in $|dV_{th}/dT|$ in p-MOSFET. On the other hand, the condition of capping layer such as La_2O_3 or Al_2O_3 does not affect the dV_{FB}/dT.

[The 3rd row: *EOT*] *EOT* is enlarged by thick TiN or thick Al_2O_3 capping. On the other hand, a clear increase is not seen even though La_2O_3 capping becomes thick.

[The 4th row: $\pm\frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a|\phi_f|}$] This term means the temperature coefficient of the potential difference generated by the gate oxide electric field that the depletion charge in silicon substrate makes. The magnitude of this term is proportional to the product of the temperature coefficient of the depletion charge (for which all samples have the same value) and *EOT*. When T_{TiN} increases, this term shifts toward the negative direction in n-MOSFET and positive direction in p-MOSFET. Each direction means the increase in $|dV_{th}/dT|$ in both n-MOSFET and p-MOSFET.

[The 5th row: dV_{th}/dT] The value of dV_{th}/dT is negative in n-MOSFET and positive in p-MOSFET. The change in dV_{th}/dT is the summation of both changes in the factor of dV_{FB}/dT in the 2nd row and the factor caused by the depletion charge in the 4th row. Therefore, when T_{TiN} increases, two ingredients are synthesized and an outstanding shift to negative direction is observed in n-MOSFET. On the other hand, two ingredients cancel each other and only a small shift to negative direction is observed in p-MOSFET.

Table 3.4. Analysis of changes in $|dV_{th}/dT|$ in high-k/TiN/poly-Si metal gate transistors based on the ingredients of terms in equation (3.4.1).

	n-MOSFET				p-MOSFET	
	positive or negative	shift direction for thicker La_2O_3	shift direction for thicker Al_2O_3	shift direction for thicker TiN	positive or negative	shift direction for thicker TiN
$\frac{d\Phi_{TiN}}{dT}$	negative			negative	negative	negative
$\frac{dV_{FB}}{dT}$	positive	no change	no change	negative	negative	negative
EOT	positive	no change	positive	positive	positive	positive
$\pm\frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a\lvert\phi_f\rvert}$	negative	no change	negative	negative	positive	positive
$\frac{dV_{th}}{dT}$	negative	no change	negative	large negative	positive	small negative
$\left\lvert\frac{dV_{th}}{dT}\right\rvert$		no change	increase	large increase		small decrease

	Remarks column
$\frac{d\Phi_{TiN}}{dT}$	Temperature coefficient of work function of TiN.
$\frac{dV_{FB}}{dT}$	Temperature coefficient of flat band voltage. 1st term in equation (3.4.1).
EOT	$1/C_{ox}$ in the lower column is proportional to EOT.
$\pm\frac{1}{C_{ox}}\frac{d}{dT}\sqrt{4q\varepsilon_0\varepsilon_{Si}N_a\lvert\phi_f\rvert}$	Temperature coefficient of the effect of depletion charge. 3rd term in equation (3.4.1). "+" for n-, "–" for p-MOSFET.
$\frac{dV_{th}}{dT}$	Temperature coefficient of V_{th}.
$\left\lvert\frac{dV_{th}}{dT}\right\rvert$	Absolute value of temperature coefficient of V_{th}.

3.6.2 Summary

In this chapter, the temperature coefficient of the threshold voltage (=dV_{th}/dT) of poly-Si/TiN/capping/high-k dielectric gate MOSFETs was investigated. When the TiN layer becomes thick, the dV_{FB}/dT of both n- and p-MOSFETs shifts to the negative direction, which increases $|dV_{th}/dT|$ of n-MOSFET and decrease $|dV_{th}/dT|$ of p-MOSFET. Meanwhile, the condition of capping layer doesn't affect the dV_{FB}/dT. The change in $|dV_{th}/dT|$ is remarkable, especially for n-MOSFETs, because the influence of the temperature coefficient of the depletion charge additively affects the dV_{FB}/dT of n-MOSFET, while it oppositely affects p-MOSFET. The cause of the change in the dV_{FB}/dT in n- and p-MOSFETs is a change in the temperature coefficient of work function of TiN (=$d\Phi_{TiN}/dT$). $d\Phi_{TiN}/dT$ has a negative value, and $|d\Phi_{TiN}/dT|$ becomes large when the TiN becomes thick.

In this chapter, the characteristics of temperature dependence of V_{th} in metal gate MOSFETs have been analyzed. One of the main factors is the T_{TiN} dependence of $d\Phi_{TiN}/dT$. In the next Chapter 4, the mechanism which changes $d\Phi_{TiN}/dT$ depending on T_{TiN} was investigated.

References

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4. Mechanism of temperature dependence of work function

4.1. Introduction

As clarified in the previous Chapter 3, the temperature coefficient of work function of TiN ($d\Phi_{TiN}/dT$) is changed by the thickness of TiN (T_{TiN}). In this Chapter 4, the cause of this phenomenon will be revealed [1].

Various studies have already reported that Φ_{TiN} increases when T_{TiN} becomes large [2, 3]. For example, Singanamalla *et al.* reported that the effective work function of HfSiON(or SiO_2)/TiN/poly-Si increases as T_{TiN} increases from 0.5 to 5.0 nm. The shift of the work function depending on T_{TiN} was different between HfSiON and SiO_2, and the shift was attributed to a change in ratio of the Hf-Si bond and Hf-Ti bond at the HfSiON/TiN interface [3]. In their report, however, the T_{TiN} of samples was thinner than that of our sample, and the results are not the same as our results, in which the change in the work function on high-k was almost coincident with that on SiON. Therefore, another model for explaining our results is required. In addition, the fact that not only Φ_{TiN} but also $|d\Phi_{TiN}/dT|$ increases depending on T_{TiN} has been newly revealed in the previous Chapter 3. In the Chapter 3, we speculated that the reason why Φ_{TiN} and $d\Phi_{TiN}/dT$ change depending on T_{TiN} is the effect of the change in TiN itself. Then, as explained in this chapter, we considered the mechanism by which Φ_{TiN} and $|d\Phi_{TiN}/dT|$ increase depending on T_{TiN}. As a result, we concluded that the main factor by which a thick TiN has large Φ_{TiN} and large $|d\Phi_{TiN}/dT|$ is a change in the crystallinity of TiN.

In this Chapter 4, three kinds of physical analysis for elucidation of temperature dependence mechanism revealed the differences in the physical properties of TiN which is affected by T_{TiN}. The first experiment was ultraviolet photoelectron spectroscopy (UPS), by which the relation between the thickness of TiN and the work function of TiN was directly measured. Next, the relationship between the thickness of TiN and its crystallinity was observed using transmission electron microscope (TEM) images. In addition, the crystal structure of TiN was confirmed by X-ray Diffraction (XRD). The results of these experiments showed a change in the crystallinity of TiN caused by change of T_{TiN}. After consideration, it was interpreted that this crystallinity change is the direct cause of the changes of Φ_{TiN} and $d\Phi_{TiN}/dT$.

Hereinafter, the experiment method is indicated in the next section 4.2. After that, the results of three kinds of physical analysis are described in section 4.3. In section 4.4, the mechanism in which crystallinity affects Φ_{TiN} and $d\Phi_{TiN}/dT$ is discussed. Finally, the total consideration of this Chapter 4 is described in section 4.5.

4.2. Experimental method

4.2.1 Fabrication of blanket sample

The experimental samples that were used to investigate the changes of the physical properties of the TiN layer depending on T_{TiN} were as follows. Three samples were fabricated with blanket Si wafers. After the formation of a high-k dielectric layer, three thicknesses of TiN layers were

deposited, sample (A) with 5-nm TiN, (B) with 10-nm TiN, and (C) with 30-nm TiN. Then, all samples passed through a 1000°C spike RTA process. The maximum T_{TiN} in the blanket samples, which was 30 nm, was larger than that of the MOSFET samples used in the Chapter 3, which was 15 nm, in order to detect the differences in the physical properties.

4.2.2 Reference sample for the blanket sample

As shown in Fig. 3.16, when T_{TiN} increases from 5 nm to 15 nm, $\Delta\Phi_{TiN}$ (=ΔV_{FB}) increases by approximately 130 mV in the metal gate n-MOSFETs. Here, in order to correspond to the above-mentioned blanket-wafer samples which contain T_{TiN}=30 nm, $\Delta\Phi_{TiN}$ was additionally measured with "reference samples" for the data of T_{TiN} larger than 15 nm. These reference samples for the blanket samples were MIPS gate MOS capacitors, in which T_{TiN} was set from 8 nm to 30 nm.

Although the fabrication method of the reference sample for the blanket sample was the basically same as that of MOSFET sample in Chapter 3, etching condition for patterning of the metal gate electrode was different. In MOSFET, because a part of the edge of gate electrode is in active areas, it is necessary to stop etching of TiN at thin gate insulator. Because this technique is difficult, there is a limit of T_{TiN} in the case of MOSFET sample. Therefore, the maximum T_{TiN} of the MOSFET sample in Chapter 3 was 15 nm.

On the other hand, the new fabricated reference sample for the blanket sample was MOS capacitor. In the structure of MOS capacitor, all of the gate edge is on isolation oxide (STI: Shallow Trench Isolation). Therefore, in MOS capacitor samples, because it is not necessary to stop etching of TiN at thin gate insulator, samples with thick TiN metal gate can be fabricated.

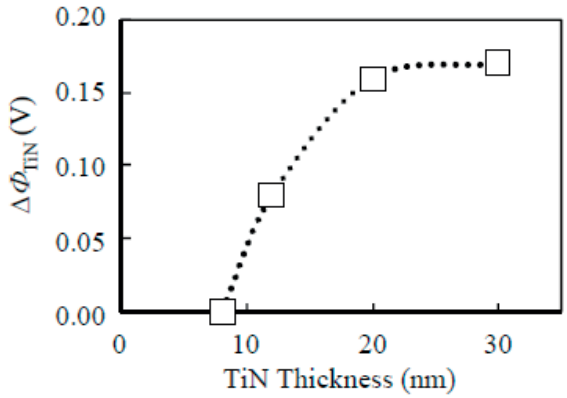

Fig. 4.1. The change in Φ_{TiN} depending on the TiN thickness in metal gate MOS capacitors with p-type Si substrate.

The results of $\Delta\Phi_{TiN}$ obtained by C-V measurement with MOS capacitors are shown in Fig. 4.1. It is confirmed that the increase in $\Delta\Phi_{TiN}$ between 8-nm TiN and 15-nm TiN is approximately 110 mV, the slope of which is almost the same value as in Fig. 3.16 (14.2 mV/nm), Fig. 3.17 (15.7 mV/nm), and Fig. 4.1 (15.7 mV/nm). Therefore, T_{TiN} dependence of Φ_{TiN} is thought to be basically the same in both the MOSFET sample in Chapter 3 and MOS capacitor sample in Chapter 4. And, the behavior of Φ_{TiN} for T_{TiN} larger than 15 nm was revealed only by the MOS capacitor sample. The increase in $\Delta\Phi_{TiN}$ becomes gradual as T_{TiN} becomes large, and $\Delta\Phi_{TiN}$ almost saturates at a certain level for T_{TiN} larger than 20 nm in the MOS capacitor sample. It means that the rise of Φ_{TiN} caused by increase in T_{TiN} has a limit for some reason. The reason will be explained in the section 4.3.

4.2.3 The physical analysis method

The methods of the three kind of physical analyses are explained.

(1) Ultraviolet Photoelectron Spectroscopy (UPS)

In UPS measurement, photoelectrons are released by irradiating a sample with ultraviolet rays. He I (21.22 eV) was used for ultraviolet. The maximum kinetic energy of released electron was measured by an analysis of the UPS spectrum. From the difference between the maximum kinetic energy of electron and the energy of the excitation UV light, the energy necessary to take one electron out of the solid surface to a vacuum (work function) was calculated.

UPS obtains the information of the sample at the depth less than several nm from the surface. To eliminate surface contamination etc., the surface of sample TiN is etched before the UPS measurement by Ar sputtering (depth is 2 nm in SiO_2 conversion).

(2) Transmission Electron Microscope (TEM)

TEM is an electron microscope in which an electron beam irradiates ultra-thin sample and the electrons which is transmitted through the sample make a microscope image. The density of electron which is transmitted through a certain site in the sample changes depending on the difference of the structure or the component at the site, and it is reflected in a microscope image.

(3) X-ray Diffraction (XRD)

XRD is a method for investigation of the crystal structure of the sample using diffraction phenomenon of X-rays in crystal lattice. The distance between the lattice planes in the sample crystal is measured using the angle where the diffraction peak appears, and the crystal structure can be identified. The width of the peak reflects the size of crystals, and the mean size of the crystallite (L_c) can be calculated with Scherrer equation, which is

$$B = \frac{K\lambda}{L_c \cos\theta}, \tag{4.2.1}$$

where B is the peak width at half the maximum intensity (FWHM), K is a dimensionless shape factor (Scherrer constant), which is typically about 0.9 but varies by the actual shape of the crystallite, λ is the wavelength of X-ray, θ is the Bragg angle [4].

4.3. Crystallinity and work function of TiN

4.3.1 Result and consideration of UPS

The work functions of TiN (Φ_{TiN}) were directly measured by UPS and plotted in Fig. 4.2 for sample (B), T_{TiN} = 10 nm, and (C), T_{TiN} = 30 nm. Figure 4.2, in which the average of two measurements for sample (B) was set to zero, indicates that the average measurement for sample (C) was higher than that of sample (B) by approximately 100 meV.

As shown in Fig. 4.1, the difference in the Φ_{TiN} obtained by C-V between 10-nm TiN and 30-nm TiN is approximately 120 mV, which is close to the UPS result (100 meV). It indicates that most of the increase in Φ_{TiN} with the increase in T_{TiN} is reasonably explained by the actual increase in the work function of TiN itself.

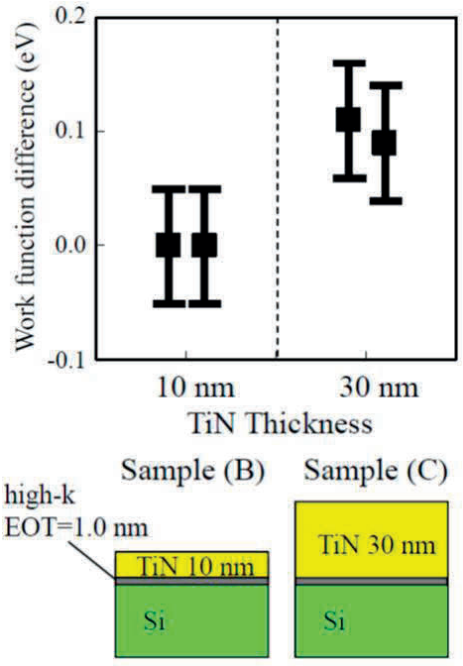

Fig. 4.2. The work function difference in TiN between sample (B) and sample (C) as measured by UPS. The average of two measurements for sample (B) was set to zero. The margin of error in the UPS measurement is ±50 meV. The work function of 30-nm TiN is higher than that of 10-nm TiN by approximately 100 meV.

Correctly, what is observed in UPS is original WF, and what is obtained by C-V measurement is effective WF which contains the effect of S_{FLP} in the equation (3.5.1). The S_{FLP} contains, for example, the effect of the dipole formed by bonds of different atoms at the TiN/insulator interface [5], or the effect of the dipole at the extrinsic states generated at the interface [6], or the change of the effect of surface dipole at TiN surface caused by the contact with the gate insulator film [7]. In general, the difference of UPS will not necessarily become the difference of effective WF. But S_{FLP} is regarded as almost a constant during the change in the T_{TiN}, as it was explained at the section 3.5.2. In the case that S_{FLP} does not change, it can be said that the difference of UPS (original WF) becomes the difference of effective WF.

4.3.2 Result and consideration of TEM

TEM images of each sample are compared in Fig. 4.3. The TEM image of sample (C) shows that columnar crystal grains are obvious in 30-nm TiN. The boundary of grains is clear, and many lattice fringes are observed in the black area, which is thought to be a crystallized region. Next, in the TEM image of 10-nm TiN (sample (B)), the grain boundaries become fuzzy, and the number of lattice fringes becomes smaller than that of the 30-nm TiN. In addition, the ratio of the black area, which is a crystallized region, decreases, and the ratio of the white area, which is thought to be an amorphous-like region, increases. Finally, the lattice fringes completely vanish in the 5-nm TiN (sample (A)). These analyses indicate the following conclusion. The crystallinity of 30-nm TiN is high. However, as T_{TiN} becomes smaller, the ratio of the crystallized region becomes low. Simultaneously, the crystallinity of the crystallized region also becomes low. As a result, the crystallinity of 5-nm TiN becomes lower, and its structure becomes more amorphous.

Here, the 30-nm TiN is discussed in more detail. The feature of high crystallinity is observed not only from the upper part of the 30-nm TiN, but also from the lower part of the 30-nm TiN, although lower part had been deposited before TiN film became thick. Since the whole of a 30-nm TiN has almost the same crystallinity, it is thought that almost the same result is obtained both from the lower part and the upper part, if the observation is a measurement of a property affected by the crystallinity of TiN. Therefore, although UPS obtains a WF which reflects only the characteristics of the upper part of 30-nm TiN, it is supposed that also the lower part, which is the part which influences the effective WF of the MOSFET, has almost the same WF.

Moreover, we measured the heights of the TiN grains in each TiN sample and calculated the average size. The resulting average size is 5.0 nm in 5-nm TiN (which is limited by sample thickness), 8.4 nm in 10-nm TiN, and 13.6 nm in 30-nm TiN. The grains become large depending on the increase in T_{TiN}.

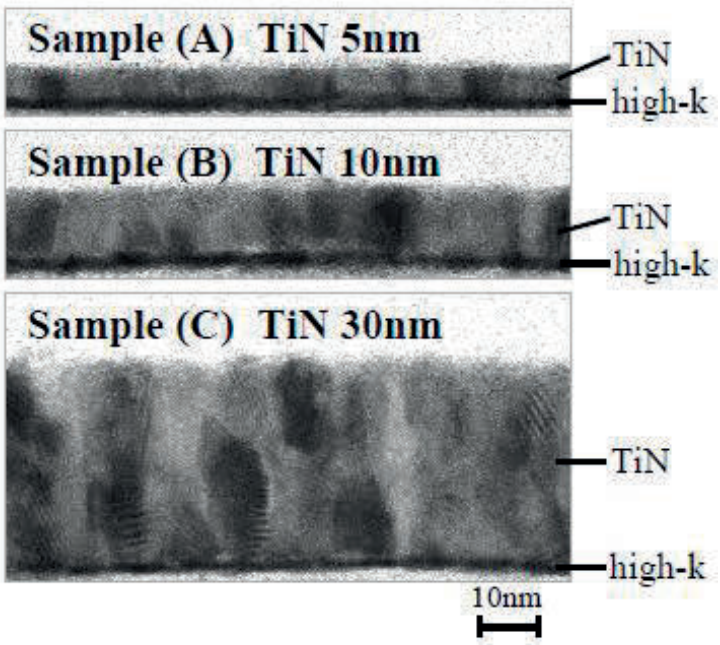

Fig. 4.3. TEM images of the TiN layers in samples (A) 5 nm, (B) 10 nm, and (C) 30 nm.

4.3.3 Result and consideration of XRD

In order to confirm the change in TiN crystallinity, which depends on T_{TiN}, the XRD results of each sample are compared in Fig. 4.4 (a). When T_{TiN} is 5 nm (sample (A)), the peak at the position of (200), representing a diffraction of approximately $2\theta = 43°$, is very small. In the sample of 10-nm TiN (sample (B)), the peak of (200) appears clearly, and it becomes higher in the 30-nm TiN (sample (C)). The peak of (111), approximately $2\theta = 37°$, is also observed in the 30-nm TiN. The full width at half maximum (FWHM) of the peak of (200) and (111) were measured, and they are plotted in Fig. 4.4 (b) (only the FWHM of (111) in 5-nm TiN could not be read). Scherrer indicated that FWHM is inversely proportional to the mean size of the crystallite according to the equation (4.2.1) [4]. Therefore, when the horizontal axis of Fig. 4.4 (b) is the reciprocal of grain size, all of the measurement points should be located on a straight line through the origin if the crystallinities of all samples are the same. The dashed lines in Fig. 4.4 (b) are the ideal lines, which indicate the case that all samples have the same crystallinity as the 30-nm TiN sample. The observed points of 10-nm TiN and 5-nm TiN are, however, located at higher positions than the ideal lines. These results indicate that the FWHM of 10-nm and 5-nm TiN is larger than the expected width from the 30-nm TiN, and the crystallinity of the generated crystal region becomes lower as T_{TiN} becomes smaller. Therefore, the XRD results agree with the conclusion from the previous TEM image analyses.

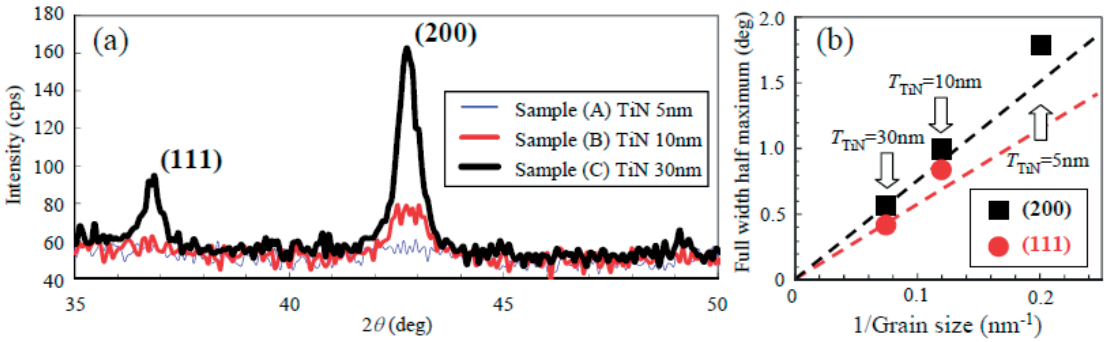

Fig. 4.4. (a) Results of XRD measurement with samples (A), (B) and (C).
(b) The change in FWHM depending on the reciprocal of grain size. The dashed lines mean the case in which the TiN film maintains the crystallinity of 30-nm TiN.

4.3.4 Total consideration of physical analysis

From the results of these physical analyses, the 5-nm TiN contains many more amorphous regions. Then, the crystallinity of TiN is enhanced in 10-nm TiN, and the crystallinity becomes still clearer in 30-nm TiN. Because TiN has a property that shows a trend of making columnar crystals, it is thought that making crystal structures is difficult until the TiN layer reaches a sufficient thickness.

It is considered that the change in the crystallinity of TiN influences the shift of Φ_{TiN}. As explained in the section 2.3, the value of the work function is affected by the difference in the crystal structure or the orientation of the crystal layer [8-11]. Lang *et al*. reported that the redistribution of the electron density on the surface forms a surface dipole barrier that depends on the anisotropy of the crystal structure [8, 9]. Because the work function is influenced by the energy that is necessary for an electron to jump over the dipole barrier, the work function reflects the difference in crystallinity. In the case of TiN, the work functions of 30-nm-thick TiN layers were measured by Kelvin Probe Force Microscopy, and their crystallinities (affected by the difference in substrates) were confirmed using XRD by Gaillard *et al.* [10]. They reported that Φ_{TiN} with a clear crystal structure was higher than that with an amorphous-like structure by 240 meV, which was explained in section 2.3.2 in detail.

In the case of our samples, the TiN layer has an amorphous-like structure when T_{TiN} is small, and the crystal orientation of (200) or (111) is observed more clearly when T_{TiN} becomes large, as shown in Figs. 4.3 and 4.4. This result indicates that a thick TiN layer in a metal gate electrode has higher Φ_{TiN} than a thin TiN layer because of the enhancement of the crystallinity of TiN, and it explains the origin of the V_{FB} shift that is shown in Figs. 3.16 and 3.17. As shown in Fig. 4.1, the increase in Φ_{TiN} depending on T_{TiN} becomes almost saturated when T_{TiN} exceeds 20 nm. It is thought that the TiN layer obtains a sufficient crystal structure when it reaches a certain thickness (> 20 nm). Therefore, it is reasonable that Φ_{TiN} saturates when T_{TiN} exceeds a certain thickness.

4.4. Temperature coefficient of work function of TiN

4.4.1 Consideration of temperature coefficient of work function in metal

It has been reported that the temperature coefficient of the metal work function changes with crystal orientations. Blevis and Crowell measured the temperature dependence of the work function of Cu with various crystal orientations [11]. At room temperature, the Cu work function changes from 4.89 eV to 5.64 eV depending on the change in crystal orientation from (111) to (100). At high temperatures, the work function decreases in all crystal orientations, and its crystal orientation dependence is weakened. They predicted that the crystal orientation dependence of the work function will completely disappear at the melting point. More detailed explanation about temperature coefficient of metal work function was described in the previous section 2.3.3 in the Chapter 2.

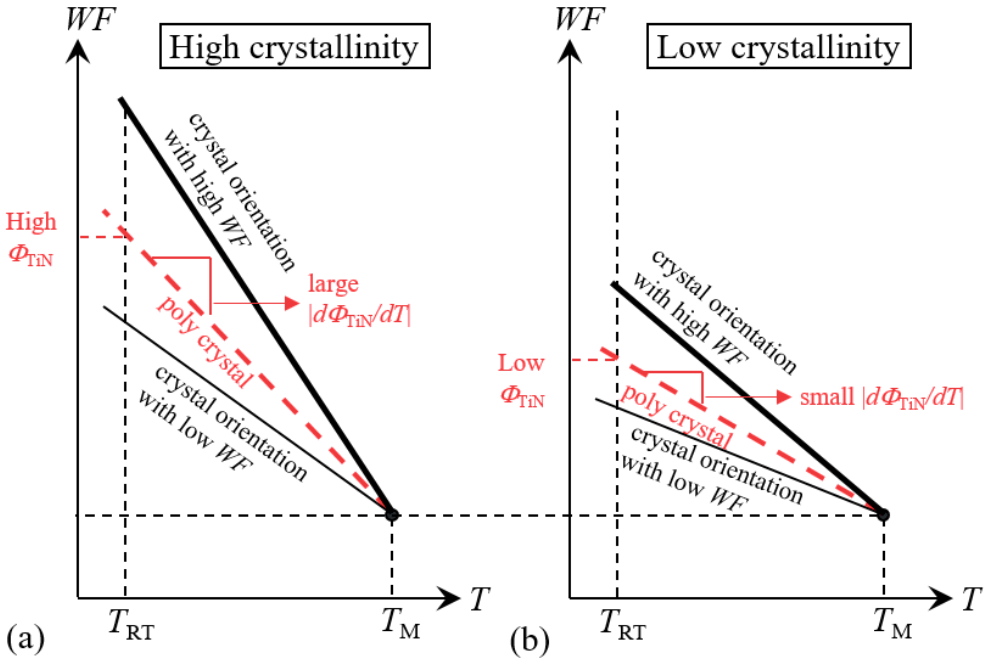

Fig. 4.5. Schematic diagram that indicates the expected temperature dependence of work functions (*WF*s) in polycrystalline metal film that has (a) high crystallinity or (b) low crystallinity. T_{RT} is room temperature, and T_M is the melting point. The heavy solid line indicates the crystal orientation with the higher work function, the fine solid line indicates that with the lower work function, and the dashed line indicates the total poly crystal (Φ_{TiN}). (a) corresponds to the thick TiN film, and (b) corresponds to the thin TiN film. In these figures, it is assumed for simplicity that Φ_{TiN} changes linearly depending on temperature.

A simplified explanation for polycrystalline structure of Cu is demonstrated in Fig. 4.5 (a). In Fig. 4.5 (a), the heavy solid line indicates the temperature dependence of the work function of Cu (100), and the fine solid line indicates that of Cu (111). These two lines meet at the melting point. Thus, the crystal orientation dependence of the work function is large at low temperatures and small at high temperatures (almost no difference at the melting point). When the Cu film is polycrystal, the work function of the film must be equal to an average of the work functions for various crystal orientations, which is indicated as a dashed line in Fig. 4.5 (a). As a result, the work function of the polycrystalline Cu film will also be reduced at high temperatures.

4.4.2 Consideration for TiN

I applied this reported characteristic of work function of Cu to TiN. In the case of the TiN samples used in this study, Fig. 4.5 (a) indicates the property of 30-nm or 15-nm TiN film, and (b) indicates that of 5-nm TiN film. The 30-nm or 15-nm TiN is polycrystal, which consists of more rigid (200) and (111) faces. The heavy solid line, which has a higher work function at room temperature, corresponds to (200) face, and the fine solid line, which has a lower work function at room temperature, corresponds to (111) face [11]. Φ_{TiN}, which is the detected work function of the total polycrystal, is represented by the dashed line in Fig. 4.5 (a). Alternately, the 5-nm TiN shown in Fig. 4.5 (b) has lower crystallinity. Therefore, the work functions at room temperature are lower than those in Fig. 4.5 (a). Φ_{TiN} decreases as the temperature becomes higher. Because the difference disappears at the melting point, the work functions at the melting point are the same both in Fig. 4.5 (a) and (b). Φ_{TiN}, which is the total work function of the polycrystalline 5-nm TiN film, is indicated by the dashed line in Fig. 4.5 (b). The slope of the dashed line in Fig. 4.5 (a) is steeper than that in Fig. 4.5 (b), which means that 15-nm TiN film has larger $|d\Phi_{TiN}/dT|$ than 5-nm TiN film.

Based on the above discussion, the difference in $|d\Phi_{TiN}/dT|$ between TiN films was calculated concretely. The melting point of TiN is 3223 K [12]. The Φ_{TiN} of 15-nm thick TiN with a more rigid crystal structure is higher than the Φ_{TiN} of 5-nm TiN with an amorphous-like structure by 130 mV at room temperature (Fig. 3.16). If Φ_{TiN} decreases from 300 K to 3223 K in a roughly linear manner and the crystal orientation dependence of the work function becomes zero at the melting point, then it is expected that the value of $|d\Phi_{TiN}/dT|$ of 15-nm TiN becomes larger than that of 5-nm TiN by 0.045 mV/K, which is obtained by 130 mV/(3223 K–300 K).

In fact, as shown in Fig. 3.25, the difference in the measured $|d\Phi_{TiN}/dT|$ between 5-nm TiN and 15-nm TiN is more than 0.08 mV/K, which is approximately 1.8 times larger than the expected value based on the above model (=0.045 mV/K, which means the average slope from room temperature to the melting point). The actual temperature dependence of the work function may not be linear, as shown in Fig. 4.5, but may be nonlinear, i.e., the slope is steep at low temperatures and becomes moderate at high temperatures. In the case of (111) face of Cu [13], the maximum slope ($|d\Phi_{Cu}/dT|_{max}$) is approximately 1.5 times larger than that of the straight line between room temperature and melting point (the average slope from room temperature to the melting point), as shown Fig. 2.8. Because similar behavior is expected for TiN film, the experimentally obtained difference in $|d\Phi_{TiN}/dT|$ between 5-nm TiN and 15-nm TiN (0.08 mV/K) may be explained by the

above model. For example, if the same factor as the case of Cu (1.5 times) is applied, the expectation value becomes about 0.068 mV/K (= 0.045 x 1.5), which is thought a considerably close value to the experiment result.

The increase in T_{TiN} causes the change in the crystal structure of TiN, and it causes the changes in both Φ_{TiN} and $d\Phi_{TiN}/dT$. It is concluded that this is the main reason by which $|d\Phi_{TiN}/dT|$ is affected by T_{TiN}. Although this model does not necessarily deny the existence of other factors that affect $d\Phi_{TiN}/dT$, we can explain the T_{TiN} dependences of Φ_{TiN} and $d\Phi_{TiN}/dT$ simultaneously by using only the change in the crystallinity of TiN.

4.5. Total consideration

4.5.1 Experimental results and considerations in Chapter 4

In this chapter, the mechanism of the phenomenon that the temperature coefficient of work function of TiN ($d\Phi_{TiN}/dT$) is changed depending on the thickness of TiN (T_{TiN}) have been revealed. The experiments and results to investigate the mechanism are as follows:

(1) Additional measurement of Φ_{TiN} (T_{TiN} > 15 nm)

[Experiment] Additional data of Φ_{TiN} were observed with MOS capacitors samples in wider range of T_{TiN} (> 15 nm) than that with MOSFET samples in the Chapter 3 ($T_{TiN} \leq$ 15 nm).

[Result] It was confirmed T_{TiN} dependence of Φ_{TiN} in MOS capacitor samples was basically the same as the MOSFET samples in common range of T_{TiN}. In newly added range of T_{TiN}, the increase in $\Delta\Phi_{TiN}$ became gradual as T_{TiN} became large, and $\Delta\Phi_{TiN}$ was almost saturated when T_{TiN} became larger than 20 nm.

(2) Ultraviolet photoelectron spectroscopy (UPS)

[Experiment] The work function of TiN was directly measured by UPS with blanket wafer samples with T_{TiN} = 10 nm, 30 nm.

[Result] Φ_{TiN} in 30-nm TiN was higher than Φ_{TiN} in 10-nm TiN by about 100 meV.

(3) Transmission electron microscope (TEM)

[Experiment] TEM images of blanket wafer samples were compared among T_{TiN} = 5 nm, 10 nm, 30 nm.

[Result] The crystallinity of TiN was thought to become higher as T_{TiN} became larger. The average grain size became larger, the ratio of the crystallized region becomes higher, and the crystallinity of the crystallized region also becomes higher, simultaneously.

(4) X-ray Diffraction (XRD)

[Experiment] X-ray diffraction results from the sample with T_{TiN} = 5 nm, 10 nm, 30 nm are compared.

[Result] By the comparison of diffraction ray from each sample, T_{TiN} dependence of the crystal structure of TiN were considered quantitatively. The previous analyses about the crystallinity of TiN with TEM image were confirmed also by XRD.

From the results of above experiments and knowledge of past literature, we concluded that the main cause of the phenomenon that the thicker TiN has the larger Φ_{TiN} and the larger $|d\Phi_{TiN}/dT|$ is a change in the crystallinity of TiN. The mechanism is explained as follows:

(1) Enhancement of crystallinity of TiN caused by an increase of T_{TiN}

TiN has a trend of making columnar crystal grains in a longitudinal direction. Therefore, it is thought that the TiN layer cannot obtain a sufficient crystal structure before it reaches a certain thickness (> 20 nm). The crystallinity of 5-nm TiN is low, and its structure is more amorphous. The crystallinity of TiN is enhanced by the increase in TiN thickness, and 15-nm TiN has more rigid crystallinity than 5-nm TiN.

(2) Increase in Φ_{TiN} caused by enhancement of crystallinity of TiN

The redistribution of the electron density on the surface forms a surface dipole barrier, which influences the value of the work function [8, 9]. Therefore, it is thought that the work function reflects the difference in crystallinity. In our experiment, UPS measurement actually demonstrated Φ_{TiN} in 30-nm TiN was higher by about 100 meV than that of 10-nm TiN. It is thought that the cause of the difference of the effective work function in our samples between T_{TiN}=5 nm and 15 nm (it is about 130 meV as shown in Fig. 3.16) is approximately explained by this mechanism.

(3) Cause of difference in $|d\Phi_{TiN}/dT|$ depending on crystallinity

In the case of Cu, when temperature becomes higher, the work function of Cu becomes smaller, and the difference of work function caused by difference of crystal orientations becomes smaller [11]. It is predicted that the work function difference by crystal orientation will disappear at the melting point. If this model is applied to TiN, the difference in $|d\Phi_{TiN}/dT|$ between 5-nm TiN and 15-nm TiN can be calculated. The estimated value of the difference is 0.045 mV/K if the average slopes of $|d\Phi_{TiN}/dT|$ are used. If the actual slopes at room temperature are used, the difference is able to become larger, and may become close to the observed value shown in Fig. 3.25 (more than 0.08 mV/K). This model can explain the T_{TiN} dependences of Φ_{TiN} and $d\Phi_{TiN}/dT$ simultaneously by using only the change in the crystallinity of TiN.

This is the mechanism of T_{TiN} dependence of Φ_{TiN} and $|d\Phi_{TiN}/dT|$ that we considered in this Chapter 4. This mechanism affects the behavior of V_{FB} and dV_{FB}/dT described in Chapter 3 as follows: When T_{TiN} becomes large, the crystallinity of TiN becomes more rigid. As a result, the value of Φ_{TiN} shift to the positive direction (Fig. 4.1), and $d\Phi_{TiN}/dT$ shifts to the negative direction (Fig. 3.24). Then, also the value of V_{FB} shifts to the positive direction (Figs. 3.16, 3.17), and dV_{FB}/dT shifts to the negative direction (Figs. 3.20, 3.21).

4.5.2 Summary

The physical mechanism that changes Φ_{TiN} and $d\Phi_{TiN}/dT$ was investigated in this chapter. The crystal structure of TiN becomes more rigid as the TiN becomes thicker, which was proved by TEM and XRD analyses. If the crystallinity is improved, the work function of the metal is changed by the

effect of the surface dipole. It was confirmed by UPS measurement that Φ_{TiN} becomes higher in a thicker TiN layer. Φ_{TiN} becomes lower at higher temperatures. The Φ_{TiN} difference due to the difference in the crystal structure becomes smaller as the temperature rises, and the difference is thought to become almost zero at a melting point. Therefore, the $|d\Phi_{TiN}/dT|$ of a thick TiN layer becomes larger compared to that of a thin TiN layer. The change in the crystallinity of TiN film is thought to be the main factor that generates the TiN thickness dependence of both Φ_{TiN} and $d\Phi_{TiN}/dT$.

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5. Possibility of control of dV_{th}/dT

5.1. Introduction

To consider the control methods of $|dV_{th}/dT|$ in metal gate transistor is one of the purposes of this thesis. Generally, if the temperature coefficient of V_{th} ($|dV_{th}/dT|$) is small, it is thought that the operation margin of the circuit becomes large, which is advantageous to enhancement of yield in mass production. The magnitude of the $|dV_{th}/dT|$ is an important parameter that might influence also the production efficiency of the products. Based on the results that became clear in this study, control methods of $|dV_{th}/dT|$ are discussed in this chapter. Then, in the next section 5.2, I will explain the mechanism which decides the dV_{th}/dT based on the consideration described in the Chapter 3 and 4. In the section 5.3, the possibility of control of dV_{th}/dT in a gate first metal gate transistor process, which was also the process used in this study. Next, in the section 5.4, the control of dV_{th}/dT in a gate last metal gate transistor process was considered.

5.2. Mechanism of TiN thickness dependence of dV_{th}/dT

First, the mechanism that decides the temperature coefficient of work function of TiN ($d\Phi_{TiN}/dT$) is indicated. The crystal structure of TiN is thought to become more rigid when the TiN thickness (T_{TiN}) becomes thicker, because TiN film has a trend of making columnar crystal grains in a longitudinal direction (Fig. 4.3). If the crystallinity of TiN, which is fcc structure, is enhanced, the original work function of TiN (Φ_{TiN}) increases by the effect of the surface dipole (Fig. 2.5). At a higher temperature, the original Φ_{TiN} becomes lower and the difference of Φ_{TiN} caused by the difference in the crystal structure is thought to become smaller. And at a melting point, the difference by the crystal structure is thought to become zero. Therefore, the sign of $d\Phi_{TiN}/dT$ is negative, and the magnitude of $|d\Phi_{TiN}/dT|$ becomes larger in a thick TiN layer compared to that of a thin TiN layer, as shown in Fig. 5.1. The change in the crystallinity of TiN film is thought to cause the TiN thickness dependence of both Φ_{TiN} and $d\Phi_{TiN}/dT$.

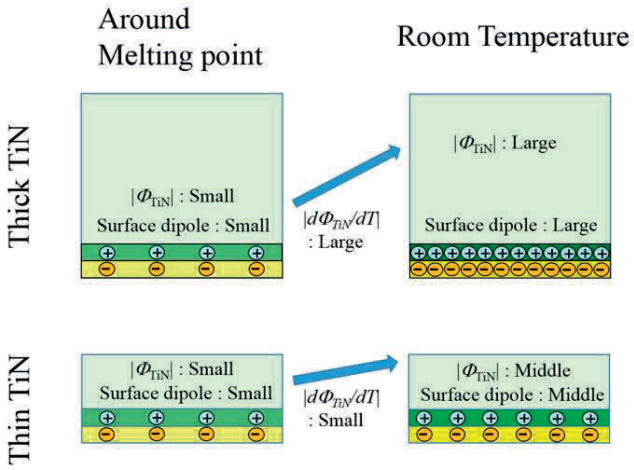

Fig. 5.1. Schematic diagram that indicates the change of surface dipole depending on TiN thickness and temperature.

Next, behaviors of dV_{FB}/dT are analyzed. When the TiN layer contacts with the gate insulator, the effective Φ_{TiN} becomes different from the original Φ_{TiN}, because of interface effects at the metal/insulator interface, such as Fermi level pinning. But, it is thought that the interface effects are relatively stable and almost constant in the case of the change of T_{TiN}. Therefore, the shift of effective Φ_{TiN} or $d\Phi_{TiN}/dT$ caused by a change of T_{TiN} are almost the same as the shift of original Φ_{TiN} or $d\Phi_{TiN}/dT$. As explained previously, when T_{TiN} becomes large, the original Φ_{TiN} shifts to positive direction, and the original $d\Phi_{TiN}/dT$ shifts to negative direction. Therefore, also the effective Φ_{TiN} shifts to positive direction and the effective $d\Phi_{TiN}/dT$ shifts to negative direction similarly regardless of the material of the gate insulator (Fig. 3.23). As described by equation (3.5.3) and (3,5,5), the behavior of dV_{FB}/dT is different from the behavior of effective $d\Phi_{TiN}/dT$, only by the effects of temperature coefficients of Fermi level and band structure in Si substrate, which are common in all nMOSFET samples or all pMOSFET samples. As a result, when T_{TiN} becomes thick, the dV_{FB}/dT of both n- and p-MOSFETs shifts to the negative direction (Fig. 3.20, 3.21).

Finally, the property of $|dV_{th}/dT|$ is explained. As described by equation (3.4.1), dV_{th}/dT is influenced by the dV_{FB}/dT and the temperature coefficient of the depletion charge. The shift of the dV_{FB}/dT to the negative direction caused by the increase in T_{TiN}, attributes an increase in the $|dV_{th}/dT|$ of an n-MOSFET and a decrease in the $|dV_{th}/dT|$ of a p-MOSFET. In addition, when T_{TiN} becomes large, the effect of the temperature coefficient of the depletion charge enlarges the $|dV_{th}/dT|$ in both n- and p-MOSFETs. The change in $|dV_{th}/dT|$ is large in n-MOSFETs, because the influence of the temperature coefficient of the depletion charge additively affects the dV_{FB}/dT of an n-MOSFET, while it oppositely affects the dV_{FB}/dT of a p-MOSFET (Fig. 3.18, 3.19). The cause of the change in the temperature coefficient of the depletion charge is an increase in *EOT*, which is affected by the increase in T_{TiN}.

On the other hand, there is not significant intrinsic effect caused by the difference of condition of capping layer such as La_2O_3 or Al_2O_3.

5.3. Gate-first process

5.3.1 Reduction of $|dV_{th}/dT|$ in both n- and p-MOSFET

A method which reduces $|dV_{th}/dT|$ is considered using the equation (3.4.1). If the sign of each term in the equation is considered (see Table 3.3), reduction of the effect of the 3rd term is effective for reduction of $|dV_{th}/dT|$ in both n- and p-MOSFETs. To enlarge C_{ox} can reduce the absolute value of the 3rd term. It means shrinkage of *EOT*. Therefore, further scaling of *EOT* is thought to have an effect which reduce the $|dV_{th}/dT|$ in both n- and p-MOSFET.

On the other hand, the effect of the 1st term always increases the $|dV_{th}/dT|$ in either n- or p-MOSFETs, while it decreases the $|dV_{th}/dT|$ of the other. Therefore, as long as n- and p-MOSFETs use the same TiN layer for gate electrodes, control of the crystallinity of TiN cannot be used as a technique to simultaneously suppress $|dV_{th}/dT|$ in both n- and p-MOSFETs.

5.3.2 Consideration of 'balance-point' in gate-first metal gate transistors

Given this situation, one of the methods for optimization is to adjust the $|dV_{th}/dT|$s in both n- and p-MOSFETs to the same value. Thereby, a balance of V_{th} between n- and p-MOSFETs in circuits will be maintained even though the operation temperature changes. Figures 3.20 and 3.21 indicate that both the n- and p-MOSFET samples in this study have the same $|dV_{FB}/dT|$ (approximately 0.65 mV/K) around T_{TiN} = 12~13 nm. This 'balance-point,' however, will shift depending on conditions of N_a and N_d (acceptor and donor concentrations in the Si substrate) because $d|\phi_f|/dT$ in equation (3.5.3) is changed by the substrate impurity concentration. When the substrate impurity concentration becomes higher, $|dV_{FB}/dT|$ will become smaller. Therefore, in the case that the N_a in the n-MOSFET becomes higher, the balance-point of $|dV_{FB}/dT|$ will be shifted toward the direction of smaller T_{TiN}. On the contrary, when the N_d of the p-MOSFET becomes higher, the balance-point will move to the direction of larger T_{TiN}.

The balance-point of $|dV_{th}/dT|$ of the samples in this study is around T_{TiN} = 8 nm, where $|dV_{th}/dT|$ is approximately 1.04 mV/K, as shown in Figs. 3.18 and 3.19. When the substrate impurity concentration becomes higher, whether $|dV_{th}/dT|$ increases or decreases changes depending on the thickness of *EOT*. However, in the case of recent MOSFETs [1] in logic circuits, which have thin *EOT* (several nanometers or less), $|dV_{th}/dT|$ will become smaller as N_a or N_d becomes higher [2]. Therefore, when the N_a of the n-MOSFET becomes higher, T_{TiN} of the balance-point of $|dV_{th}/dT|$ will become larger. Conversely, if the N_d of the p-MOSFET becomes high, T_{TiN} of the balance-point will become small.

5.4. Gate-last process

Consideration of gate-last metal gate transistors

If other process techniques are also considered, the control of the crystallinity of TiN might become an available technique for the suppression of $|dV_{th}/dT|$ in both the n- and p-MOSFETs in gate-last metal gate transistors, which have already succeeded in mass production [3]. It has been reported that even though there is no high-temperature process, such as an activation anneal, for TiN film, the effective work function of the TiN metal gate shifts depending on the TiN thickness [4], as is the case with the TiN film with the high-temperature process. In a gate-last process, it is common to apply different metals as gate materials for the n- and p-MOSFETs. If, for example, only the p-MOSFET uses TiN as a gate material [5], the p-MOSFET can suppress $|dV_{th}/dT|$ by increasing the TiN thickness or enhancing the crystallinity of TiN, without considering the n-MOSFET. The technique of suppressing $|dV_{th}/dT|$ by controlling the crystallinity of TiN would be useful in the gate-last metal gate process in the future.

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6. Conclusion

For stable operation of MOSFETs in current semiconductor devices under a wide temperature range, the temperature coefficient of the threshold voltage (=dV_{th}/dT) of high-k dielectric/capping/TiN/poly-Si gate MOSFETs was investigated.

When the TiN layer becomes thick, the dV_{FB}/dT of both n- and p-MOSFETs shifts to the negative direction, which causes an increase in the $|dV_{th}/dT|$ of an n-MOSFET and a decrease in the $|dV_{th}/dT|$ of a p-MOSFET. On the other hand, when the TiN layer becomes thick, the effect of the temperature coefficient of the depletion charge enlarges the $|dV_{th}/dT|$ in both n- and p-MOSFETs. The change in $|dV_{th}/dT|$ is large in n-MOSFETs, because the influence of the temperature coefficient of the depletion charge additively affects the dV_{FB}/dT of an n-MOSFET, while it oppositely affects the dV_{FB}/dT of a p-MOSFET. The cause of the change in the temperature coefficient of the depletion charge is an increase in *EOT*, which is affected by the increase in TiN layer thickness. The cause of the change in the dV_{FB}/dT is a change in the temperature coefficient of the work function of TiN (=$d\Phi_{TiN}/dT$). $d\Phi_{TiN}/dT$ has a negative value, and $|d\Phi_{TiN}/dT|$ becomes large when the TiN becomes thick. On the other hand, we did not find a significant intrinsic effect which was caused by an existence of a capping layer (La_2O_3 or Al_2O_3) or by the change of their thicknesses.

The physical mechanism that changes Φ_{TiN} and $d\Phi_{TiN}/dT$ was further investigated. The crystal structure of TiN becomes more rigid as the TiN becomes thicker, which was proved by TEM and XRD analyses. If the crystallinity is improved, the work function of the metal is changed by the effect of the surface dipole. It was confirmed by UPS measurement that Φ_{TiN} becomes higher in a thicker TiN layer. Φ_{TiN} becomes lower at higher temperatures. The Φ_{TiN} difference due to the difference in the crystal structure becomes smaller as the temperature rises, and the difference is thought to become almost zero at a melting point. Therefore, the $|d\Phi_{TiN}/dT|$ of a thick TiN layer becomes larger compared to that of a thin TiN layer. The change in the crystallinity of TiN film is thought to be the main factor that generates the TiN thickness dependence of both Φ_{TiN} and $d\Phi_{TiN}/dT$.

As long as n- and p-MOSFETs use the same TiN layer for gate electrodes, control of the crystallinity of TiN cannot be used as a technique to simultaneously suppress $|dV_{th}/dT|$ in both n- and p-MOSFETs. In a gate-last metal gate process, however, controlling the crystallinity of the metal layer for each of n- and p-MOSFET could become a relatively simple technique. To suppress $|dV_{th}/dT|$ by controlling the crystallinity of TiN could become an available technique, especially for gate-last metal gate transistors.

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List of Publication

Full Papers Related to This Doctoral Thesis （公表論文）

(1) Temperature Coefficient of Threshold Voltage in High-k Metal Gate Transistors with Various TiN and Capping Layer Thicknesses
Y. Nishida, K. Eikyu, A. Shimizu, T. Yamashita, H. Oda, Y. Inoue, and K. Shibahara
Japanese Journal of Applied Physics **49** (2010) 04DC03 pp. 1-5.
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