博士論文

Grain Growth Control by Atmospheric Pressure Micro-Thermal-Plasma-Jet Irradiation on Amorphous Silicon Strips and Its Application to High-Speed CMOS Circuit Fabrication

（アモルファスシリコン細線への大気圧マイクロ熱プラズマジェット照射による結晶成長制御とその高速CMOS回路作製への応用）

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2015年10月

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Journal of Display Technology **10**, 950-955 (2014).

(2) Effect of Grain Growth Control by Atmospheric Micro-Thermal- Plasma-Jet Crystallization of Amorphous Silicon Strips on TFT Characteristics
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(1) Investigation of Silicon Grain Structure and Electrical Characteristics of TFTs Fabricated Using Different Crystallized Silicon Films by Atmospheric Pressure Micro-Thermal-Plasma-Jet Irradiation
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(2) Investigations on crack generation mechanism and crack reduction by buffer layer insertion in thermal-plasma-jet crystallization of amorphous silicon films on glass substrate
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主論文

Abstract

From the beginning of 2000s, flat panel displays (FPDs), such as liquid crystal displays (LCDs) and organic light emitting displays (OLEDs), have been widely in practical use for television (TVs), personal computers (PC), and mobile device. In order to drive the pixel of FPDs, an active-matrix driving method has been adopted by taking over the Cathode ray tube (CRT) in the past. FPDs, which are based on large area electronics, have been achieved remarkable development to enlarge and dilute the size of displays. It should be noted that thin film transistors (TFTs) had contributed to the remarkable development of FPDs. Hydrogenated amorphous silicon (a-Si:H) film was used for fabrication of TFTs as a switching device for pixels. Resent years, however, small and middle-sized displays, such as smart phone, tablet and wearable displays, have rapidly come into wide use. For these portable displays, high-reliability and higher-resolution than 500 pixels per inch (ppi), which is far beyond the limit resolution of human eyes, were strictly required. In addition, with the object of battery operation, low-power consumption is strictly required. With the shrink of pixel size and the increase of pixel number, the formation of narrow flames was strictly required because the number of wiring around display area rapidly increased.

In terms of field effect mobility (μ_{FE}) higher than 100 cm^2/Vs, high-reliability and the exclusive capability of complementary metal-oxide semiconductor (CMOS) fabrication, crystalline silicon (c-Si) technology is quite promising for next generation displays with low power consumption and multi-functions. Excimer laser annealing (ELA) has been widely utilized for fabrication of c-Si TFTs. However, because of the expensive equipment and running cost, lower fabrication cost technique has been required. In addition, c-Si TFTs has a critical issue of variation. TFT characteristics were sensitive to defects, such as grain boundaries (GBs) and intra-grain defects. The key research purposes for higher performance TFT is to enlarge the grain size. However, with increase of grain size, the characteristic variability of TFTs has become critical issue instead of high-$\mu_{FE.}$ Especially, the variation of threshold voltage prevents the operation at a low supplying voltage, namely, low power consumption.

For these issues, we have proposed new crystallization technique of thermal plasma jet (TPJ) and advanced micro-TPJ (μ-TPJ) with higher plasma density. Because of its simple structure and atmospheric pressure process, μ-TPJ enables low fabrication of TFT. In our previous work, grains larger than ~60 μm were formed by high-speed lateral crystallization (HSLC) using micro-thermal-plasma-jet (μ-TPJ) irradiation. In addition, we have

demonstrated a high field effect mobility of 350 cm^2/Vs with HSLC by a high scanning speed (v) of 4000 mm/s. However, random grain boundaries (GBs) were formed by HSLC. Random GBs cause characteristic variability in thin film transistors (TFTs).

In this work, we attempted to control the grain growth using μ-TPJ irradiation on a-Si patterns. This approach is promising for high performance TFT with low fabrication cost because additional and difficult process step are not necessary by applying the grain growth controlling pattern to active layer of TFT. We attempted to improve the variation issue and to operate CMOS circuit by a low voltage at a high speed. I will discuss about the practicability based on research results in this thesis.

In chapter 1, the back grounds of c-Si TFTs for fabrication of FPDs were described. The crystallization of a-Si and CMOS formation on glass substrate is required for industry.

In chapter 2, I will describe about the developments of TPJ andμ-TPJ crystallization technique. TPJ formed small grains with ~100 nm and its application to TFT fabrication was demonstrated. NMOS and PMOS TFTs was successfully operated with μ_{FE} of ~20 cm^2/Vs. While this result was promising for CMOS fabrication, the improvement of TFT performance was required. So μ-TPJ was developed to form larger size of grains. Grains with ~60 μm were formed by high-speed lateral crystallization (HSLC) after liquid phase crystallization. By applying HSCL to TFT fabrication, TFT with high μ_{FE} of 350 cm^2/Vs was achieved.

In chapters from 3 to 6, the research results are described. In chapter 3, we improved the most important issue of variation in TFTs. we have proposed a new TFT pattern which is composed of 1-μm-wide strip channels. This strip channel is effective to suppress random GBs by filtering effects. In addition, by applying this strip to channel area of TFTs, field effect mobility higher than 300 cm^2/Vs with significantly low variation were achieved. This high-performance enabled us to operate CMOS circuits. We were able to operate 8-bit shift-register at a supply voltage of 5V and a clock frequency of 4 MHz.

In chapter 4, the relationship between channel crystallinity and TFT characteristics were investigated. After eliminating random GBs, a small amount less than 1.0×10^{17} cm^{-3} of intra-grain defects were formed in channel area. In order to miniaturize TFTs, accurate control of Fermi-level is important.

In chapter 5, the mechanism of defect formation was investigated. The agglomeration of liquid Si affected to the formation of intra-grain defects. In order to suppress these defects, μ-TPJ condition was optimized. By controlling the reaching temperature of liquid Si less at most 1747 K, intra-grain was extremely suppressed.

In chapter 6, we attempted to operate short channel TFT and CMOS circuit at a very high speed. Using optimized μ-TPJ condition and strip pattern, TFTs with high μ_{FE} of 500 cm^2/Vs were achieved. A 9-stage ring oscillator fabricated with strip channel TFTs,

oscillation frequency increased to 108 MHz and the delay time decreased to 0.52 ns at a supply voltage of 5V. The cut-off frequency of 1.9 GHz was achieved by μ-TPJ crystallization technique.

From the achievement of this research, we could demonstrate the practicability of μ-TPJ crystallization technique for next generation displays in terms of the high-performance TFTs and its low process cost.

Contents

Chapter 1

Introduction

1.1 Background

1.1.1 Flat panel display

From the beginning of 2000s, flat panel displays (FPDs), such as liquid crystal displays (LCDs) and organic light emitting displays (OLEDs), have been widely in practical use for television (TVs), personal computers (PC), and mobile device. In order to drive the pixel of FPDs, an active-matrix driving method has been adopted by taking over the Cathode ray tube (CRT) in the past. FPDs, which are based on the large area electronics, have been achieved development to enlarge or dilute the size of displays. It should be noted that thin film transistors (TFTs) had contributed the remarkable development of FPDs. Hydrogenated amorphous silicon (a-Si:H) film was used for fabrication of TFTs as a switching device for pixels of a display [1-2]. By enlargement of mother glass size, a-Si:H TFTs have achieved low fabrication cost. At this moment, the 10^{th} generation glass substrate with the width of 3 m × 3 m has used for the large sized displays. It can be said that the mother glass size is limited by the width of roadway.

In resent year, however, small and middle-sized displays, such as smart phone, tablet and wearable displays, have rapidly come into wide use because of their portability. For these portable displays, high-reliability and higher-resolution than 500 pixels per inch (ppi), which is far beyond the limit resolution of human eyes, were strictly required [3]. In addition, with the object of battery operation, low-power consumption is strictly required. Instead of LCDs, organic electro-luminescence diode (OLED) displays have been developed. Because of a self-luminous device, OLED is quite promising for lower power consumption compared to LCD, which consumes away approximately 70% of a backlight.

For driving the pixels of both of LCDs and OLED displays, development of TFT is one of the most important technological issue for next generation displays.

1.1.2 Thin-film transistor

For the AM-LCDs, TFTs are connected with data lines and scanning lines as shown in Fig. 1.1. In order to drive each pixels, TFTs are required high- on/off ratio ($R_{on/off}$) of current. In the case of large sized displays, a-Si:H film is applied because of its uniform deposition, in spite of a low field effect mobility (μ_{FE}) of ~ 0.5 cm^2/Vs [1-2]. In the case of small sized displays, however, in order to achieve higher resolution, small sized TFTs are required. So in order to contain high $R_{on/off}$, alternative channel materials with higher μ_{FE} have been developed. by increase of pixel numbers and frame rate. For new channel materials, an organic TFT [4-6], oxide TFT [7-12], and crystalline Si (c-Si) TFT including

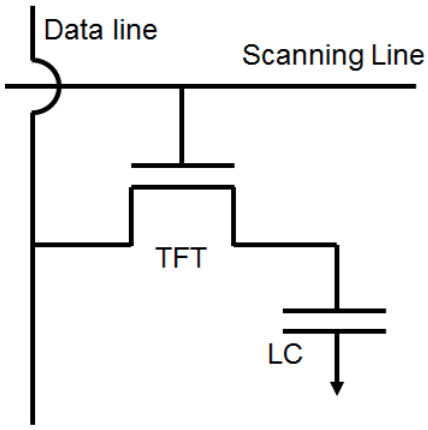

Fig. 1.1. Circuit diagram of TFT for driving pixel of LCD.

polycrystalline silicon (poly-Si) [13-43] have been studied. Above all, oxide and c-Si TFTs come into practical use.

In terms of μ_{FE} higher than 100 cm^2/Vs, high-reliability and the exclusive capability of complementary metal-oxide semiconductor (CMOS) fabrication, c-Si technology is quite promising for next generation displays with low power consumption and multi-functions.

1.1.3 Fabrication of crystalline-silicon film

The c-Si films are formed by direct deposition techniques such as low pressure chemical vapor deposition (LPCVD) [13-16], plasma enhanced CVD (PECVD) [17], sputtering [18] and reactive thermal CVD [19]. However, in order to form c-Si on a substrate, generally temperature higher than 600ºC is necessary. Because this temperature is higher than heat-resistance of glass substrate, low temperature fabrication process using rapid thermal annealing of a-Si film has developed. Excimer laser annealing (ELA) has been widely utilized. By investigation of the mechanism about crystallization by ELA, large grains with the size of several hundred nm are formed by melting and crystallizing Si films within nanosecond period [20-25]. However, because of the expensive equipment and running cost, various crystallization techniques utilizing pulsed-laser crystallization [20-25], solid-phase crystallization (SPC) [26], metal-induced crystallization [27-28], continuous-wave (CW) laser crystallization [29 - 33], flash lamp annealing (FLA) [34-35], and thermal plasma jet (TPJ)[36-40] have been studied industriously. The key research purposes for higher performance TFT is to enlarge the grain size using these crystallization techniques, including ELA [41-44]. Conventionally, large grains are formed after phase transformation of liquid phase by zone-melting recrystallization (ZMR).

However, with increase of grain size, the characteristic variability of TFTs has become critical issue instead of high-$\mu_{FE.}$ These variation and degradation of TFTs are caused by

crystal defects in channel region, such as grain boundaries (GBs) and intra-grain defects[45 - 47]. So advanced crystallization technique with the aim of the location control of GBs and termination method of defects have been developed.[48-51]

1.1.4 CMOS circuit formation on glass substrate

As mentioned in Sect. 1.1.2, c-Si TFT has a capability of CMOS fabrication and a high-μ_{FE}. The μ_{FE} higher than 100 cm^2/Vs is promising for circuit operation at a high speed, and CMOS structure is quite effective for low power consumption. These advantage enables a circuit formation on glass substrate as same as pixel area, what is called system on panel (SOP) [52-54]. By increasing the number and resolution of pixels, the number of wirings increases. In order to drive each pixels, a control circuit must be connected to wirings with a large number and narrow pitch dependent of pixels. This incurs higher fabrication cost because of the difficulty of packaging or enlargement of frame. For the small sized displays, narrow frame is strictly required in order shrink the total size.

To solve this issue, SOP technique has developed as shown in Fig. 1.2. By the formation of peripheral circuit on glass substrate, the number of wirings is extremely suppressed and narrow frame is achieved [53-54]. In addition, for the lower power consumption by low supply voltage and higher speed operation, improvement of TFT performance, such as low threshold voltage (V_{th}) and μ_{FE} higher than 300 cm^2/Vs, is required.

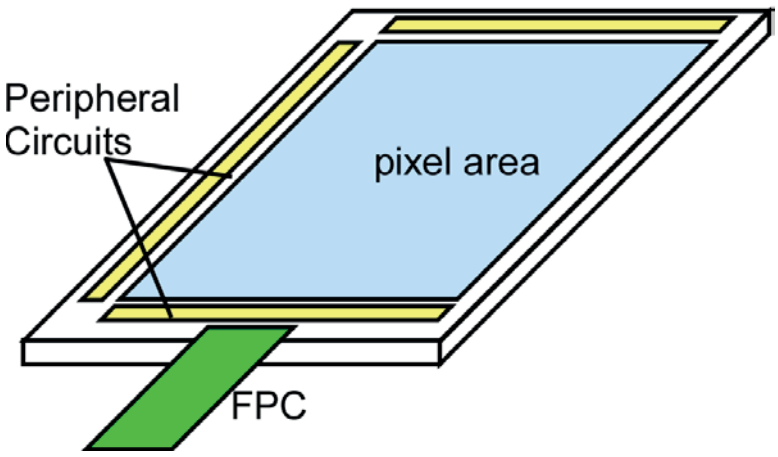

Fig. 1.2. Schematic diagram of system on panel (SOP) on glass substrate.

1.2 Overview of thesis

1.2.1 Motivation and purpose

In our previous works, we proposed the application of an atmospheric-pressure direct current (DC) arc discharge thermal-plasma-jet (TPJ) to the crystallization of a-Si films on quartz substrates. This innovative technique has been demonstrated its capability for the application to industry by its TFT performance. In addition, advanced plasma induced crystallization method of micro-thermal plasma jet (μ-TPJ), which generates higher density of plasma, has been proposed [55 - 56]. Large grains with ~60 μm were formed by μ-TPJ irradiation and demonstrated a high-performance TFT with a field effect mobility (μ_{FE}) of 350 cm^2/Vs. These high crystallinity and high-performance TFT were quite promising for the application to industry because of its cost fabrication cost. However, by increasing the grain size and TFT performance, significant issue of variability in TFTs were also stood out as same as other LTPS technique. So in this work, we forced on this variation issue, which is the most important to be practical use of μ-TPJ.

1.2.2 Components

This doctoral thesis was composed of following chapters.

Chapter 1: Introduction
Chapter 2: Fabrication of Thin Film Transistor by Micro-Thermal-Plasma-Jet Crystallization
Chapter 3: Improvement of Characteristic Variability in TFTs by Micro-Thermal-Plasma-Jet irradiation on Amorphous Silicon Strips
Chapter 4: Investigation of the Effects and Crystallinity of Strip Patterns
Chapter 5: Investigation of Intra-Grain Defect Formation in Amorphous Silicon Strips During Micro-Thermal-Plasma-Jet Irradiation
Chapter 6: High-Speed Operation of CMOS Circuit with Short Channel TFTs

In previous work, TPJ and μ-TPJ applied for the crystallization of a-Si films. These techniques for crystallization and application of TFT fabrication are introduced in Chap. 2. Experimental results and discussions were described in Chap. 3 ~ 6. In Chap. 3, the variation issue was significantly improved by the control of grain growth using μ-TPJ irradiation on a-Si strips. A new TFT pattern was proposed and demonstrated high-performance TFTs with low variation by suppressing random GBs. CMOS circuits were successfully operated at a low supplying voltage. We attempted to operate CMOS circuit at a higher speed. Our approaches are as follows. In Chap. 4, we investigated the

relationship between TFT performance and the channel crystallinity. A small amount of defects were still formed in crystallized channels while GBs were eliminated out. It was extremely important to control the Fermi level as same as single-crystalline silicon because of its high crystallinity. In addition, higher crystallinity channel was required for short channel TFTs. So we focused on intra-grains in crystallized Si. In Chap. 5, the mechanism of intra-defects formation was investigated and improved crystallization method of μ-TPJ. The control of properties of liquid Si is important to suppress the intra-grain defects. In Chap. 6, we attempted CMOS circuit at a very high speed based on the results in Chap. 3 to 5. It should be noted that the most important approach for high performance TFT was based on crystallization.

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Chapter 2

Fabrication of Thin Film Transistor by Micro-Thermal-Plasma-Jet Crystallization

2. 1 Application of TPJ irradiation to TFT fabrication

An excimer laser annealing (ELA) has been utilized as a crystallization technique of amorphous Si (a-Si) film as mentioned in Sect. 1.1.3. However, a lower cost crystallization technique is required for the large area electronics because of the high fabrication cost by ELA. We proposed the application of an atmospheric-pressure direct current (DC) arc discharge thermal plasma jet (TPJ) to the millisecond crystallization of a-Si films on quartz substrates [1-5]. Schematic diagram of TPJ crystallization is shown in Fig. 2.1. An anode and a cathode electrodes were made from copper (Cu) and tungsten (W), respectively. Arc discharge was generated by supplying DC power (*P*) between an anode and a cathode electrodes. TPJ was generated by blowing out the thermal plasma using Argon (Ar) gas thorough the orifice (Φ) of 4 mm in a diameter. Ar gas flow rate and the distance between substrate and TPJ are shown by *f* and *d*, respectively. The substrate was lineally moved by a motion stage with a scanning speed (*v*) in front of TPJ.

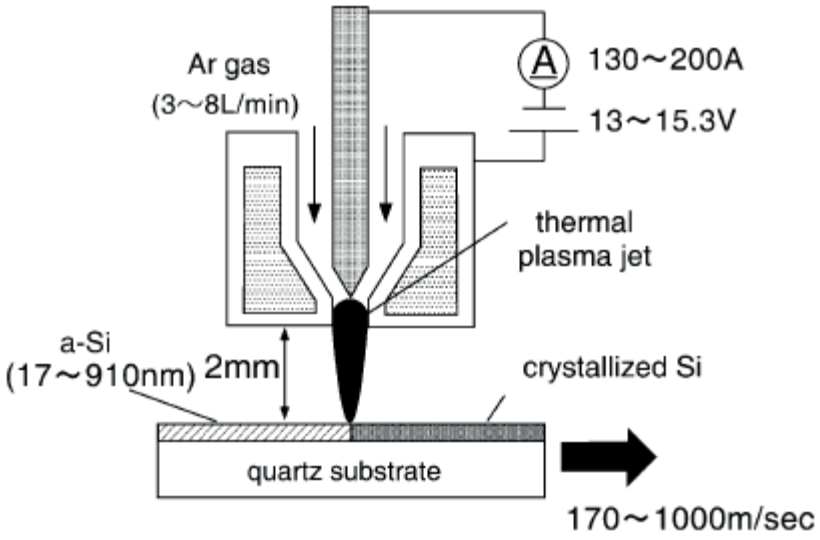


Fig. 2.1. Schematic diagram of crystallization of a-Si films on quartz substrate by TPJ irradiation. The TPJ is formed by blowing out the Ar arc plasma through a 4 mm Φ nozzle [5].

Figure 2.2 shows the Raman scattering spectra of crystallized Si film by TPJ irradiation with different *v*. As shown in Fig. 2.2 (a), the c-Si transversal optical (TO) phonon peak appears after TPJ crystallization. By decreasing *v*, the full width at half maximum (FWHM) gradually decreased and the peak positions were close to the single c-Si at 520 cm^{-1} (Fig. 2.2 (b)). From these results, the crystallinity of Si film was improved by TPJ crystallization with slow *v* because of the higher temperature conditions by long annealing duration.

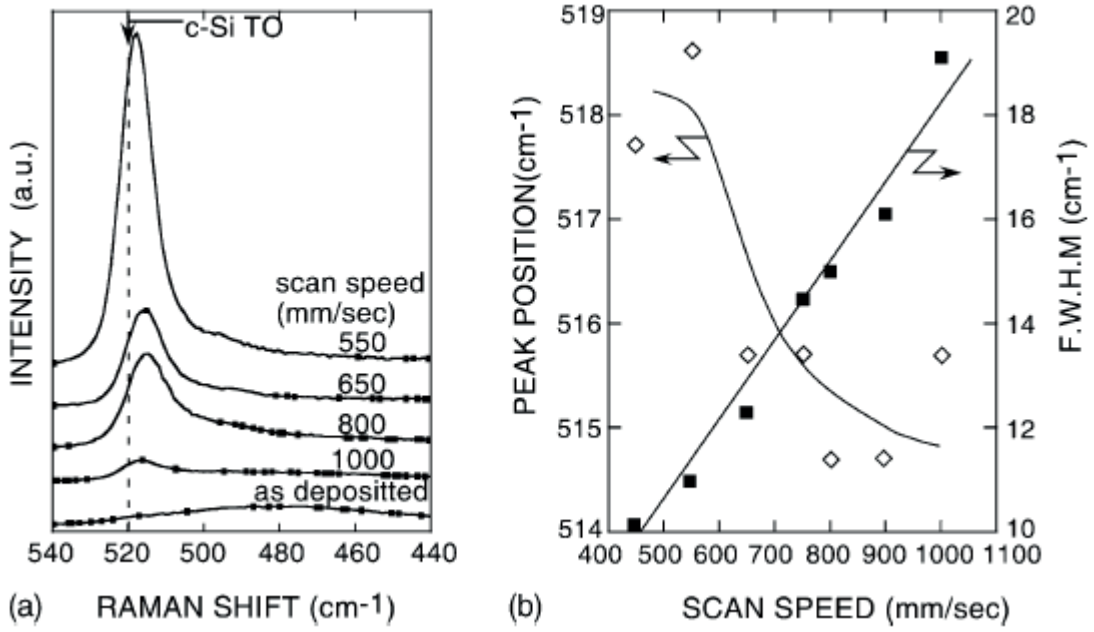


Fig. 2.2. (a) Raman scattering spectra of Si films crystallized by TPJ irradiation with different *v*. (b) FWHM and position of the c-Si TO phonon peaks. The Si film thickness is 80 nm, and *P* is ~2.4 kW [5].

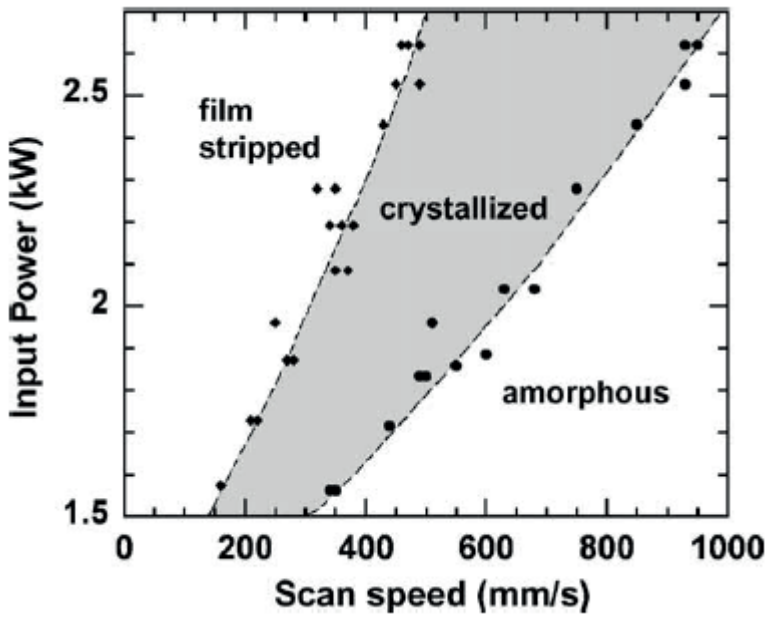


Fig. 2.3. . Phase diagram of the Si film after the crystallization as functions of *P* and *v*. With increase of *P*, a-Si films are crystallized at higher *v* and the process window becomes larger. However, the film stripping was facilitated with decreasing *v*. [2]

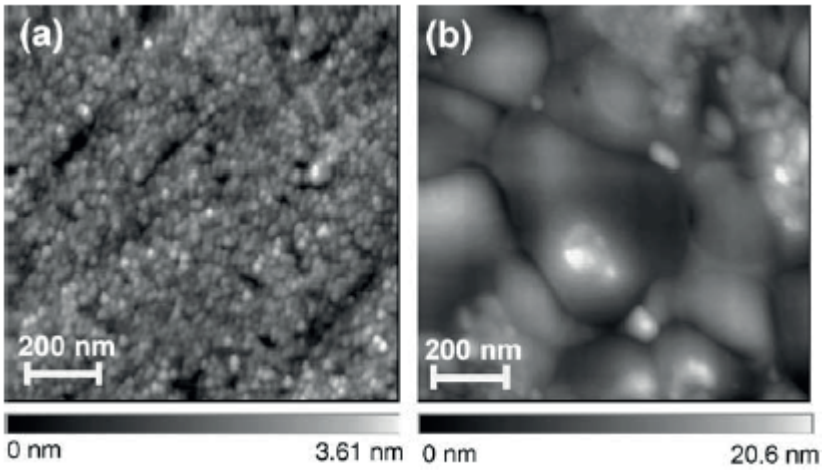


Fig. 2.4. . AFM images of 20-nm-thick Si films crystallized in (a) SPC and (b) LPC modes. Typical grain sizesof (a) and (b) were 20 to 30 nm and 300 to 600 nm,respectively.[2]

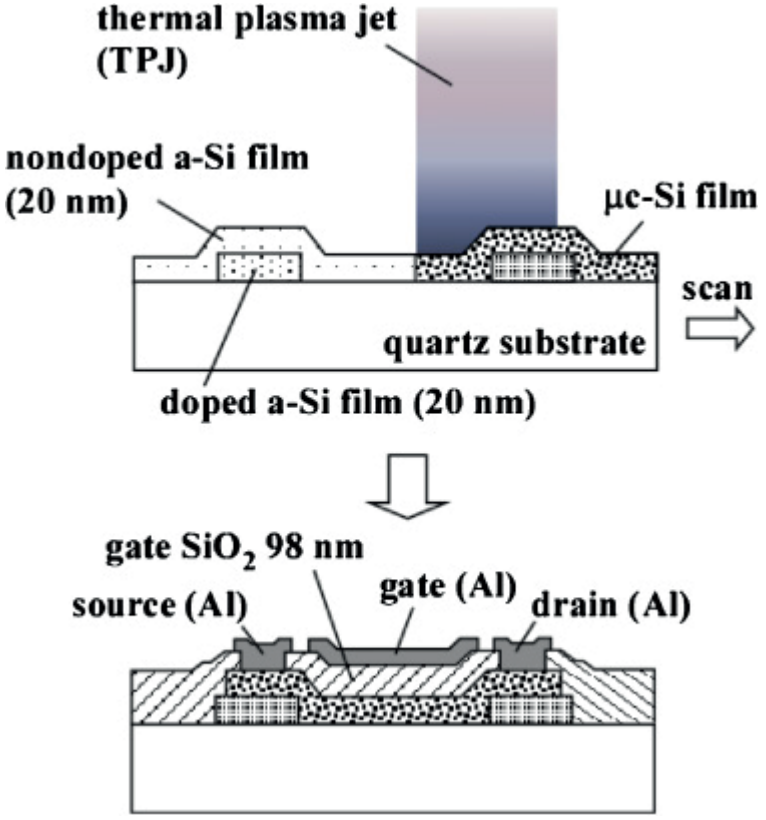


Fig. 2.5. . Schematic diagram of TFT fabrication process using TPJ crystallization.[5]

As shown in Fig. 2.3, by increasing *P*, a-Si films are crystallized at higher *v* and the process window becomes larger. However, the film stripping was facilitated with a

decrease in the v down to a certain value. The surface morphology by atomic force microscopy (AFM) of the Si film crystallized in solid phase crystallization (SPC) show fine grain structure with the typical size from 20 to 30 nm, while that of the film crystallized in liquid phase crystallization (LPC) mode show much larger grain structure with typical size around 300 to 600 nm, as shown in Figs. 2.4 (a) and (b). The surface roughness increased from 0.5 to 3.4 nm in RMS value. These results suggest that large grains are formed by LPC conditions. In this experiment, however, the process window of LPC was extremely narrow and silicon films ware easily stripping with LPC condition because dehydrogenation was not carried out before crystallization. Moreover, the grain size was still under submicron.

In addition, thin-film transistors (TFTs) with a top-gate structure were formed using SPC film by TPJ crystallization. The process steps were as follows (Fig. 2.5) [5]. Phosphorus-doped a-Si films with a thickness (t_{Si}) of 20 nm were deposited by plasma-enhanced chemical vapor deposition (PECVD) on quartz substrate. After formation of source (S) and drain (D) regions by chemical dry etching (CDE), non-doped a-Si films with t_{Si} = 20 nm were deposited by PECVD at 250ºC. TPJ was irradiated for crystallization and dopant activation simultaneously. TPJ crystallization was performed with P = 2.3 kW, d = 2 mm, and v = 350 – 550 mm/s. After etching the Si layer to form S, D, and channel (C) by CDE, a 98-nm-thick gate SiO_2 was deposited at 300ºC by remote-PECVD. After formation of contact holes, gate (G), S, D electrodes were formed by aluminum (Al) evaporation and wet etching. Post metallization annealing was performed at 250ºC for 1 h in clean room air ambient.

The transfer characteristics by 50 TFTs with channel length (L) and channel width (W) of 10 μm were measured. Figure 2.6 shows TFTs crystallized by v = 350 mm/s and the characteristics of μ_{FE}, threshold voltage (V_{th}), and swing factor (S) were summarized in Fig. 2.7. TFT performance was observed from output and transfer characteristics. When lower V_d, a trans-conductance (g_m) and I_d can be described as [6]

$$g_m = \frac{\partial I_d}{\partial V_g} = \mu_{FE}\frac{W}{L}c_i V_d, \tag{2.1}$$

$$I_d = \mu_{FE}\frac{W}{L}c_i\left(V_{th} - V_g\right)V_d. \tag{2.2}$$

Here, W and L are channel width and length, respectively. The c_i is capacitance per unit area of gate SiO_2. By using Eqs. (2.1) and (2.2), μ_{FE}, V_{th}, sub-threshold swing value (S) can be estimated by equation as

$$\mu_{FE} = \frac{g_m}{\frac{W}{L}c_i V_d}, \tag{2.2}$$

$$V_{th} = V_g - \frac{I_d}{\mu_{FE}\frac{W}{L}c_i V_d}. \tag{2.4}$$

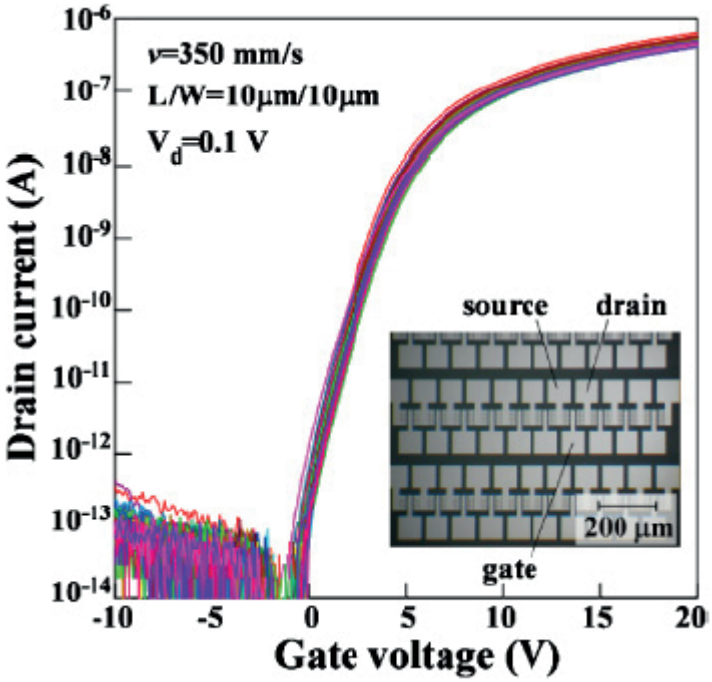


Fig. 2.6. . Transfer characteristics of 50 TFTs superimposed in the graph. The inset shows a photograph of the TFTs [5].

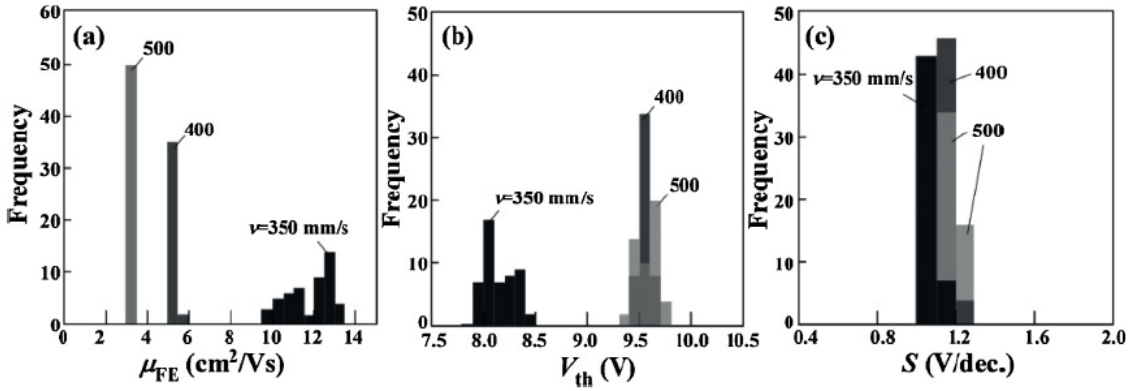


Fig. 2.7. Histograms of characteristics of TFTs fabricated with v = 350, 400, and 500 mm/s.[5]

$$S = \ln 10 \frac{\partial V_g}{\partial \ln I_d}. \tag{2.5}$$

By decreasing v, the average μ_{FE} increased from 3.3 to 12.1 cm^2/Vs. At v = 350 mm/s, the variation in μ_{FE}, V_{th}, and S were within 1.06 (± 4.4%), 0.14 (± 1.1%), and 0.04 (± 4.0%). These small variations were achieved because SPC-Si films were formed by microcrystalline Si (μc-Si) with the size of ~20 nm. These results indicate that TPJ crystallization of a-Si film is quite promising for fabrication of TFTs.

2.2 Noncontact temperature measurement of TPJ irradiation

We have developed a direct observation technique for the temperature distribution in the quartz substrate during TPJ irradiation [7-8]. A transient reflectivity measurement was applied to measure the temperature as shown in Fig. 2. 8. The transient reflectivity during TPJ annealing was measured by irradiating the quartz substrate with a He-Ne laser (633 nm) from backside of the substrate and detecting the reflected light intensity using a photodiode through a band pass filter (root A in Fig. 2.18). Root B using an yttrium aluminum garnet (YAG) laser (532 nm, 10 mW) was used to investigate phase transformation of Si films. The transient reflectivity is oscillated by the interface of the incident light multiply reflected as shown in the inset of Fig. 2.8. The oscillation was reproduced by numerical simulations on heat diffusion and optical interference. The simulation has been based on two-dimensional heat diffusion equation shown as

$$\frac{\partial T}{\partial t} = \frac{\kappa}{\rho c_p}\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2}\right) + \frac{S}{\rho c_p} - \alpha(T - T_0)\ . \qquad (2.6)$$

Here, x and y are positions along TPJ scanning direction and depth from substrate surface, respectively. Temperature (T) at each position and time (t) is obtained from Eq. 2.6 using

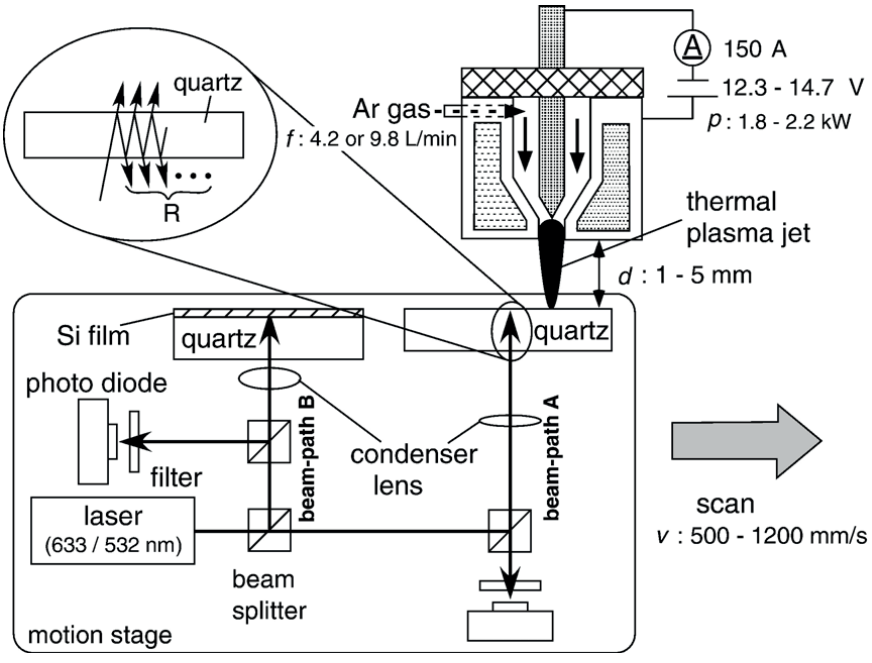


Fig. 2. 8. Schematic diagram of experimental set up for the temperature measurement. The optical beam paths A and B are used to measure the temperature profile in the substrate and phase transformation of Si films, respectively. [7]

thermal conductivity (κ), density (ρ), and specific heat (c_p) of quartz with considering temperature dependence. S, α, and T_0 are the thermal incidence, heat dissipation factor and ambient temperature, respectively. Then, the TPJ profile has been assumed by two-dimensional Gaussian power profiles, and the TPJ width and effective power transfer efficiency to quartz substrate ware used as parameters for fitting the numerical and experimental data. Two transient reflectivity measured and simulated with different v were shown in Fig. 2.19. From the figure, simulated reflectivity corresponded with measured reflectivity at all v. At the simulation, surface temperature and temperature distribution can be reproduced well as shown in Fig. 2.10. The substrate surface temperature increased with the decrease in v, and heated depth over 1000 K was within several 10 μm in this experiment. The margin of error by this temperature measurement technique is less than 30 K, which is confirmed by the comparison between temperature and transient reflectivity of Si film measured from root B in Fig. 2.18 [7]. In, addition, this technique has been also applied to Si wafer and conventional glass substrate [9-10].

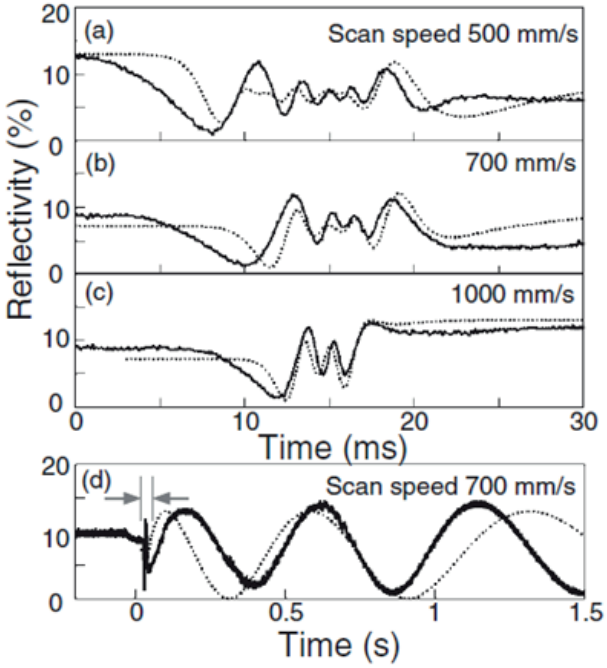


Fig. 2.9. Measured transient reflectivity (solid lines) and simulated reflectivity (dotted lines) of quartz substrate when plasma jet was scanned at different v. A long-term oscillation is shown in (d), where the period indicated by arrows corresponds to the period in (a) to (c). [7]

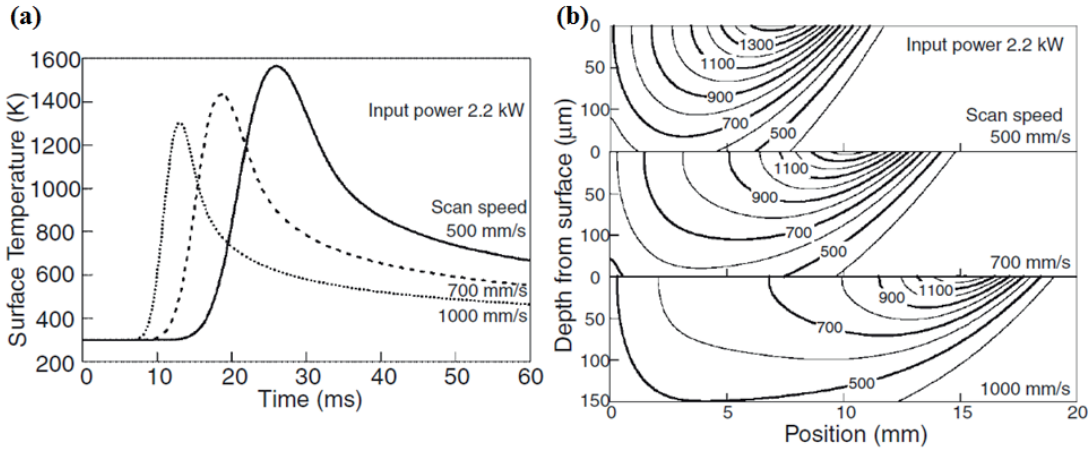


Fig. 2.10. (a) Surface temperature and (b) two-dimensional temperature profile under different annealing conditions obtained by analysis. The numerals indicate temperatures in the unit of K. [7]

2.3 Fabrication of NMOS and PMOS TFTs

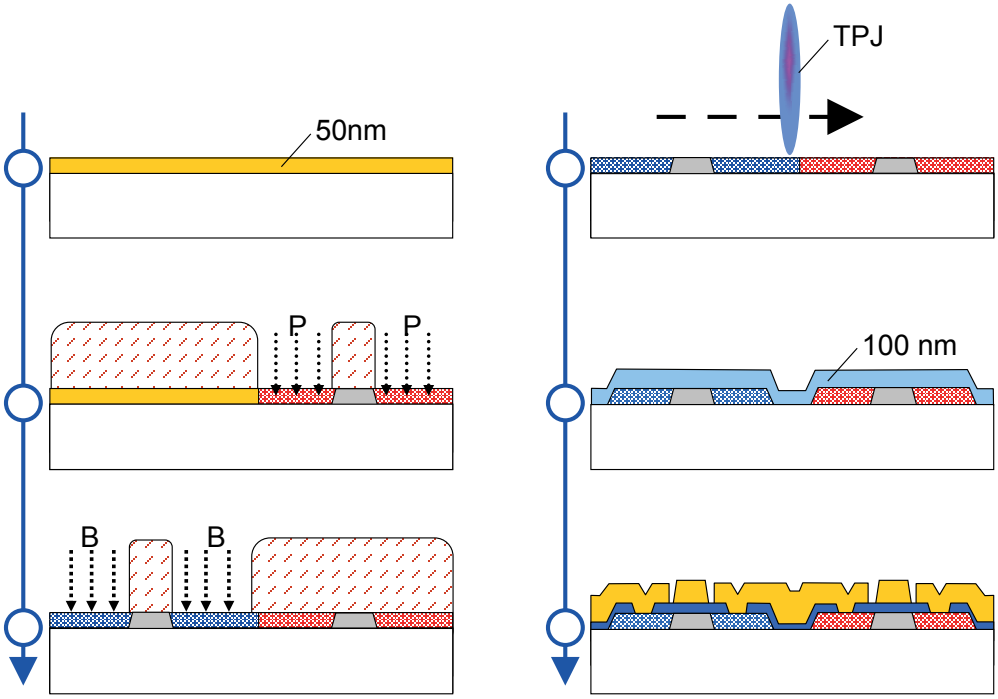


Fig. 2.11. The process steps for fabrication of NMOS and PMOS TFT using ion implantation and TPJ crystallization.

In order to fabricate CMOS circuit, both of NMOS and PMOS should be fabricated on the same substrate. In this section, NMOS and PMOS characteristics by TPJ crystallization were investigated. The process steps were modified as follows (Fig. 2.11)

In order to distinguish NMOS and PMOS region, impurity doping method by ion implantation was applied instead of depositing a doped-Si film. A 50-nm-thick non-doped a-Si was formed on quartz substrate by PECVD at 250ºC. Using photolithography, Phosphorus (P^+) and Boron (B^+) ions were implanted at the dose of 3.2×10^{15} cm^{-2} on the S/D areas of NMOS and PMOS regions, respectively. Then TPJ was irradiated to crystallize channel region and to activate S/D region, simultaneously. TPJ condition was f = 7.0 L/m, d = 3 mm, P = 2.25 kW, and v = 350 mm/s. After formation of TFT pattern with S/D and C by CDE, gate SiO2 with the thickness of 100 nm was formed by remote-PECVD at 300ºC. After formation of contact holes, Al-Si (1%) electrodes were formed by DC sputtering and wet etching. Finally, PMA was performed at 250ºC in the clean room air ambient. The highest temperature of this process steps was 400ºC during a-Si deposition.

As shown in Fig. 2.12, NMOS and PMOS TFTs were successfully operated. The μ_{FE} and

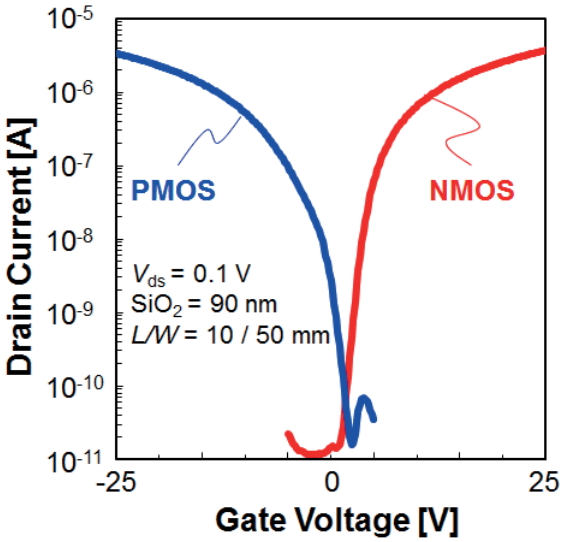


Fig. 2.12. Transfer characteristics of NMOS and PMOS TFTs using TPJ crystallization.

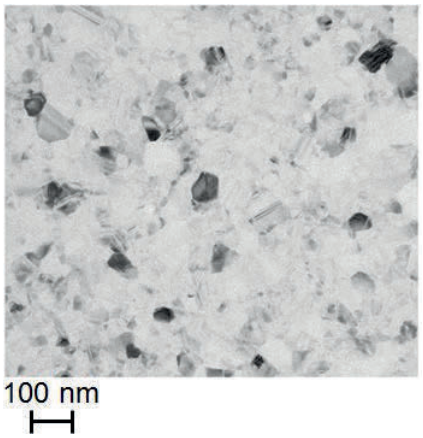


Fig. 2.13. . Plane-view TEM image of crystallized Si film with v = 350 mm/s.

V_{th} were 19 cm^2/Vs and 11 V by NMOS, respectively. They were 17 cm^2/Vs and 11 V by PMOS, respectively. From these results, TPJ crystallization was promising for CMOS operation on glass substrate. Figure 2.13 shows plane-view transmission electron microscopy of crystallized Si film with v = 350 mm/s. In this TPJ condition, grains with the size from 50 to 100 nm were easily formed by SPC. However, LPC condition was hardly controlled because molten Si film was almost stripped or agglomerated.

Unfortunately, however, taking account of practical application to CMOS circuit operation, higher μ_{FE} and lower V_{th} are strictly required. Enlargement of grain size is one of the research purpose to improve these TFT performance. So a new crystallization method using plasma induced annealing to form higher crystallinity Si, such as LPC, was required.

2. 4 High-speed lateral crystallization by micro-thermal plasma jet irradiation

In order to fabricate higher performance TFTs using TPJ technique, the method to achieve high power density plasma was introduced [11 - 12]. Figure 2.14 shows the special profiles of TPJ and introduced micro-TPJ (μ-TPJ). By reducing (Φ) and increasing the spacing between anode and cathode (*ES*), the power density was further increased. The FWHM and the power profile were reduced from 3.4 to 1.2 mm and the peak power density transferred to a substrate increased from 8.3 to 53.2 kW/cm^2 by decreasing Φ from 4.0 to 0.8 mm and increasing *ES* from 1.0 to 2.0 mm. These results suggest that the μ-TPJ can efficiently anneal the substrate surface by transmitting the heat by high-temperature gas stream with high power density.

Figure 2.15 shows the application of μ-TPJ to crystallization of a-Si film. A 100-nm thick a-Si film was crystallized by μ-TPJ irradiation with v = 2000 mm/s after dehydrogenation. By optical microscope observation, dendritic morphology was observed, which indicates the grain growth by lateral solidification after phase transformation of liquid phase. By scanning electron microscope observation after secco etching, the grain size was ~5 μm in the width and ~60 μm in the length (Fig. 2.16). These large grains were formed by a strong lateral temperature gradient by high speed scanning speed of melting region. Therefore, we

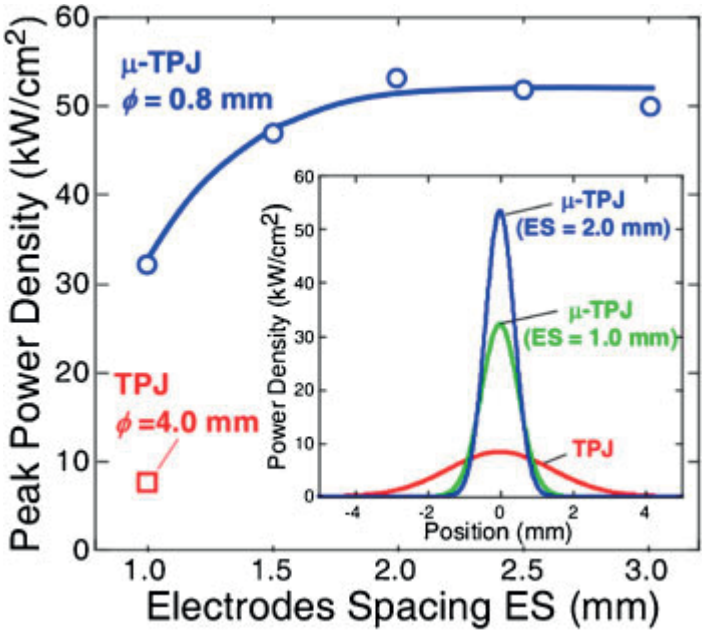


Fig. 2.14. Peak power density transferred from plasma jet to substrate surface as a function of *ES* from 1.0 to 2.0 mm and Φ from 4.0 to 0.8 mm during TPJ or μ-TPJ irradiation. [11]

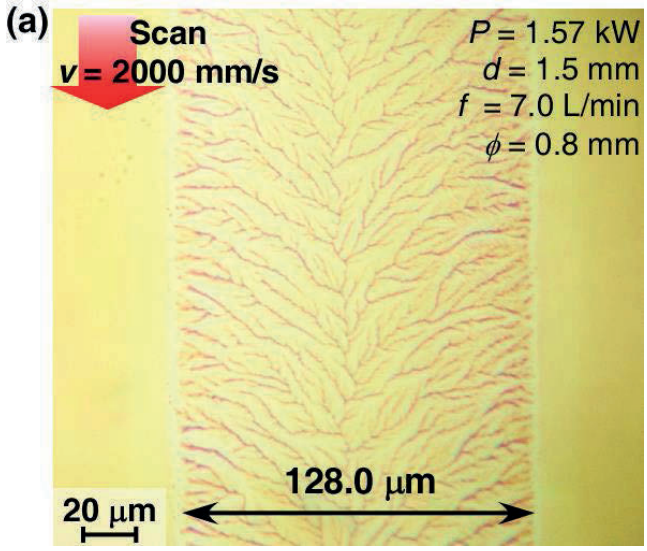


Fig. 2.15. Optical microscope image of Si film after μ-TPJ irradiation with HSLC condition [12].

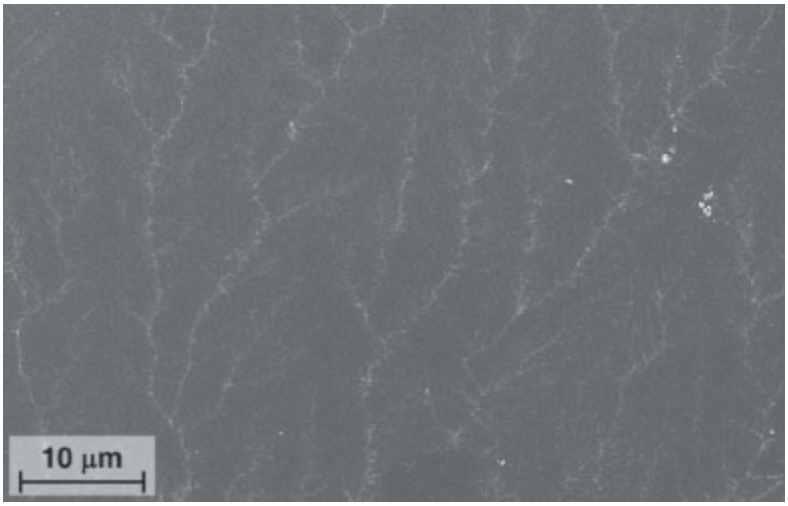


Fig. 2.16. SEM image of crystallized Si film using μ-TPJ irradiation after secco etching [12].

called this growth method high-speed lateral crystallization (HSLC).

Moreover, the grain growth during μ-TPJ irradiation was investigated by *in-situ* observation using high-speed camera (HSC) [13 - 14]. Figure 2.17 shows the schematic diagram of *in-situ* observation during μ-TPJ irradiation on a-Si film. A 100-nm thick a-Si film was formed on quartz substrate by PECVD at 250ºC. Then dehydrogenation was carried out at 450ºC for 1h. The μ-TPJ was generated under atmospheric pressure with P = 1.1 kW, d = 1.5 mm, f = 2.8 L/min, and v = 800 mm/s. For *in-situ* observation of grain growth, an optical microscope and an HSC were set on the motion stage in the backside of the substrate. The frame rate (f_r) was set to 1600 frames per second (fps).

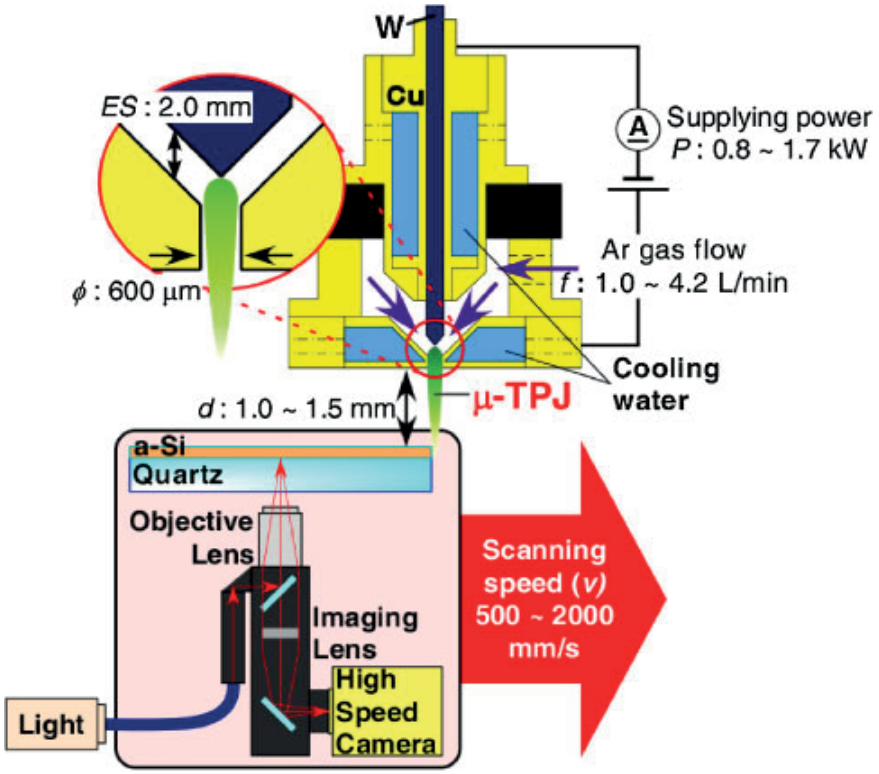


Fig. 2.17. Schematic diagram of *in-situ* observation during μ-TPJ irradiation.

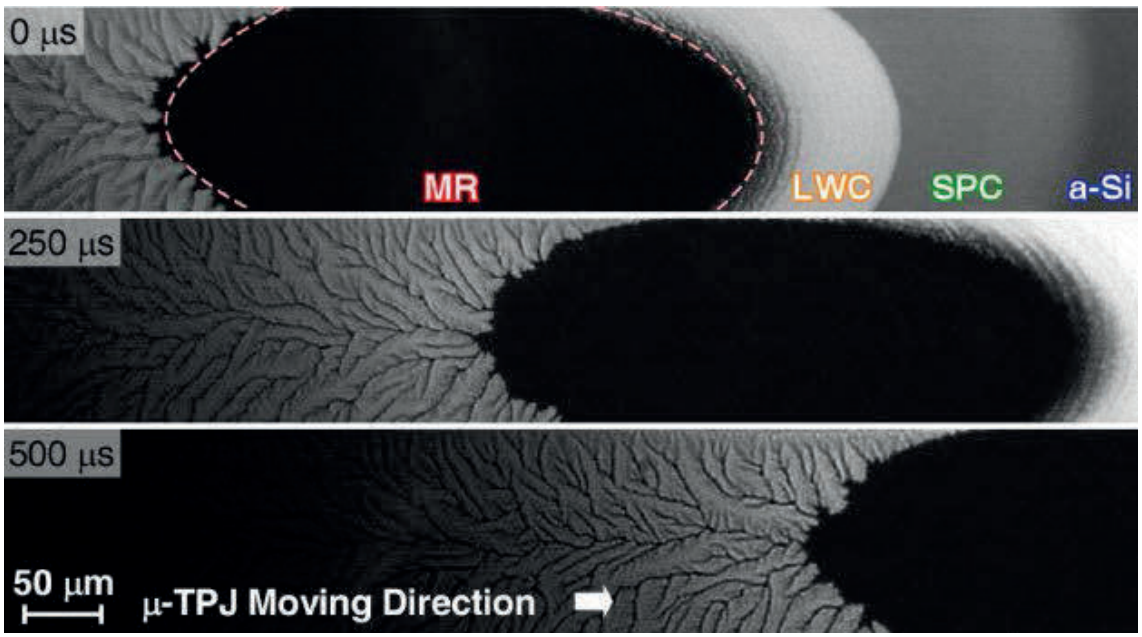


Fig. 2.18. Snapshot of the high-speed camera movie during μ-TPJ irradiation. After phase transformation from a-Si, SPC to LWC, HSLC was formed from molten region (MR) [13].

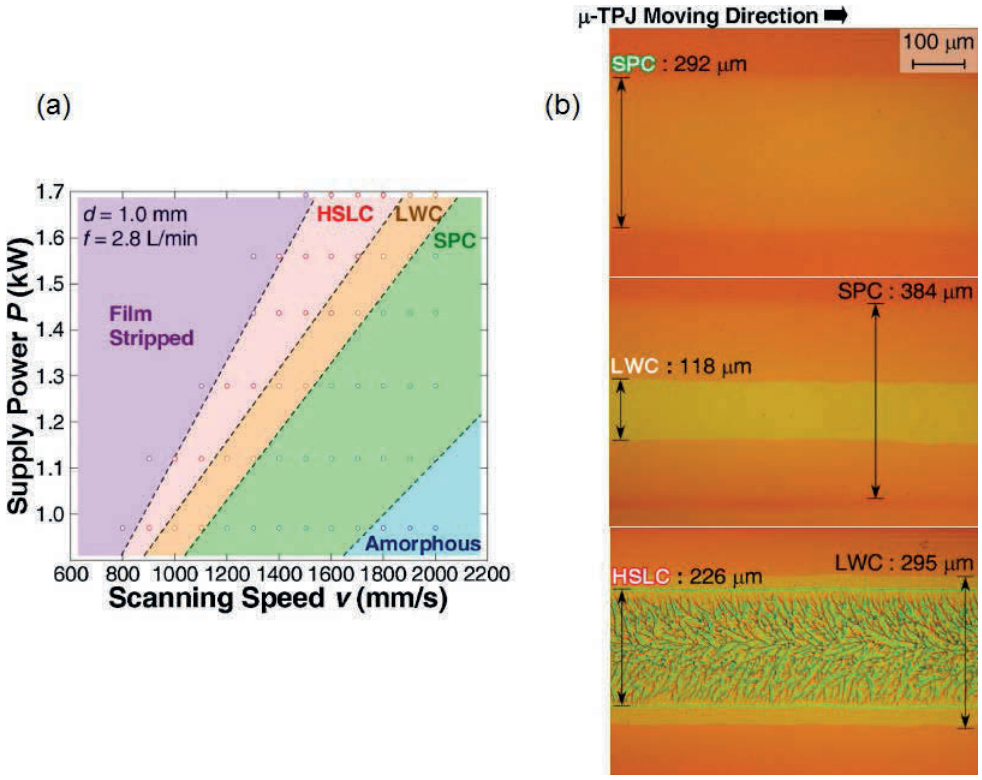
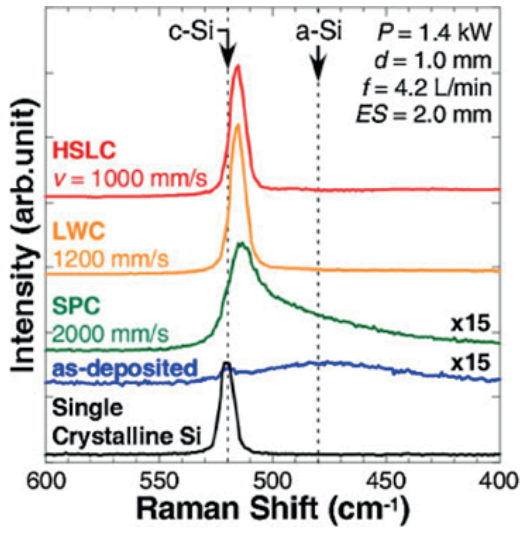


Fig. 2.19. (a) Crystallization mode with respect to μ-TPJ crystallization condition by *P* and *v*. (b) Optical microscope images of SPC, LWC and HSLC, respectively [14].



	Peak position (cm^{-1})	FWHM (cm^{-1})	R_C (%)
HSLC	515.5	7.9	100
LWC	515.4	7.2	100
SPC	510.4	21.5	70
a-Si	479.0	88.8	0
c-Si	520.0	7.1	100

Fig. 2.20. Peak position and FWHM of c-Si TO phonon peak and crystallinity of crystallized Si films shown in Fig. 2. 19[14].

Figure 2.18 shows the snapshot by HSC. The molten region was observed as black due to high reflectivity of liquid-Si (*l*-Si). In front of the molten region, the transformation from

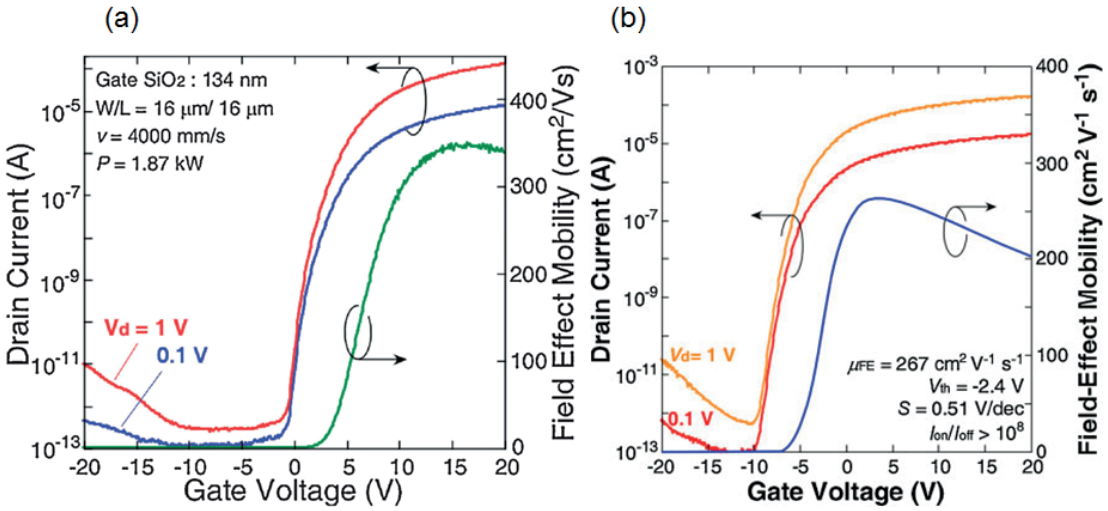


Fig. 2.21. Transfer characteristics of TFTs on (a) quartz substrate and (b) glass with buffer SiO_2 layer substrate [16].

a-Si, SPC, to periodic and repeating wavy crystallization were observed. The explosive crystallization (EC) [15] like mode was named leading wave crystallization (LWC) [13-14]. The driving force of EC is generally the released latent heat at the liquid-amorphous interface [13-15]. In the case of LWC, EC propagates into SPC region, which has less latent heat because the melting point of a-Si and SPC-Si is different [13-14].

As shown in Figs. 2.19(a) and (b), the crystallization modes of SPC, LWC and HSLC were successfully controlled by the combination of P and v. The crystalline volume fractions of each crystallization mode were estimated from Raman scattering spectra, as shown in Fig. 4.20. The SPC shows a crystalline volume fraction (R_c) of almost 70%. This result suggests that a substantial amount of a disordered structure or amorphous component remains in the SPC region. On the other hand, both of LWC and HSLC showed an R_c of almost 100%. These results suggest that the melting points of LWC- and HSLC-Si are identical to that of single-crystalline Si (T_m). From these results we concluded that HSLC is induced by melting almost single crystalline Si after phase transformation of SPC and LWC.

Furthermore, μ-TPJ crystallization with HSLC was applied to TFT fabrication [10, 16]. In order to demonstrate its practicability, TFTs were fabricated on quartz and glass substrate. Figure 2.21(a) shows the transfer characteristics of NMOS TFT fabricated by HSLC film on quartz substrate. TFT showed extremely high μ_{FE} of 350 cm^2/Vs and low S. On the other hand in the case of glass substrate, the crack generation was frequently occurred by HSLC of a-Si film on glass substrate. However, they were significantly suppressed by the inter SiO_2 buffer layer between a-Si and substrate. As shown in Fig. 2.21(b), TFT with high μ_{FE} of 267 cm^2/Vs was successfully fabricated on glass substrate with 500 nm thick

of SiO_2 buffer layer.

From these results, μ-TPJ crystallization technique is quite promising for high-performance TFT fabrication because of its practicability with low cost and low temperature process.

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Chapter 3

Improvement of Characteristic Variability in TFTs by Micro Thermal Plasma Jet irradiation on Amorphous Silicon Strips

3.1 Introduction

As described in Sect 2.1, grains larger than ~60 μm were formed by high-speed lateral crystallization (HSLC) using micro-thermal-plasma-jet (μ-TPJ) irradiation. In addition, we have demonstrated a high field effect mobility of 350 cm^2/Vs with HSLC by a high scanning speed (v) of 4000 mm/s [1]. However, random grain boundaries (GBs) were formed by HSLC on continuous amorphous silicon (a-Si) films. Random GBs cause characteristic variability in thin film transistors (TFTs)[2 - 4]. So the improvement of characteristic variability of TFTs is one of the greatest challenge for crystalline silicon (c-Si) TFTs. For this variability issues, we have attempted to control the grain growth by μ-TPJ crystallization of a-Si pattern. This method is very simple and easy to apply TFT fabrication without additional process steps.

In this section, we concluded that μ-TPJ irradiation on a-Si strip patterns was quite effective to control grain growth and a new TFT channel pattern is proposed. Additionally, we improved variability in TFTs and attempted to operate CMOS circuits at low supply voltage.

3.2 Experimental procedure

3.2.1 Grain growth control using a-Si strip patterns

The a-Si films with a thickness of 50 nm were formed on quartz substrates by plasma-enhanced chemical vapor deposition (PECVD), followed by dehydrogenation at 450 °C for 1 hour. Subsequently, a-Si patterns were formed by chemical dry etching (CDE). μ-TPJ source used for the crystallization of a-Si films is schematically shown in Fig. 3.1. Thermal plasma was generated by DC arc discharge under atmospheric pressure with supplying DC power (P) of 1.6 kW between the anode and cathode electrodes with the spacing (ES) of 2.0 mm with an Ar gas flow (f) of 3.0 L/min. The μ-TPJ was formed by blowing out the arc plasma through an orifice (Φ) of 0.6 mm in diameter. The distance to the substrate was kept at 1.5 mm away from the plasma source and the substrate was linearly translated in front of the μ-TPJ with a scanning speed at 1600 mm/s. In this condition, ~100 μm wide molten zone is formed and rapid lateral re-crystallization was induced by the rapid movement of molten Si. Here, we formed several a-Si patterns. First, lines and spaces from 1 to 10 μm wide patterns were formed. Their crystallinity was investigated by scanning electron microscope (SEM) after secco etching. From these results, a new TFT pattern for location control of grain growth was proposed. Two types of TFT patterns were formed to evaluate grain growth in a-Si pattern: (1) conventional TFT

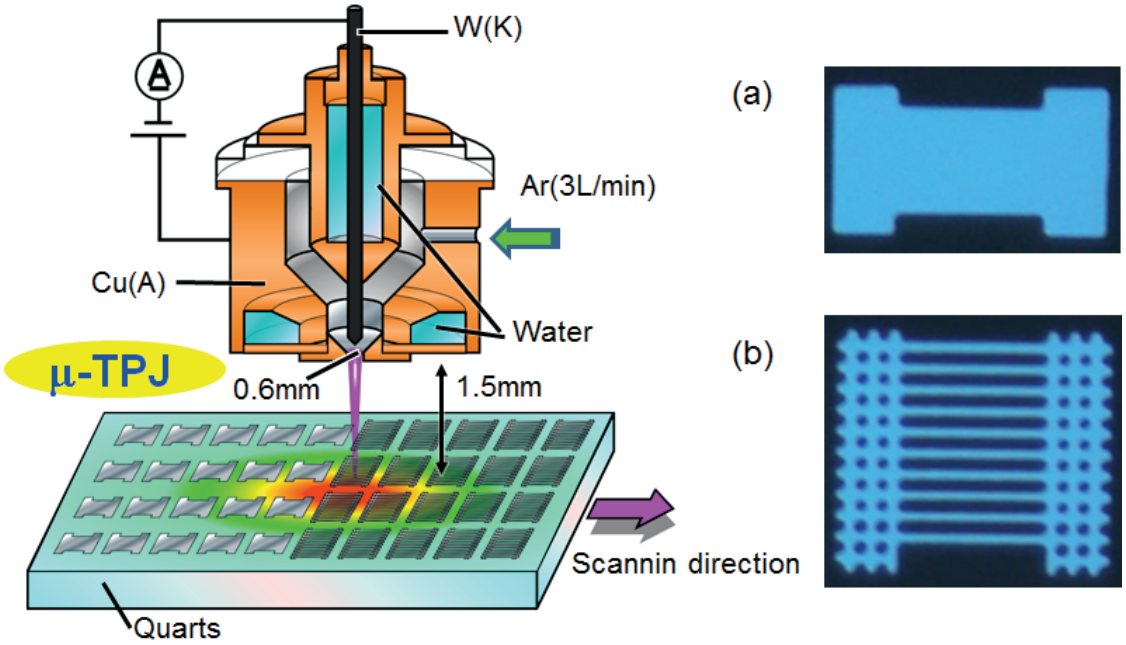

Fig. 3.1. schematic diagram of μ-TPJ irradiation on on a-Si patterns. (a) conventional TFT pattern with L/W = 10/10 μm, and (b) 1 μm-wide strip TFT pattern with L/W = 10/1 × 10 lines.

pattern with the channel length (L) and width (W) of 10 μm is shown in Figs. 1(a) and (2) our proposed pattern with L = 10 μm and W = 1 μm times 10 lines is shown in Fig.1(b), respectively. The proposed pattern was formed by 1μm wide strips, not only in the channel area but also in the source and drain area. For evaluation, crystallographic orientations and GBs were investigated by the electron-backscattering-diffraction (EBSD) method.

3.2.2 In-situ observation of grain growth in a-Si patterns during μ-TPJ irradiation

Un-doped a-Si film with the thickness (t_{Si}) of 100 nm was formed on quartz substrate by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 and H_2 at 250ºC. Dehydrogenation was carried out in N_2 ambient at 450ºC for 1 hour. Then a-Si was patterned by chemical dry etching (CDE). μ-TPJ was generated by DC arc discharge under

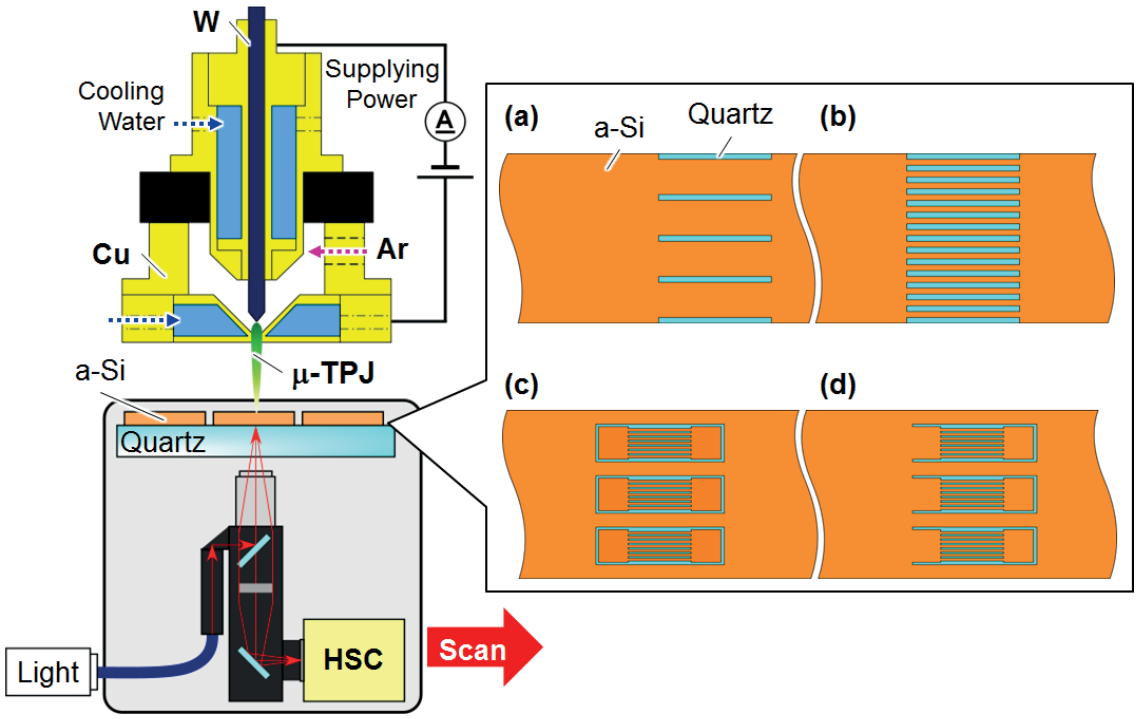

Fig. 3.2. The schematic diagram of experimental set up for the in-situ observation of grain growth during μ-TPJ irradiation on a-Si patterns. The observed patterns are as follows: slit patterns with (a) W =10 μm and (b) W =3 μm, and (c) isolated and (d) continuous TFT patterns with 1 μm wide strip channel.

atmospheric pressure with a supplying power (P) of 1.1 – 1.3 kW between a W cathode and Cu anode separated by 2.0 mm. The Argon gas flow rate (f) was 1.0 L/min. μ-TPJ was formed by blowing out the thermal plasma through an orifice with a diameter of 600 μm. The substrate was linearly moved by a motion stage in front of the μ-TPJ with a scanning speed (v) ranging from 800 to 1600 mm/s. The distance between the plasma source and substrate (d) was kept at 1.0 mm. For the *in-situ* observation of grain growth of a-Si patterns during μ-TPJ irradiation, an optical microscope and an high-speed camera (HSC) were set on the motion stage in back of the substrate (Fig. 3.2) [5 - 6]. The frame-rate (R_f) was varied from 25000 to 50000 frames per second (fps).

The a-Si patterns used in this experiment are schematically shown in Figs. 3.2(a) to (c). First, slit patterns with 10 μm and 3 μm were formed in order to compare grain growth with respect to pattern width (Figs. 3.2(a) and (b)). Secondly, the application of strip pattern to TFTs was investigated. Taking into account of fabrication process steps, it is practical to crystallize isolated patterns with source (S), channel (C) and drain (D) of TFT. In this work we defined TFT pattern as an isolated pattern with S, C, and D in the Si layer. For comparison, we formed isolated and continuous TFT patterns (Figs. 3.2(c) and (d)), and grain growth was observed. After crystallization of these patterns, crystallographic orientation and the kind of grain boundaries in observed area were investigated by EBSD.

3.2.3 Fabrication of CMOS-TFTs with strip channel

We fabricate CMOS TFTs with the self-aligned top-gate structure. First, the a-Si film with a thickness of 50 nm is formed on quartz substrate by PECVD at 230 °C, followed by dehydrogenation at 450ºC in N_2 ambient for 1 h. The channel (C), source (S), and drain (D) are patterned by photolithography and CDE as shown in Figs. 3. 1(a) and (b). Then, a-Si patterns were crystallized only in the area of TFTs by μ-TPJ irradiation in order to increase throughput of fabrication process. The a-Si patterns were crystallized under same condition of above mentioned. Subsequently, the gate-SiO_2 with a thickness of 50 nm was deposited by remote PECVD at 300 °C [7], and poly-Si gate electrode with a thickness of 250 nm was formed by low pressure CVD (LPCVD) at 520 °C. The gate electrodes were patterned using photolithography and CDE. Afterwards, the photoresist was used as an implantation mask for NMOS and PMOS regions, respectively. Then 6.2×10^{15} cm^{-2} phosphorus ions and boron ions were implanted at 55 and 67 keV, respectively, to form the self-aligned gate (G), S, and D. Next, the μ-TPJ is used to activate dopants [8 - 9], with P = 1.5 kW and v = 2000 mm/s. Under this condition, Si films were not melted, rather, dopant activation was achieved by rapid annealing [10]. After formation of the 650 nm passivation layer by atmospheric pressure CVD (APCVD), the contact holes were formed

by photolithography and wet etching. Al-Si (1%) wires were formed by DC sputtering and patterned by photolithography and wet etching. Finally, CMOS transistor fabrication was completed by high pressure H_2O vapor annealing (HWA) at 260ºC in 1 MPa for 6 h [11 -12]. The maximum temperature of fabrication process was 520ºC in gate a-Si deposition.

3.2.4 Operation of CMOS circuits with strip pattern TFTs

CMOS Circuit was also fabricated by the process steps shown in Sect. 3.2.1. In order to demonstrate industrial applications, shift register (SR), which is which is one of the key circuits for the peripheral driver of displays [13 - 15], was formed with conventional and strip pattern TFTs. CMOS circuit operation at a low supply voltage of 5V was targeted with the object of external interface. For the evaluation of circuits, a data generator (Tektronix: DG 2020A) and an active prove of 0.1 pF (GGB industries: model 12C) were used.

3.3 Results and discussion

3.3.1 Grain growth induced by μ-TPJ irradiation on a-Si pattern

Firstly, we observed the crystallinity with respect to pattern width. As shown in Fig. 3.3, all patterns seemed to be crystallized by HSLC condition. In the case of 10-μm wide pattern, the pattern shapes were frequently broken up (Fig. 3.3(a)). On the other hand, by

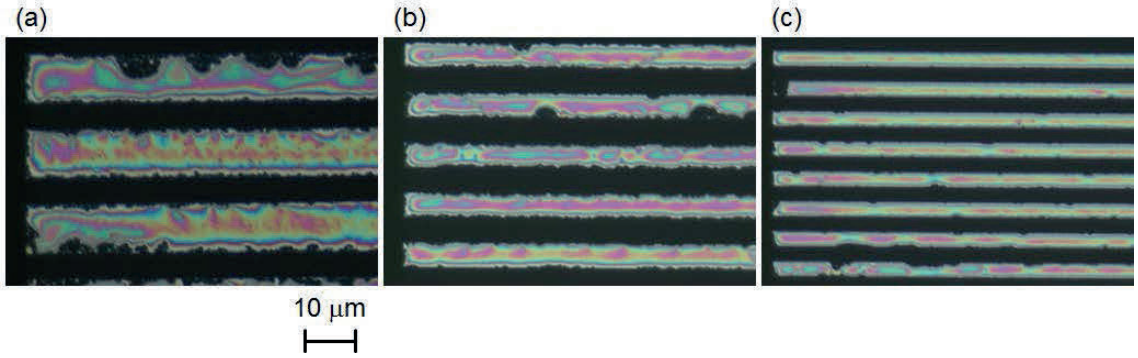

Fig. 3.3. Optical microscope images of crystallized Si patterns with the width of (a) 10 μm, (b) 5 μm, and (c) 3 μm.

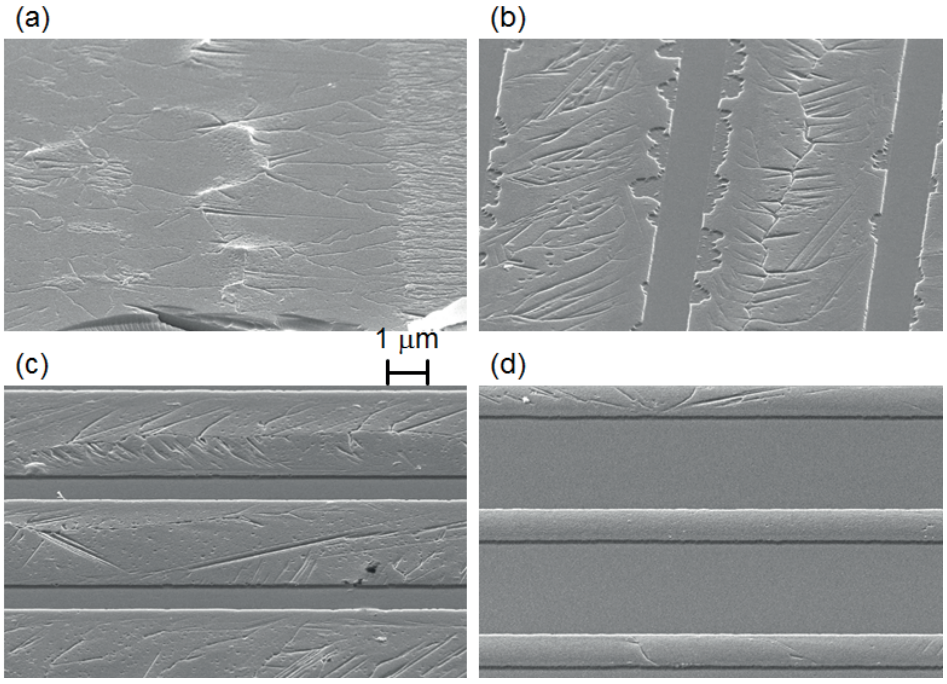

Fig. 3.4. The birds eye view SEM images of crystallized Si patterns with (a) continuous film and the lines with the width of (b) 10 μm, (c) 5 μm, and (d) 1 μm after secco etching.

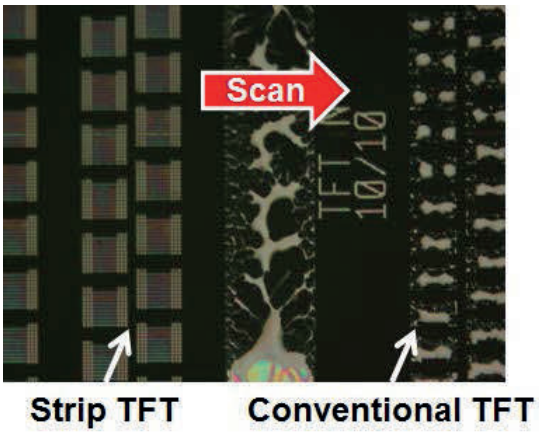

Fig. 3.5. An optical microscope image of strip and conventional TFT patterns after μ-TPJ irradiation. Continuous film and conventional pattern were drastically agglomerated.

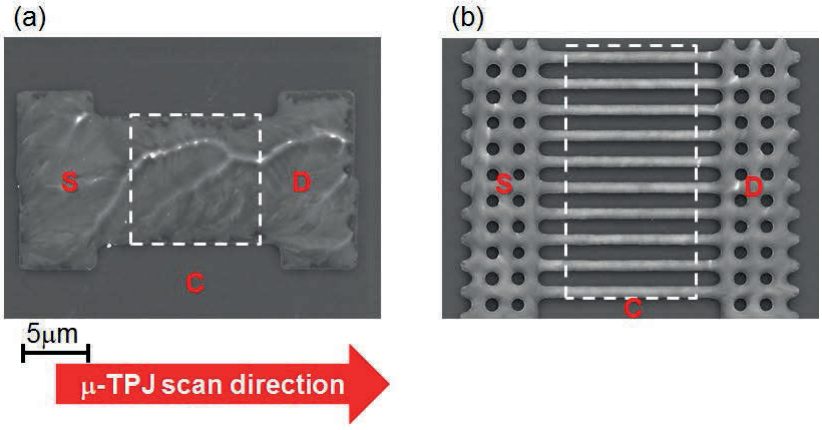

Fig. 3.6 SEM images of (a) conventional pattern with L/W=10/10 μm and (b) strip pattern with L/W=10/1 μm × 10 lines after μ-TPJ crystallization..

decreasing pattern width to 3 μm, the deformations of pattern shape were obviously reduces. So we investigated the defect formation in each patterns. Figure 3.4 shows the bird's-eye view SEM images. As shown in Figs. 3.4(a) and (b), many GBs were formed in continuous film and 10- μm-wide patterns. In the case of 5-μm-wide patterns, GBs were still formed but were reduced in some patterns (Fig. 3.4(c)). By reducing the width to 1 μm, GBs were obviously reduced and no GBs were formed in some patterns (Fig. 3.4(d)). These results suggest that narrow strip pattern is quite effective to suppress the formation of GBs and deformation of pattern shape. So we proposed a new TFT pattern, which is consisted of 1 μm-wide strips. As shown in Fig. 3.5, while continuous film and conventional TFT patterns were drastically broken up by μ-TPJ irradiation with high-*P*

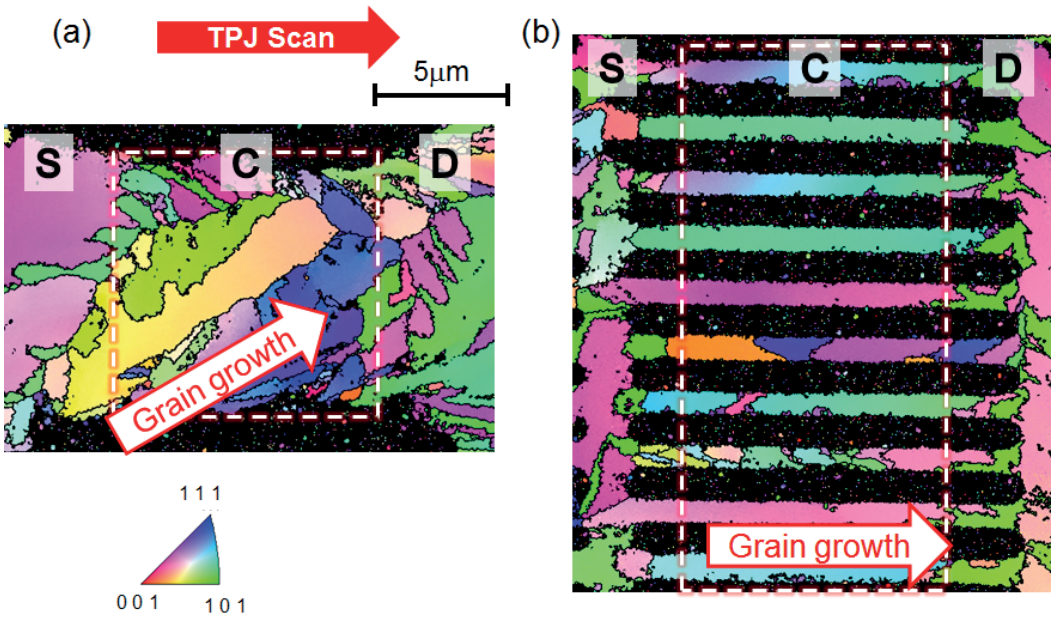

Fig. 3.7 Inverse Pole Figure (IPF) map from surface direction of (a) conventional and (b) strip pattern. The scan direction of μ-TPJ was from left to right, and the center was upper side of both figures.

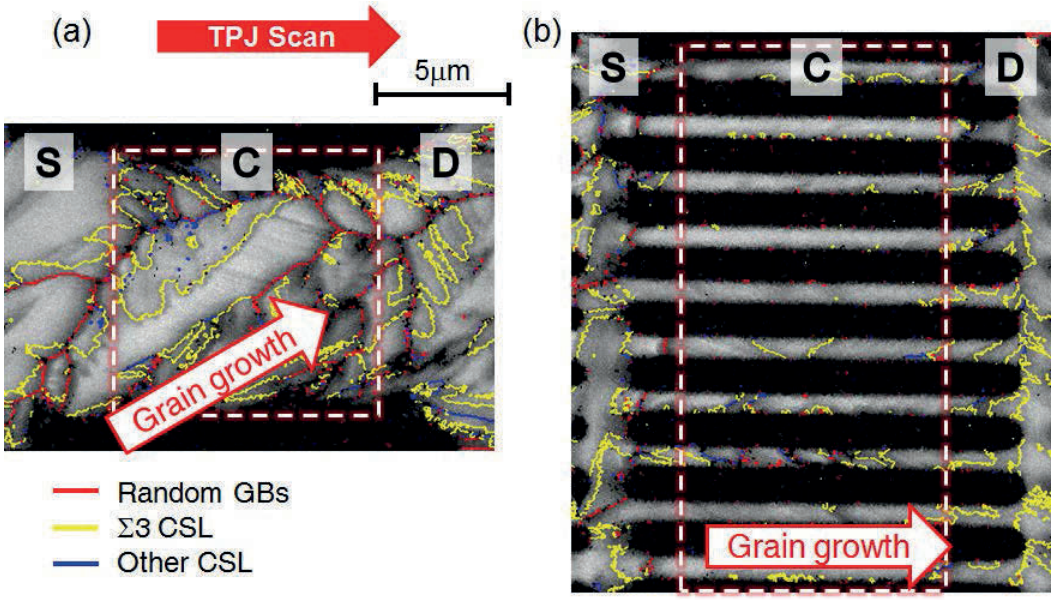

Fig. 3.8 GBs formed in (a) conventional and (b) strip pattern. Red, blue and yellow lines show random GBs, CSLs from 5 to 19 and Σ3 CSLs, respectively.

condition, all of the proposed strip TFT patterns retained their original shape. From these results, strip TFT pattern is quite promising to suppress the formation of GBs and to improve process window of μ-TPJ crystallization.

So we investigated the application of strip TFT pattern compared to conventional TFT pattern (Fig. 3.5(a) and (b)). The crystallographic orientations in the channel region with

conventional and strip pattern were investigated by EBSD. As shown in Fig. 3.7(a), the growth direction of grains was tilted. The grains grow with a slope according to thermal gradient and scan direction of μ-TPJ [1], and GBs crossed the channel region in

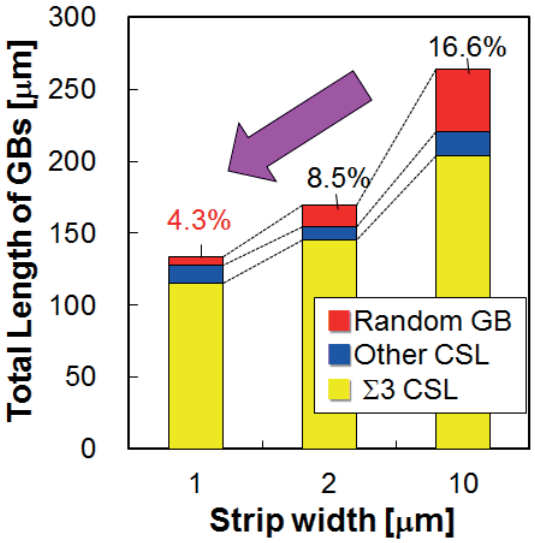

Fig. 3.9 Total length of GBs in 10 μm × 10 μm area with respect to strip width. Red, blue and yellow lines show random GBs, CSLs from 5 to 19 and Σ3 CSLs, respectively.

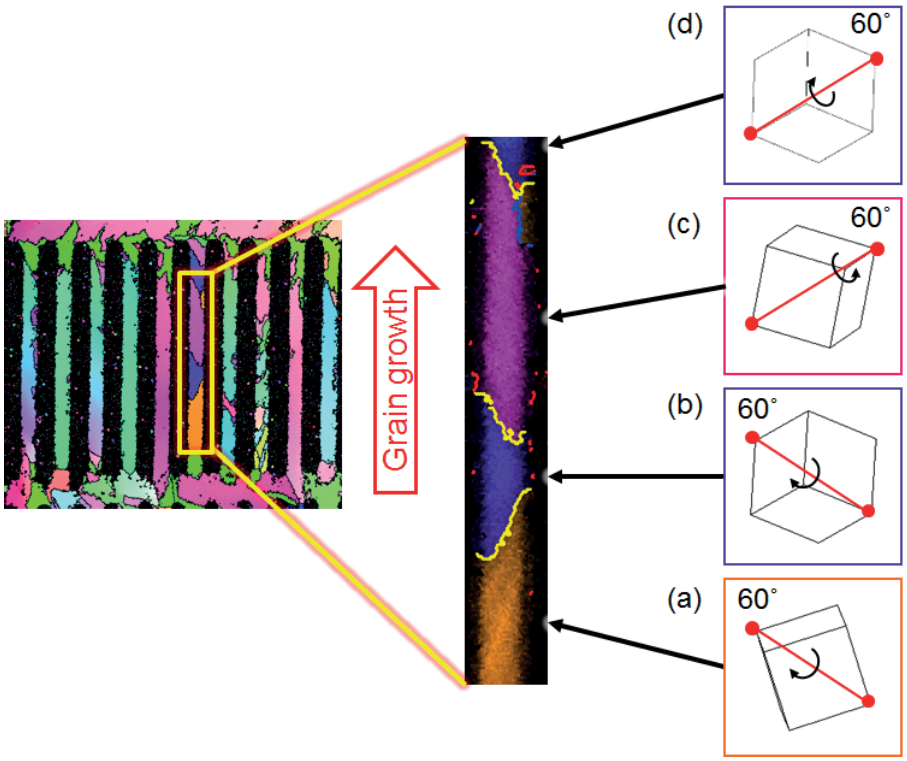

Fig. 3.10 IPF map with GBs of 6th line in Fig. 3.7(b). The lattice of (111) axis and rotation axis of each grains are shown in (a) to (d).

conventional pattern. Thus, in the conventional pattern, grain growth was tilted against the source-drain direction, because of thermal gradient, which is the highest in the center, and the scan direction of μ-TPJ. On the other hand, in strip pattern, grain growth direction is controlled by the strip direction and GBs are filtered out by the strip pattern as shown in Fig. 3.7(b). In addition, single-grain growth was observed in some strips.

Secondly, we investigated the GBs in both patterns. Figure 3 shows ∑3 coincidence site lattice (CSL) with yellow, other CSLs with blue, which were CSLs from 5 to 19, and random GBs with red, respectively. In the case of conventional pattern, random GBs and CSLs [16 - 19] were formed in the channel area, as shown in Fig. 3.8(a). On the other hand in the strip pattern, GBs were clearly reduced and random GBs were mostly stopped in front of channel area, as shown in Fig. 3.8 (b). Figure 3.9 shows the total length of GBs in 10 × 10 μm2 area with respect to pattern width. All GBs in strip pattern were clearly

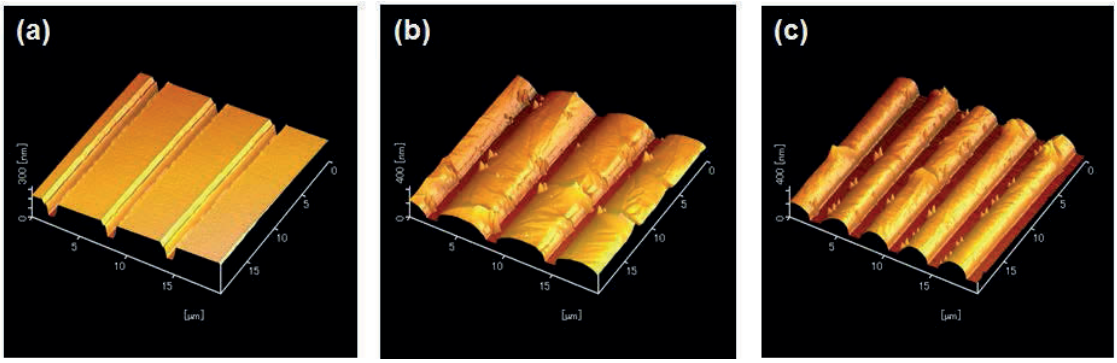

Fig. 3.11 Atomic Force Microscope (AFM) images of Si pattern (a) a-Si pattern of 5 μm and (b), (c) after μ-TPJ crystallization of 5 and 3 μm, respectively.

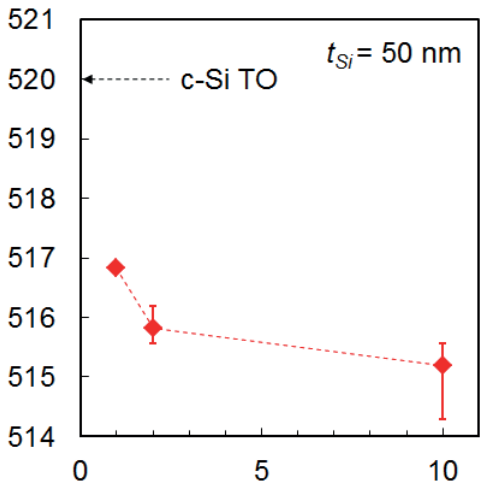

Fig. 3.12 Raman peak position of crystallized Si patterns with respect to strip width.

reduced.

Random GBs were reduced to 4.3% and ∑3 CSLs were also reduced in the 1-μm strip pattern. This suggests that random GBs were eliminated out by the filtering effect of strips. However, CSLs were still formed in channel area of strip pattern. We found that GBs in the strip pattern were mostly ∑3 CSLs which are reported as electrically inactive [19 -21] (Fig. 3.8(b)). Figure 3.10 shows unique grain growth of the 6th line in Fig. 3.8(b). All of these ∑3 CSLs were formed by 60˚ rotation around (111) axis. In the case of ∑3 CSL between Fig. 3.10(a) and (b), grain was rotated 60˚ around (111) axis. In the case between Fig. 3.10(b) and (c), the grain was rotated 60˚ around sthe other (111) axis and returned by counter rotation in next ∑3 CSL between Fig. 3.10(c) and (d). this grain growth suggests that narrow strips suppress the formation of random GBs and only limited crystallographic rotations such as ∑3 CSLs are allowed.

In addition, as shown in the atomic force microscope (AFM) image in Fig. 3.11, Si pattern shape is rounded at the upper side but interface between Si and substrate remained at the same position. The pattern shape become roundly by decreasing pattern width (Figs. 3.11 (b) and (c)) Figure 3.12 shows raman peak position as a function of channel width, which shows that tensile stress in narrow strip was clearly reduced [22]. These results suggest that the deformation of Si strips during the phase transformation plays a role to suppress random GB generation and preferential formation of CSL boundaries. It should be noted that there are no additional the process steps, such as capping layer formation for crystallization [18 - 19], which cause higher fabrication costs. The proposed strip channel TFT pattern s enable the suppression of random GBs by simple process steps.

3.3.2 In-situ observation of grain growth in a-Si patterns during μ-TPJ irradiation

Grain growth in HSLC of amorphous silicon (a-Si) strips during μ-TPJ irradiation is successfully observed by HSC. A-Si film was melted following solid phase crystallization (SPC) and leading wave crystallization (LWC) [5 - 6]. Figure 3.13 shows the snapshots with 32 μm wide area within the molten region ~ 100 μm. A liquid Si (*l*-Si) is observed in black because light from μ-TPJ is obstructed by very high reflectivity of molten Si. After solidification, c-Si are shown in gray scale by transmitting the light and slit lines without a-Si film are shown in the brightest white. In the case without patterns, a number of dendritic growths were observed as shown in Fig. 3.13(a). The lateral growth was observed and nucleation was not observed. The growth direction of each dendritic growth was induced by scanning direction and thermal gradient of μ-TPJ. In the case of 10 μm-wide

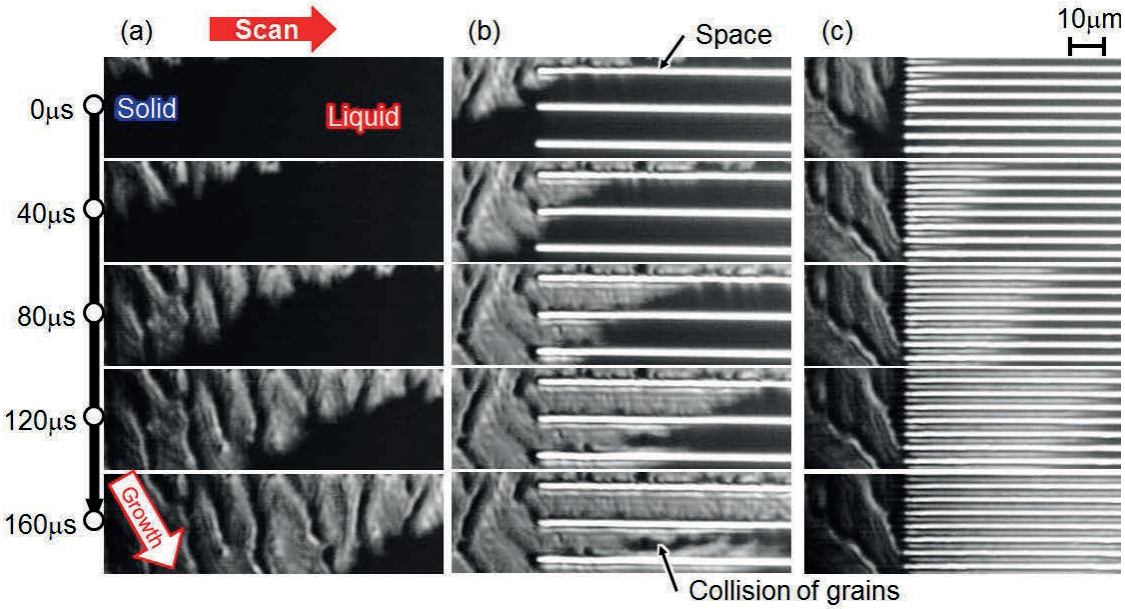

Fig. 3.13 Snap shots by HSC of HSLC on a-Si patterns during μ-TPJ irradiation under the conditions of P = 1.3 kW, d = 1.5 mm, v = 800 mm/s, and f_r = 25000 fps. 1 μm-wide slits were formed by periods of (a) continuous film, (b) slit pattern with W =10 μm, and (c) W = 3 μm

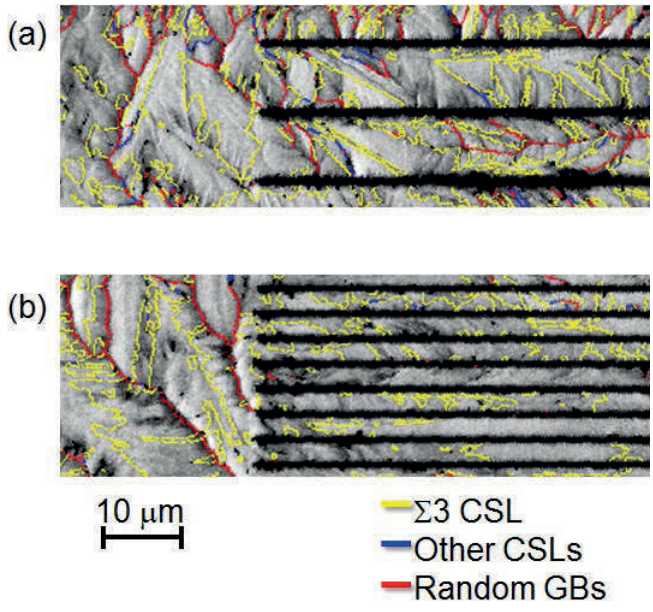

Fig. 3.14 GBs in crystallized patterns of (a) W =10 μm and (b) W = 3 μm were drawn with superimposition on image quality (IQ) maps. These maps were observed at the same positions with Figs. 3.13 (b) and (c). Yellow, blue, and red lines express Σ 3 CSL, Σ 5 ~Σ 19 CSLs, and random GBs, respectively.

pattern, no nucleation was occurred in the pattern edge and dendritic growth went into slit area. However, liquid-solid interfaces from both pattern edges collide with grain growth as shown in Fig. 3.13(b). On the other hand, in the case of 3 μm-wide pattern, single liquid-solid interface moved into each strips by controlling growth direction from left to right (Fig. 3.13(c)). Consequently, in order to compare the grain growth and formation of GBs, we investigated the GBs corresponding to observed patterns in Figs. 3.13(b) and (c). As shown in Fig. 3.14(a), random GBs with red line were formed in the place where grains collided. On the other hand, 3 μm–wide strips obviously suppressed the formation of random GBs. From these results, random GBs were suppressed by preventing collision of grains. However, Σ 3 CSL was formed in both patterns. Because Σ 3 CSL, which is electrically inactive,[19-21] was formed by rotating 60º around (111) axis as mentioned in Sect. 3.3.2, adjacent grains take over the crystallinity during solidification and formed no dangling bonds. So we concluded that narrow strip pattern forms high crystallinity by eliminating out the formation of random GBs. Moreover, we observed different condition of μ-TPJ irradiation by decreasing v from 800 to 730 mm/s (Fig. 3.15). In this condition, the slit pattern was gradually agglomerated and the pattern shape was obviously transformed during melting period.

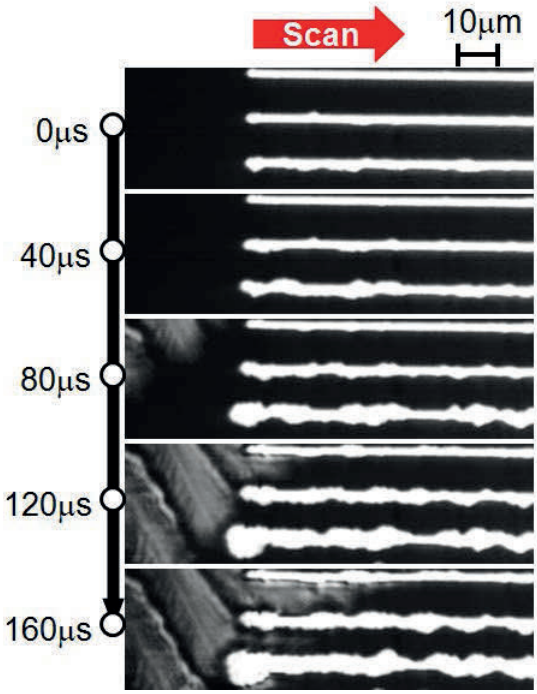

Fig. 3.14 Snap shots by HSC of HSLC on a-Si patterns with W = 10 μm during μ-TPJ irradiation under the conditions of P = 1.3 kW, d = 1.5 mm, v = 750 mm/s, and f_r = 25000 fps.

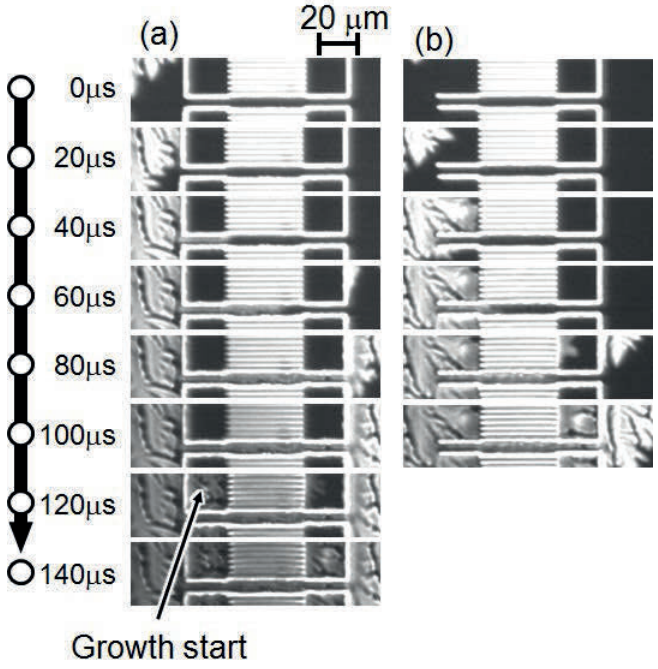

Fig. 3.15 Snap shots by HSC of HSLC on TFT patterns during μ-TPJ irradiation under the conditions of P= 1.1 kW, d = 1.0 mm, v = 1600 mm/s, and f = 50000 fps. (a) isolated and (b) continuous TFT patterns with 1 μm-wide strip channel were formed.

Table I. Characteristics of *l*-Si on TFT pattern shown in Fig. 3.15.

	w/o pattern	Isolated pattern	Continuous pattern
Delay time (μs)	0	100	0
Growth velocity (m/s)	1.2	3.2	0.8
Undercooling degree (ºC)	~100	~150	~90

Subsequently, we investigated the application of strip pattern to TFTs. Grain growth in TFT patterns as shown in Figs. 3.2(c) and (d) were observed. As shown in Figs. 3.15(a) and (b), in the case of isolated pattern, the continuous growth reached next to the TFT pattern at 20μs, however, the TFT pattern was fully melted and still in liquid phase. Solidification of TFT pattern at 120μs indicated the nucleation, delayed by 100 μs compared with continuous pattern (Fig. 3.15 (b)). This is because the complete melting of TFT pattern lost the nucleus and the molten Si goes into undercooling condition. Once nucleation takes place at 120 μs, rapid lateral solidification occur (with growth velocity of ~3.2 m/s). Here we considered about the reason that homogeneous nucleation, which results in defective grains [23 - 24], did not occur in spite of complete melting. As shown in Table I, ΔT of 150ºC and cooling rate of 5×10^5 K/s were estimated by growth velocity using Ref. 25. This slow cooling rate, compared with > 10^{10} K/s by ELA [23 - 24], was achieved because μ-TPJ heats Si patterns and the substrate simultaneously [26]. So

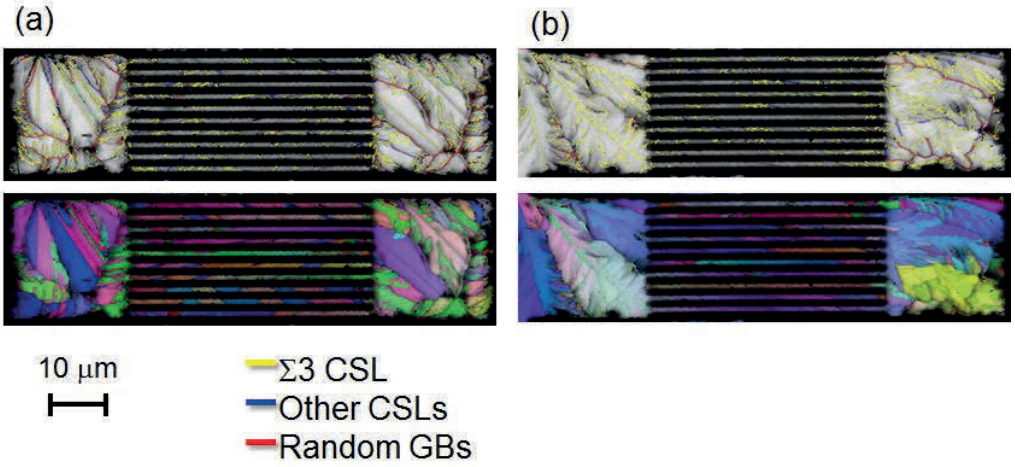

Fig. 3.16 GBs and crystallographic orientations of surface direction in crystallized patterns of TFT pattern were drawn with superimposition on image quality (IQ) maps. This map was observed at the same positions with Fig. 3.15 (a) and (b), respectively.

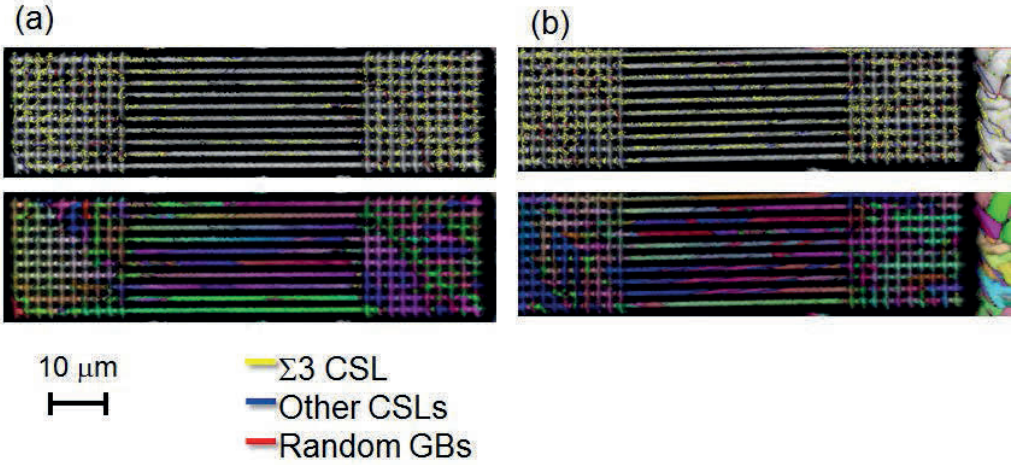

Fig. 3.17 GBs and crystallographic orientations of surface direction in crystallized patterns of TFT pattern were drawn with superimposition on image quality (IQ) maps. These patterns were composed of 1-μm wide strip not only in channel but also S/D areas.

once nucleation occurred, lateral growth was induced by thermal gradient of μ-TPJ in spite of homogeneous nucleation. In fact, as shown in Figs. 3.16 (a) and (b), random GBs are significantly suppressed in channel area as same as before. This grain growth was observed in the case of TFT patterns with lattice S/D as shown in Figs. 3.17 (a) and (b). These results indicate that we can grow crystalline Si without random GBs even in isolated TFT pattern with strip channel.

3.3.3 Self-aligned top gate CMOS TFT fabrication

TFTs with conventional and strip channels were successfully fabricated as shown in Figs. 3.18(a) and (b). In the case of the conventional channel pattern, pattern defects frequently occurred due to agglomeration of molten Si during μ-TPJ crystallization (Fig. 3.18 (c)). On the other hand in the strip pattern, pattern defects were markedly reduced and yield of TFT operation was improved. We could operate N-type and P-type TFTs with both patterns. TFTs with strip pattern show higher on-current especially in N-channel. Figure 3.19 shows the characteristic variability in TFTs in both patterns. As shown in Fig. 3.19(a), TFTs with the conventional pattern showed large variation although only a fewer numbers of TFTs could be operated. On the other hand, TFTs with the strip pattern showed high-performance and smaller variation, as shown in Fig. 3.19(b). Figures 3.20(a) and (b) show histograms of the characteristic variability of threshold voltage (V_{th}), field effect mobility (μ_{FE}) and subthreshold swing value (S) of TFTs in both patterns. Characteristic variability in strip pattern was reduced to roughly 1/3, by comparison with conventional

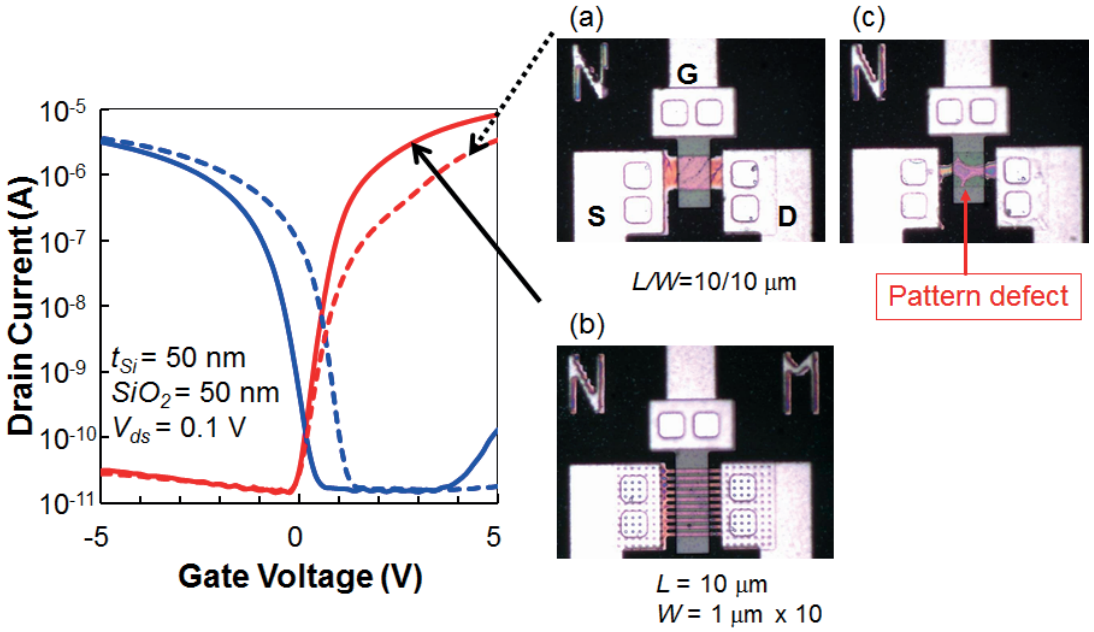

Fig. 3.18 Transfer characteristics of TFTs fabricated with conventional (broken line) and strip pattern (solid line). Insets were optical images of TFTs with (a)conventional pattern, (b) strip pattern, and (c) agglomerated conventional pattern.

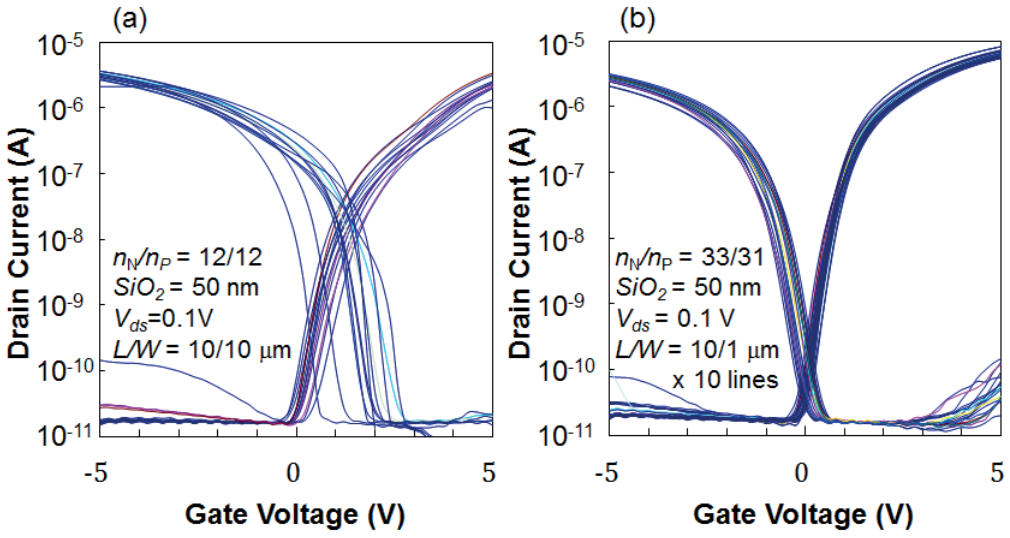

Fig. 3.19 Transfer characteristics of TFTs with (a) conventional and (b) strip pattern. No good TFTs, such as gate leakage and pattern defects, were eliminated among 35 TFTs.

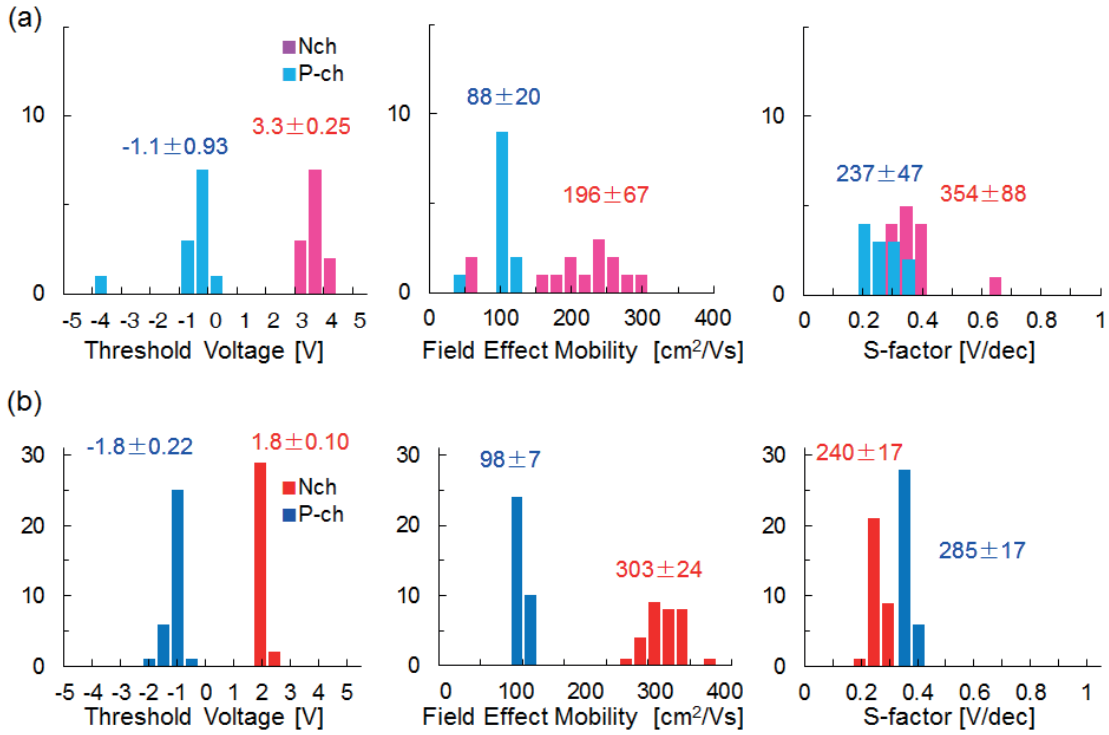

Fig. 3.20 The histograms of V_{th}, μ_{FE}, and S in TFTs with (a) conventional and (b) strip pattern. Average ± standard deviation (σ) of NMOS and PMOS were shown, respectivery.

pattern. However, the p-ch characteristics of the strip TFTs shifted to left compared to the conventional TFTs. We concluded that the differences of p-ch TFTs were caused by small

amount of defects and un-doped channels which behaved as n-type. Thus acceptor-type defect density in strip TFTs is lower than in conventional TFTs. These results indicate that reduction of random GBs effectively suppresses the variability and improve the μ_{FE}.
So we investigated the application of strip TFTs to CMOS operation. Figure 3.21 shows the output characteristic of TFT with strip pattern.

3.3.4 CMOS circuit operation

In order to control the output of CMOS invertor, NMOS and PMOS outputs were investigated. Figure 3.21 shows output characteristics of strip pattern TFTs. They were quite promising for the operation at supplying voltage (V_{dd}) of 5V and the size ratio ($R = W_P/W_N$) for CMOS layout was well-balanced at $R = 2$. As shown in Fig. 3.22, CMOS inverter with the strip pattern operated at a low supply voltage of 5 V with no hysteresis and showed a $V_{th} = 2.5$V at $R = 2$.
We fabricated a shift register (SR), which is a key circuit for peripheral circuit formation on glass substrate [27-30]. To evaluate the effect of channel patterns, we fabricated SR with both patterns. We could not operate SRs with conventional pattern because of the poor yield as mentioned previously. We fabricated the SR with the strip channel pattern as shown in Fig. 3.23. We were able to operate 8-bit shift-register at a supply voltage of 5V and a clock frequency of 4 MHz as shown in Fig. 3.24. This low-voltage operation was achieved because the proposed strip channel pattern can effectively to improve both the yield and performance of TFTs. This result demonstrates that the μ-TPJ crystallization process on a-Si strip pattern is quite promising for the fabrication of high-performance displays.

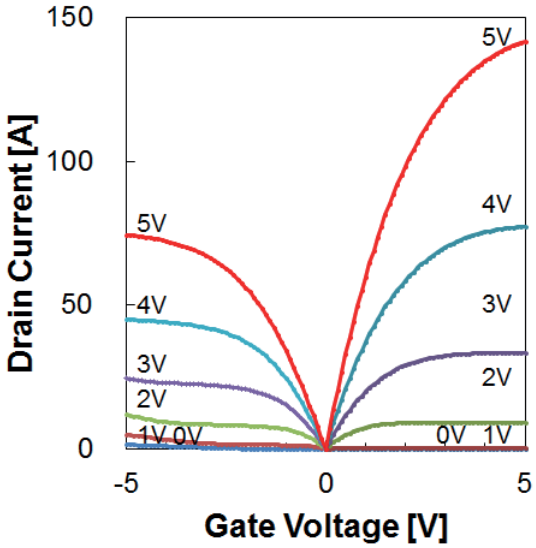

Fig. 3.21 Output characteristics of TFTs with strip pattern. NMOS and PMOS were same size and evaluated by the condition with V_{gs} of 5V and V_{ds} from 0 to 5V.

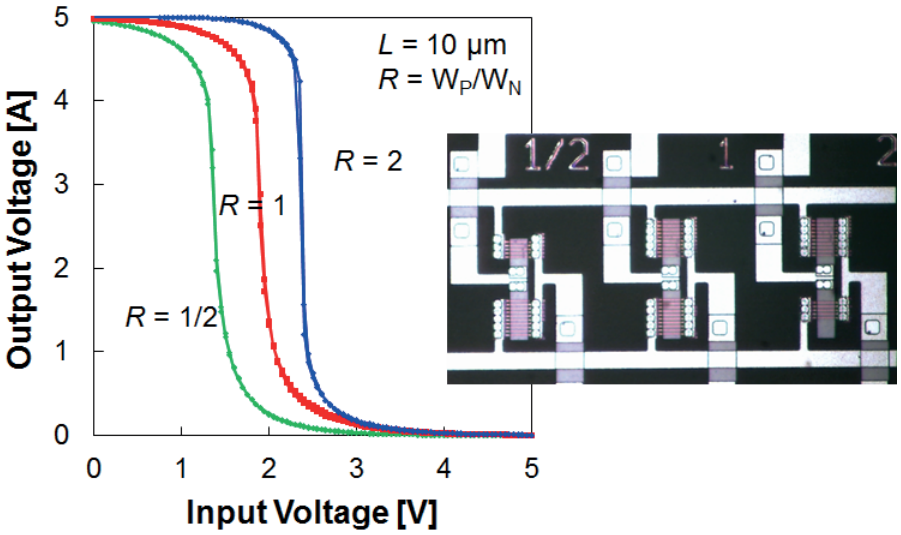

Fig. 3.22 Output characteristics of CMOS inverters with different size ratio (R). Inset shows the CMOS inverters with L =10 μm and R = 1/2, 1 and 2, respectively.

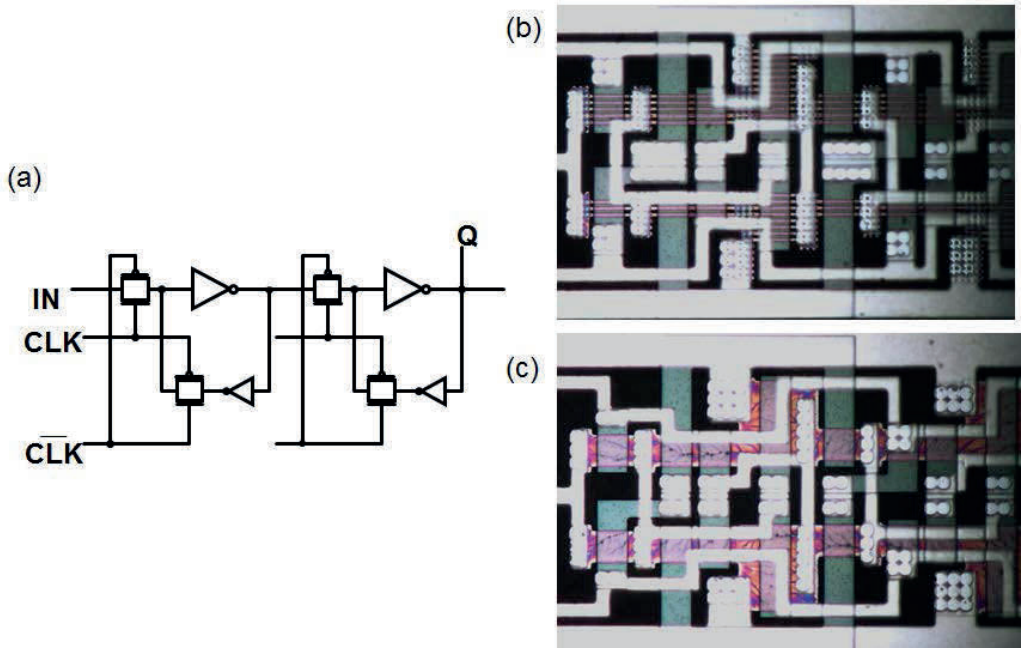

Fig. 3.23 The optical microscope image of shift register (SR) with strip pattern and circuit diagram of 1 bit SR. 16 TFTs with (L =10 μm) are composed in 1bit SR with a bit pitch of 169 μm.

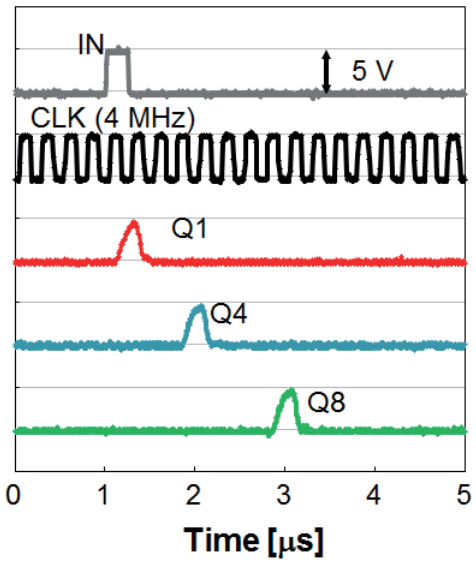

Fig. 3.24 Output characteristics of shift register with strip pattern operated by the supply voltage of 5V at the clock frequency of 4MHz. The input signal and shifted outputs with each bits of SR were shown.

3.4 Summary

We fabricated a shift register (SR), which is one of the key circuits for the peripheral driver of displays. To evaluate the effect of channel patterns, we fabricated SR with both patterns. We could not operate SRs with conventional pattern because of the poor yield as mentioned previously. We fabricated the SR with the strip channel pattern. We were able to operate 8-bit shift-register at a supply voltage of 5V and a clock frequency of 4 MHz. This low-voltage operation was achieved because the proposed strip channel pattern can effectively to improve both the yield and performance of TFTs. This result demonstrates that the μ-TPJ crystallization process on a-Si strip pattern is quite promising for the fabrication of high-performance displays.

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Chapter 4

Investigation of the Effects and Crystallinity of Strip Patterns

4.1 Introduction

As mentioned in Sect. 3. 3.3, we have successfully improved the variation issue of c-Si TFTs. Our proposed new thin film transistor (TFT) pattern, which is composed of 1-µm-wide strips, suppressed the formation of random GBs. This pattern enabled us to operate CMOS circuit with channel length (L) of 10 µm at a low supply voltage of 5V and a high frequency of 4MHz. However, considering its application for next generation displays, higher integration and higher operation speed is required. For instance, in the case of high resolution display with 500 pixels per inch (ppi), the size of each pixel is shrunk to 51 µm including red, green, and blue cells. In addition, higher operation speed is required for peripheral circuits. In order to demonstrate these performances, miniaturization of TFT size is quite promising. In our previous work (Sect. 3), however, TFTs showed sub-threshold leakage current (I_{sub}) with decrease of L (Fig. 4.1). In order to suppress I_{sub}, structural approaches have been applied for crystalline silicon (c-Si) TFTs, such as lightly-doped drain and dual gate structures[1-2]. These approaches are definitely effective, but need additional process steps or sacrifice the open area of pixel.

So in this work, in order to make a correct judgement for structural approaches, we attempted to improve the crystallinity of in strips. Moreover, we investigated, in detail, the characteristics of TFTs by comparing electrical properties and crystallinity in channel area.

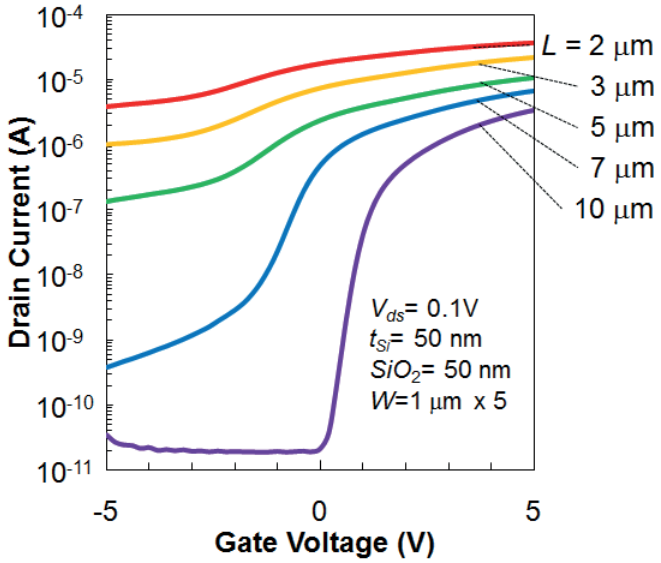

Fig. 4.1. Transfer characteristic of strip pattern TFTs with respect to L from 2 to 10 µm (W = 1 µm × 5 lines). TFTs were fabricated by process steps shown in Sect.3.

4.2 Experimental procedure

4.2.1 Investigation of the correlation between TFT characteristics and its crystallinity

As shown in Fig. 3. 10, after μ-TPJ crystallization of a-Si strips, pattern shape was rounded. So we considered that the surface tension of liquid silicon (*l*-Si) after transformation affects the formation of grain boundaries, not only random GBs but also Σ3 coincidence site lattice (CSL). We investigated the relationship between formation of GBs and remaining stress after micro-thermal-plasma-jet (μ-TPJ) irradiation with the condition of high-speed lateral crystallization (HSLC). Amorphous silicon (a-Si) patterns with the thickness (t_{Si}) from 15 to 200 nm were crystallized by μ-TPJ irradiation. Crystallized patterns were investigated by micro-Raman scattering microscope and electron backscattering diffraction (EBSD) method.

In order to investigate the relationship the electrical properties and crystallinity in channels of TFTs, non-self-aligned top gate TFTs were fabricated for simplicity to remove TFT structure without channel silicon. The gate-last process steps were as follows.

A 200-nm-thick un-doped a-Si film was formed on quartz substrate by plasma-enhanced chemical vapor deposition (PECVD) using SiH_4 and H_2 at 250 ºC. Dehydrogenation was carried out in N_2 ambient at 450 ºC for 1 hour. Then a-Si was patterned by chemical dry etching (CDE) to form source, drain and channel. In this work, we designed conventional pattern and strip pattern whose channel, source, and drain were consisted of 1 μm-wide strips. Here, un-doped and doped channels were formed for comparison. Channel doping was carried out by ion implantation at the dose from 1×10^{12} to 3×10^{12} /cm^2 phosphorus ions (P^+) and boron ions (B^+) in PMOS and NMOS, respectively. The μ-TPJ was generated by DC arc discharge under atmospheric pressure with a supply power (*P*) of 1.2 kW and Ar gas flow (*f*) of 1.0 L/min. The substrate at a distance (*d*) of 1.0 mm from μ-TPJ was linearly moved with a scan speed (*v*) of 1200 mm/sec. In this condition, ~200 μm wide molten zone is formed and rapid re-crystallization to lateral direction is induced by the fast movement of molten Si. Then, source and drain region were formed by ion implantation at the dose of 3.1×10^{12} /cm^2 BF^{2+} and P+ in PMOS and NMOS, respectively. After a 100-nm-thick gate SiO^2 was formed by the remote-PECVD at 350ºC [3], μ-TPJ was irradiated again with the condition of P = 1.4 kW, d= 1.5 mm, f = 1.0 mm/s, and v = 1400 mm/sec. Under this condition, Si films were not melted, rather, dopant activation was achieved by rapid annealing [4-5]. After formation of contact holes by wet etching, Al-Si(1%) electrodes were formed by DC sputtering and wet etching. Finally, post

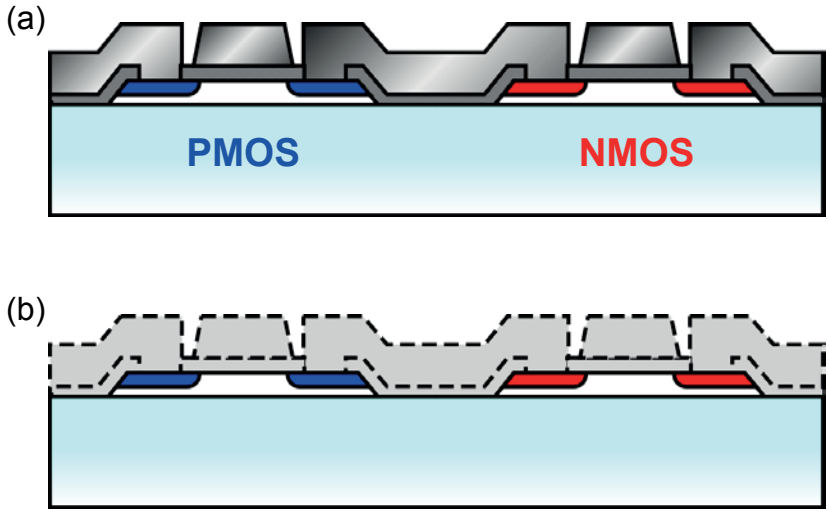

Fig. 4.2. TFTs with non-self-aligned top gate structure of after (a) fabrication process and (b) peeling off the gate insulator and electrodes.

metallization annealing (PMA) was performed at 350ºC and in H_2 + N_2 ambient for 30 min. After the electrical characteristics measurement, the gate electrode and gate SiO_2 were etched off in order and the crystallographic orientations and GBs were investigated by EBSD.

We also investigated self-aligned top gate TFTs with short L = 2 μm. The modified process steps were as follows. The thickness of gate SiO_2 was reduced from 100 nm to 50 nm, gate Al electrode was replaced with a-Si by low pressure CVD (LPCVD) at 520ºC and heavily doped simultaneously with source and drain (self-align), and a 650-nm-thick interlayer dielectric was added. Here, we investigated, in detail, TFT characteristics with respect to channel width (W).

4.3 Results and discussion

4.3.1 Investigation of the correlation between TFT characteristics and its crystallinity

Figure 4.3 (a) shows the Raman peak spectra with respect to t_{Si}. The c-Si transversal optical (TO) phonon peak appears in all thickness. In the case of t_{Si} =15 nm, the Raman spectrum was shifted to low wave number direction and the full width at half maximum (FWHM) was spread. However, the TO phonon peak positions and FWHM got close to single-Si with increase of t_{Si}. As shown in Fig. 4.3 (b), by increasing tSi to 200nm, TO phonon peak and FWHM were close to 517 cm^{-1} and 4 cm^{-1}, respectively. These results indicate that tensile stress were remained in crystallized patterns but were suppressed with increase of t_{Si}. So we concluded that thick a-Si film is effective to form high-crystallinity.

Therefore, we investigated GBs in crystallized patterns with t_{Si} = 200 nm. Figure 4.4 shows the map of GBs and their kinds. In the case with W > 3 μm, random GBs were clearly formed. However, in the case in narrow strips, they were eliminated. In addition, it should be noted that Σ3 coincidence site lattice (CSL) was significantly suppressed by

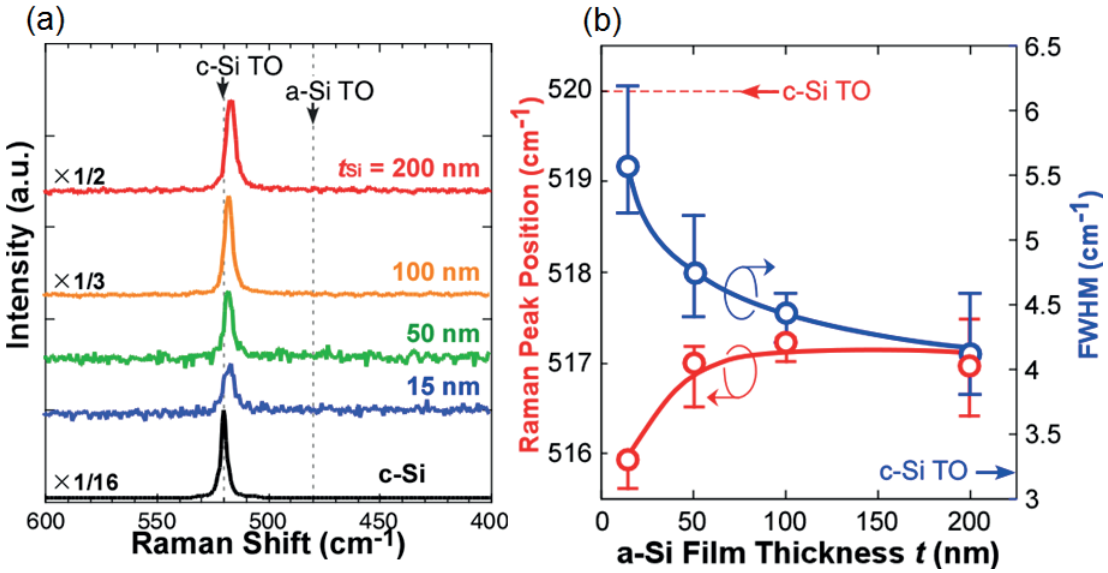

Fig. 4.3. (a) Raman spectra of 1 μm-wide strips with respect to tSi from 15 to 200 nm after μ-TPJ crystallization and referential single c-Si substrate. (b) The TO phonon peak position and FWHM of Raman spectra in Fig. 4.3 (a).

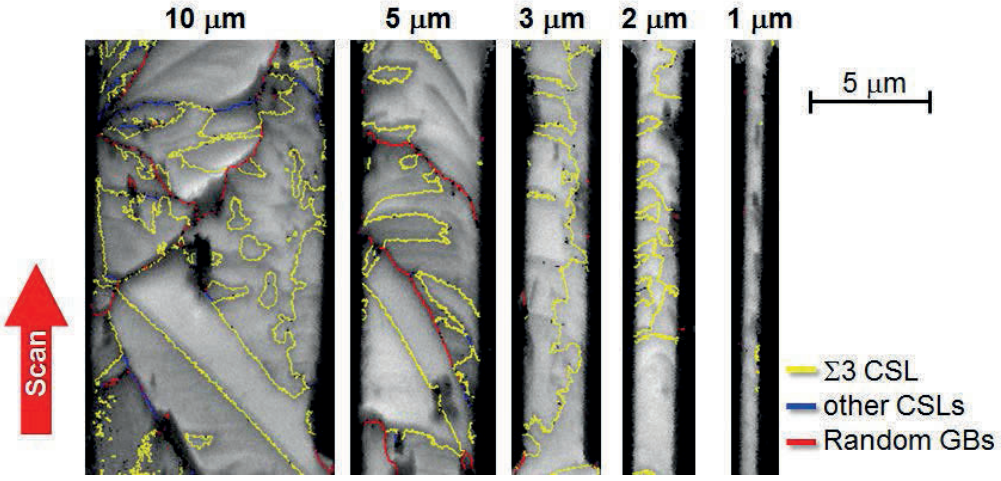

Fig. 4.4. Map of GBs with respect to pattern width. Σ3 CSL, Σ5 – 19 CSLs and random GBs were distinguished. While random GBs were formed in the width more than 5 μm, they were significantly suppressed by decreasing the width to 1 μm.

decreasing *W* to 1 μm even though still exists. From these results, we concluded that μ-TPJ crystallization of narrow strip and thick a-Si film is promising for the formation of higher crystallinity channel because the relaxation of tensile stress in Si might have relation to form GBs or other defects.

We investigated the characteristics of TFT with short channel length. Figure 4.5(a) shows transfer characteristics of TFTs with the channel length from 1 to 10 μm and non-doped

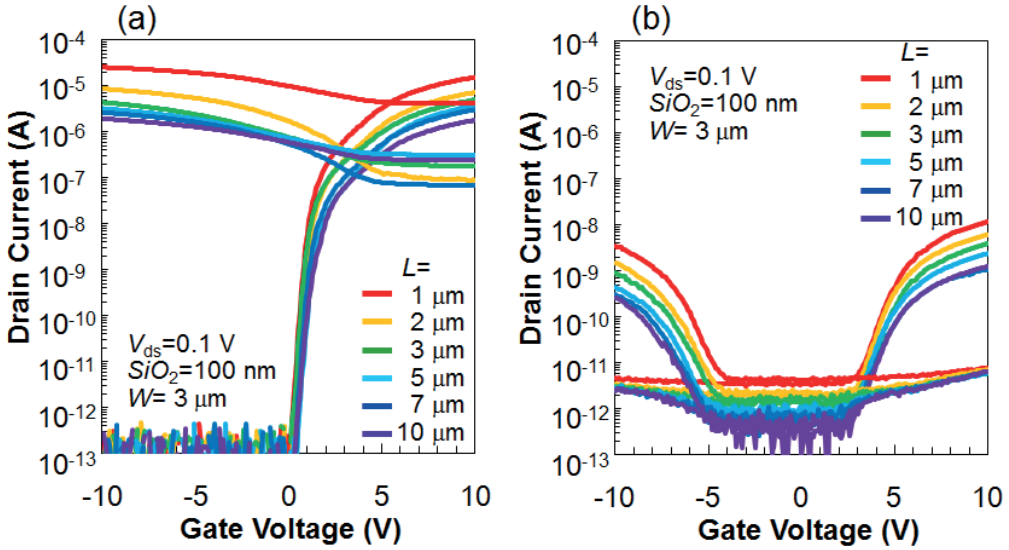

Fig. 4.5. Transfer characteristics of TFTs with respect to *L*. The conditions of μ-TPJ crystallization were (a) HSLC with *v* =1200 mm/s and (b) SPC with *v* = 1900 mm/s.

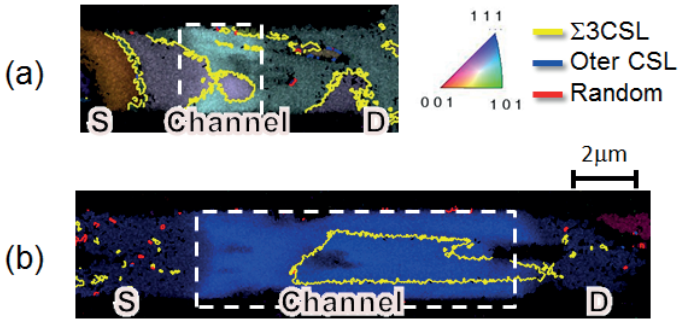

Fig. 4.6. Maps of crystallographic orientation s and GBs in channel area by HSLC. These figures show the channel area in PMOS TFTs shown in Fig. 4.5(a).

channel crystallized by HSLC condition. In the case of NMOS TFTs, high on current with the on/off ratio ($R_{on/off}$) higher than 10^7 was observed in all L. On the other hand in PMOS TFTs, $R_{on/off}$ was degraded to less than 10^2 due to high I_{sub} with decrease of L while on current was as high as NMOS. Because we suspected the contamination in the channel Si, we investigated TFTs with solid phase crystallization (SPC) channel, which were crystallized by v = 1900 mm/s (Fig. 4.5(b)). Off current of SPC was extremely low in all L, even in PMOS TFTs. The back channel punch through was not observed when the channel crystallinity was poor. So we investigated crystallographic orientations and GBs in

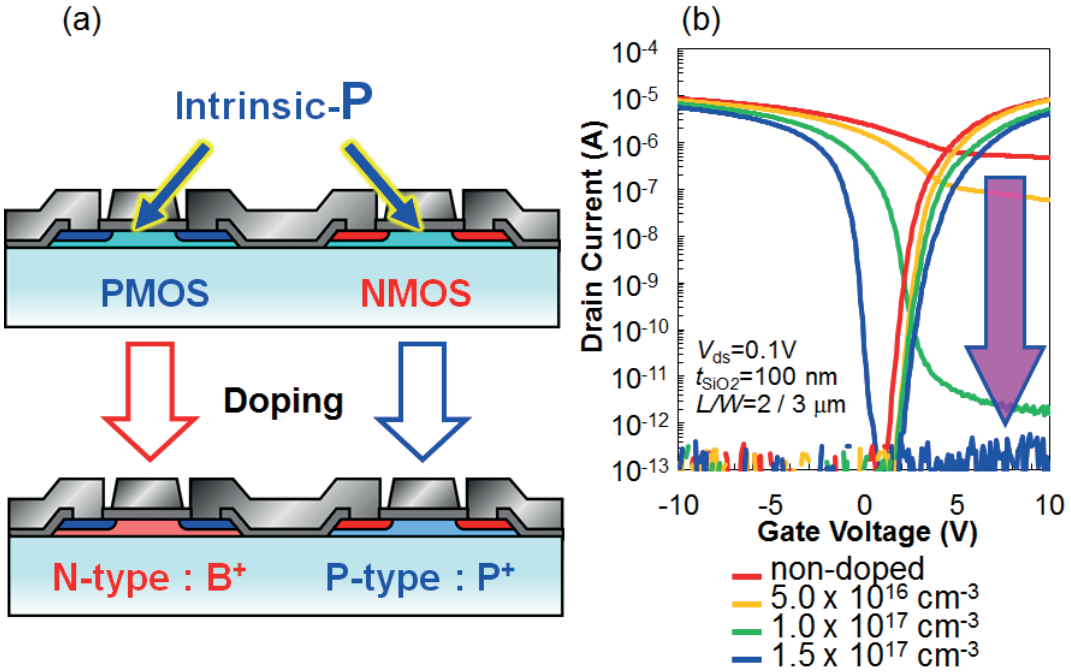

Fig. 4.7. (a) Schematic diagram of the control of Fermi level in channel area. Non doped channel is intrinsic P-type and were controlled by counter doping. (b) Transfer characteristics with respect to N_C.

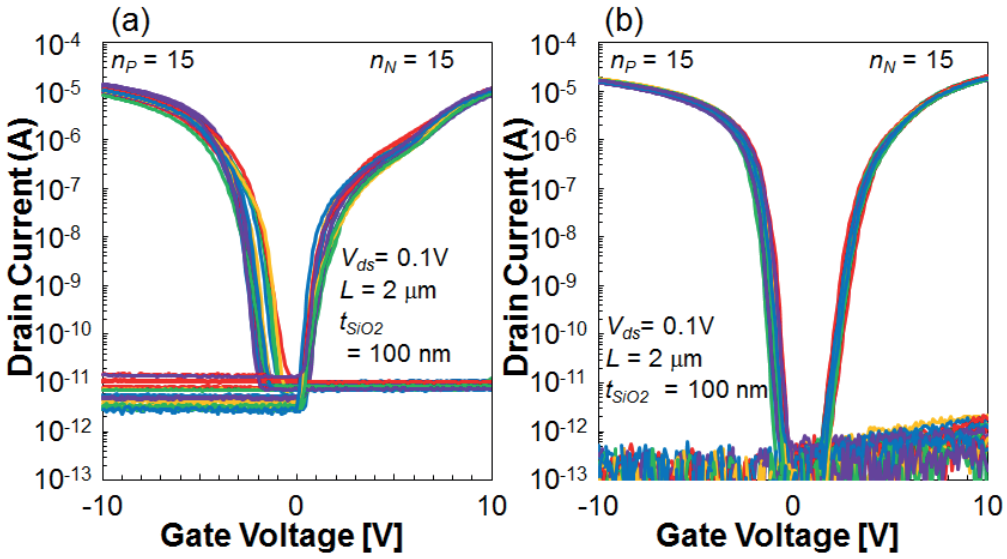

Fig. 4.8. (a) Schematic diagram of the control of Fermi level in channel area. Non doped channel is intrinsic P-type and were controlled by counter doping. (b) Transfer characteristics with respect to N_C.

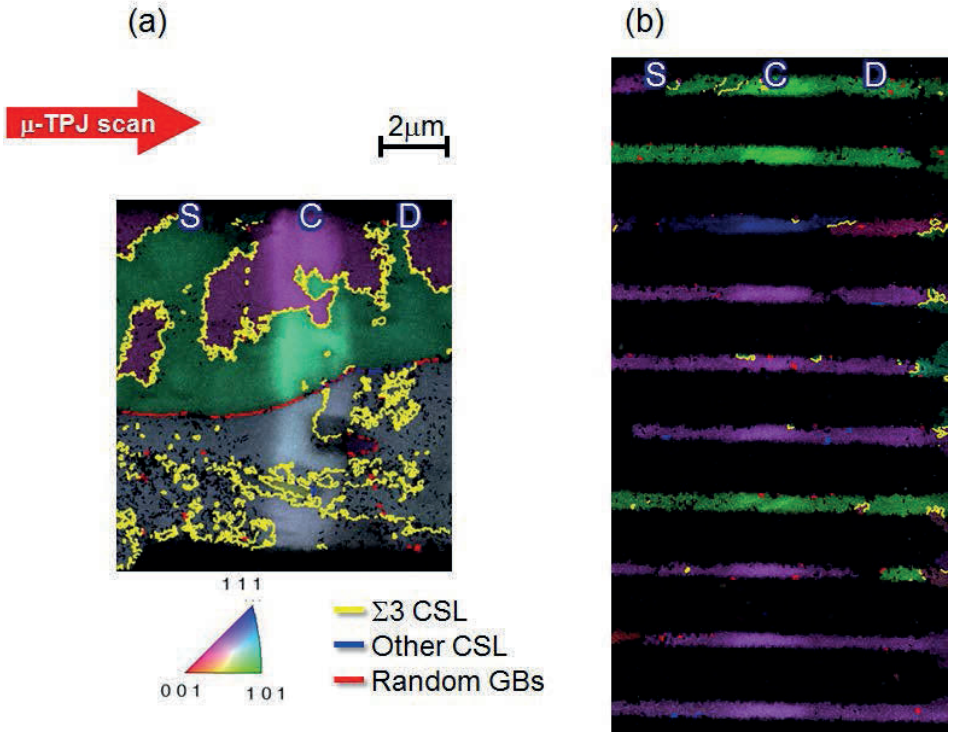

Fig. 4.9. (a) Schematic diagram of the control of Fermi level in channel area. Non doped channel is intrinsic P-type and were controlled by counter doping. (b) Transfer characteristics with respect to N_C.

TABLE I. TFT characteristics with L =2 μm of (a) strip pattern and (b) conventional pattern shown in Figs. 4.8(a) and (b). Averages of μFE and Vth are calculated from 15 TFTs.

(a)

Average (n=15)	Conventional NMOS	PMOS
μ_{FE} [cm²/Vs]	197	116
V_{th} [V]	7.1	-4.5

(b)

Average (n=15)	Strip NMOS	PMOS
μ_{FE} [cm²/Vs]	360	170
V_{th} [V]	5.7	-2.6

measured TFTs. As shown in Figs. 4.6 (a) and (b), crystallographic orientations were not uniform but single grain or no GBs except Σ3 CSL were formed in all L. From these results, we considered that high I_{sub} in PMOS TFTs was caused by small amount of defects and non-doped channel behaved as p-type.

So we considered that I_{sub} could be suppressed by channel doping over defect density and formation of PN junction between S/D and channel, because defects in channel Si trap impurities [6] (Fig. 4.7(a)). We investigated TFT characteristics with respect to channel doping concentrations (N_C). Figure 4.7(b) shows the transfer characteristics of TFTs with respect to N_c from non-doped to 1.5×10^{-17} cm^{-3}. Sub-threshold characteristics in PMOS were extremely improved with increase of N_c. Especially, between 5.0×10^{16} cm^{-3} and 1.0×10^{17} cm^{-3}, I_{sub} was obviously suppressed. On the other hand in NMOS, sub-threshold characteristics were preciously controlled and showed low I_{sub} dependence on boron doping concentration, but threshold voltage (V_{th}) shift due to free holes. These results suggest that high crystallinity channel with the defect density less than 1.0×10^{-17} cm^{-3} was formed by μ-TPJ crystallization of a-Si pattern with HSLC condition. The channel was behaved as intrinsic p- type nature by donor-type defect level. However, Fermi level was preciously controlled by slight N_C because of the extremely low defect density.

Figures 4.8(a) and (b) show superimposed transfer characteristics of n- and p-type short channel (L = 2 μm) TFTs with conventional patterns, respectively. Channel doping was carried out by N_C = 1.5 cm^{-3} on both of NMOS and PMOS. In the case of conventional pattern, n- and p-type TFTs showed high on/off ratio of ~10^6 and off current (I_{off}) of ~10^{-11} A, but still have variation even in short channel. On the other hand, strip pattern suppressed I_{off} and showed high on-state current compared with conventional pattern. Strip channel TFTs showed higher on/off ratio of ~10^8, and lower I_{off} of 10^{-13} A. So we investigated crystallinity of corresponding channels as shown in Fig. 4.9. In conventional pattern, random GB parallel to source and drain direction was formed (Fig. 4.9(a)). On the other hand, no GBs or only sigma 3 coincidence site lattice (CSL), which is thought to be electrically inactive [7-8], was formed in strip pattern (Fig. 4.9(b)). We found that random GBs in channel area degraded TFT characteristics and increased I_{off} even though

TABLE II. TFT characteristics with L =2 μm of (a) strip pattern and (b) conventional pattern shown in Figs. 4.8(a) and (b). Averages of μFE and Vth are calculated from 15 TFTs.

(a)

μ_{FE} [cm²/Vs]		W = 1μm	2 μm	3 μm	5 μm	10 μm
Conventional	NMOS	336	352	396	238	235
	PMOS	159	120	107	109	107
Strip	NMOS	433	411	393	390	380
	PMOS	160	143	140	145	141

(b)

V_{th} [V]		W = 1μm	2 μm	3 μm	5 μm	10 μm
Conventional	NMOS	3.4	3.7	3.8	4.2	4.4
	PMOS	-1.1	-1.2	-2.1	-1.2	-1.6
Strip	NMOS	3.6	3.6	3.6	3.7	3.7
	PMOS	-1.0	-1.2	-1.2	-1.3	-1.4

they did not cross over the channel. TFT characteristics are obviously improved including V_{th} (Table.I) In addition, we considered that high I_{off} in conventional pattern was mostly occupied by junction leakage current induced by carrier generation, such as re-combination, through random GBs [9-11]. It should be noted that random GBs, regardless whether they cross channel area or not, degraded TFT characteristics. These results suggest that grain growth control by strip pattern is quite effective even in the short channel in order to suppress the variation and off leakage current.

Next, we investigated the characteristics of self-aligned gate TFTs. The transfer characteristics of conventional and strip patterns with respect to W from 1 μm to 10 μm are shown in Tables II (a) and (b), respectively. In conventional pattern TFTs, degraded μ_{FE} and V_{th} shift with respect to W were observed (Table II (a)). Especially, the characteristics in W > 3 μm showed absolutely inferior characteristics in both n- and p-type TFTs. On the other hand, strip pattern showed stable characteristics in all W (Table II (b)). As typical GB maps are shown in Fig. 4.9, random GBs were formed in W > 3 μm, but were clearly suppressed in narrow strips. While μ_{FE} and V_{th} varied by increasing of W in conventional pattern, stable characteristics were obtained in strip pattern. As shown in Tables II (a) and (b), even though accurate control of N_c is necessary, n-type TFTs with strip patterns in all W showed μ_{FE} > 380 cm²/Vs and V_{th} = 3.6 ± 0.1 V. In the case of p-type TFTs, they were

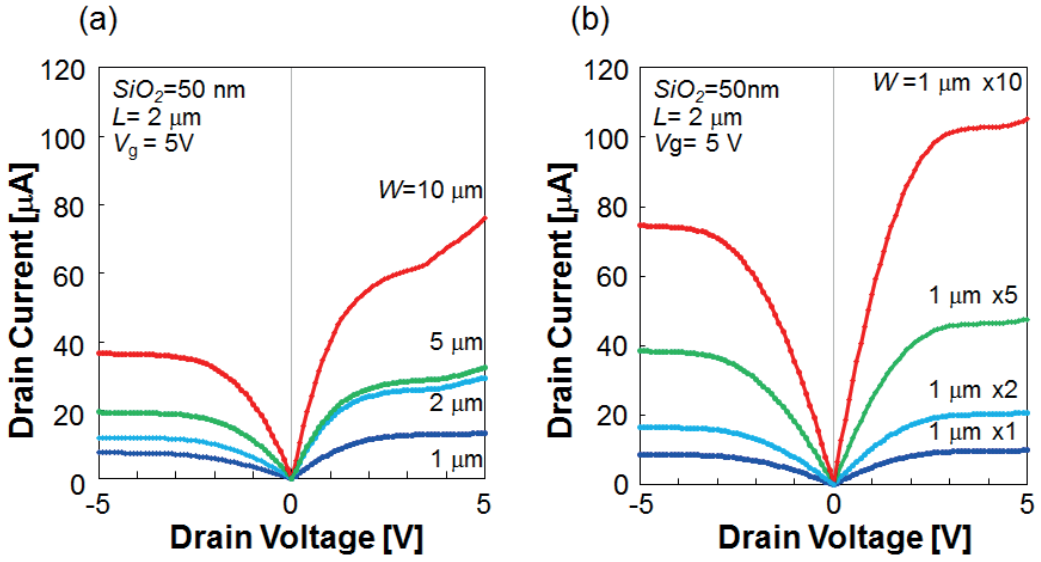

Fig. 4.10. (a) Schematic diagram of the control of Fermi level in channel area. Non doped channel is intrinsic P-type and were controlled by counter doping. (b) Transfer characteristics with respect to N_C.

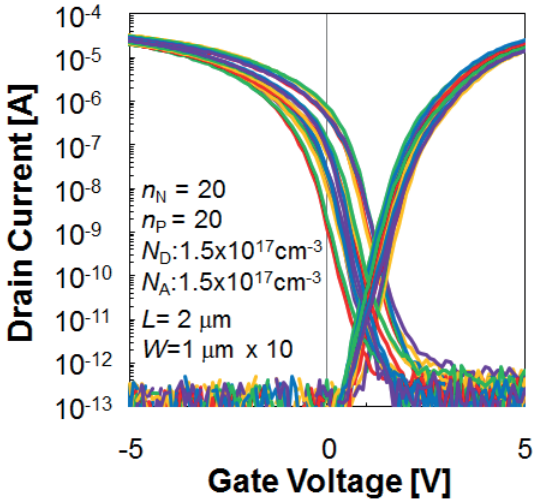

Fig. 4.11. (a) Schematic diagram of the control of Fermi level in channel area. Non doped channel is intrinsic P-type and were controlled by counter doping. (b) Transfer characteristics with respect to N_C.

μ_{FE} > 140 cm2/Vs and V_{th} = 1.2 ± 0.2 V. In addition, we investigated output characteristics with respect to W by conventional and strip pattern. While varied outputs, especially extremely low output in W = 10 μm, were obtained in conventional pattern, stable output relative to W were obtained in strip pattern. Furthermore, as shown in Fig. 4.10(a),

although the kink effect in n-type TFTs increased by degradation of V_{th} in conventional pattern, they were significantly suppressed in strip pattern by its uniformity of V_{th} (Fig.4.10(b)). In consideration of drawback of area loss by strip pattern as shown in Fig. 4.9(b), high μ_{FE} , low V_{th} and stable outputs by strip pattern are sufficient to compensate it as understood by the output characteristics, because variation of W is necessary to layout for any circuits or control V_{th} of CMOS invertor. Thus, strip pattern is quite promising for layout and operation of CMOS circuit with high reliability and low power consumption, unless we can ignore the effects by defects in crystal.

Finally we investigated characteristic variability of strip pattern TFTs with L = 2μm and W = 1 μm × 10 lines. As shown in Fig. 4. 11, TFTs showed still small variation and the control of sub-threshold characteristics by N_C was not enough. In order control short channel TFTs, we considered that precise control of Fermi level should be achieved. For this issue, higher crystallinity is strictly required.

4.4 Summary

The μ-TPJ irradiation to a-Si strip pattern is quite effective for grain growth control even in short channel TFTs. TFTs with the proposed pattern showed high performance and stable output characteristics. Even in consideration of area loss by strip pattern, this is quite promising to operate CMOS circuit on insulating substrate under low supply voltage with low power consumption.

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Chapter 5

Investigation of Intra-Grain Defect Formation in Amorphous Silicon Strips During Micro-Thermal-Plasma-Jet Irradiation

5.1 Introduction

In order to achieve high-speed CMOS circuit operation based on micro-thermal plasma jet (μ-TPJ) crystallization, high-performance thin-film transistor (TFT) with short channel length (L) is required. The summary of our previous work is as follows.

- Large grains ~60 μm was formed by high-speed lateral crystallization (HSLC) induced by μ-TPJ irradiation.
- Crystallographic orientations were not controlled but random grain boundaries (GBs) were suppressed using μ-TPJ crystallization of amorphous silicon (a-Si) strips.
- Small amount of defects less than 1.0×10^{17} cm^{-3} were remaining in the crystallized a-Si strips.
- Precise control of Fermi level is necessary in order to operate short channel TFTs.

From these results, going back to starting point, we attempted to improve the crystallinity. This means extremely high crystallinity almost as same as single crystalline silicon (c-Si) is required. So we investigated the formation of defects, not only GBs but also intra-grain defects.

5.2 Experimental procedure

5.2.1 Improvement of GBs and intra-grain defects in a-Si strips

In addition, the condition of μ-TPJ crystallization was optimized using TFT pattern with L = 10 μm and W = 1 μm. The μ-TPJ was irradiated on TFT patterns with the conditions of P = 1.3 kW, f = 1.0 L/min, and d = 1.0 mm. HSLC with different conditions were formed by changing only v ranged from 1200 mm/s to 1600 mm/s. Under the same power condition, the reaching temperature of surface increased by decreasing v [1]. The size and the temperature of molten region were increased by decreasing v. After crystallization of these TFT patterns, the pattern shape and GBs were investigated by SEM and EBSD. The intra-grain defects were observed by SEM after secco-etching.

Furthermore, non-contact temperature measurement of μ-TPJ crystallization was carried out. The transient reflectivity during μ-TPJ (Φ = 0.6 mm, P = 1.0- 1.3 kW, f = 1.5 L/min, d = 1.0 mm, and v = 600 – 1800 mm/s). HSLC with different conditions were formed by changing only v ranged from 1200 mm/s to 1600 mm/s.) was measured by irradiating the quartz substrate with a He-Ne laser (633 nm) from backside of the substrate and detecting the reflected light intensity using a photodiode through a band pass filter. The oscillation was reproduced by numerical simulations on heat diffusion and optical interference as shown in Sect. 2.3.

5.2.2 Optimization of the condition by μ-TPJ crystallization on a-Si strips

The relationship between electric property, which is extremely sensitive to defects, and channel crystallinity of TFTs was investigated. Un-doped a-Si film of t_{Si} = 200 nm was formed on quartz substrate by PECVD at 250ºC. Dehydrogenation was carried out in N_2 ambient at 450ºC for 1 hour. Then a-Si was patterned by CDE to form source, drain and strip channel with L = 10 μm and W = 1 μm. The μ-TPJ was irradiated on TFT patterns with the conditions of P = 1.4 kW, f = 1.0 L/min, and d = 1.0 mm. SPC, LWC, and HSLC with different conditions were formed by changing only v ranged from 1200 mm/s to 1700 mm/s. Then, S, D and C region were formed by P^+ ion implantation at the dose of 3.1×10^{15} /cm^2. After a 100-nm-thick gate SiO_2 was formed by the remote-PECVD at 350ºC [2]. μ-TPJ was irradiated again with the condition of P = 1.4 kW, d = 1.5 mm, f = 1.0 L/min, and v = 1900 mm/s. Under this condition, Si films were not melted, rather, dopant activation was achieved by rapid annealing. [3-4] After formation of contact holes by wet etching, Al-Si(1%)

electrodes were formed by DC sputtering and wet etching. Finally, post metallization annealing was performed at 400ºC in H_2 and N_2 ambient for 30 min. After measurement of electrical properties, active layer of Si was kept intact by etching off the gate (G) electrode and SiO_2. By comparison of the performance and the crystallinity of TFTs, subtle difference by intra-grain defect was investigated.

5.3 Results and discussion

5.3.1 Improvement of GBs and intra-grain defects in a-Si strips

In order to optimize ZMR condition of μ-TPJ, we investigated the crystallinity of 1 μm-wide channel by changing scanning speed ranging from v = 1200 to 1600 mm/s. As shown in Fig. 5.1(a), Si was agglomerated from C to S/D area and roughness was clearly formed in high-Temperature (T) condition of v = 1200 mm/s. On the other hand, agglomeration and the roughness were definitely suppressed in low temperature condition by increase of v to 1600 mm/s (Figs. 5.1 (b) and (c)). In addition, intra-grain defect in strip channel area was investigated by secco etching and SEM observation. As shown in Fig. 5.2 (a), volume reduction and many dislocations were observed in v = 1200 and 1400 mm/s. On the other hand, dislocations were significantly suppressed and smooth surface was formed in v = 1600 mm/s (Fig. 5.2(b)).

Here, we considered about melting duration. As shown in Fig. 5.3 (a), a-Si strips were rounded by surface tension of l-Si during μ-TPJ irradiation. However, sharp edge was formed in wide pattern (Fig. 5.3(b)). Here, Laplace pressure (p) of liquid on a substrate is written as

$$p = \frac{2\gamma_{LV}}{R} = \frac{2\gamma_{LV}cos\theta_C}{r}. \quad (1)$$

Here, γ_{LV} is the surface tension in liquid-vapor, θ_C is contact angle, R is curvature radius, and r is radius of liquid and substrate interface, respectively [5]. In the case of TFT pattern, p is varied by r and θ_C. In the case of Fig. 5.3(a), r = 0.4 μm and θ_C = 60º were

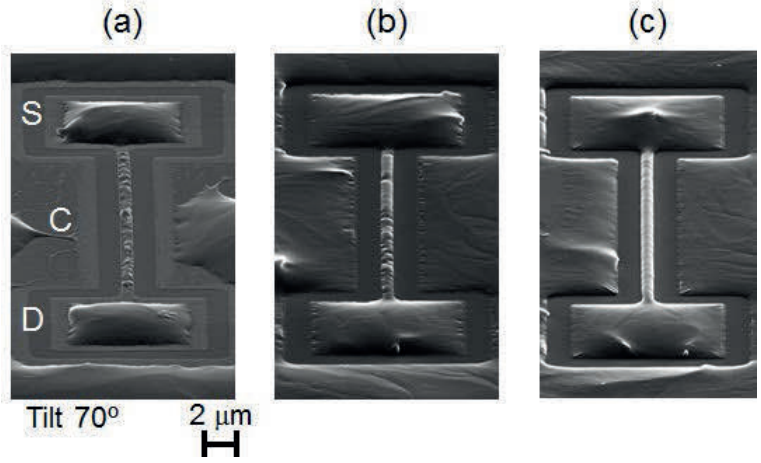

Fig. 5.1. SEM images tilted by 70º of TFT patterns crystallized by (a) v =1200 mm/s, (b) v = 1400 mm/s, and (c) v = 1600 mm/s.

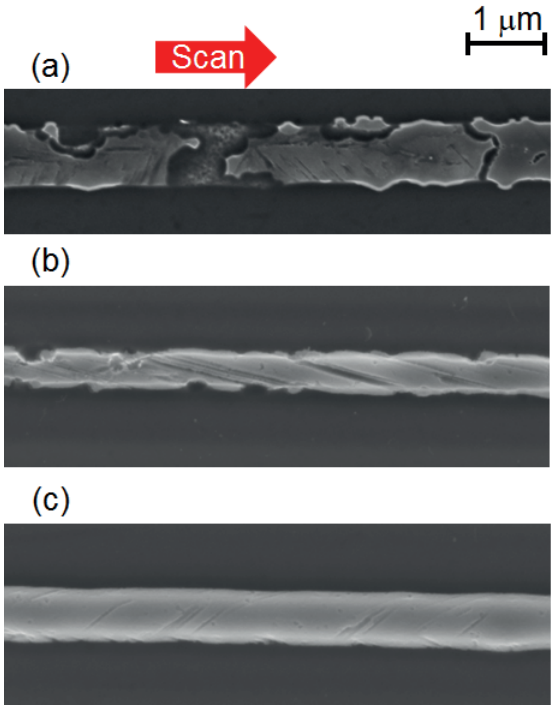

Fig. 5.2. SEM images of strips crystallized by (a) v = 1200 mm/s, (b)1400 mm/s, and (c) 1600 mm/s. These maps were observed after secco etching at the same positions Figs. 5.1 (a), (b), and (c), respectively.

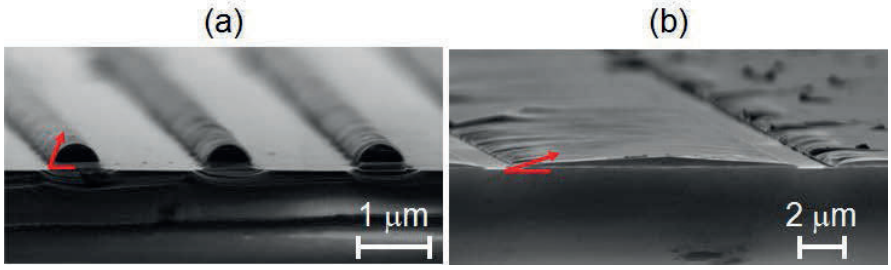

Fig. 5.3. Cross section SEM images of crystallized patterns on quartz substrate with the width of (a) W = 1 μm and (b) W = 10 μm. The contact angle (θ_C) were 60º and 20º, respectively.

measured. In the case of Fig. 5.3(b), they were r = 4.9 μm and θ_C = 20º. From these parameters, p in C (p_C) and p in S/D ($p_{S/D}$) are unbalanced with the ratio of $p_C/p_{S/D}$ = 6.6. In addition, the property of l-Si with respect to temperature, such as surface tension, density, and viscosity have been investigated in Refs. 6 - 8. Above all, viscosity of l-Si is rapidly decreased around melting point by increase of temperature [8]. Here, fluid flow (Q) was written as

$$Q \sim \frac{t_{Si}^3}{\eta} f \quad , \tag{2}$$

$$f = p\frac{dv}{dt} \quad . \tag{3}$$

Here, η and f are the viscosity and force per unit area, respectively. As above, in the case with v = 1200 mm/s, l-Si is easy to move by low-viscosity and unbalance of p_C and $p_{S/D}$. During mass transfer of l-Si, roughness was formed by the instability of surface tension on the melt [9]. On the other hand, agglomeration was suppressed and smooth surface was formed by high- viscosity in the case with v = 1600 mm/s. These results suggested that instability of surface tension due to agglomeration affected the formation of dislocations. So we concluded that it is quite promising to suppress the reaching temperature and mass transfer of l-Si by fast scan for suppression of in-grain defect, such as dislocations.

So we investigated the reaching temperature with respect to μ-TPJ conditions. Figure 5.4 shows the reaching temperature at the surface of quartz substrate by non-contact measurement. The temperature dependence of v using different P from 1.0 to 1.3 kW were investigated. As shown in Figs. 5.4, the reaching temperature was controlled by scanning speed of μ-TPJ in each P condition. As shown in Figs.5.5(a) and (b), smooth surface and extremely suppressed dislocations were formed at the reaching temperature of 1704 and 1696 K by P = 800 mm/s and 1500 mm/s, respectively. On the other hand, dislocations were obviously increased at the higher reaching temperature of 1766 and 1814 K by P = 700 mm/s and 1400 mm/s, respectively (Figs.5.6(c) and (d)). These results suggest that μ-TPJ crystallization with the reaching temperature at most T_m + 60 K is effective to suppress the formation of intra-grain defects.

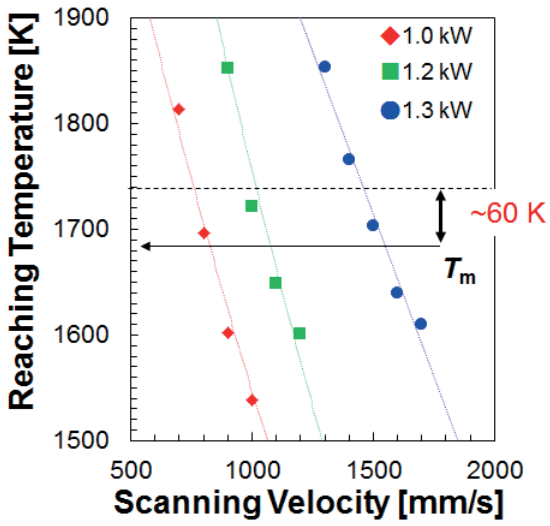

Fig. 5.4. The reaching temperature dependence by v using different P from 1.0 to 1.3 kW. The intra-grain defects were significantly suppressed at reaching temperature within ~ 60 K upper T_m.

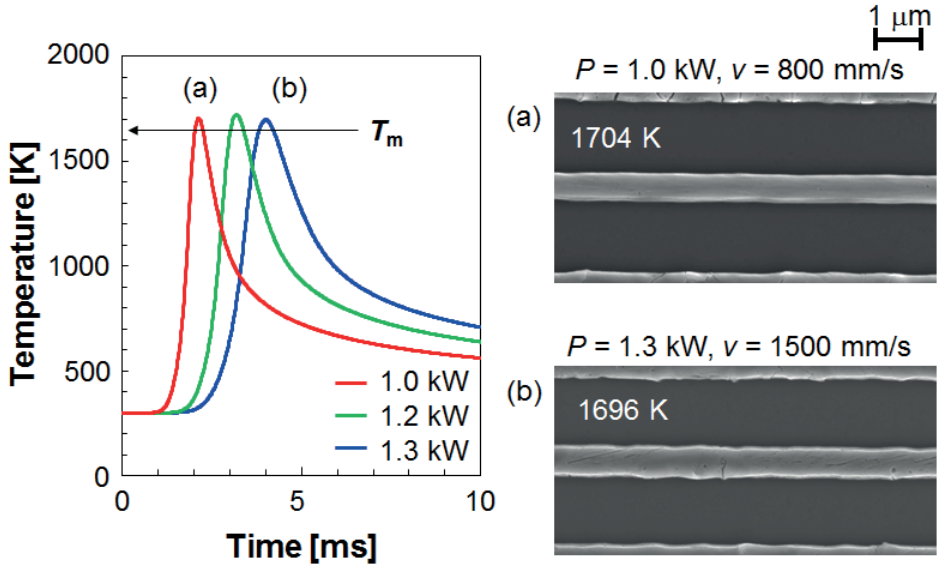

Fig. 5.5. Transition of substrate surface temperature during μ-TPJ irradiation. The reaching temperature was 1696, 1722, and 1704 K, by v = 800, 1000 and 1500 mm/s, respectively. SEM images of strips after Secco etching by different condition of (a) P = 1.0 kW and v =800 mm/s, (b) P = 1.3 kW and v =1500 mm/s.

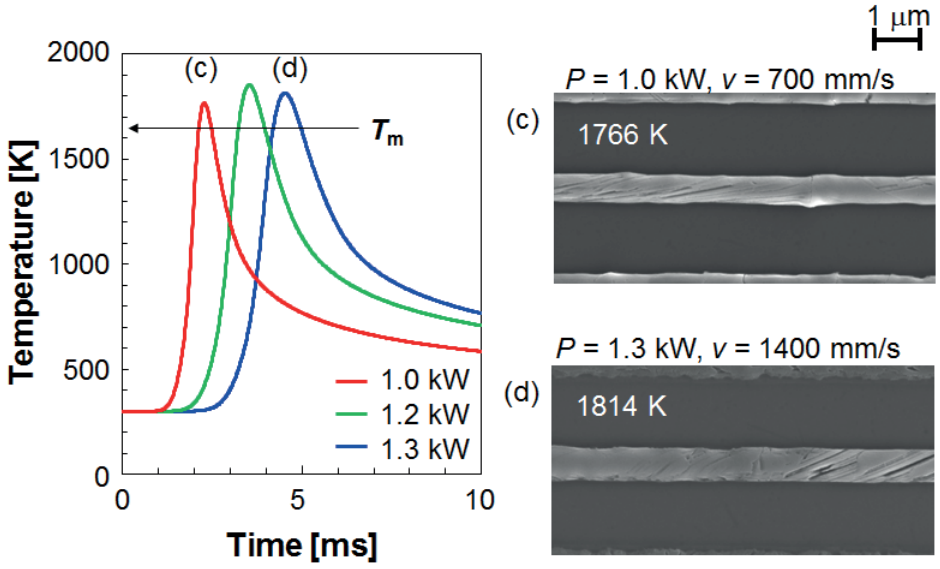

Fig. 5.6. Transition of substrate surface temperature during μ-TPJ irradiation. The reaching temperature was 1814, 1852, and 1766 K, by v = 700, 900 and 1400 mm/s, respectively. SEM images of strips after Secco etching by different condition of (a) P = 1.0 kW and v =700 mm/s, (b) P = 1.3 kW and v =1400 mm/s.

5.3.2 Optimization of the condition by μ-TPJ crystallization on a-Si strips

In order to confirm the optimized condition of μ-TPJ irradiation, we fabricated TFTs by different crystallization conditions from v = 1200 and 1700 mm/s. N-ch TFTs with L = 10 μm and W = 1 μm were investigated. Figure 5.7 shows transfer characteristics of TFTs with respect to v. TFTs with the conditions of SPC by v = 1700 mm/s, LWC by v = 1600 mm/s, and HSLC by v = 1500 ~ 1200 mm/s were fabricated. As shown in Figs. 5.8 (a) and (b), by changing crystallization mode from SPC to HSLC, field effect mobility (μ_{FE}) and swing factor (S) were markedly improved due to enlargement of grain size [10]. However, among HSLC condition, they were significantly degraded by decreasing v. All of these conditions, HSLC by v = 1500 mm/s showed the best performance with the highest μ_{FE} of 443 cm^2/Vs and the lowest S of 210 mV/dec. In order to investigate these differences in TFT performance, the crystallinity of channels was investigated after removing the gate electrode and insulator. As shown in Figs. 5.9 (a) to (d), there were no GBs except Σ3 coincidence site lattice (CSL) in all conditions, but surface roughness was formed by decreasing v as same as Fig. 5.1. Because the reaching temperature of ZMR is higher than melting point (T_m) (1687 K) and the viscosity of liquid Si (l-Si) is rapidly decreased around T_m [8]. In order to suppress the mass transfer from C to S/D by agglomeration, keeping relatively high viscosity near T_m is quite effective. From these results, 1 μm-wide strip

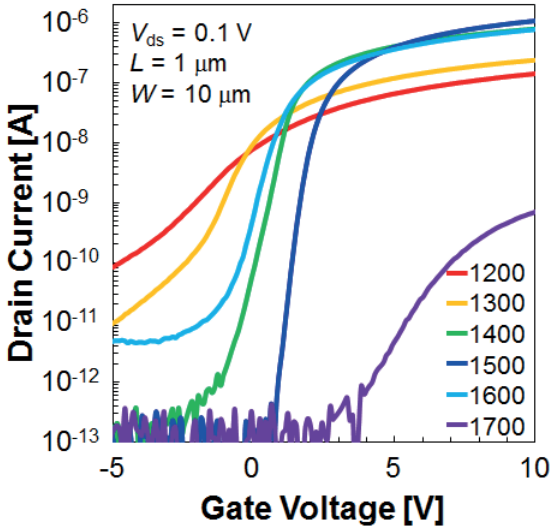

Fig. 5.7. Transfer characteristics of TFTs with different v from 1200 to 1700 mm/s..

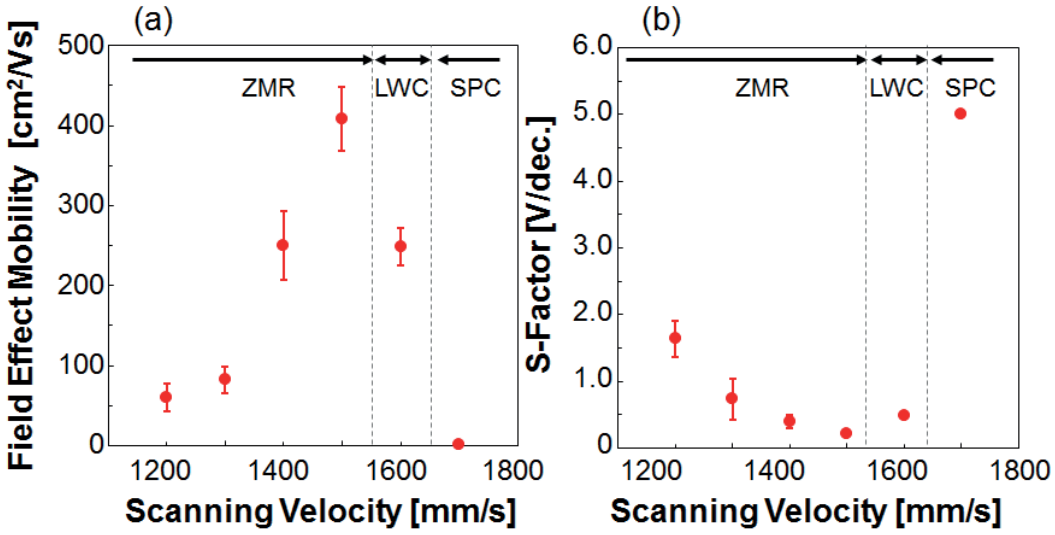

Fig. 5.8. TFT characteristics with respect to v of (a) μ_{FE} and (b) S. 5 TFTs were investigated for each plot.

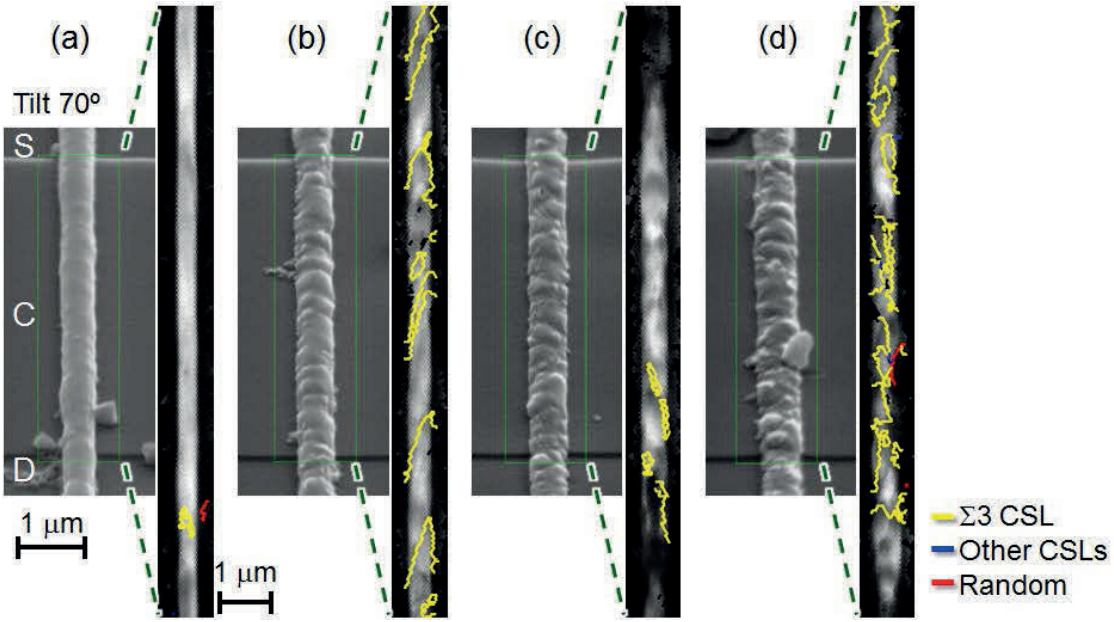

Fig. 5.9. SEM images tilted by 70º and map of GBs in TFTs crystallized by (a) v =1500 mm/s, (b) v = 1400 mm/s, (c) v = 1300 mm/s, and (d) v = 1200 mm/s. These maps were observed at the same positions with channel area of Figs. 5.7 and 5.8 after peeling off the gate electrode and insulator.

pattern and optimized HSLC condition by μ-TPJ around T_m formed extremely high-crystallinity.

5.4 Summary

High-performance TFTs have achieved by LTPS technology on the basis of μ-TPJ crystallization. Strip pattern is effective to suppress random GBs. In-grain defect is improved by control of surface tension. These high-crystallinity enabled precise control of Fermi level in channel and operation of short channel TFT. This technique is quite promising for next generation displays in terms of low cost process and high-performance.

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Chapter 6

High-Speed Operation of CMOS Circuit with Short Channel TFTs

6.1 Introduction

A high-crystallinity channel was formed by suppressing random grain boundaries (GBs) and intra-grain defects, such as dislocations. Using micro-thermal-plasma-jet (μ-TPJ) crystallization on amorphous silicon (a-Si) strip pattern, random GBs were eliminated. In addition, by optimizing the condition of μ-TPJ irradiation at the reaching temperature around melting point (T_m) of crystalline Si (c-Si) , intra-grain defects were obviously improved. These high-crystallinity channel is quite promising for high-performance thin film transistor fabrication and high-speed CMOS circuit operation.

In this work, we attempted operate TFTs with short channel length (L) and CMOS circuit at a very high-speed.

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6.2 Experimental procedure

6.2.1 Characteristic variability of short channel TFTs with respect to channel width

We attempted to operate CMOS circuit using TFTs with short L of 1 μm. In order to fabricate CMOS, the process steps were for self-aligned top gate structure as same as Sect. 3.2.3. Because of simple process steps, additional structure, such as lightly doped drain (LDD), was not formed. The process steps were as follows (Fig. 6.1). After formation of TFT patterns, non-doped and doped channels were formed by B^+ and P^+ implantation. The doping concentrations of donor (N_D) and acceptor (N_A) were changed at the dose (1.0 – 3.0) × 10^{12} cm^{-2} on NMOS and PMOS region, respectively. The a-Si patterns were crystallized by μ-TPJ irradiation with the conditions of P = 1.3 kW, f = 1.0 L/min, d = 1.5 mm, and v = 1400 mm/s. The thickness of gate SiO_2 was reduced from 100 nm to 50 nm, gate Al electrode was replaced with a-Si by low pressure CVD (LPCVD) at 520 ºC and heavily doped simultaneously with S and D (self-align). P^+ and BF_2^+ were implanted at the dose of 6.0 × 10^{15} cm^{-2} on NMOS and PMOS region, respectively. A 650-nm-thick interlayer dielectric was added in order to form metal wire.

Characteristic variability of short channel TFTs with strip and conventional patterns were

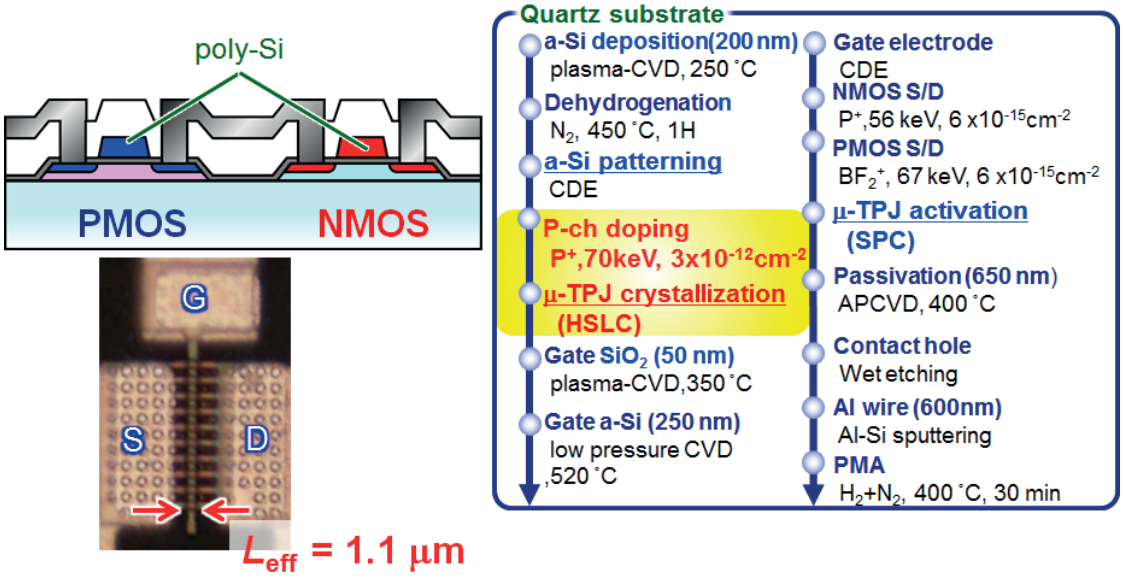

Fig. 6.1. The fabrication process steps of self-aligned CMOS TFTs. The modified process steps from Sect. 3.2.3 are channel doping to PMOS and μ-TPJ crystallization condition.

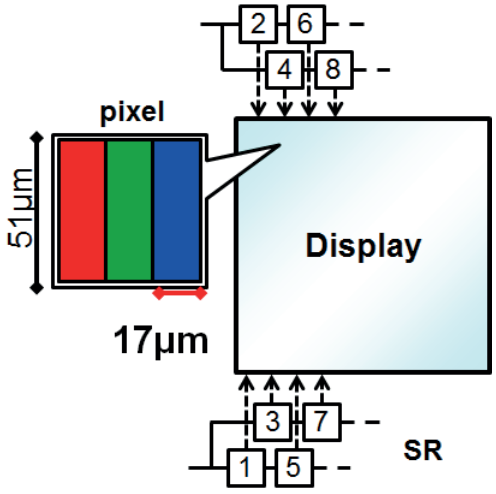

Fig. 6.2. The schematic diagram of peripheral circuit for 500 ppi display. By 4 parallel driving of pixels with 17 μm pitch, SRs were formed with a bit pitch of 68 μm

investigated. The strip pattern was formed by 1μm wide strips, not only in the channel area but also in the source and drain area to suppress the agglomeration on the melt (L = 1 μm and W = 1 μm times 1 - 10 lines).

6.2.2 CMOS circuit operation using short channel TFTs

CMOS circuits with conventional and strip patterns were also fabricated. For the measurement of CMOS circuit, an active prove with the capacity of 0.1 pF was used.

Firstly, shift register (SR), which is commonly formed for peripheral circuit of displays, were formed. As shown in Fig. 6.1, SR was formed with a bit pitch of 68 μm with the object of high integration of peripheral circuits for 500 pixels per inch (ppi) displays by 4 parallel driving. Ring oscillator, which shows the maximum operation frequency of circuit, were evaluated.

6.3 Results and discussion

6.3.1 Characteristic variability of short channel TFTs with respect to channel width

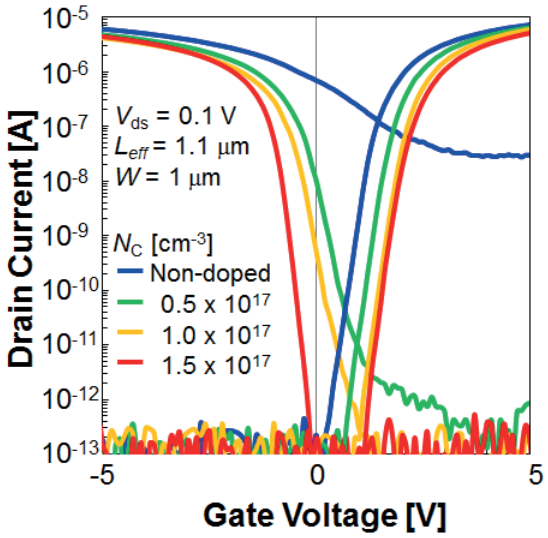

Fig. 6.3. Transfer characteristics of TFTs with respect to N_C. B^+ was doped on NMOS and P^+ was doped on PMOS region, respectively.

Table I. Characteristics of TFTs with respect to doping concentrations. (a) B^+ was doped on NMOS and (b) P^+ was doped on PMOS.

(a)

N_D (cm^{-3})	μ_{FE} (cm^2/Vs)	V_{th} (V)	S (mV/dec.)
Non-doped	553	1.7	182
5.0×10^{16}	564	2.1	174
1.0×10^{17}	556	2.4	172
1.5×10^{17}	498	2.6	158

(b)

N_A (cm^{-3})	μ_{FE} (cm^2/Vs)	V_{th} (V)	S (mV/dec.)
Non-doped	316	0.6	832
5.0×10^{16}	330	-0.1	252
1.0×10^{17}	317	-0.9	230
1.5×10^{17}	308	-1.3	158

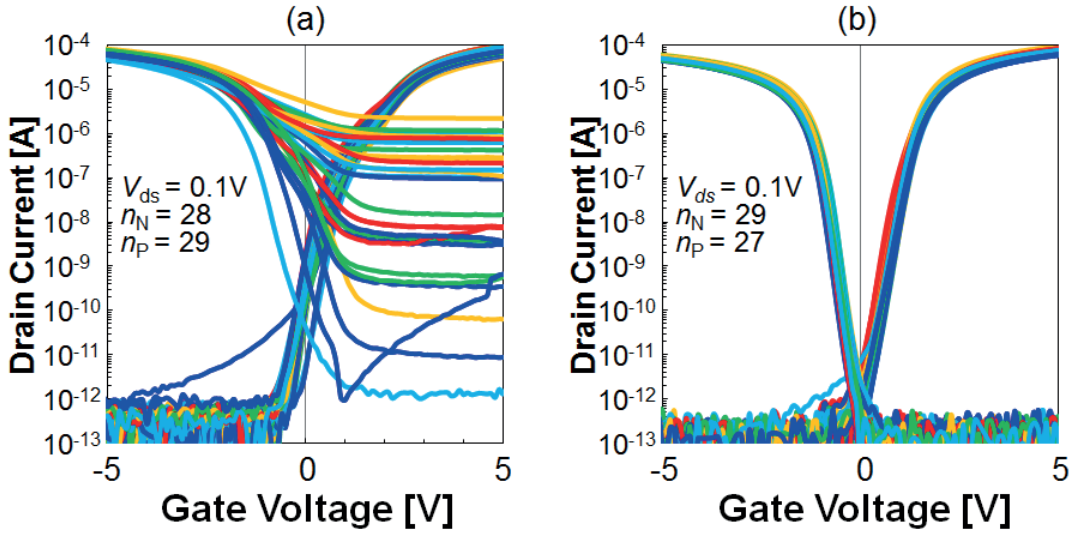

Fig. 6.4. Transfer characteristics of TFTs with (a) conventional pattern (L_{eff} =1.1 µm, W = 10 µm) and (b) strip pattern (L_{eff} =1.1 µm, W = 1 µm times 10 lines)

Table II. Characteristics of TFTs shown in Figs. 13(a) and (b).

(a)

	μ_{FE} (cm^2/Vs)	V_{th} (V)	S (mV/dec.)
NMOS	493 ± 94	2.3 ± 0.51	223 ± 46
PMOS	314 ± 43	-1.3 ± 0.22	1102 ± 654

(b)

	μ_{FE} (cm^2/Vs)	V_{th} (V)	S (mV/dec.)
NMOS	503 ± 54	1.7 ± 0.06	196 ± 15
PMOS	335 ± 30	-1.4 ± 0.07	152 ± 17

TFTs with the effective channel length (L_{eff}) of 1.1 µm were successfully fabricated (Fig. 6.1). We firstly investigated NMOS and PMOS characteristics with respect to N_C as shown in Fig. 6.3. Non-doped channel TFTs behaved as intrinsic p-type by donor-type defects in deep state and showed obviously high off current as same as Sect. 4.3.2. However, subthreshold characteristics were precisely controlled by slight channel doping of 5.0 × 10^{16} cm^{-3} as shown in Table I. This suggests that high crystallinity channel with slight defect density less than 5 × 10^{16} cm^{-3} enabled precise control of Fermi level [1]. NMOS with non-doped channel and PMOS with N_A = 1.5 × 10^{16} cm^{-3} were applied because they were well balanced for CMOS operation.

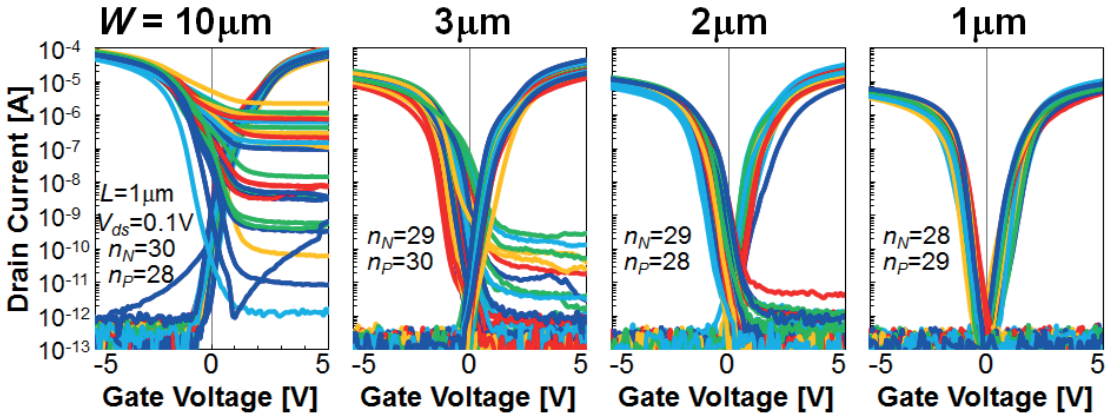

Fig. 6.5. Transfer characteristics of TFTs conventional pattern of L_{eff} = 1.1 μm and W = 1 – 10 μm.

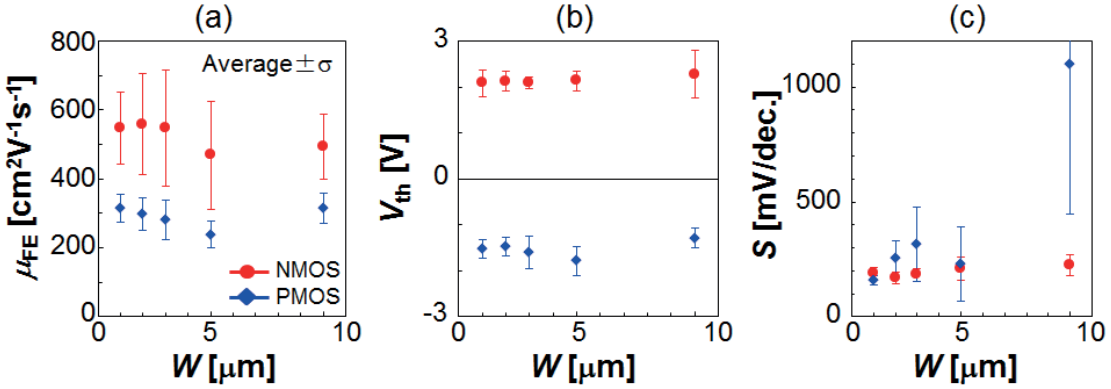

Fig. 6.6. Characteristic variability of TFTs with conventional pattern TFTs with respect to W. Average and standard deviation (σ) of (a) μ_{FE}, (b) V_{th}, and (c) S are calculated by more than 25 TFTs. They were calculated using TFTs shown in Fig.6.5.

Characteristic variability with conventional and strip channel were investigated by 30 TFTs. As shown in Fig. 6.4 (a), conventional pattern showed large variation especially in PMOS. On the other hand, as shown in Fig. 6.4 (b) and Table II, characteristic variability was significantly suppressed to at least 1/3 by strip pattern. In the case of conventional pattern, subthreshold characteristics, such as I_{off} and S, were gradually degraded by increasing W as shown in Figs. 6.5. As shown in Figs. 6.5(a)-(c), characteristics variability was gradually increased in conventional pattern by increase of W. Especially, subthreshold characteristics in p-type TFTs were obviously degraded. It should be noted that, in conventional pattern, degradation with respect to W was clearly observed even in the case of W = 2 or 3 μm. These variation and I_{off} with respect to W is hardly promising

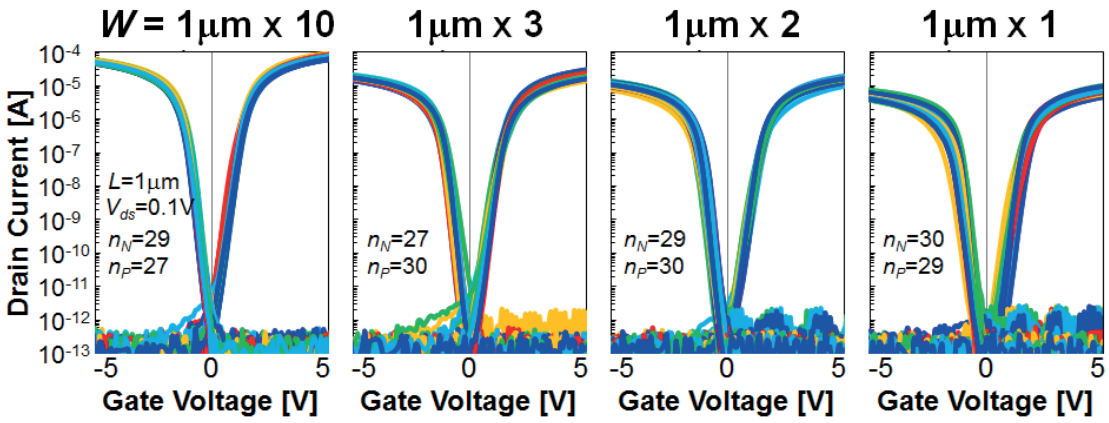

Fig. 6.7. Transfer characteristics of TFTs conventional pattern of L_{eff} = 1.1 μm and W = 1 μm × 1 – 10 lines.

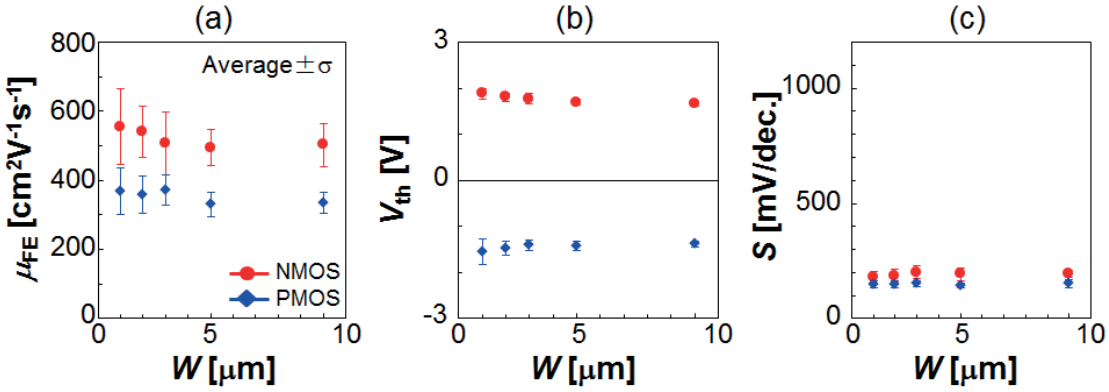

Fig. 6.8. Characteristic variability of TFTs with strip pattern TFTs with respect to W. Average and standard deviation (σ) of (a) μ_{FE}, (b) V_{th}, and (c) S are calculated by more than 25 TFTs. They were calculated using TFTs shown in Fig.6.7.

for circuit layout. On the other hand, as shown in Figs.6.7 and 6.8(a)-(c), strip pattern showed uniform characteristics in all W. These results suggest that channel crystallinity is not limited to just a crystallization condition. In-grain defect was suppressed only in narrow strips.This result indicate that defects density increase by increasing W and Fermi level became uncontrollable. On the other hand, as shown in Figs. 6.8(a) to (c), strip pattern TFTs showed uniform characteristics in all W. As opposed to conventional pattern, characteristics variability was gradually improved by increasing W. In the case of 1 line (i.e W = 1 μm x 1), μ_{FE} showed still variation, because crystallographic orientations were not controlled. By averaging characteristics in each strip channels, the variations were gradually suppressed with increase of W. This performance by strip pattern is quite

promising for CMOS operation by low supply voltage (V_{dd}) and low power consumption of circuits.

6.3.2 CMOS circuit operation using short channel TFTs

Subsequently, we attempted to operate SR, which is one of the key circuits for the peripheral driver of flat panel displays (Fig. 6.9) [2-5]. 8-bit SR with a bit pitch of 68 μm was formed by conventional and strip patterns as shown in Figs 6.10 (a) and (b). Contrary to our expectation, The SRs with both patterns were successfully operated. As shown in Figs 6.11 (a) and (b), 8-bit SRs with both patterns were operated at V_{dd} = 5V by a clock frequency of 50 MHz. These results indicated that the operation clock frequency of SR does not show the highest speed because of the parasite resistance and capacity in the

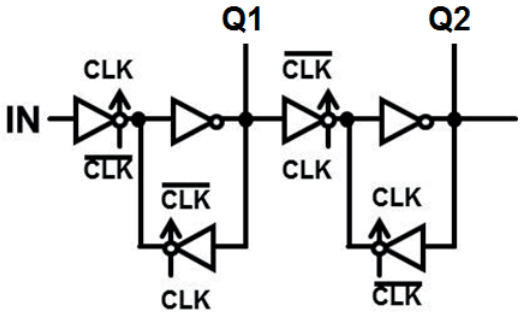

Fig. 6.9 Circuit diagram of SR for peripheral circuit of flat panel displays.

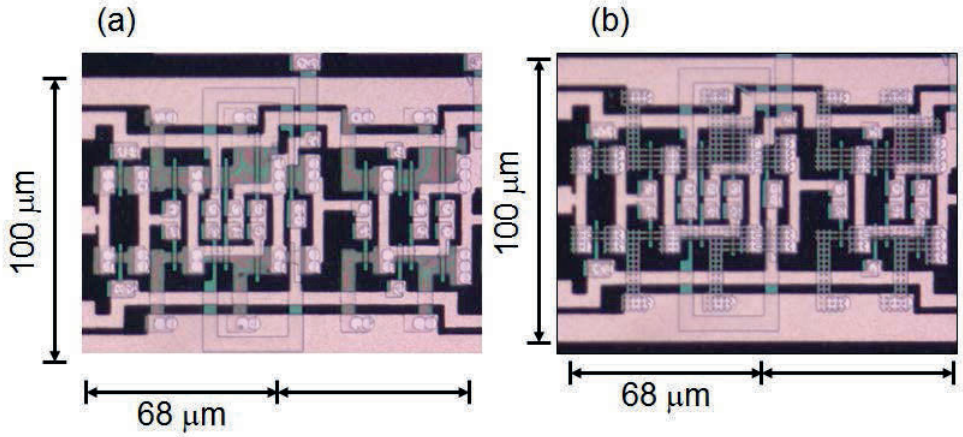

Fig. 6.10 Optical microscope images of SR with (a) conventional and (b) strip pattern TFTs.

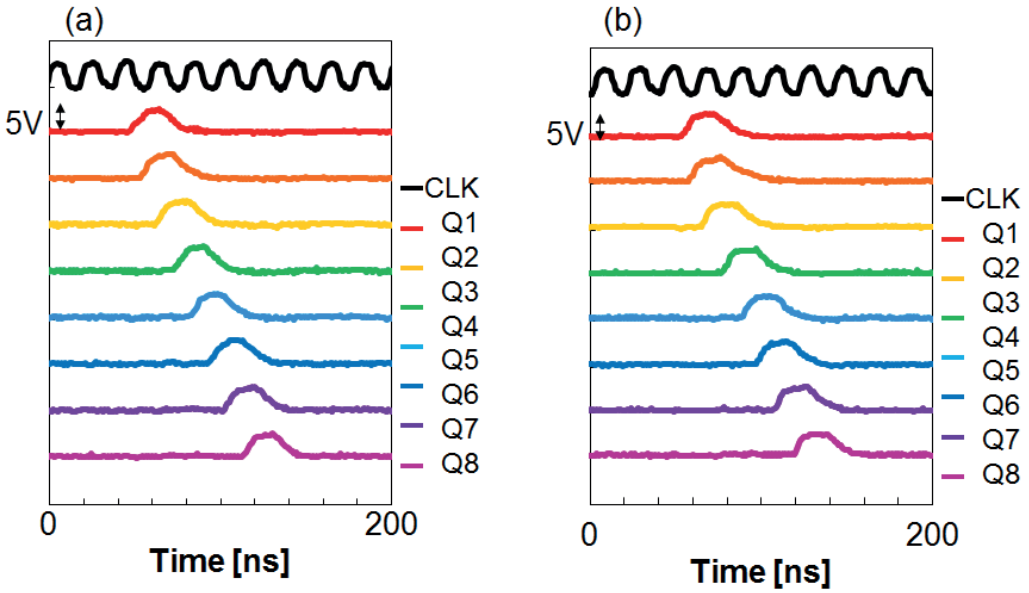

Fig. 6.11 Output characteristics of 8-bit SR with (a) conventional and (b) strip pattern TFTs operated at V_{dd} = 5V by clock frequency of 50 MHz.

circuit. In addition, 0.1 pF of active prove is too large to measure at a high speed without buffer circuits. So SRs with conventional and strip patterns should be operated at higher speed and there should be a difference of operation speed between both patterns. We confirmed that TFTs have a capability of higher speed operation because of their high μ_{FE} with 500 cm^2/Vs.

Then, we investigated the delay time (τ) by ring oscillator (RO), which shows the highest oscillation frequency (Fig. 6.12) [6]. As shown in Fig. 6.13, RO with both pattern was oscillated from 3 V. Strip pattern showed 107.5 MHz at V_{dd} =5 V in contrast with 50.8 MHz by conventional pattern. Strip pattern showed τ = 0.52 ns twice as high as τ = 0.94 ns by conventional pattern. From these results, a uniformity and small V_{th} by strip pattern enabled high-speed operation of CMOS circuit. A low cost crystallization technique using μ-TPJ achieved higher μ_{FE} over 500 cm^2/Vs and equally low variation compared with advanced ELA technique.[18] We could demonstrate a high performance for next generation displays by μ-TPJ crystallization on strip pattern.

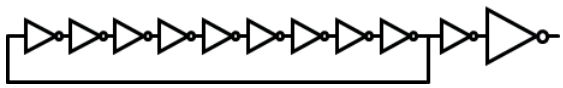

Fig. 6.12 Output characteristics of 8-bit SR with (a) conventional and (b) strip pattern TFTs operated at V_{dd} = 5V by clock frequency of 50 MHz.

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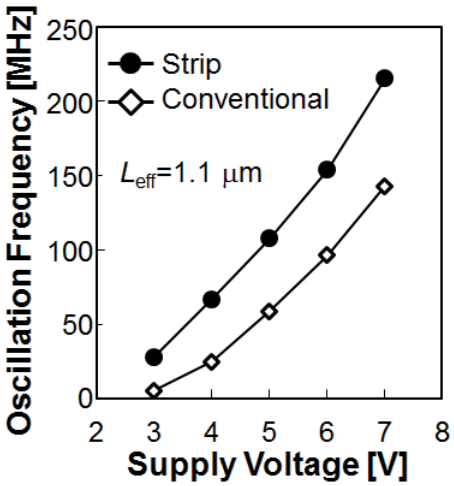

Fig. 6.13 Output characteristics of 8-bit SR with (a) conventional and (b) strip pattern TFTs operated at V_{dd} = 5V by clock frequency of 50 MHz.

6.4 Summary

High-performance TFTs have achieved by LTPS technology on the basis of μ-TPJ crystallization. Strip pattern is effective to suppress random GBs. Intra-grain defect is improved by control of surface tension. These high-crystallinity enabled precise control of Fermi level in channel and operation of short channel TFT. This technique is quite promising for next generation displays in terms of low cost process and high-performance.

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Conclusion

I have proposed a new TFT pattern which is composed of 1-μm-wide strip channels for μ-TPJ crystallization. This strip channel is effective to control lateral growth during μ-TPJ irradiation. By suppressing the collision of liquid and solid interface, random GBs were eliminated by filtering effects. In addition, by applying this strip to channel area of TFTs, field effect mobility higher than 300 cm^2/Vs with significantly low variation were achieved. These high-performance enabled us to operate CMOS circuits. We fabricated a shift register (SR), which is one of the key circuits for the peripheral driver of displays. To evaluate the effect of channel patterns, we fabricated SR with both patterns. We could not operate SRs with conventional pattern because of the poor yield as mentioned previously. We fabricated the SR with the strip channel pattern. We were able to operate 8-bit shift-register at a supply voltage of 5V and a clock frequency of 4 MHz. This low-voltage operation was achieved because the proposed strip channel pattern can effectively to improve both the yield and performance of TFTs. This result demonstrates that the μ-TPJ crystallization process on a-Si strip pattern is quite promising for the fabrication of high-performance displays.

In order to achieve higher-performance of TFTs and higher-speed operation of CMOS circuits, we attempted to improve the crystallinity. After suppressing random GBs, it was clarified that there exists a small amount of defects less than $1.0 \times 10^{17}\ cm^{-3}$. In order to control short channel TFTs, accurate control with lower defect density was strictly required. From the investigation of these intra-grain defects formation, suppressing the agglomeration during melting period is quite important for higher crystallinity. In order to suppress the agglomeration of liquid silicon, the suppression of reaching temperature less than melting point plus 60 K by fast scan is effective. By these optimized μ-TPJ condition, intra-grain defects, such as dislocations, were significantly suppressed.

From these realization, short channel TFTs with the effective length of 1.1 μm was successfully operated. They shoed extremely high field effect mobility of $503 \pm 63\ cm^2/Vs$. By applying short channel TFTs to CMOS fabrication, SR was operated by supply voltage of 5 V, at the clock frequency of 50 MHz. A 9-stage ring oscillator fabricated with conventional TFTs was operated at F= 58 MHz under supply voltage of 5V which corresponds to 1-stage delay (τ) of 0.94 ns. On the other hand, in the case of strip channel TFTs, F increased to 108 MHz and τ decreased to 0.52 ns. It should be noted that the μ_{FE} of each channel pattern is not largely different, but the significant differences are its

variability and sub-threshold uniformity. Therefore, elimination of random GBs and suppression of characteristic variability is essentially important for high speed CMOS operation.

Acknowledgement

I am most indebted to my principal supervisor professor Seiichiro Higashi, supporting me by keeping my research on track with logical consistency. He advanced me with gentlemanship by taking his time freely for fruitful discussions and putting through a large variety of experiences. I could not have completed my thesis without his great deal of supports.

I would like to appreciate Professor James S. Im (Columbia University) for giving me guidance in scientific thinking through a collaborative research and discussions. His respectful humanity changed my way of thinking about a lot of things.

I am grateful to Professor Shin Yokoyama for supporting kindly my research, especially fabrication process of devices. His thoughtful advices and guidance expand my knowledge of semiconductor devices.

My sincere appreciation is extended to Professor Takamaro Kikkawa, Associate Professor Shin-Ichiro Kuroki, Associate professor Tetsuo Tabei, Assistant professor Hideki Murakami, Assistant professor Yoshiteru Amemiya, Assistant Professor Akio Ohta (Nagoya University), and Assistant professor Hiroaki Hanafusa.

I would like to give special thanks to Dr. Shohei Hayashi (Toray Industries, Inc.), Dr. Kohei Sakaike (Toshiba Corporation), Dr. Muneki Akazawa (SanDisk Limited), Mr. Yuji Fujita (Towa Corporation), and Mr. Shogo Yamamoto (Toshiba corporation).

I also would like to acknowledge Radial Research Group (Department of Applied Physics and Applied Mathematics, Columbia University): Dr. Alexander B. Limanov, Mr. Adrian Chitu, Mr. Jin Wang, Ms. Ying Wang, Mr. Vernon Wang, Mr. Miao Yu, Mr. Jaewon Moon, and Wenkai Pan, for their kind supports and discussions.

I would like to acknowledge my fellow students in Semiconductor Laboratory (Graduate School of Advance Sciences of Matter, Hiroshima University) for their kind supports and discussions.

I am also grateful to the professors of the graduate school of Advanced Sciences of Matter for their kind and relevant advice.

I owe Oki Digital Imaging Corporation a great debt of gratitude for their kind understanding to my retirement. I had learned a lot of things on the job through their kind advices.

A part of this work was supported by the Research Institute for Nanodevice and Bio Systems (RNBS) and the Natural Science Center for Basic Research and Development (N-BARD), Hiroshima University and the Funding Program for Next Generation World-Leading Researchers (NEXT Program) from the Japan Society for the Promotion of Science (JSPS).

Finally, I would like to express my gratitude to my family for their understanding and spiritual supports.

2015

Seiji Morisaki

List of Publications and Awards

Papers related to this thesis

International conference papers

1. Seiji Morisaki, Shohei Hayashi, Yuji Fujita, and Seiichiro Higashi,
   "Improvement in Characteristic Variability of Thin Film Transistors Using Grain Growth Control by Micro Thermal Plasma Jet Irradiation to Amorphous Silicon Strips and CMOS Circuit Operation at Supply Voltage of 5V",
   The 9th International Thin-Film Transistor Conference (ITC 2013) (Tokyo, Japan, Mar. 1-2, 2012) [2pAO05]
2. Takahiro Kamikura, Shohei Hayashi, Seiji Morisaki, Yuji Fujita, Muneki Akazawa, and Seiichiro Higashi,
   "Explosive Crystallization of Amorphous Germanium Films Induced by Atmospheric Pressure Micro-Thermal-Plasma-Jet Irradiation",
   Proceedings of 8th International Conference on Silicon Epitaxy and Heterostructures (ICSI-8) and the 6th International Symposium on Control of Semiconductor Interfaces (ISCSI-VI) (Fukuoka, Japan, Jun. 2-7, 2013) pp.157-158.
3. Seiichiro Higashi, Shohei Hayahi, Seiji Morisaki, and Yuji Fujita,
   "Growth Control of Crystalline Silicon during Microsecond Phase Transformation and Its Application to Thin-Film Transistor Fabrication,"
   Proceedings of 2013 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices(AWAD2013),(Seoul, Korea, Jun. 26 - 28 , 2013), pp. 265-269.
4. Shohei Hayashi, Yuji Fujita, Seiji Morisaki, Takahiro Kamikura, Shogo Yamamoto, Muneki Akazawa, and Seiichiro Higashi,
   "Grain Growth Control by Micro-Thermal-Plasma-Jet Irradiation to Amorphous Silicon Strips through Slit Masks and Its Application to High-Performance Thin-Film Transistors",
   Proceedings of the Twentieth International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD 13) (Kyoto, Japan, Jul. 2-5, 2013) pp. 113-116.
5. Shohei Hayashi, Seiji Morisaki, Takahiro Kamikura, Shogo Yamamoto, Kohei Sakaike,

Muneki Akazawa, and Seiichiro Higashi, "Grain Growth Control during Leading Wave Crystallization Induced by Micro-Thermal-Plasma-Jet Irradiation to Amorphous Silicon Films",
Proceedings of 35th International Symposium on Dry Process (DPS2013) (Jeju, Korea, Aug. 29-30, 2013) pp. 43-44.

6. Seiichiro Higashi, Kohei Sakaike, Shohei Hayashi, Seiji Morisaki, Muneki Akazawa, Shogo Nakamura, and Takashi Fukunaga,
"Low-Temperature Formation of Single-Crystalline Silicon on Glass and Plastic Substrates and Its Application to MOSFET Fabrication",
Proceedings of 20th International Display Workshops (IDW'13) (Sapporo, Japan, Dec. 4-6, 2013) pp. 258-261.
7. Seiji Morisaki, Shohei Hayashi, Takahiro Kamikura, Shogo Yamamoto, and Seiichiro Higashi,
"Fabrication of Short Channel Thin Film Transistors by Channel Doping and Micro Thermal Plasma Jet Crystallization and Their Application to High Frequency Operation of CMOS Circuits",
The 10th International Thin-Film Transistor Conference (ITC2014) (Delft ,Netherlands, Jan.23-24,2014) p.15.
8. Shohei Hayashi, Seiji Morisaki, Shogo Yamamoto, Taichi Nakatani, and Seiichiro Higashi,
"Grain Growth Induced by Micro-Thermal-Plasma-Jet Irradiation to Narrow Amorphous Silicon Strips",
Proceedings of the 21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD 14) (Kyoto, Japan, Jul. 2-4, 2014) pp. 181-184.
9. Shogo Yamamoto, Seiji Morisaki, Shohei Hayashi, Taichi Nakatani, and Seiichiro Higashi,
"Grain Growth Control by Micro-Thermal-Plasma-Jet Irradiation to Very Narrow Amorphous Silicon Strips and Its Application to Thin Film Transistors",
Extended abstract of 2014 International Conference on Solid State Devices and Materials (SSDM2014) (Ibaraki, Japan, Sep. 8-11, 2014) pp. 562-563.
10. Muneki Akazawa, Kohei Sakaike, Shogo Nakamura, Shohei Hayashi, Seiji Morisaki, and Seiichiro Higashi,
"Fabrication of Single Crystalline Silicon Thin Film Transistor on Glass Substrate by

Using Meniscus-Force-Mediated Local Layer Transfer Technique",
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11. Seiji Morisaki, Shohei Hayashi, Shogo Yamamoto, Taichi Nakatani, and Seiichiro Higashi,
"CMOS Integration Based on Zone Melting Recrystallization of Amorphous Silicon Strips Induced by Micro Thermal Plasma Jet Irradiation",
Proceedings of International Workshop of Nanodevice Technologies (Higashi-Hiroshima, Japan, March 3, 2015), pp. 52-53.
12. Seiji Morisaki, Shohei Hayashi, Takuya Kasahara, Taichi Nakatani, Seiichiro Higashi,
"*In-situ* Observation of Zone-Melting-Recrystallization in Amorphous Silicon Strips during Atmospheric Pressure Micro-Thermal-Plasma-Jet Irradiation",
Proceedings of 2015 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD 2015) (Jeju Island, Korea, June 29- July 1, 2015), pp. 230–233.
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"Atmospheric Pressure Micro-Thermal-Plasma-Jet Crystallization of Amorphous Silicon Strips for High-Performance Thin Film Transistor Fabrication",
Proceedings of the 9th International Conference on Reactive Plasmas / 68th Gaseous Electronics Conference and 33rd Symposium on Plasma Processing (ICRP-9/68th GEC/SPP-33) (Honolulu, USA, October 14, 2015), LW1.00178.

Presentations related to this thesis

International conference

First author

1. Seiji Morisaki, Shohei Hayashi, Yuji Fujita, and Seiichiro Higashi,
"Improvement in Characteristic Variability of Thin Film Transistors Using Grain Growth Control by Micro Thermal Plasma Jet Irradiation to Amorphous Silicon Strips and CMOS Circuit Operation at Supply Voltage of 5V",
The 9th International Thin-Film Transistor Conference (ITC 2013) (Tokyo, Japan, Mar. 1-2, 2012) [2pAO05] : Oral Presentation
2. Seiji Morisaki, Shohei Hayashi, Yuji Fujita, and Seiichiro Higashi,

"Improvement in Characteristic Variability of Thin Film Transistors Using Grain Growth Control by Micro Thermal Plasma Jet Irradiation to Amorphous Silicon Strips and CMOS Circuit Operation at Supply Voltage of 5V",
Ext. Abs. International Workshop on Nanodevice Technologies 2013 (Hiroshima, Japan, Mar. 5, 2013) pp. 40-41 : Poster Presentation

3. Seiji Morisaki, Shohei Hayashi, Takahiro Kamikura, Shogo Yamamoto, and Seiichiro Higashi,
"Fabrication of Short Channel Thin Film Transistors by Channel Doping and Micro Thermal Plasma Jet Crystallization and Their Application to High Frequency Operation of CMOS Circuits",
10th International Thin-Film Transistor Conference (ITC2014) (Delft ,Netherlands, Jan.23-24,2014) : Oral Presentation
4. Seiji Morisaki, Shohei Hayashi, Shogo Yamamoto, Taichi Nakatani, and Seiichiro Higashi,
"Effect of Grain Growth Control by Atmospheric Micro-Thermal- Plasma-Jet Crystallization of Amorphous Silicon Strips on TFT Characteristics",
226th The Electrochemical Society Meeting (ECS) (Cancun, Mexico, Oct. 5-10, 2014) [1908]: Oral Presentation
5. Seiji Morisaki, Shohei Hayashi, Shogo Yamamoto, Taichi Nakatani, and Seiichiro Higashi,
"CMOS Integration Based on Zone Melting Recrystallization of Amorphous Silicon Strips Induced by Micro Thermal Plasma Jet Irradiation",
International Workshop Nanodevice Technologies (Higashi-Hiroshima, Japan, March 3, 2015) [P-17]: Poster Presentation
6. Seiji Morisaki, Shohei Hayashi, Shogo Yamamoto, Taichi Nakatani, Seiichiro Higashi,
"Micro-Thermal-Plasma-Jet Crystallization of Amorphous Silicon Strips and High-Speed Operation of CMOS Circuit",
2015 Material Research Society (MRS) Spring Meeting & Exhibit (San Francisco, USA, Apr. 6-10, 2015) [A23.06] : Oral Presentation
7. Seiji Morisaki, Shohei Hayashi, Takuya Kasahara, Taichi Nakatani, Seiichiro Higashi,

"*In-situ* Observation of Zone-Melting-Recrystallization in Amorphous Silicon Strips during Atmospheric Pressure Micro-Thermal-Plasma-Jet Irradiation",
2015 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices (AWAD 2015) (Jeju Island, Korea, June 29- July 1, 2015) [3A-4] : Oral Presentation

8. Seiji Morisaki, Taichi Nakatani, Ryota Shin, and Seiichiro Higashi,
"Atmospheric Pressure Micro-Thermal-Plasma-Jet Crystallization of Amorphous Silicon Strips for High-Performance Thin Film Transistor Fabrication",
68th Annual Gaseous Electronics Conference/9th International Conference on Reactive Plasmas/33rd Symposium on Plasma Processing Volume 60, Number 9 (Honolulu, USA, October 12-16) [LW1.00178]: Poster Presentation

Second author

1. Shohei Hayashi, Seiji Morisaki, Takahiro Kamikura, Shogo Yamamoto, Kohei Sakaike, Muneki Akazawa, and Seiichiro Higashi,
"Grain Growth Control during Leading Wave Crystallization Induced by Micro-Thermal-Plasma-Jet Irradiation to Amorphous Silicon Films",
35th International Symposium on Dry Process (DPS2013) (Jeju, Korea, Aug. 29-30, 2013) [C-3] : Oral Presentation
2. Shohei Hayashi, Seiji Morisaki, Shogo Yamamoto, Taichi Nakatani, and Seiichiro Higashi,
"Grain Growth Induced by Micro-Thermal-Plasma-Jet Irradiation to Narrow Amorphous Silicon Strips",
Proc. The 21st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD 14) (Kyoto, Japan, Jul. 2-4, 2014) : Poster Presentation
3. Shogo Yamamoto, Seiji Morisaki, Shohei Hayashi, Taichi Nakatani, and Seiichiro Higashi,
"Grain Growth Control by Micro-Thermal-Plasma-Jet Irradiation to Very Narrow Amorphous Silicon Strips and Its Application to Thin Film Transistors",
2014 International Conference on Solid State Devices and Materials (SSDM2014) (Ibaraki, Japan, Sep. 8-11, 2014) [C-9-2] : Oral Presentation
4. Ying Wang, Seiji Morisaki, Shohei Hayashi, Alex B Limanov, Adrian Chitu, Seiichiro Higashi, James S. Im,

"Melting and Solidification of Si Films Using Continuous Radiative and Non-Radiative Beams",
2015 Material Research Society (MRS) spring meeting (San Francisco, USA, Apr. 6-10, 2015) [A20.06] : Poster Presentation

Domestic Conferences

First author

1. 森崎 誠司、林 将平、藤田 悠二、東 清一郎、
"マイクロ熱プラズマジェットを用いたアモルファスシリコン細線の結晶成長制御および薄膜トランジスタ特性ばらつきの改善"、
第 30 回プラズマプロセシング研究会 (SPP-30) Proc. 30th Symposium on Plasma Processing (アクトシティ浜松・研修交流センター, 2013.1.21-23) pp. 99-100 [B6-02] : 口頭講演
2. 森崎 誠司、林 将平、藤田 悠二、東 清一郎、
"a-Si 細線を用いた大気圧マイクロ熱プラズマジェット結晶成長制御による TFT 特性ばらつきの改善および 5V 電源電圧での CMOS 回路動作"、
2013 年　第 60 回応用物理学会春季学術講演会 (神奈川工科大学, 2013.3.27-30) 13-135 [28p-G6-14] : 口頭講演
3. 森崎 誠司、林 将平、上倉 敬弘、山本 将悟、赤澤 宗樹、酒池 耕平、東 清一郎、
"大気圧マイクロ熱プラズマジェット結晶化を用いた微細薄膜トランジスタの特性評価"、
2013 年　第 74 回応用物理学会秋季学術講演会 (同志社大学, 2013.9.16-20) 13-093 [19p-B4-2] : 口頭講演
4. 森崎 誠司、林 将平、上倉 敬弘、山本 将悟、酒池 耕平、赤澤 宗樹、東 清一郎、
"大気圧マイクロ熱プラズマジェット結晶化 Si 膜を用いた薄膜トランジスタの微細化および CMOS 回路の高速駆動"、
薄膜材料デバイス研究会　第 10 回研究集会 (龍谷大学アバンティ響都ホール, 2013.10.31-11.2) pp. 64-67 [31R11] : 口頭及びポスター講演
5. 森崎 誠司、林 将平、上倉 敬弘、山本 将悟、山根 雅人、中谷 太一、東 清一郎、
"大気圧マイクロ熱プラズマジェット結晶化による従来構造および細線構造 TFT の特性評価"、
2014 年　第 61 回応用物理学会春季学術講演会 (青山学院大学, 2014.3.17-20) 13-130 [19a-E14-7] : 口頭講演
6. 森崎 誠司、林 将平、山本 将悟、東 清一郎、
"a-Si 細線を用いた大気圧マイクロ熱プラズマジェット結晶成長制御による短チャネル薄膜トランジスタの特性ばらつき評価"、
第 6 回 薄膜太陽電池セミナー (広島大学 広仁会館, 2014.10.15-16) p. 115 [P16] : ポスター講演
7. 森崎 誠司、林 将平、山本 将悟、中谷 太一、東 清一郎、

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