博士論文

Local transfer of single crystalline silicon films to glass substrate at low temperature using meniscus force and fabrication of high-performance thin-film transistors

（メニスカス力を利用したガラス基板への
単結晶シリコン膜の低温局所転写
及び高性能薄膜トランジスタの作製）

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Local transfer of single crystalline silicon films to glass substrate at low temperature using meniscus force and fabrication of high-performance thin-film transistors
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2. 公表論文

(1)Fabrication of N-channel single crystalline silicon (100) thin-film transistors on glass substrate by meniscus force-mediated layer transfer technique
Muneki Akazawa, Kohei Sakaike, Shogo Nakamura, and Seiichiro Higashi
Japanese Journal of Applied Physics, **53**, 108002-1 – 108002-3 (2014).
(2)Formation of silicon-on-insulator layer with midair cavity for meniscus force-mediated layer transfer and high-performance transistor fabrication on glass
Muneki Akazawa, Kohei Sakaike, and Seiichiro Higashi
Japanese Journal of Applied Physics **54**, 086503-1 – 086503-7 (2015).

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(3)Fabricating High-Performance Silicon Thin-Film Transistor by Meniscus Force Mediated Layer Transfer Technique
Kohei Sakaike, Muneki Akazawa, Akitoshi Nakagawa, and Seiichiro Higashi

ECS Transactions **64**(10), 17-22 (2014).

(4)Meniscus-force-mediated layer transfer technique using single-crystalline silicon films with midair cavity: Application to fabrication of CMOS transistors on plastic substrates

Kohei Sakaike, Muneki Akazawa, Akitoshi Nakagawa, and Seiichiro Higashi

Japanese Journal of Applied Physics, **54**, 04DA08-1 – 04DA08-5 (2015).

主論文

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Chapter 1

Introduction

1.1. Background

1.1.1. Three dimensional integration

Silicon complementary metal-oxide semiconductor (CMOS) technology has been developed by scaling down as shown in Fig. 1.1. However, the scaling limitation is approaching. In addition, the fabrication cost is increased by scaling down as shown in Fig. 1.2. A novel independent technology from scaling is introduced.

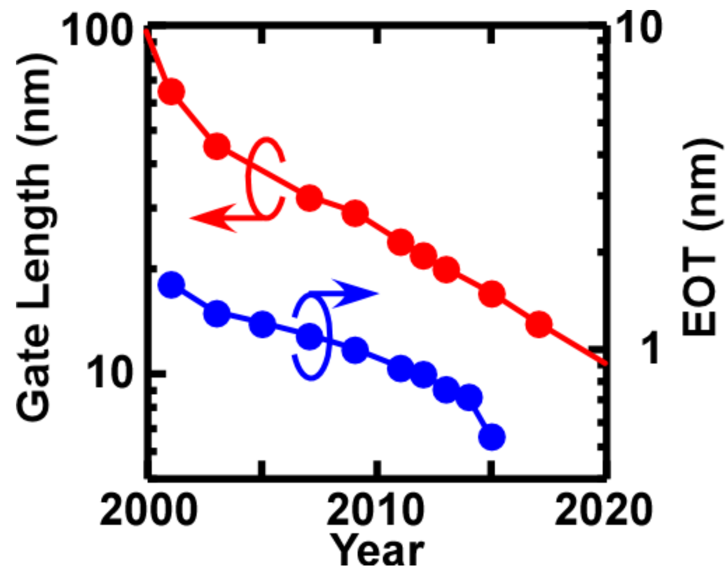

Fig. 1.1. Gate length and equivalent oxide thickness aimed in each year [1].

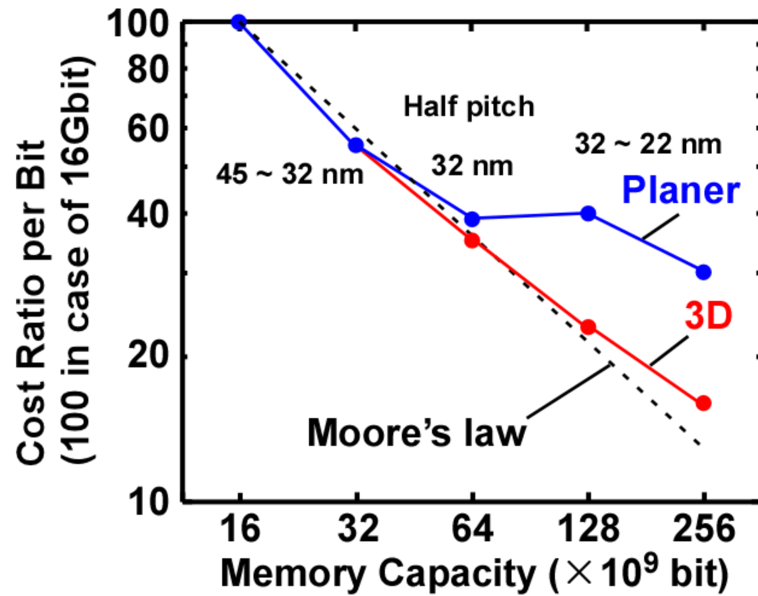

Fig. 1.2. Cost per bit plotted against capacity of memory [2].

In particular, Three-dimensional (3D) integration [3-5], which is the technology stacking transistors in a vertical direction, is investigated. In this technology, through silicon via (TSV) is one of the most important process. Figure 1.3 shows a process flow of 3D integration with TSV. The TSV is divided into four parts (via first, via middle, via last, and via after stack). Table 1.1 shows materials used as wirings of the TSV. In order to make wiring delay low, the material having low resistivity is used as a wiring material in the TSV. Although a wiring material with heat-resisting property is chosen as the material corresponding a maximum process temperature after formation of TSVs. For that reason, the timing to form TSVs is important.

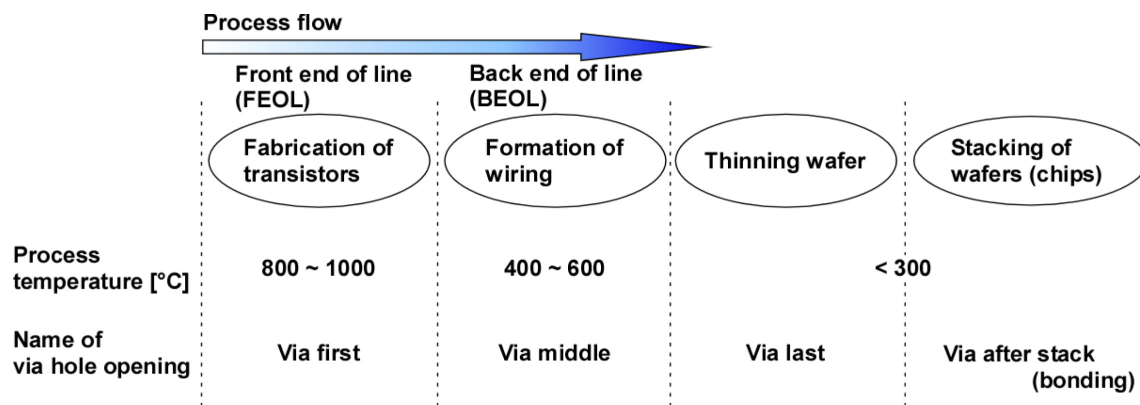

Fig. 1.3. Process flow of 3D integration with TSV.

Table 1.1. Materials used as wirings of TSV.

	Poly-Si	Tungsten(W)	Copper(Cu)
Main via	Via first	Via middle	Via last and after stack
Resistibility[Ωcm]	$> 10^{-5}$	5.3×10^{-6}	1.7×10^{-6}

1.1.2. Large area electronics

The large area electronics are classified into thin-film solar cells, imaging sensors, flat panel displays (FPDs), etc. In particular, as for FPDs, cathode ray tube (CRT) was the main display until about 2000. By the starting of the mass-production of thin-film transistor liquid crystal display (TFT-LCD) in 1991, the TFT-LCD spread to home. By means of enlargement, higher pixilation, and lower price of LCDs, the market grew in 2000, and the market was further expanded in the late 2000s. However, after that, the market of LCD has become stagnant. On the other hand, the smart device, such as smart phone and tablet personal computer (PC), has spread due to release of Apple's iPhone in 2007.

The development of display market is related to improvement of TFTs. The TFTs are fabricated on a substrate with low heat resistance, such as glass and quartz. Table 1.2 shows channel materials of TFTs in a field of display. Organic TFTs [6-10] have the advantages of flexibility, low production costs, while, the reliability is a serious problem. Oxide TFTs [11-15] have transparency and the possibility of formation on flexible substrate at a low temperature. Nevertheless, it is difficult that complementary metal-oxide semiconductor (CMOS) circuits are fabricated owing to lack of CMOS capability. On the other hand, low-temperature poly-Silicon (LTPS) TFTs [16-18] have higher reliability and mobility in both conduction types.

Table 1.2. Channel materials of TFTs.

	a-Si:H	Organic semiconductor	Oxide semiconductor	Low temperature poly-Si(LTPS)
Conduction type	n-ch	p-ch	n-ch	CMOS
Field effect mobility [$cm^2/(Vs)$]	0.5 ~ 1.5	< 5	10 ~ 80	> 100
Cost	Good	Excellent	Good	Fair
Process temperature [°C]	< 350	< 100	< 300	< 600

1.2. Motivation and purpose

In fields of both 3D integration and large-area electronics, fabrication technique of high-performance transistors on an insulator at low temperature is required. In our previous work, we have proposed layer transfer of Si films with a midair cavity to a foreign substrate using meniscus force at low temperature [19].

In this paper, I proposed a novel TFT fabrication process using meniscus force-mediated local layer transfer. Figure 1.4 shows the schematic diagram of the proposed process flow of a Si TFT fabrication on an insulator by meniscus force. By adopting parts of the conventional Si CMOS fabrication technique, high-performance TFTs are fabricated. The most important feature of the process is to complete high-temperature treatment methods of silicon on insulator (SOI) layers with the Si substrate before transfer of the layers to a foreign substrate with low-heat resistance. In order to demonstrate Si TFT fabrication on an insulator, it is necessary to investigate each treatment method of the sample. In particular, I focused on two processes (ion implantation and thermal oxidation) before transfer.

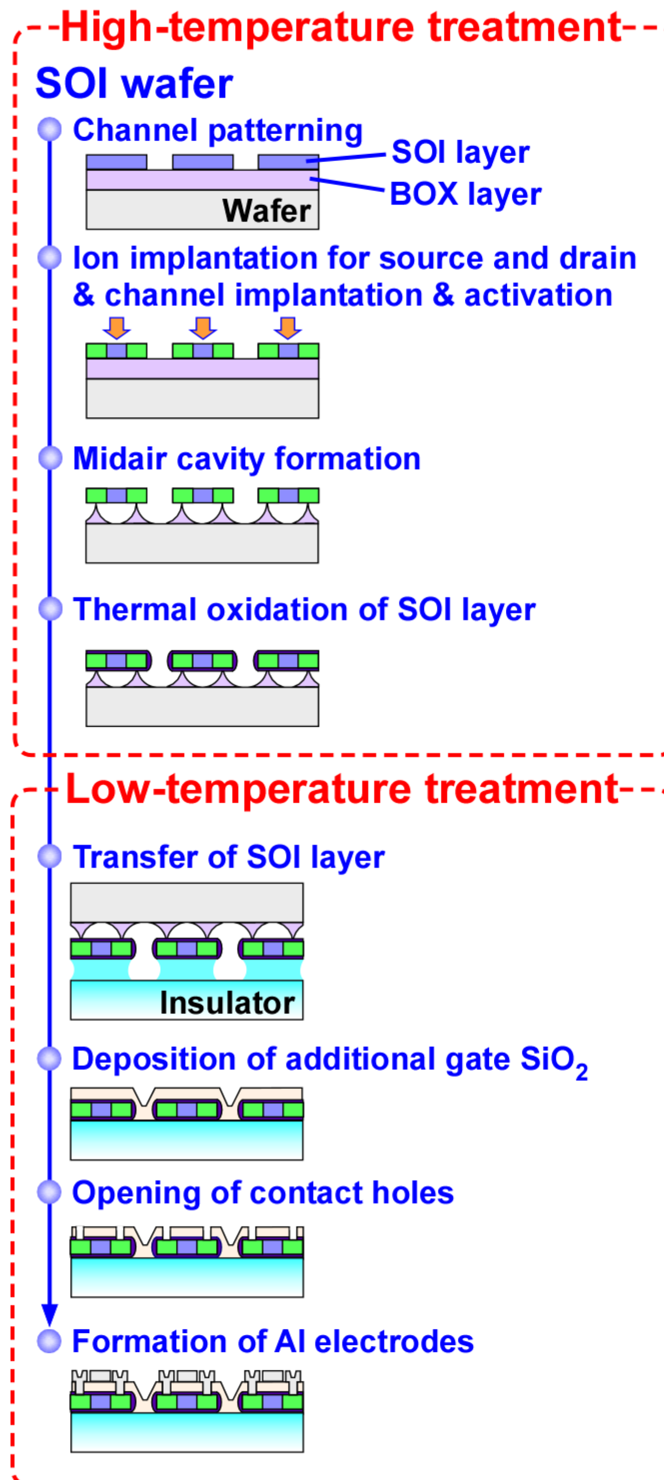

Fig. 1.4. Schematic diagram of proposed process flow of Si TFT fabrication on insulator by meniscus force.

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Chapter2

Fundamental technologies

2.1. Meniscus force

2.1.1. Surface tension

Capillary action is a phenomenon at an interface between non-mixed liquids or an interface between a liquid and an air. The interface moves to minimize the energy at the interface. Figure 2.1 shows a schematic diagram of molecules at the surface and the inside of a liquid. The molecules in a liquid pull against each other because the molecules condense. When the effect of intermolecular force is greater than thermal fluctuation, molecules change from gas to liquid. The molecules in the inside of liquid are stable by intermolecular forces with the surrounding molecules. On the other hand, the molecules at the surface of liquid lose the intermolecular forces on the side of gas. Because of these reasons, the liquid changes the shape to minimize the surface area of the liquid. When the aggregation energy per molecule is defined as U in Fig. 2.1, the molecules at the surface of liquid lose half of U. Surface tension (γ) is obtained by measuring the quantity of the energy loss. Table. 2.1 shows the surface tension of familiar liquids at a room temperature. For oil, the interaction is related to van der Waals. The aggregation energy is equal to thermal fluctuation. When kT is 0.025 eV at 25 °C, γ is 20 mN/m. The γ of water is larger than that of oil owing to hydrogen bond. Mercury is a liquid and a metal. The γ is ~ 500 mN/m because the cohesive force is strong.

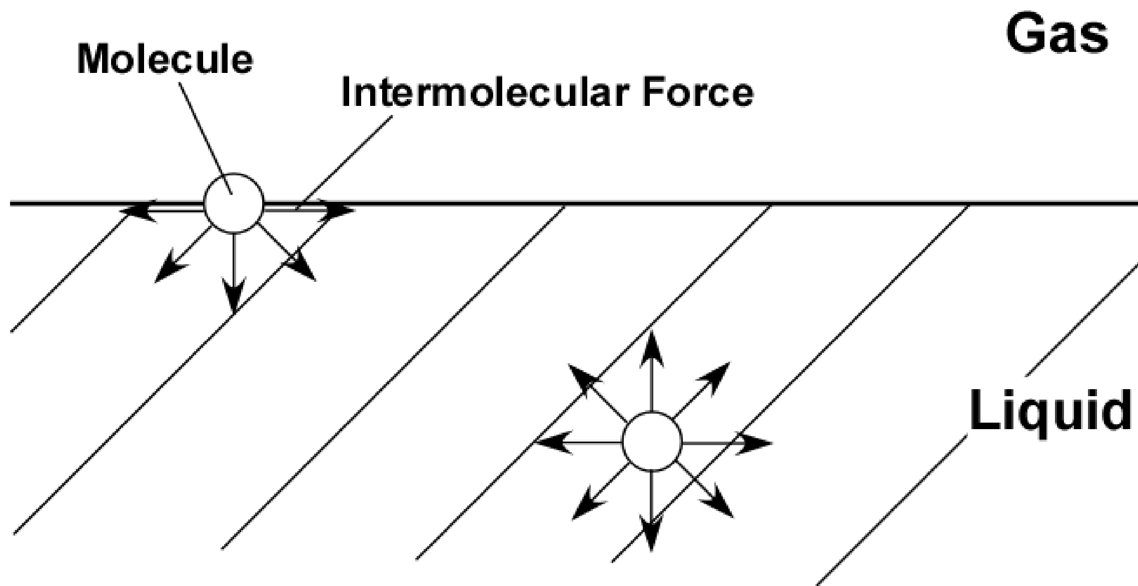

Fig. 2.1. Schematic diagram of molecules at surface and inside of liquid.

Table. 2.1. Surface tension of familiar liquids at room temperature.

Liquid	Ethanol	Acetone	Cyclohexane	Glycerol	Water	Mercury
γ [mN/m]	23	24	25	63	72	485

2.1.2. Capillary adhesion

The meniscus force generates by pressure difference between internal and external of the meniscus curved surface. The formula consists of two terms about Laplace pressure (Δp) and the surface tension formed among liquid and gas and solid of a liquid bridge.

When a liquid is contained between two plates, capillary bridge is formed as shown in Fig. 2.2 The height between the plates is defined H. When the direction of arrows in Fig. 2.2 is a positive direction, the meniscus force (F) represents as follow.

$$F = \pi R^2 \Delta p - 2\pi R \gamma \sin\theta. \qquad (2.1.1)$$

Where R is the radius of capillary bridge, and θ is the contact angle of a liquid.

When Θ < 90°, Laplace pressure is given by

$$\Delta p = \gamma(\frac{1}{R} - \frac{2\gamma cos\theta}{H}), \quad (2.1.2)$$

$$\approx -\frac{2\gamma cos\theta}{H}. \text{ (R<<H)} \quad (2.1.3)$$

From Eq. (2.1.1), the meniscus force (F) represents as follow.

$$F = -\frac{2\pi R^2 \gamma cos\theta}{H} - 2\pi R\gamma sin\theta, \quad (2.1.4)$$

$$\approx -\frac{2\pi R^2 \gamma cos\theta}{H}. \text{ (R<<H)} \quad (2.1.5)$$

The meniscus force generates by decreasing H.

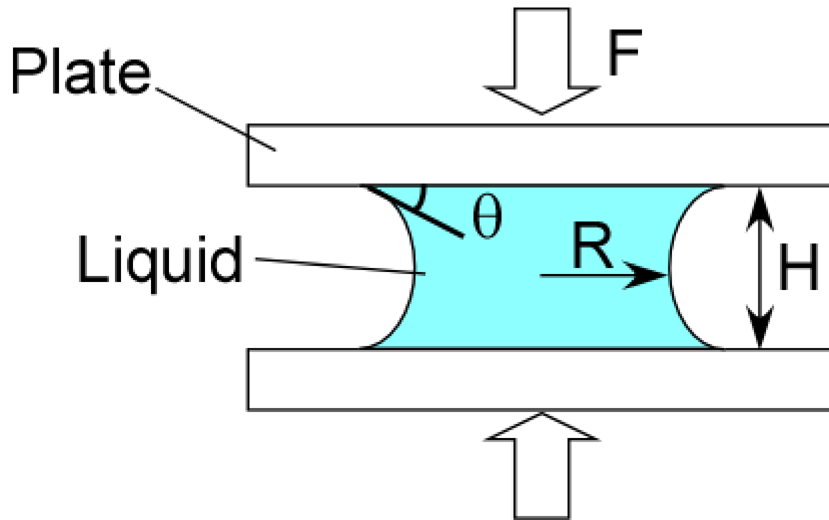

Fig. 2.2. Schematic diagram of sandwiched liquid by two plates.

2.2. Characteristics of thin-film transistor

2.2.1. Thin-film transistor

A thin-film transistor (TFT) is a kind of field effect transistors (FETs). Figure 2.3 shows a typical structure of a TFT on an insulator. The TFT is a three-terminal device without ground terminal. The structure is similar to metal-oxide-semiconductor field effect transistor (MOSFET) built on SOI with the exception that the active film is a deposited thin film and that the substrate can be of any form.

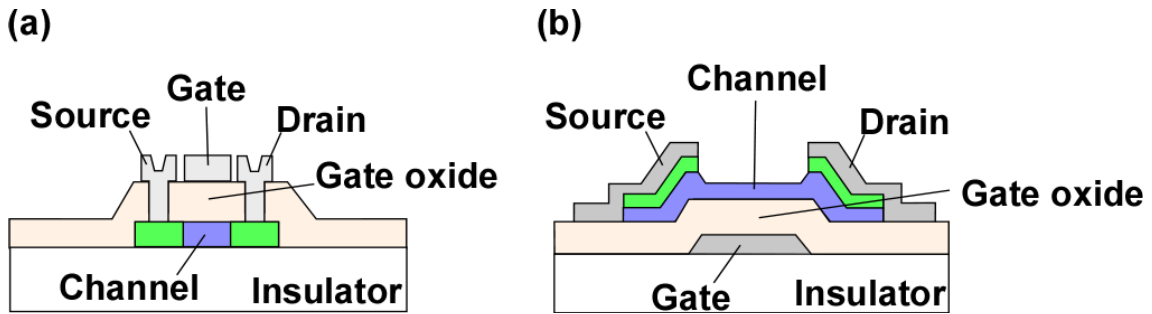

Fig. 2.3. Schematic diagram of cross section of (a) top gate TFT and (b) bottom gate TFT.

Field-effect mobility

The field-effect mobility (μ_{FE}) is determined from the transconductance (g_m), defined by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} | V_{DS} = constant. \quad (2.2.1)$$

When V_{DS} is low, the channel charge is more uniform from source to drain. The drain current is

$$I_D = \frac{W \mu_{FE} Q_n V_{DS}}{L}, \quad (2.2.2)$$

where L and W are the gate length and the width of a TFT, and Q_n is the mobile channel charge density, respectively.

The mobile channel charge density is approximated by

$$Q_n = C_{ox}(V_{GS} - V_{th}), \quad (2.2.3)$$

where V_{th} is the threshold voltage and C_{ox} is the oxide capacitance.
From Eq. 2.2.3, the drain current is

$$I_D = \frac{W}{L}\mu_{FE}C_{ox}(V_{GS} - V_{th})V_{DS}. \qquad (2.2.4)$$

From Eq. 2.2.4, the transconductance is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L}\mu_{FE}C_{ox}V_{DS}. \qquad (2.2.5)$$

The field-effect mobility becomes

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}}. \qquad (2.2.6)$$

Threshold Voltage

The threshold voltage (V_{th}) is given by

$$V_{th} = V_{FB} + 2\Psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\Psi_B)}}{C_{ox}}, \qquad (2.2.7)$$

where V_{FB} is the flat-band voltage, Ψ_B is fermi level from intrinsic fermi level, ε_s is permittivity of semiconductor, q is unit electronic charge, N_A is acceptor impurity concentration.

The flat-band voltage is related to fixed oxide charges (Q_f) and the work-function difference (ϕ_{ms}) between the gate material and the semiconductor, Eq. 2.2.7 becomes

$$V_{th} = (\phi_{ms} - \frac{Q_f}{C_{ox}}) + 2\Psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\Psi_B)}}{C_{ox}}. \qquad (2.2.8)$$

Subthreshold swing

The parameter to quantify how sharply the transistor is turned off by the gate voltage is called the subthreshold swing *S* (inverse of subthreshold slope), defined as the gate-voltage change needed to induce a drain-current change of one order of magnitude. By definition, the subthreshold swing can now be calculated as follow.

$$S \equiv (ln10)\frac{dV_G}{d(lnI_D)}$$

$$= (ln10)(\frac{kT}{q})(\frac{C_{ox}+C_D}{C_{ox}}). \qquad (2.2.9)$$

Here, k is the Boltzmann constant, C_D is the depletion-layer capacitance.

When the MOS interface-trap density D_{it} is high, the subthreshold swing is given by

$$S = (ln10)(\frac{kT}{q})(\frac{C_{ox}+C_D+C_{it}}{C_{ox}}). \tag{2.2.10}$$

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Chapter 3
Measurement of meniscus force

3.1. Introduction

The meniscus force generates between two parallel plates increases by decreasing the height between plates as shown in Eq. 2.1.5 [1]. It is important to investigate the force actually generates between glass and Si substrates. In order to examine relationship between the meniscus force and the distance between the substrates (the height of capillary bridge), the distance changing by time was measured, and the force was obtained when the substrates separated.

3.2. Experiments

Figure 3.1 shows the schematic diagram of a system of measurement. The change of distance between an Al mirror and a glass substrate with filling water during natural drying was observed by optical interferometer. The measurement step is described as follow.

At first, an Al mirror 10 mm square is fixed, and a glass substrate with a fixed amount of pure water (1.5 μL) was approached to the mirror from the lower side. When the mirror contacted with water, the glass clung to the mirror by surface tension of water. After that, the distance between the substrates decreased by natural drying. During natural drying, I observed the wave signal results from optical interference by using He-Ne laser irradiation from back-side of glass. From the signal, the height from Al mirror to glass substrate (H) was calculated. The change of the height (ΔH) is given by

$$\Delta H = N * \frac{\lambda}{2n}, \tag{3.1}$$

where N is the number of the observed wave, and λ is the wavelength of He-Ne laser, and n is the refractive index of water, respectively. The height (H) at an arbitrary time represents as follow.

$$H = H_0 - \Delta H, \tag{3.2}$$

Here, H_0 is the initial height immediately after formation of capillary bridge. Finally, at an arbitrary time, the glass was separated from the Al mirror, and the generated force was read by digital force gauge.

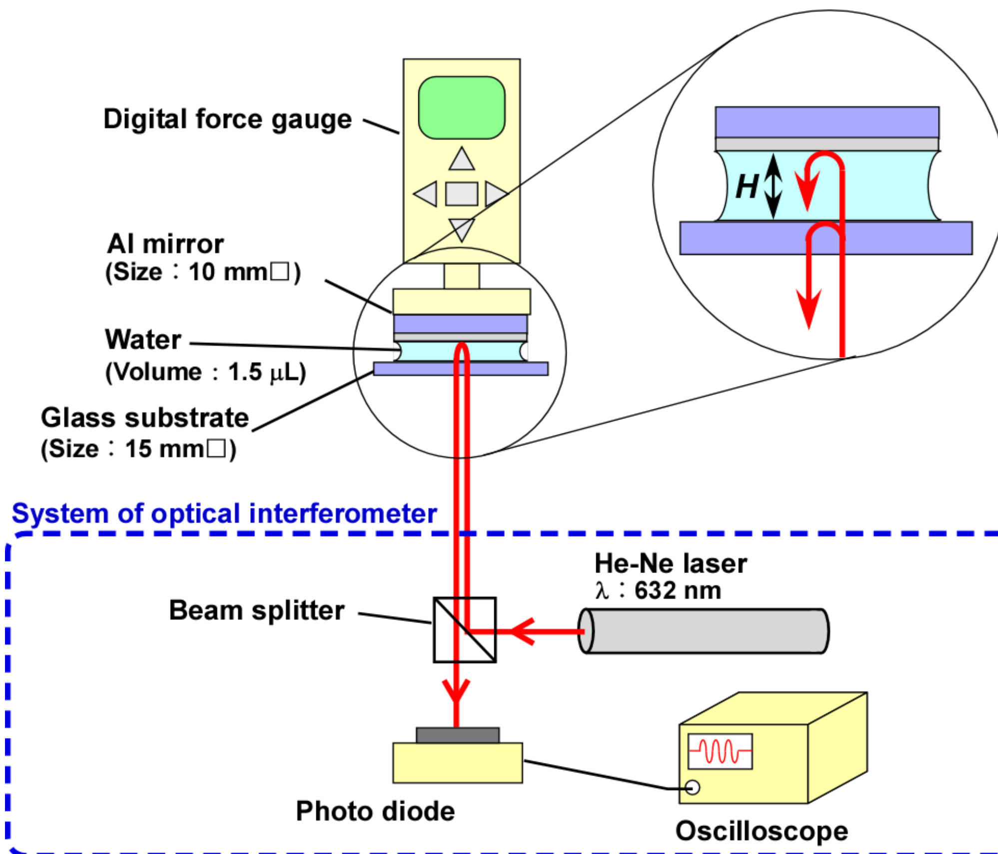

Fig. 3.1. Schematic diagram of observation of distance between Al mirror and glass substrate by optical interference.

3.3. Results and discussion

Figure 3.2 shows an example of observation results. The signal began to be observed when the substrates clung to each other by surface tension of water (step I in Fig. 3.2). After that, the waves were confirmed by natural drying (step II in Fig. 3.2). Finally, the substrates were removed (step III in Fig. 3.2).

In this case, the number of waves is 19. From Eq. 3.1, the change of the height is 4.5 μm. Here, the initial height was calculated as 13 μm from the volume of water and the area of the substrate. From these values, the height was 8.5 μm when substrates were separated. When removed substrates, the separating force was 470 mN. The measurement was made several times. The separating force was plotted with respect to the height value as shown in Fig. 3.3 by the filled circles. This result indicated that the decrease of the height increased the separating force. In addition, the experimental data corresponded to the calculated data from meniscus force equation (Eq. 2.1.5). These results suggest that the stronger meniscus force generates at lower height.

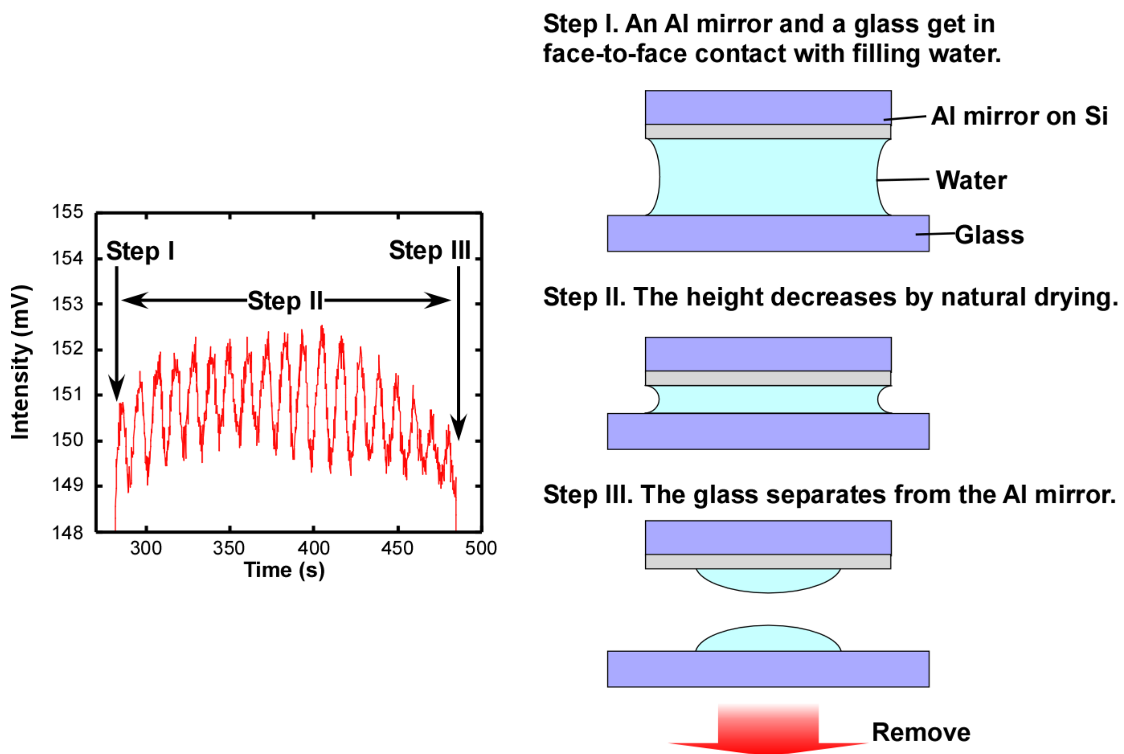

Fig. 3.2. Wave signal generates by optical interference during evaporating water and schematic diagram of the sample in each step during measurement.

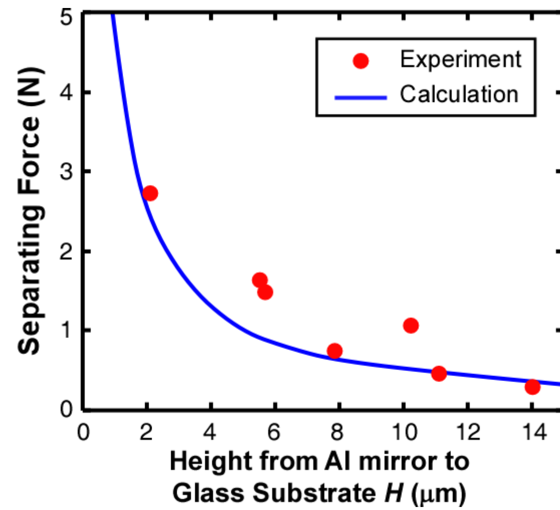

Fig. 3.3. Separating force plotted with respect to height from Al mirror to glass substrate. Filled circles: experimental data. Line: calculated meniscus force.

3.4. Conclusion

I attempted to measure the attracting force generates between an Al mirror and a glass substrate. It was confirmed that the force to separate the glass substrate from the Al mirror increased by decreasing the height from the glass substrate to the Al mirror, and the separating force corresponded to meniscus force.

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Chapter 4

Transfer of SOI layers to glass substrate

4.1. Introduction

In a field of large-area electronics such as flat panel display (FPD), thin film transistors (TFTs) are fabricated on a substrate having low heat resistance such as glass substrate. In conventional display, a circuit for switching pixels and external circuits fabricated on separate substrates are connected by electric wiring. For the realization of system on glass (SOG), fabrication of complementary MOS (CMOS) circuits on a glass substrate at low temperature is required. For fabrication of CMOS circuits, higher mobility in both n- and p- channel TFTs is required. Hydrogenated amorphous silicon (a-Si:H) [1, 2], organic [3-5], and oxide [6-8] are investigated as the channel material of TFT for low-temperature fabrication technology. However, there are serious problems originated from their low electrical performance, poor reliability, and lack of CMOS capability. On the other hand, low-temperature poly-Si (LTPS) TFT fabricated by rapid thermal annealing and crystallization of a-Si using excimer laser has high mobility in both conduction types [9]. However, the serious problem of LTPS TFT is characteristic variation due to grain boundaries.

In order to implement silicon technology, transfer of single crystalline silicon to foreign substrates has been attempted on basis of conventional wafer bonding approaches [10, 11]. However, these techniques require high process temperature or bonding pressure.

In previous work, we have proposed layer-transfer of Si films with a midair cavity to a counter substrate using meniscus force [12]. In Chap. 3, I measured the stronger meniscus force generated between parallel plates. In this chapter, I attempted transfer of single crystalline silicon films with a midair cavity to a glass substrate using meniscus force at low temperature.

4.2. Experiments

Figure 4.1 shows the process flow of transfer. A silicon-on-insulator (SOI) wafer with (100)-oriented SOI layer and BOX layer thicknesses of 100 and 300 nm, respectively was prepared. The SOI layer was patterned to a channel shape (channel length of 18 μm) by photolithography and chemical dry etching as shown in Fig. 4.2, and the BOX layer was etched by HF solution until fine SiO_2 columns were left underneath the source and drain regions. The size of SiO_2 columns was controlled to less than 1 μm by etching time. After that, transfer of the SOI layer with a midair cavity to glass substrate (Corning Eagle 2000) was performed. At first, the layer and a glass substrate were placed in close face-to-face contact with filling water, and the sample was heated at 80 ºC on a hot plate for 15 min. After the water evaporated, the wafer was removed. The shape of the SOI layer before and after transfer was observed by optical microscope and scanning electron microscope (SEM).

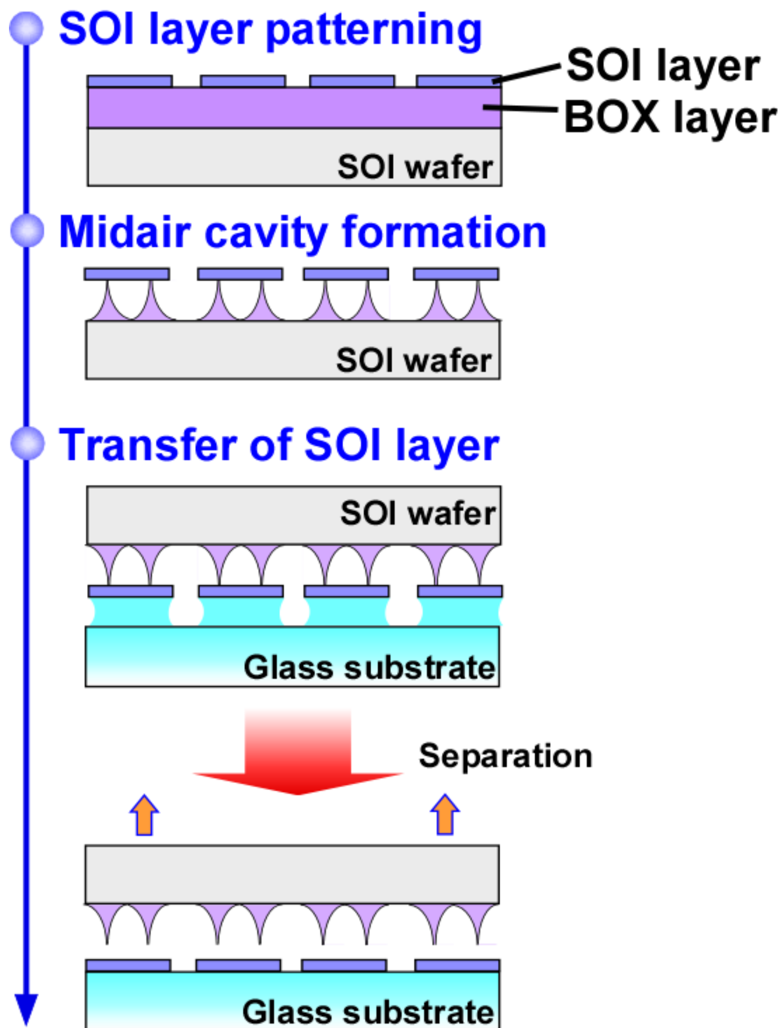

Fig. 4.1. Schematic diagram of transfer of SOI layer with midair cavity to glass substrate.

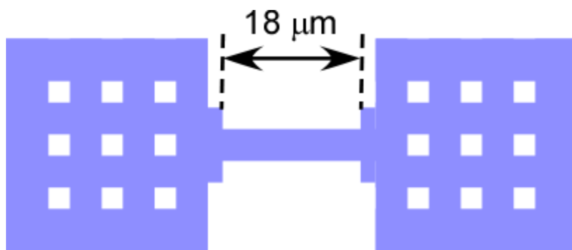

Fig. 4.2. Device pattern of SOI layer.

4.3. Results and discussion

The SEM image of the SOI layer with midair cavity was shown in Fig. 4.3 (a). From that result, it was confirmed that midair cavity was formed without shape change of the SOI layer. From the SEM image in Fig. 4.3 (b), the shape of an SOI layer on glass substrate was completely maintained after transfer. Further, from electron back-scattering diffraction (EBSD) pattern of the layer on glass, it was confirmed that the transferred layer was oriented to (100) direction. From these results, we called this transfer technique as "meniscus force-mediated layer transfer (MLT) technique".

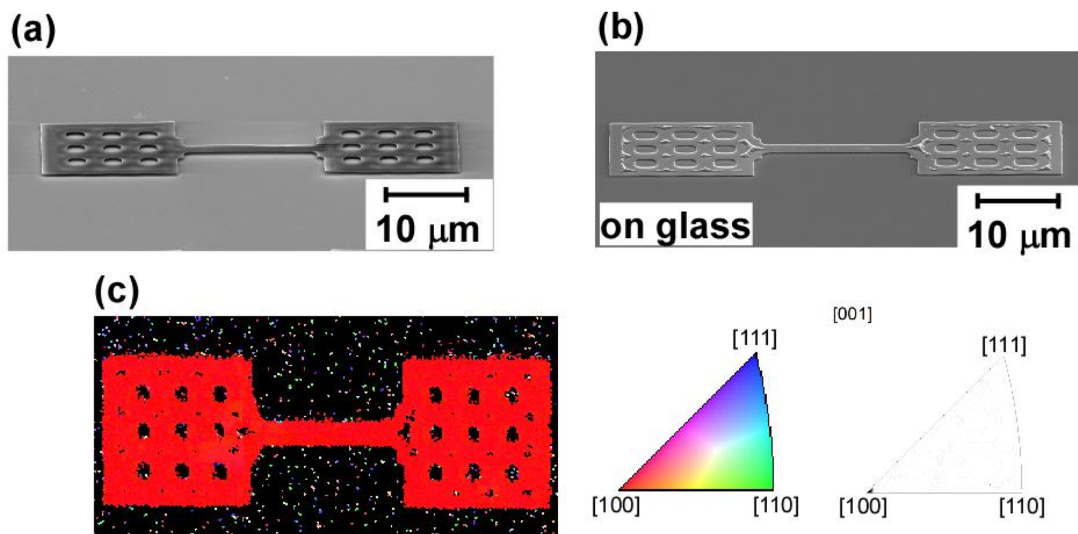

Fig. 4.3. SEM images of SOI layer (a) before and (b) after transfer and (c) EBSD pattern of transferred film on glass.

4.4. Conclusion

I attempted to transfer SOI layers with a midair cavity to a glass substrate. The SOI layer was completely transferred to glass without deformation. From this result, I succeeded in local transfer of single crystalline silicon layer to glass substrate at a low temperature of 80 ℃.

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Chapter 5

Thermal oxidation of SOI layers with midair cavity

5.1. Introduction

In Chap. 4, local transfer of single crystalline silicon with midair cavity to glass substrate was performed at a low temperature. In addition, for fabrication of high-performance MOS transistor, it is necessary that high quality insulator is formed. Thermal SiO_2 with high electrical property has been known [1]. In this chapter, I proposed that SOI layers with midair cavity were oxidized. Thermal oxidation is a key process for fabrication of high-performance TFTs. The SiO_2 layer work as the blocking layer of contamination from glass. The shape of SOI layers with midair cavity after oxidation was observed, and effect of the transfer process of SOI layers with midair cavity was investigated. Furthermore, n-channel single crystalline silicon TFT fabrication process on glass substrate at a low temperature was demonstrated.

5.2. Experiments

The SOI wafer was used with 100-nm-thick SOI layer in this experiment. First, the SOI layer was patterned to a channel shape by photolithography and chemical dry etching. Channel length (L) is set in the range from 5 to 15 μm as shown in Fig. 5.1. In order to form "midair cavity", the BOX layer was etched by HF solution, and the size of SiO_2 columns was controlled to less than 1 μm by etching time. Next, thermal oxidation of SOI layers with midair cavity was performed in dry oxygen at 1000 °C to form from 13 to 26 nm conformal SiO_2, as shown in Fig. 5.2. Here, the oxide thickness was defined as t. After that, the SOI layer with midair cavity was transferred to glass substrate (Corning Eagle 2000) by meniscus force. After that, the MLT of thermally oxidized SOI is performed. The sample is heated at 80ºC on a hot plate for 15 min. Eventually, the SOI layer is transferred when removing from the SOI wafer.

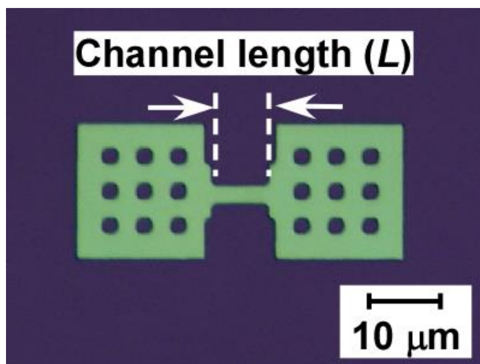

Fig. 5.1. Photograph of SOI layer pattern.

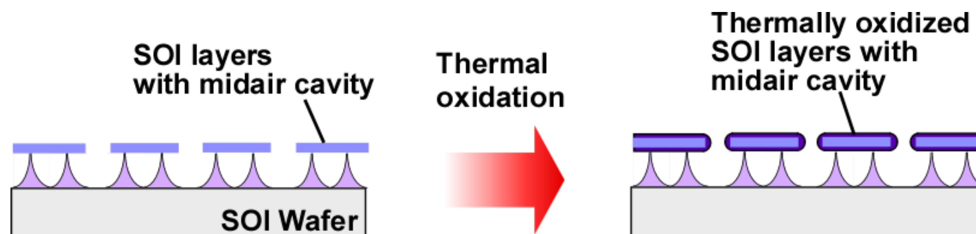

Fig. 5.2. Schematic diagram of thermal oxidation of SOI layer with midair cavity.

5.3. Results and discussion

First, the SOI layers changed the channel length was observed. The Optical microscope images of SOI layers with midair cavity before and after thermal oxidation are shown in Fig. 5.3. Here, the oxide thickness is fixed at 13 nm. I observed that the channel color of the SOI layers with midair cavity changed after oxidation. From this result, it appeared that the deformation of the SOI layers occurred because of formation of thermal SiO_2. In addition, from the SEM images of the channel of the SOI layers in Fig. 5.3, the bend of the oxidized SOI layers was observed. It was confirmed that the displacements from the original position (D) were ~370 nm (L = 15 μm) and ~ 85 nm (L = 5 μm), respectively. From the result, the shorter channel length decreased the displacement of the layer. Next, the SEM images of the SOI layers for various oxide thicknesses were shown in Fig. 5.4. Here, the channel length of the samples is 15 μm. From these results, thicker oxide showed larger deformation due to accumulation of oxidation strain. Figure 5.5 summarized the relationship between displacement of the SOI layer and thermal SiO_2 thickness on each channel length of the SOI layer. This result indicated the decrease of the channel length and oxide thickness could restrain the deformation of the layer.

Then, transfer of the oxidized SOI layers with a midair cavity in different displacements was performed to glass substrate. In the large displacement, the SOI layer at L = 15 μm was transferred to glass substrate, however, a part of the channel wrinkling was observed, as shown in Fig. 5.6(b). In contrast, when the L was as short as 5 μm and the oxide thickness (t) was 13 nm, deformation of SOI layer was less than 100 nm (red area in Fig. 5.5) and the layer transfer to glass was carried out without any problem as shown in Fig. 5.6(a). From these results, we succeeded in local transfer of the thermally oxidized SOI layer with short channel using meniscus force at a low temperature.

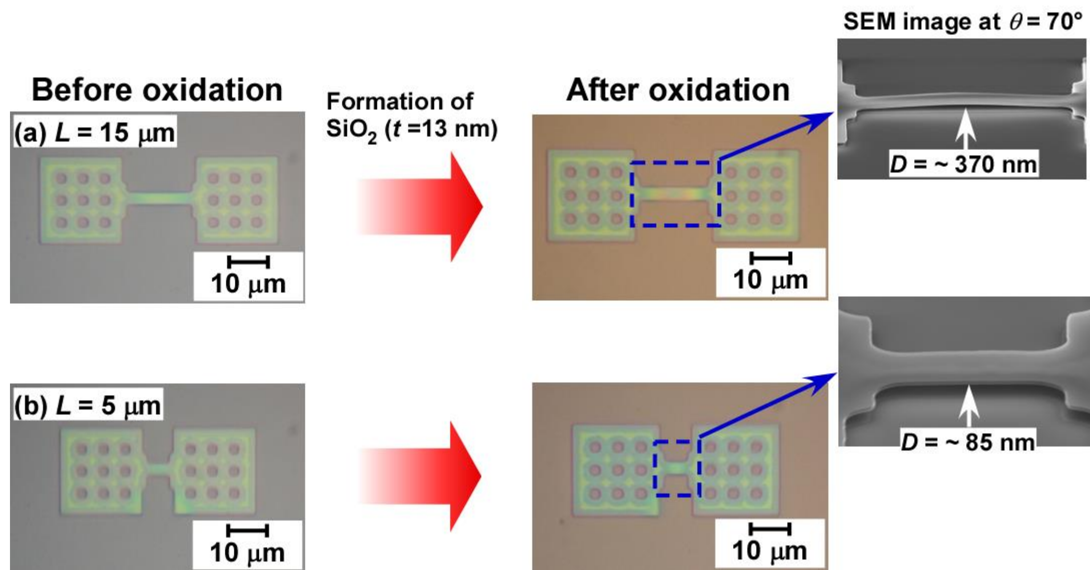

Fig. 5.3. Optical microscope images of SOI layers on midair cavity before and after thermal oxidation at 1000 °C, and SEM images (θ = 70°) of channel of oxidized SOI layer with midair cavity. (a) L = 15 μm and (b) L = 5 μm.

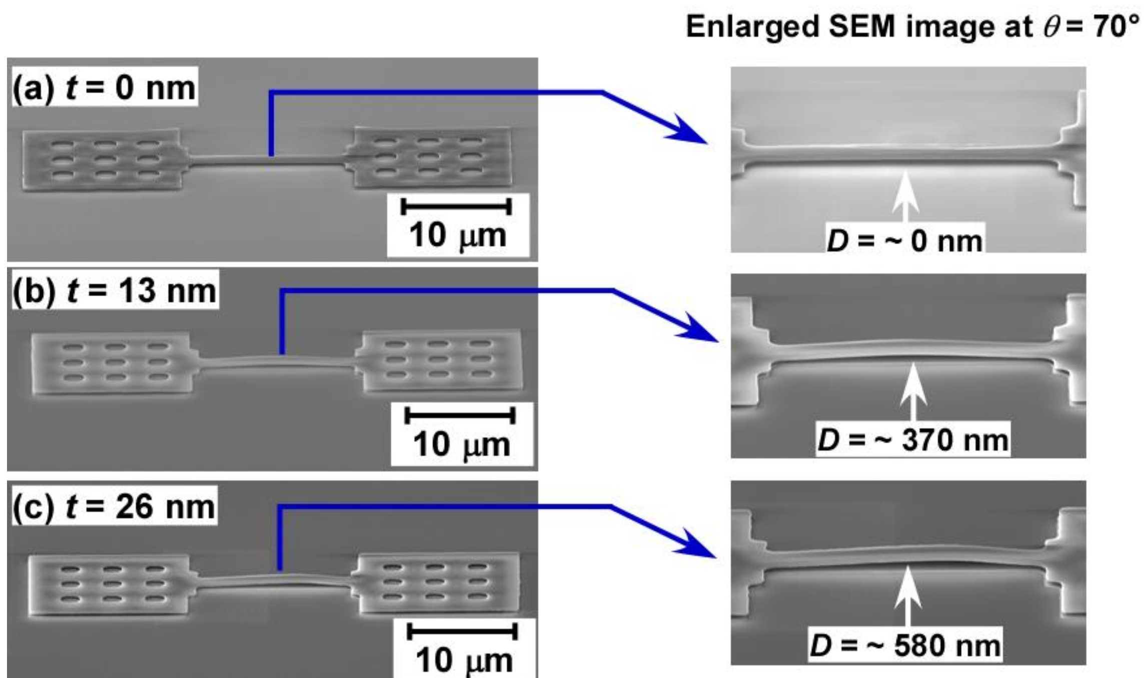

Fig. 5.4. Whole and enlarged SEM images of oxidized SOI layers with midair cavity. (a) t = 0 nm and (b) t = 13 nm and (c) t = 26 nm.

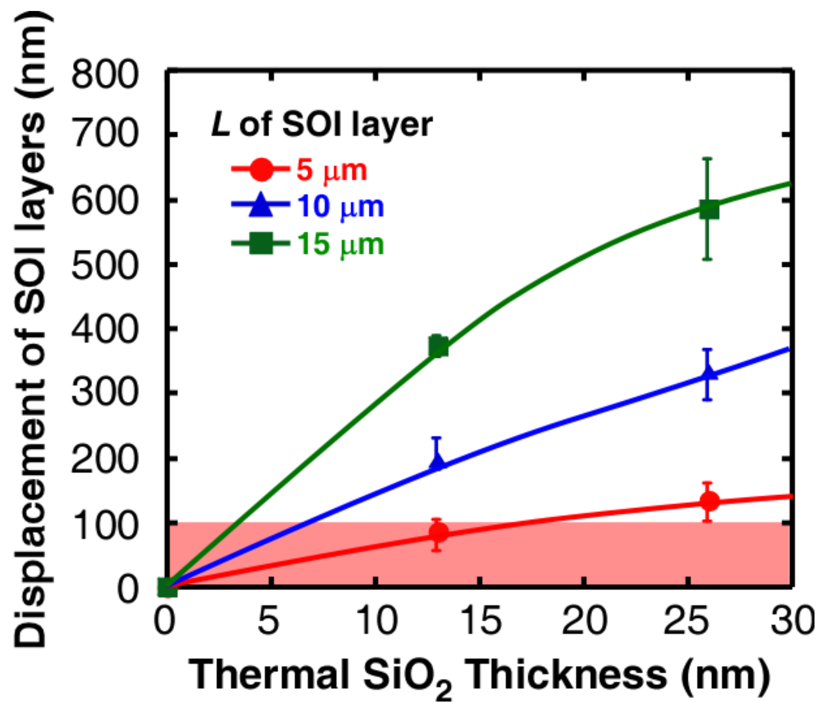

Fig. 5.5. Displacement of SOI layer plotted with respect to thermal SiO_2 thickness for various channel length of SOI layer.

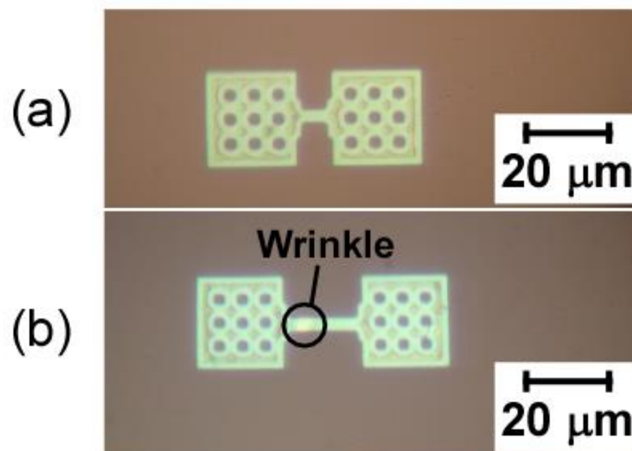

Fig. 5.6. Optical microscope images of the SOI layer transferred to glass substrate after thermal oxidation: (a) $L = 5$ μm and (b) $L = 15$ μm.

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Capacitance versus voltage (C-V) characteristics of MOS capacitors fabricated by thermal SiO_2 (10 nm) + PECVD SiO_2 (196 nm): sample A, and PECVD SiO_2 (204 nm): sample B, are shown in Fig. 5.7. By the high-

low-frequency capacitance method [2], the interface state density (D_{it}) at the midgap of sample A is 2.6×10^{10} $cm^{-2}eV^{-1}$, which is about two and a half times smaller than that of sample B. This result indicated that proposed process offers high quality Si/SiO_2 interface.

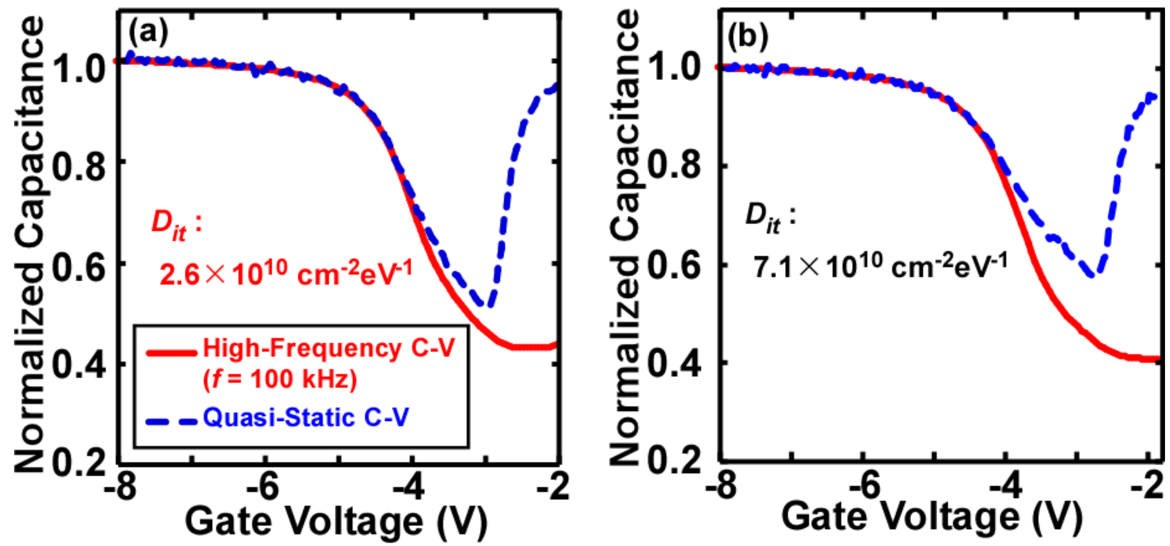

Fig. 5.7. High-frequency and quasi-static C-V characteristics of (a) thermal SiO_2 (10 nm) + PECVD SiO_2 (196 nm) and (b) PECVD SiO_2 (204 nm) MOS capacitors after PMA.

5.4. Conclusion

I attempted to transfer thermally oxidized SOI layers with a midair cavity to a glass substrate. The SOI layers with the midair cavity bent after thermal oxidation. Under the condition of shorter length and thinner oxide, the deformation of the SOI layer was less than 100 nm. In case of deformation of less than 100 nm, the layer transfer to glass was carried out without any problem. From these results, I succeeded in local transfer of the thermally oxidized SOI layer with short channel and thin oxide using meniscus force at a low temperature.

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Chapter 6
Formation of implanted SOI layers with midair cavity

6.1. Introduction

Silicon complementary metal-oxide-semiconductor (Si CMOS) technology is approaching the end of its scaling owing to unavoidable physical limitations. Therefore, three-dimensional (3D) integration technology [1–3] is being studied intensively. In 3D integration technology, through-silicon via (TSV) is an essential process in the front end of line (FEOL) and back end of line (BEOL). In order to perform TSV in FEOL above 600 ºC, the poly-Si is used as a wiring material in the via hole. The resistivity of poly-Si is two or three orders of magnitude greater than that of a metal. In a formation technology where single-crystalline Si layers are stacked on a substrate at a low temperature, a metal is used for all electrical wiring.

In order to implement Si CMOS technology on foreign substrates, the transfer of single-crystalline silicon to glass has been attempted on the basis of conventional wafer-bonding approaches [4, 5]. Wafer bonding requires an extremely low surface roughness (less than 1 nm) of the wafers. In addition, transfer techniques using a sacrificial layer [6, 7] are known.

In our previous work, we have proposed layer transfer of Si films with a midair cavity to a countersubstrate using meniscus force [8]. Furthermore, in Chap. 5, the thermal oxidation of silicon-on-insulator (SOI) for the formation of a good MOS interface was performed. However, the critical issue in MLT to a glass substrate is the low transfer yield of ~ 20%. It is necessary to improve this yield. Figure 1 shows the process steps of MLT in TFT fabrication on glass. In Fig. 6.1, I speculated that the process step before transfer affects the MLT process. In particular, I considered that it is important to control the SiO_2 column size and shape. Several groups have reported that etch rate of SiO_2 is changed by controlling the impurity concentration in a SiO_2 [9–11].

In this work, I observed SOI layers with a midair cavity after ion implantation and thermal oxidation, and attempted to improve the transfer of the SOI layers to the glass substrate.

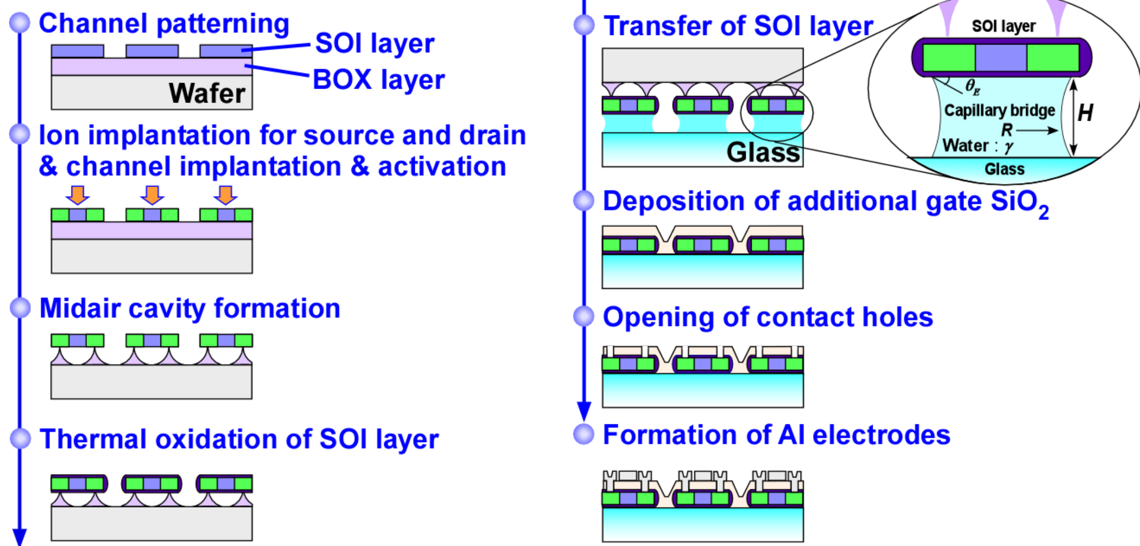

Fig. 6.1. Schematic diagram of process flow of Si TFT fabrication on glass by MLT technique.

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6.2. Experiments

An SOI wafer with (100)-oriented SOI layer and buried oxide (BOX) layer thicknesses of 80 and 400 nm, respectively, is prepared. An SOI layer is patterned to a channel shape by photolithography and chemical dry etching, as shown in Fig. 6.2(a). Next, phosphorus ions (P^+) were implanted into source and drain regions of some of the samples with a 7° tilt angle in the dose range from 1×10^{14} to 2×10^{15} cm^{-2} at 40 keV using an ion implanter (Ulvac IM 200-M). The channel region of the samples with a resist was not implanted [hatched area in Fig. 6.2(b)]. Here, the ion acceleration voltage was determined using the simulator TSUPREM4 [12] to set the projection range to a position near the SOI/BOX interface, as shown in Fig. 6.3, because a good contact between the SOI layer after transfer and a metal is provided. The implanted samples were then annealed at 1000 ºC to active the impurities. Next, the BOX layer was etched with 25% HF solution at 30 ºC to form the midair cavity. The size of residual SiO_2 columns was controlled by adjusting the etching time. The thermal oxidation of SOI layers with a midair cavity was performed in dry oxygen at 1000 ºC for 4 min. After that, the SOI layer was transferred to a glass substrate by MLT technique. At first, the wafer and a glass substrate were placed in close face-to-face contact with filling water, and the samples were heated to 80 ºC on a hot plate for 15 min. As the water evaporated through the midair cavity, capillary bridges were formed between the SOI layer and the glass substrate, and meniscus force was generated in capillary bridges. The meniscus force [13] rapidly increased with the evaporation of water, which decreased the height of the capillary bridge. Eventually, the SOI layer was transferred by removing the layer from the SOI wafer. Even if a part of the SiO_2 columns was transferred with SOI layers, the columns could be etched by HF solution or dry etching after the area, except for the columns covered with a mask such as a resist.

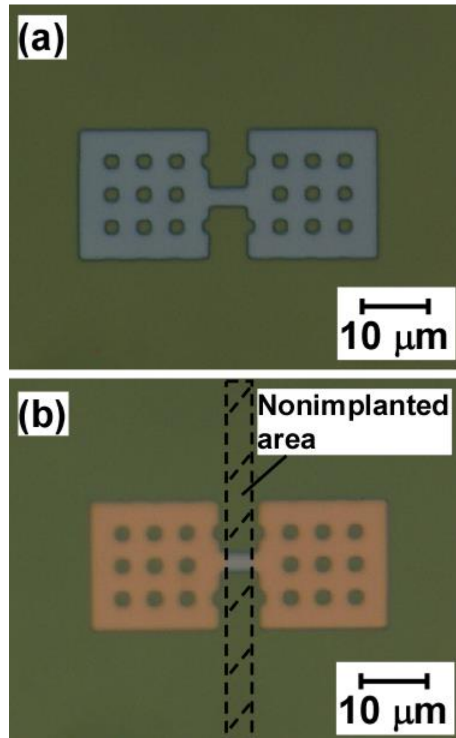

Fig. 6.2. Optical microscope images of (a) top view of channel pattern formed on SOI layer and (b) top view of implanted SOI layer.

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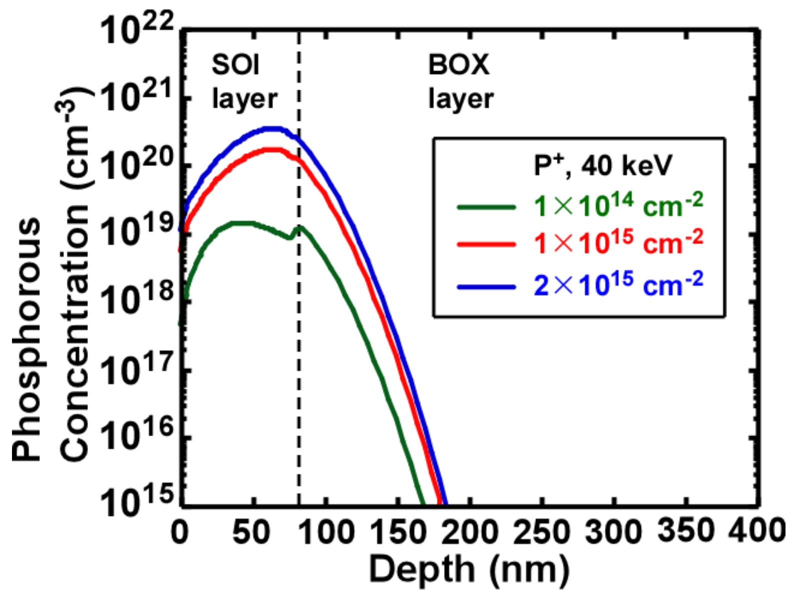

Fig. 6.3. Simulated profiles of phosphorous concentration in SOI after implantation.

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6.3. Results and discussion

The difference in the etching shape between samples with and without ion implantation (I/I) was investigated. As shown in the scanning electron microscope (SEM) images in Figs. 6.4(a)–6.4(c), the middle of the BOX layer was etched more than the area near the SOI layer and the Si substrate. On the other hand, for the implanted sample, the BOX layer near the SOI layer was etched more than the area near the Si wafer, as shown in Figs. 6.4(d)–6.4(f).

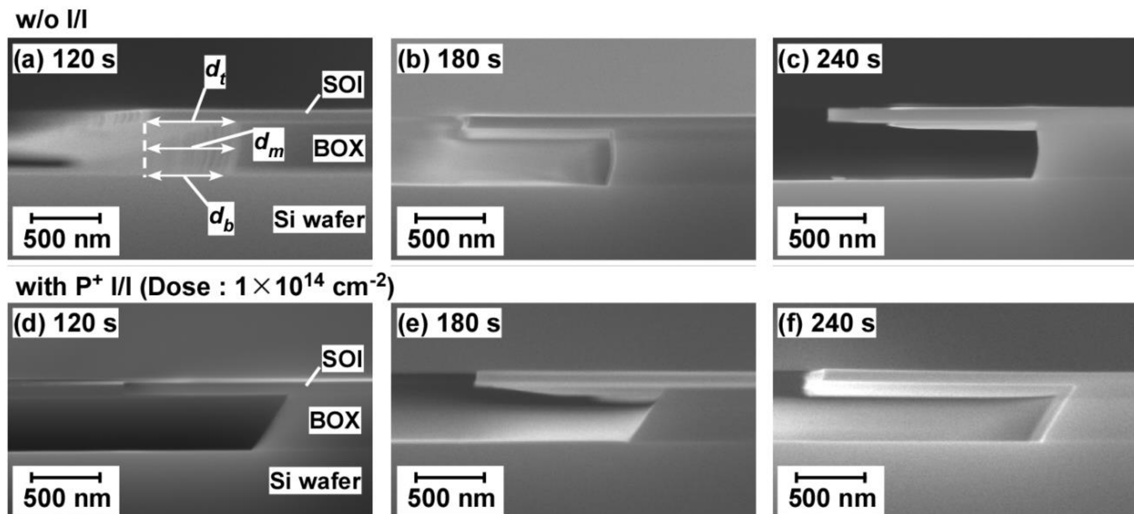

Fig. 6.4. SEM images of side view of SOI wafer (a)–(c) without implantation and (d)–(f) with implantation during midair cavity formation at each etching time.

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Next, the lateral etching distances at the top, middle and bottom of the BOX layer, as shown in Fig. 6.4(a), were measured. The d_t, d_m, and d_b in the samples without I/I and with I/I were plotted with respect to etching time in Figs. 6.5(a) and 6.5(b), respectively. The d_t increased in proportion to etching time irrespective to implantation. From this result, I considered that the lateral reaction rate at the top of the BOX layer is constant.

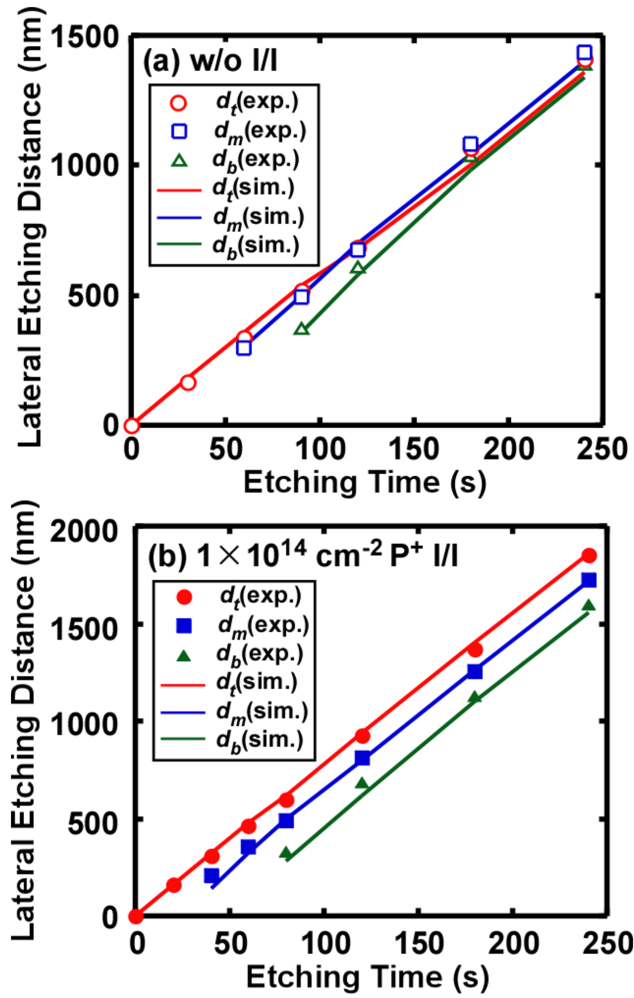

Fig. 6.5. Lateral etching distance plotted against etching time: (a) samples without implantation and (b) samples with implantation (P^+, 1×10^{14} cm^{-2}).

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In addition, in order to analyze the difference in the etching shape of the BOX layers, the etching progress of the BOX layer was modeled on the basis of the following chemical equation of HF solution and SiO_2:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O. \quad (6.1)$$

This simulation was performed using quadrilateral meshes, as schematically shown in Fig. 6.6. The positive or negative number of c in each cell distinguishes HF from SiO_2. In this model, the materials are defined as HF < 0 and $SiO_2 \geq 0$. The value of the cell is calculated using the reaction equation between a solid and a liquid [14].

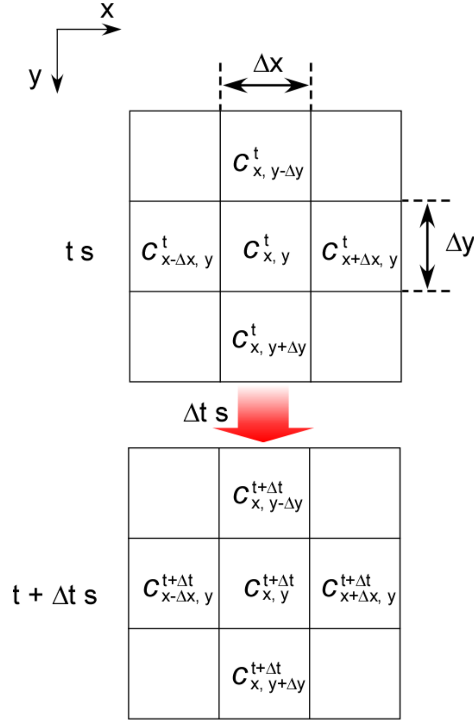

Fig. 6.6. Mesh structure from t s to $t + \Delta t$ s for simulation.

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The molar concentration of a certain mesh at $t + \Delta t$ s is represented using that of the meshes at t s as follows.

$$c_{x,y}^{t+\Delta t} = \begin{cases} c_{x,y}^{t}, \qquad (c_{x,y}^{t} < 0) \\ c_{x,y}^{t} - \frac{1}{6} \cdot \Delta t \cdot \{\mathrm{k_x} \cdot |c_{x-\Delta x,y}^{t}| + \mathrm{k_y} \cdot (|c_{x,y-\Delta y}^{t}| + |c_{x,y+\Delta y}^{t}|)\}, \\ \qquad (c_{x,y}^{t} \geq 0, c_{x-\Delta x,y}^{t} < 0, c_{x,y-\Delta y}^{t} < 0, c_{x,y+\Delta y}^{t} < 0) \end{cases} \tag{6.2}$$

Here, c is the molar concentration of HF or SiO_2, and $\mathrm{k_x}$ in the x-axis direction and $\mathrm{k_y}$ in the y-axis direction are reactive rates per second. In the case of the samples without implantation, when the etching distance along the x-axis direction is greater than the BOX thickness, a fluid flows between the parallel plates.

Without implantation, the molar concentration of HF near the edge of the BOX layer is changed by the balance of the chemical reaction and the ion

diffusion. Therefore, the molar concentration of HF c' replaces c. The c' is given by

$$c' = c * (1 - \frac{r}{a})^n, \tag{6.3}$$

where r and a are the distance from the middle of the BOX layer and half the BOX layer thickness, respectively. Furthermore, in the case of samples with implantation, the reactive rate of the SiO_2 changes depending on the P^+ concentration calculated using simulator and indicated in Fig. 6.3. Figure 6.7 shows the simulated etching profiles of the BOX layers without I/I (n =1/7) and with I/I. The lateral etching distances obtained from the profiles are shown by solid lines in Fig. 6.5. The simulation results agree well with the experimental data. These results indicate that the tapered shape of the BOX layer with I/I was formed because of the difference in the etching rate depending on P^+ concentration toward the BOX depth direction [15].

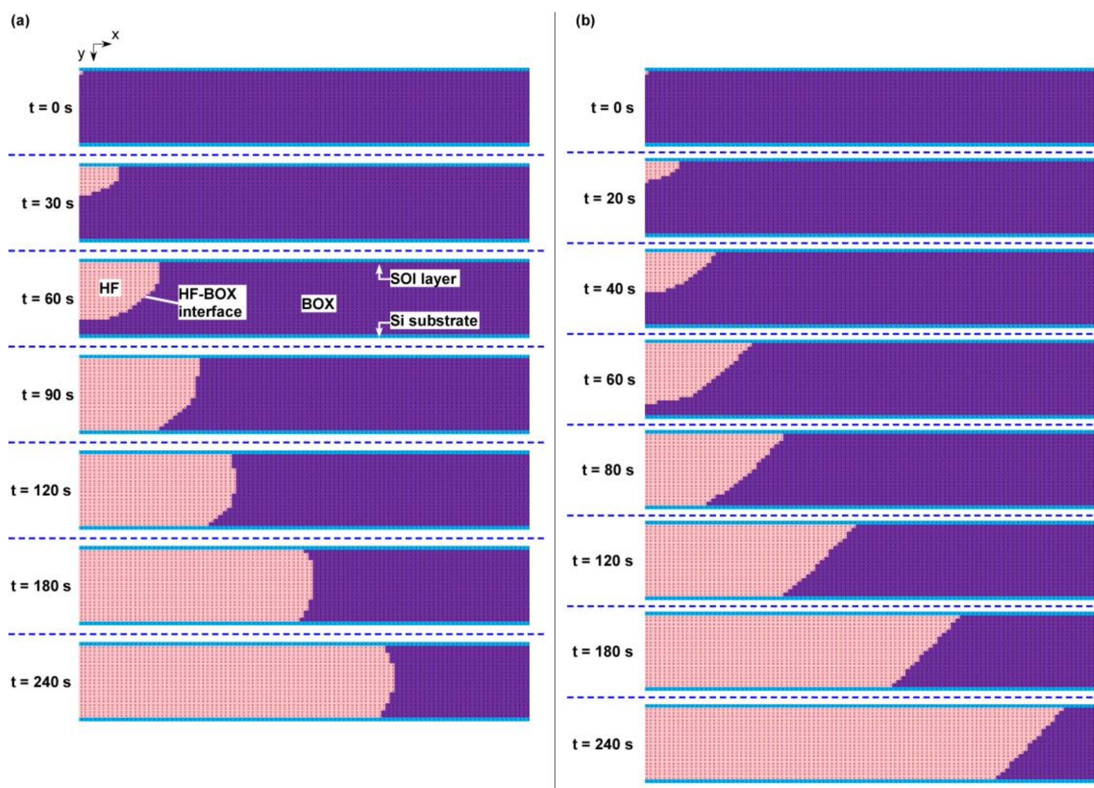

Fig. 6.7. Simulated etching profiles of BOX layer (a) without implantation (n = 1/7) and (b) with implantation (P^+, 1×10^{14} cm^{-2}) for various etching times.

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The side view of the SiO_2 column in the circle shown in Fig. 6.8 was observed. Figures 6.9(a)–6.9(c) show SEM images of the side view of SiO_2 columns of samples without I/I. Here, the column size (*S*) is defined as the narrowest width of the column. The size was decreased by increasing the etching time and it was confirmed that the minimum column size was 137 nm after 390 s of etching. Figures 6.9(d)–6.9(f) show SEM images of the side view of SiO_2 columns of the implanted samples. In the implanted samples, the column shows a tapered side wall. As a result, the SiO_2 column near the SOI layer was narrow and its size was 104 nm after 315 s of etching. This result indicates that by setting the projection range of I/I near the SOI/BOX interface, the shape of the SiO_2 column can be well controlled.

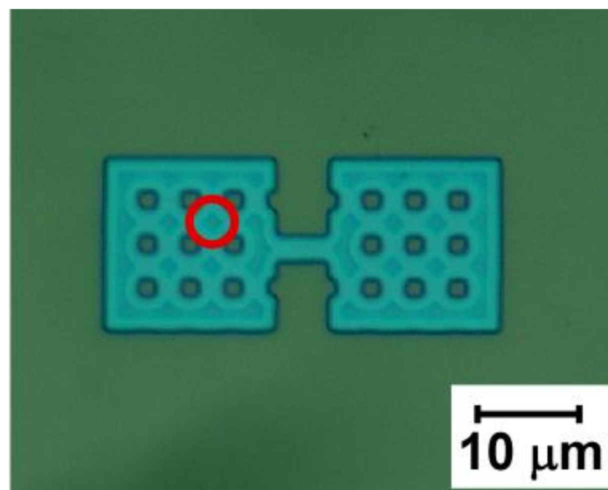

Fig. 6.8. Optical microscope image of top view of SOI layer with midair cavity formed by wet etching of BOX layer.

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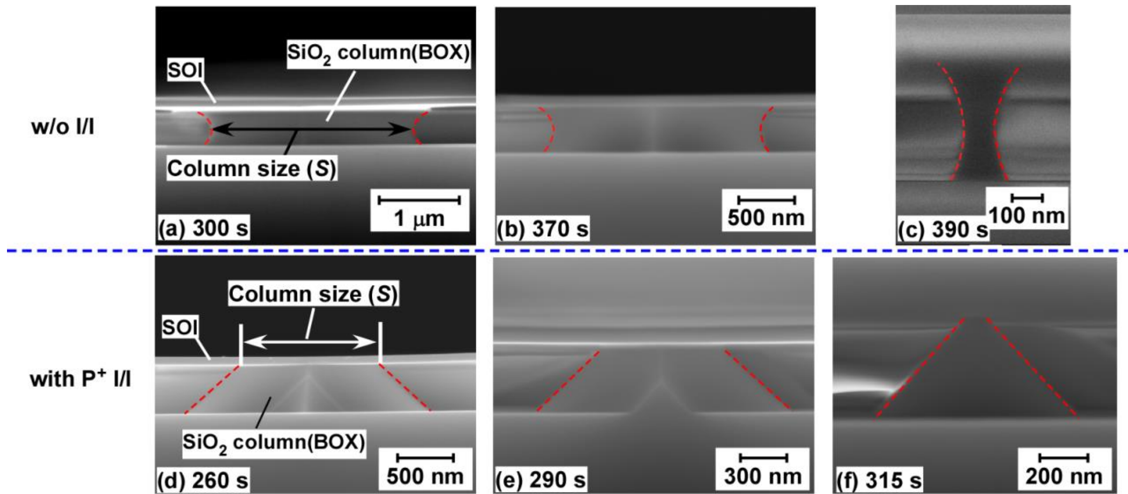

Fig. 6.9. SEM images of side view of SOI layer with midair cavity (a)–(c) without implantation and (d)–(f) with implantation for each etching time.

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Figure 6.10 shows column size as a function of etching time. The column size monotonically decreased with increasing etching time. This figure shows that the slopes of the etching rate were 25–29 nm/s for samples without implantation and 29–32 nm/s for samples with implantation. I consider that the etching of the sample with implantation was faster than that of the sample without implantation because of the higher etching rate of the P^+-implanted BOX region under the SOI pattern, leading to the etching time difference between samples with and without implantation.

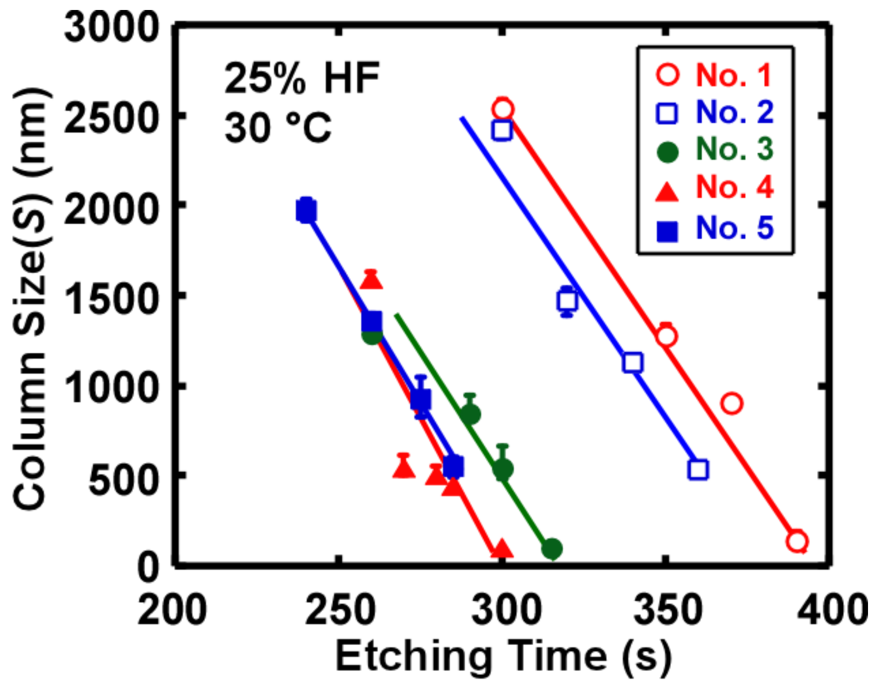

Fig. 6.10. Column size S as a function of etching time. No. 1: as-delivered SOI. No. 2: oxidized SOI. No. 3: oxidized SOI (P^+, 1×10^{14} cm^{-2}). No. 4: oxidized SOI (P^+, 1×10^{15} cm^{-2}). No. 5: oxidized SOI (P^+, 2×10^{15} cm^{-2}).

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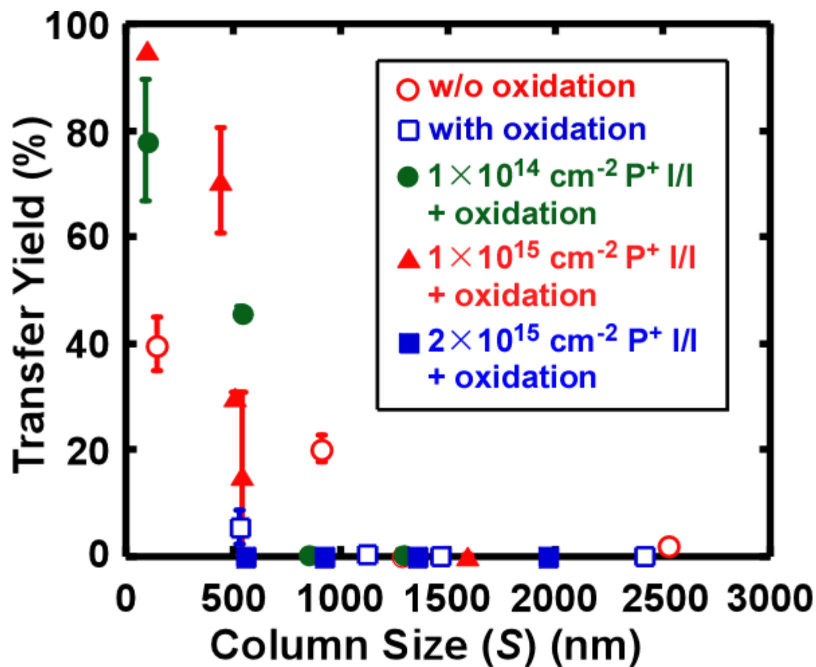

Fig. 6.11. Transfer yield plotted with respect to column size S.

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Next, the samples were transferred to the glass substrate by the MLT technique. Transfer yield is plotted as a function of column size in Fig. 6.11. Here, the transfer yield is defined as the number of SOI patterns transferred to the glass substrate divided by the total number of initial patterns on the SOI wafer. For the SOI layers without I/I, as shown in Fig. 6.11 by the open circles, the transfer yield increased upon decreasing the column size. However, the maximum transfer yield was 35%, as the photograph example shows in Fig. 6.12(a). For oxidized samples without I/I, as shown in Fig. 6.11 by the open squares, the transfer yield was lower. For the samples implanted with doses of 1×10^{14} and 1×10^{15} cm^{-2}, the transfer yield was significantly improved, as shown in Figs. 6.11 and 6.12. The maximum transfer yield was 95%.

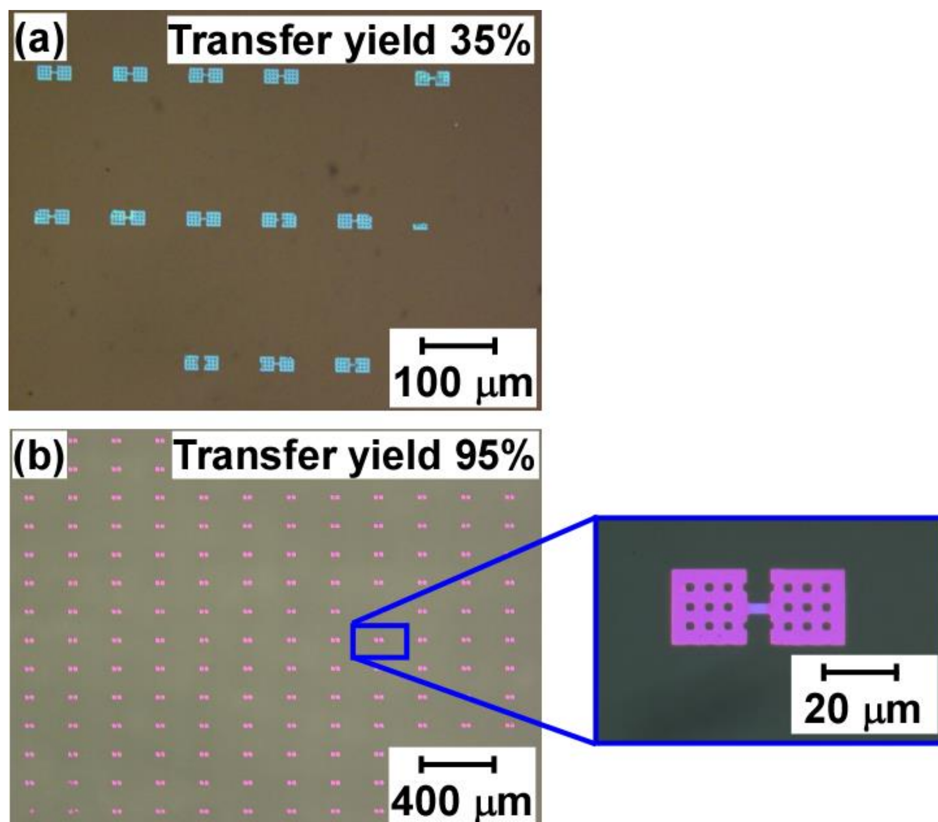

Fig. 6.12. Optical microscope images of the SOI layers transferred to glass substrate: (a) as-delivered SOI layers and (b) oxidized SOI layers implanted with a dose of 1×10^{15} cm^{-2}.

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In contrast, in the case of the samples implanted with a dose of 2×10^{15} cm^{-2}, the SOI layers were not transferred at all. I observed that the bend of the oxidized and implanted SOI layer with a midair cavity after transfer was ~ 300 nm in the position difference between the upper surface of the layer and the lower surface, owing to the formation of a thicker oxide layer in the case of heavily P^+-doped Si [16], as shown in Fig. 6.13. I confirmed that the oxide thickness was increased with increasing the dose, as shown in Fig. 6.14. The largely bent layers were not transferred to the glass substrate because the long distance between the SOI layer and the glass substrate generated less meniscus force (see transfer of SOI layer in Fig. 6.1). From these results, I concluded that the optimum implantation dose for transferring the SOI layer is 1×10^{15} cm^{-2}.

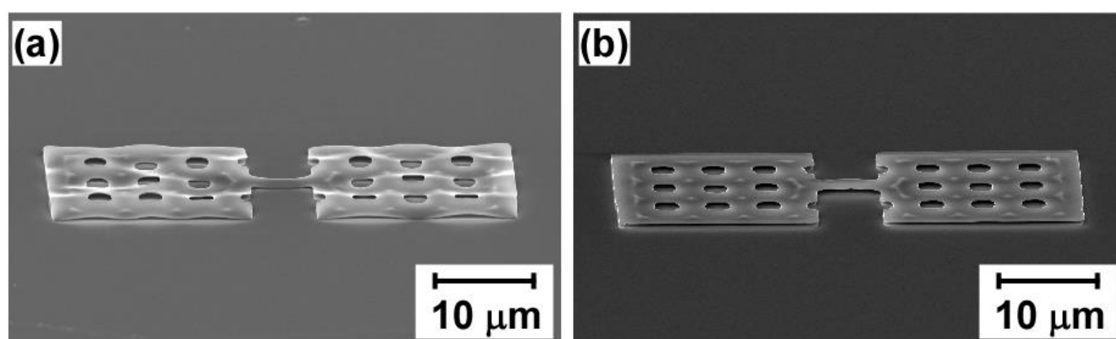

Fig. 6.13. SEM images of the oxidized and P^+-implanted SOI layers with midair cavity after transfer: (a) with a dose of 2×10^{15} cm^{-2} and (b) with a dose of 1×10^{15} cm^{-2}.

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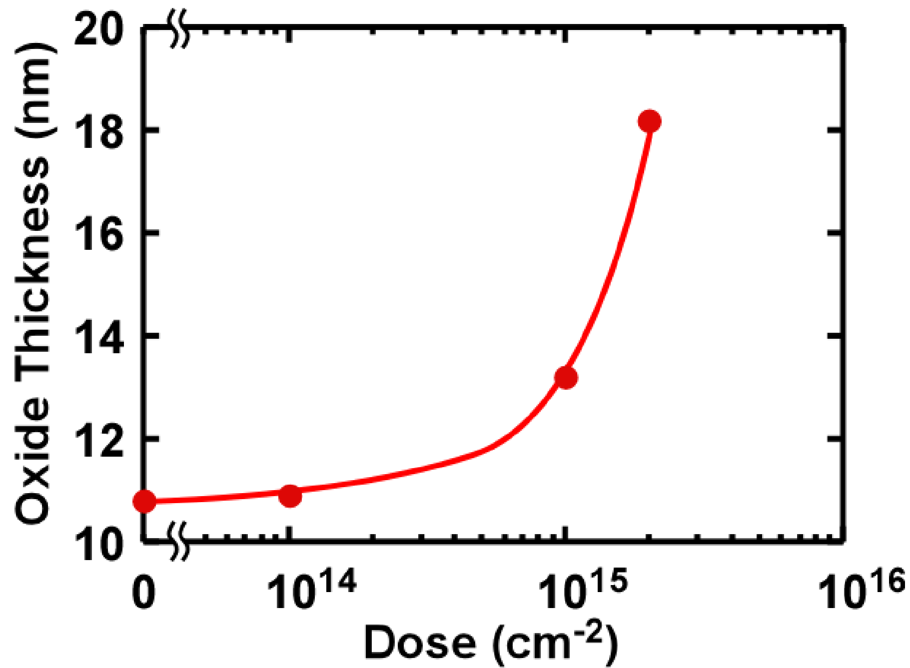

Fig. 6.14. Oxide thickness plotted with respect to ion dose.

In order to investigate other causes of the improvement of transfer yield, the hydrophilicity of the surface SOI layer was evaluated by measuring the contact angle between a water droplet and the surface of the sample (half-angle method [17]). The optical microscope images of the interface between the water droplet and the sample are shown in Fig. 6.15. The contact angle after oxidation decreased from 68° to 42°. Moreover, the contact angle of the implanted samples was decreased to 35°. The meniscus force (F) can be described as

$$F = \frac{2\pi R^2 \gamma cos\theta_E}{H} \ (H \ll R), \qquad (6.4)$$

where R is the radius of the capillary bridge, H is the height of the capillary bridge, γ is the surface tension of water, and θ_E is the contact angle (see transfer of SOI layer in Fig. 6.1) [13]. As a result, I considered that meniscus force was increased by decreasing the contact angle, which improved the transfer yield.

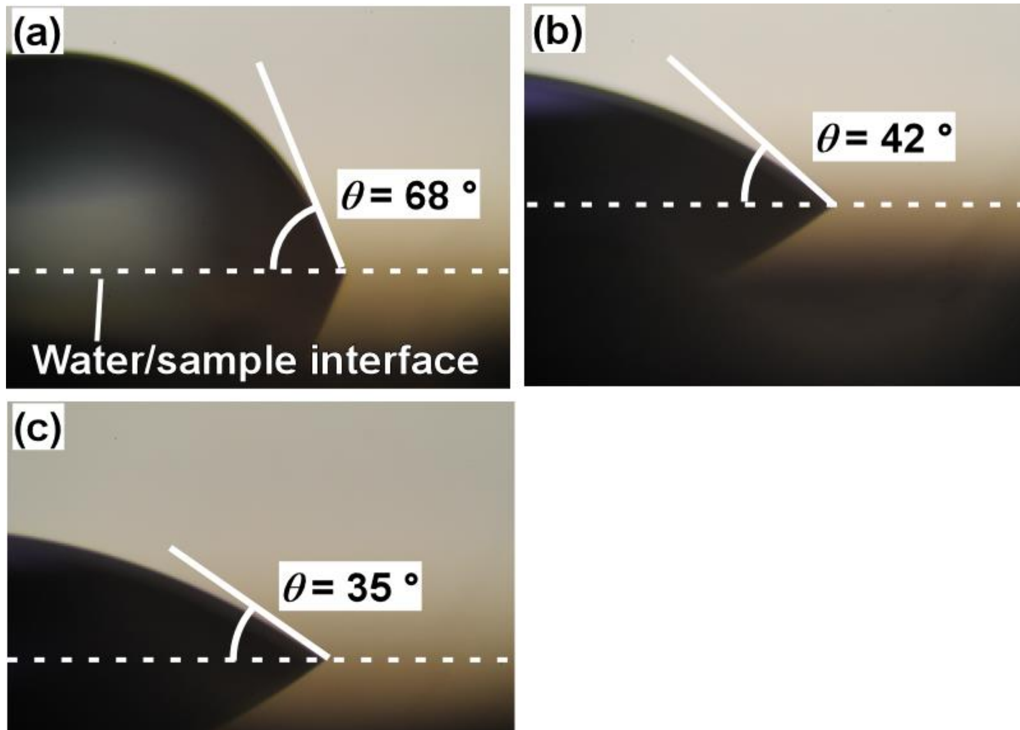

Fig. 6.15. Optical microscope images of interface between the SOI wafer and water droplet: (a) SOI wafer after HF solution and (b) oxidized SOI wafer and (c) P^+-implanted SOI wafer with a dose of 1×10^{15} cm^{-2} after oxidation.

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6.4. Conclusion

I attempted to transfer a phosphorus ion (P^+)-implanted oxidized silicon-on-insulator (SOI) layer with a midair cavity to a glass substrate using meniscus force at a low temperature. The SiO_2 column size was controlled by etching time and the minimum column size was 104 nm. The transfer yield was improved by controlling the column size, and shape, and the maximum transfer yield was 95% under the condition of an implantation dose of 1×10^{15} cm^{-2}.

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Chapter 7

Fabrication of n-channel Si TFTs on glass substrate by using meniscus force-mediated layer transfer

7.1. Introduction

In Chaps. 5 and 6, I introduced into the TFT fabrication process using the MLT technique from Si MOSFET fabrication process, and succeeded in transferring thermally oxidized SOI layers using meniscus force at low temperature.

In this chapter, n-channel TFT fabrication on glass substrate was demonstrated using what I have learned from the results in Chaps. 5 and 6. Further, the low-temperature fabrication process after transfer was introduced.

7.2. Experiments

Table 7.1 shows the TFT fabrication processing condition on each manufacture lot number. An SOI wafer with the SOI layer [p-Si (100)] was used. First, the SOI layer was patterned to a channel shape by photolithography and chemical dry etching. The channel width was 3 μm. Next, the P^+ ions for source and drain regions were implanted. The channel region of the samples with a resist was not implanted. The mask channel length was 4 μm. The channel doping was performed (see the channel doping conditions in Table 7.1). The sample was annealed at 1000 ℃ for 10 min to activate impurities. Next, a midair cavity was formed using HF solution. Then, thermal oxidation of the SOI layer on the midair cavity was performed in dry oxygen at 1000 ℃ (see the thermal oxide thicknesses in Table 7.1) and forming gas annealing (FGA) was performed. After that, the layers were transferred to the glass substrate by the MLT technique. The sample was heated at 80 ℃ on a hot plate for 15 min. Next, an additional gate SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD). Then contact holes were opened. Finally, Al electrodes were formed and post-metallization annealing (PMA) was performed at 300 ℃. The transistors were fabricated at a maximum temperature of 300 ℃ after transfer.

Table 7.1. TFT fabrication conditions on each manufacture lot number.

	Lot. 1	Lot. 2
SOI layer thickness[nm]	80	100
ρ of SOI [Ωcm]	8.5 ~ 11.5	10 ~ 30
BOX layer thickness[nm]	400	300
Ion species for source and drain	P^+	P^+
Implant dose for source and drain [cm^{-2}]	1×10^{15}	1×10^{15}
Implant acceleration energy for source and drain [keV]	40	60
Ion species for channel	BF_2^+	B^+ (1st), BF_2^+ (2nd)
Implant dose for channel [cm^{-2}]	2×10^{11}	1×10^{11}(1st), 1×10^{11}(2nd)
Implant acceleration energy for channel [keV]	30	25(1st), 12.5(2nd)
Mole-concentration of HF [%]	25	33
Thermal oxide thickness [nm]	6	11
Deposited oxide thickness [nm]	193	196

7.3. Results and discussion

First, I show that the results of the fabricated TFTs under the conditions of the manufacture lot. 1 in Table 7.1. Figure 7.1 shows I_{DS}-V_{GS} characteristics of n-channel TFTs fabricated on glass. The average values and standard deviations ($\pm \sigma$) for ten transistors were a field-effect mobility μ_{FE} of 505 ± 76 $cm^2V^{-1}s^{-1}$, threshold voltage of 2.47 ± 0.67 V, and S factor of 324 ± 54 mV/dec, respectively. We succeeded in the fabrication of n-channel TFTs with uniform characteristics on a glass substrate by the MLT technique.

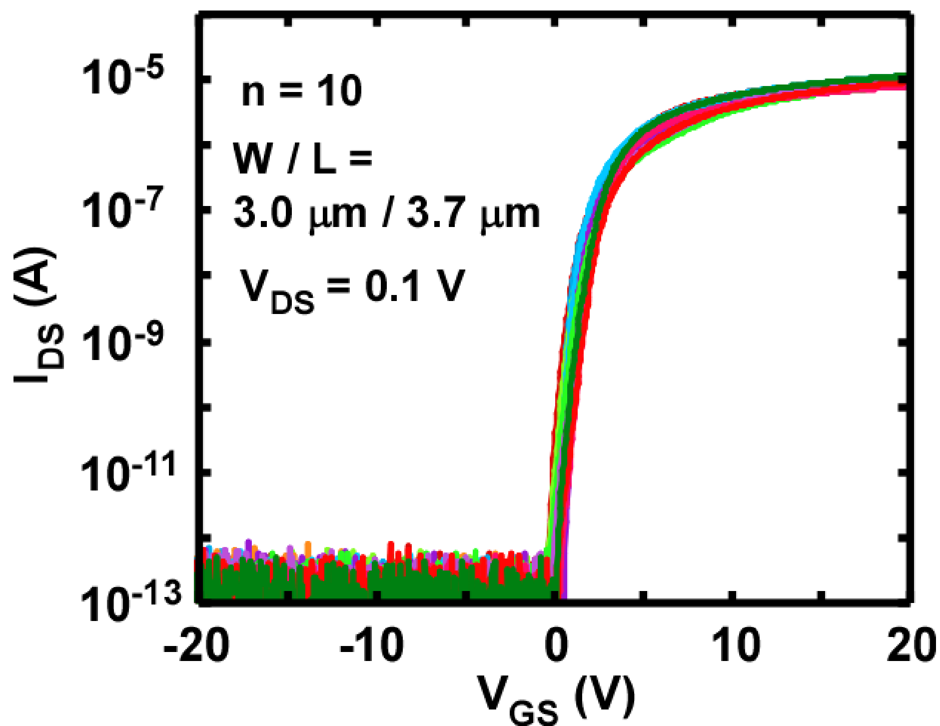

Fig. 7.1. $I_{DS} - V_{GS}$ characteristics of n-channel Si TFTs on glass substrate.

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From capacitance versus voltage (C-V) characteristics of a MOS capacitor fabricated with thermal SiO_2 (10 nm) + PECVD SiO_2 (196 nm), the interface state density (D_{it}) at the midgap, calculated by the high-low-frequency capacitance method [1], is 2.0×10^{10} $cm^{-2}eV^{-1}$. This result indicates that a good MOS interface of the capacitor is formed. At a high SiO_2/Si interface-trap density D_{it}, the S factor can be given by

$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_d+C_{it}}{C_{ox}}\right), \quad (5)$$

where k, q, C_d, C_{it} (= qD_{it}), and C_{ox} are the Boltzmann constant, the unit electronic charge, the depletion-layer capacitance, the interface-trap capacitance, and the gate oxide capacitance, respectively [2]. For an ideal thermal SiO_2 (206 nm)/Si interface, the S factor is 174 mV/dec. However, the S factor of the fabricated TFTs is high. Because of the formation of a good MOS interface in the capacitor, we consider that the cause of a poor MOS interface is the formation of too thin an oxide layer on the back surface of the SOI layer with a midair cavity before transfer, owing to a short oxidation time. We surmise that controlling the oxidation time and oxygen flow rate will lead to an improvement in the formation of oxide.

Next, I present the results of the TFTs under the conditions of the manufacture lot. 2 in Table 7.1. Figure 7.2 shows I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of the n-channel TFT fabricated on glass.

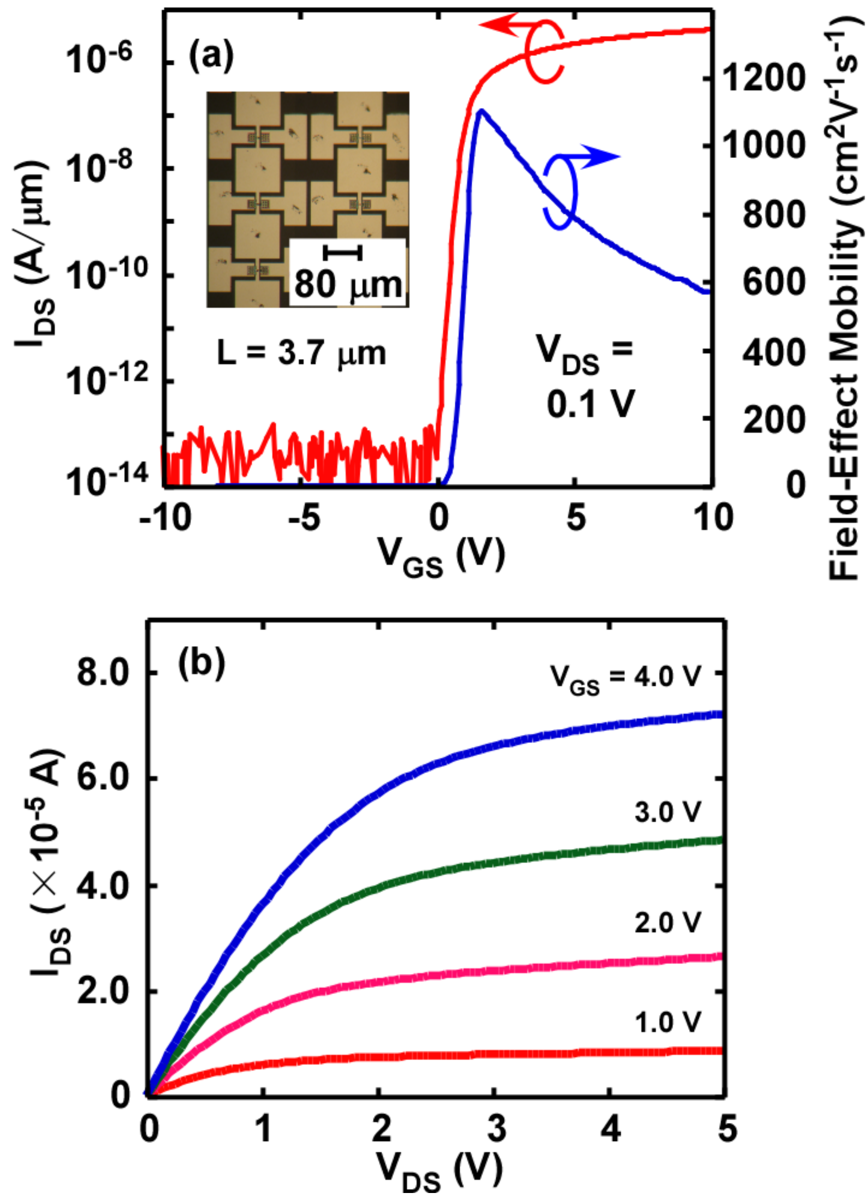

Fig. 7.2. (a) I_{DS}–V_{GS} and (b) I_{DS}–V_{DS} characteristics and field-effect mobility of TFT and optical microscope image of the TFTs.

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The transistor showed very high field-effect mobility of 1097 $cm^2V^{-1}s^{-1}$, which is ~ 53% higher than universal electron effective mobility μ_{eff} [3], and low threshold voltage of 1.1 V, and S factor of 78 mV/dec. In order to evaluate the strain in the transferred Si layer, Raman scattering spectra was measured. Figure 5.9 shows Raman scattering spectra of SOI layers in each process.

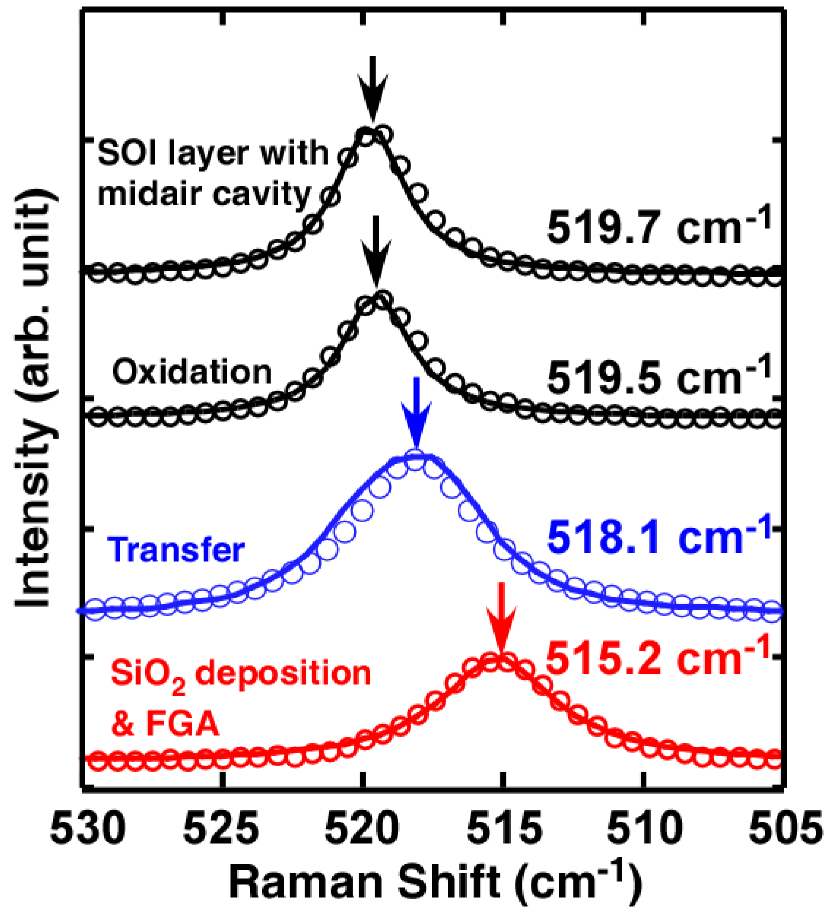

Fig. 7.3. Raman scattering spectra of SOI layers in each process.

Until thermal oxidation of SOI layer, strain of SOI layer was not observed. While, I found that the peak position decreased after transfer and additional SiO_2 deposition, and the TO phonon peak positions after additional SiO_2 deposition and FGA were shifted ~ 4.8 cm^{-1} to lower wave number compared to unstrained Si (520 cm^{-1}). This result indicates tensile strain is introduced in the transferred channel layer after gate SiO_2 deposition and the amount corresponds to μ_{eff} enhancement of ~ 53% [4]. As for the tensile strain after transfer, it is presumed that the transferred SOI layer is expanded in order to buffer the bend of thermally oxidized SOI layer, and the channel region is strained. I consider that the tensile strain of SOI layer after deposition is introduced due to coefficient of thermal expansion mismatch between Si and additional deposited SiO_2. In order to verify the correlation between mobility enhancement and channel strain, gate

electrodes of the TFTs were removed after electrical measurements, and the Raman peak shifts of the channel regions were directly measured. Laser beam of 514.5 nm wavelength was used. Laser beam diameter was 1 μm. Figure 7.4 shows the mobility enhancement ratio and the Raman peak shift $\Delta\omega$ of each TFT channel. The error bars indicate $\Delta\omega$ variation depending on the measurement position inside the channel. Mobility enhancements observed in strained Si on $Si_{1-x}Ge_x$ buffer [4] and the predicted bulk, phonon-limited mobility ratios [5] are also shown by square and solid line for comparison, respectively. The mobility enhancements observed in our TFTs show good agreement with the reference data except for data points in low enhancements. This indicates the high mobility TFTs fabricated by the proposed method is due to the tensile strain. As a conclusion, the proposed fabrication process realizes significantly higher performance TFTs compared to the transistors fabricated by conventional materials (see Table 7.2). These results suggest that the proposed MLT technique and TFT fabrication process opens up a new field of silicon applications that is independent of scaling.

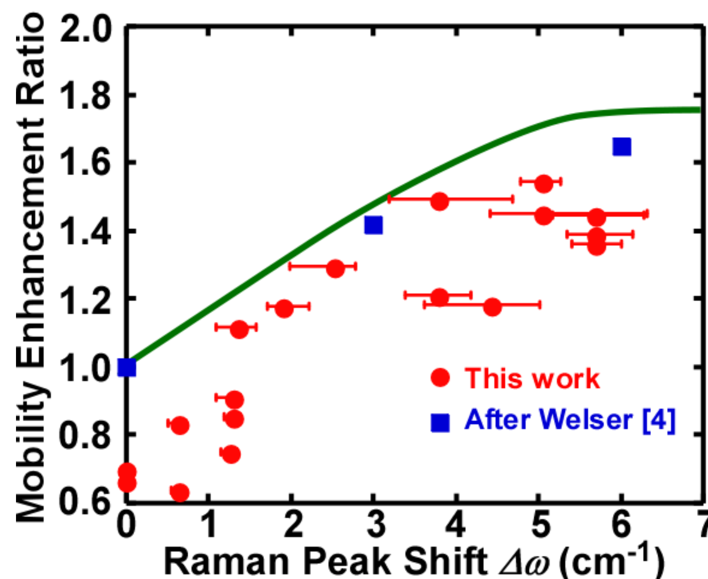

Fig. 7.4. Mobility enhancement ratios of the fabricated TFTs plotted with respect to Raman peak shift $\Delta\omega$ of channel region.

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Table. 7.2. Comparison of TFT performances based on different channel materials.

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	μ_{FE} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	S factor (mV/dec.)	Process temperature (ºC)
Pentacene[6]	2.0	4.0	-	80
C_8-BTBT[7]	16.4	-10	-	27
a-IZO[8]	15.3	-4.5	1200	280
a-InGaZnO[9]	12.4	-0.8	120	400
a-Si:H[10]	0.6	2.0	500	280
LTPS[11]	640	0.8	220	270
MLT silicon	1097	1.1	78	300

7.4. Conclusion

Under the optimum conditions in Chaps. 5 and 6, I demonstrated that n-channel thin-film transistors (TFTs) fabrication on glass at 300 ºC. The TFTs showed a field-effect mobility of 505 $cm^2V^{-1}s^{-1}$, a threshold voltage of 2.47 V and a subthreshold swing of 324 mV/dec. on average.

In addition, n-channel thin-film transistor (TFT) fabricated on glass at 300 ºC under the different conditions showed a field-effect mobility of 1097 $cm^2V^{-1}s^{-1}$, a threshold voltage of 1.1 V and a subthreshold swing value of 78 mV/dec. Raman scattering analysis suggests the mobility enhancement of the TFTs is related to tensile strain.

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Conclusions

I proposed Si thin-film transistor (TFT) fabrication on glass substrate for meniscus force-mediated layer transfer (MLT) technique.

One of the key process is the thermal oxidation of SOI layer on midair cavity. The SOI layers were bent after oxidation, and longer lines and thicker oxide showed larger deformation (> 300 nm) due to accumulation of oxidation strain. In contrast, under the condition of shorter length and thinner oxide, deformation was less than 100 nm. The SOI layer was completely transferred to glass without any problem.

Next, I observed SOI layers with a midair cavity after ion implantation and thermal oxidation, and attempted to improve the transfer of the SOI layers to the glass substrate. The SiO_2 column size was controlled by etching time and the minimum column size was 104 nm. The transfer yield of the implanted sample was significantly improved by decreasing the column size, and the maximum transfer yield was 95% when the implantation dose was 1×10^{15} cm^{-2}. The causes of increasing transfer yield are considered to be the tapered SiO_2 column shape and the hydrophilicity of the surface of oxidized samples with implantation.

Finally, I attempted to fabricate Si TFTs on glass substrate by using MLT technique. N-channel TFTs fabricated using the films on glass at 300 ºC showed a field-effect mobility of 505 $cm^2V^{-1}s^{-1}$, a threshold voltage of 2.47 V and a subthreshold swing of 324 mV/dec. on average. In addition, under different manufacturing conditions, strained-Si TFT showed very high field-effect mobility of 1097 $cm^2V^{-1}s^{-1}$, which is ~ 53% higher than universal electron effective mobility. From the Raman spectra of each TFT channel, the mobility enhancement of TFTs is related to tensile strain.

These results suggest that the MLT technique is highly promising for application to high-performance TFT fabrication on an insulator with low-heat resistance at a low temperature.

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2015

Muneki Akazawa

Appendix

List of publications and awards

Main paper

(1)Fabrication of N-channel single crystalline silicon (100) thin-film transistors on glass substrate by meniscus force-mediated layer transfer technique
Muneki Akazawa, Kohei Sakaike, Shogo Nakamura, and Seiichiro Higashi
Japanese Journal of Applied Physics, **53**, 108002-1 – 108002-3 (2014).
(2)Formation of silicon-on-insulator layer with midair cavity for meniscus force-mediated layer transfer and high-performance transistor fabrication on glass
Muneki Akazawa, Kohei Sakaike, and Seiichiro Higashi
Japanese Journal of Applied Physics, **54**, 086503-1 – 086503-7 (2015)

Reference paper

(1)Fabricating metal-oxide-semiconductor field-effect transistors on a polyethylene terephthalate substrate by applying low-temperature layer transfer of a single-crystalline silicon layer by meniscus force
Kohei Sakaike, Muneki Akazawa, Shogo Nakamura, and Seiichiro Higashi
Applied Physics Letters, **103**, 233510-1 – 233510-4 (2013).
(2)Low-temperature layer transfer of midair cavity silicon films to a poly(ethylene terephthalate) substrate by meniscus force
Kohei Sakaike, Shogo Nakamura, Muneki Akazawa, and Seiichiro Higashi
Japanese Journal of Applied Physics, **53**, 018004-1 – 018004-3 (2014).
(3)Fabricating High-Performance Silicon Thin-Film Transistor by Meniscus Force Mediated Layer Transfer Technique
Kohei Sakaike, Muneki Akazawa, Akitoshi Nakagawa, and Seiichiro Higashi
ECS Transactions **64**(10), 17-22 (2014).
(4)Meniscus-force-mediated layer transfer technique using single-crystalline silicon films with midair cavity: Application to fabrication of CMOS transistors on plastic substrates
Kohei Sakaike, Muneki Akazawa, Akitoshi Nakagawa, and Seiichiro Higashi
Japanese Journal of Applied Physics, **54**, 04DA08-1 – 04DA08-5 (2015).

Conference paper

(1) Local Transfer of Single-Crystalline Silicon (100) Layer by Meniscus Force and Its Application to High-Performance MOSFET Fabrication on Glass Substrate
Muneki Akazawa, Kohei Sakaike, Shogo Nakamura and Seiichiro Higashi
International Electron Devices Meeting Technical Digest 11.7-1 - 11.7-4 (2013).

Awards

1. IEEE EDS Japan Chapter Student Award (IEDM)/EDS Japan Chapter Chair /2014.2.3.
2. Hiroshima University Excellent Academic Award/President of Hiroshima University /2014.4.3.
3. Thin Film Materials & Devices Meeting Student Award/Thin Film Materials & Devices Meeting Chair/2014.11.1.
4. Hiroshima University Excellent Student Scholarship in the Academic Year 2014/President of Hiroshima University/2014.12.15.

公表論文

(1) Fabrication of N-channel single crystalline silicon (100) thin-film transistors on glass substrate by meniscus force-mediated layer transfer technique
Muneki Akazawa, Kohei Sakaike, Shogo Nakamura, and Seiichiro Higashi
Japanese Journal of Applied Physics, **53**, 108002-1 – 108002-3 (2014).

(2) Formation of silicon-on-insulator layer with midair cavity for meniscus force-mediated layer transfer and high-performance transistor fabrication on glass
Muneki Akazawa, Kohei Sakaike, and Seiichiro Higashi
Japanese Journal of Applied Physics **54**, 086503-1 – 086503-7 (2015).

参考論文

(1) Fabricating metal-oxide-semiconductor field-effect transistors on a polyethylene terephthalate substrate by applying low-temperature layer transfer of a single-crystalline silicon layer by meniscus force
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