博士論文

Study on Wireless CMOS Receivers for Satellite Applications

衛星機器向けワイヤレス CMOS 受信器に関する研究

満 仲　　健

広島大学大学院先端物質科学研究科

2016 年 3 月

目次

１．主論文

Study on Wireless CMOS Receivers for Satellite Applications
（衛星機器向けワイヤレス CMOS 受信器に関する研究 ）
満仲　健

２．公表論文

(1) “9 dB NF and +11 dBm OIP3 CMOS Single Conversion Front-End for a Satellite Low-Noise Block Down-Converter”
Takeshi Mitsunaka, Yusuke Kishino, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima,
IEICE Trans. Fundamentals, vol. E97–A, No.01 Jan. 2014, pp.101-108.

(2) “8-GHz Locking Range and 0.4-pJ Low-Energy Differential Dual-Modulus 10/11 Prescaler”
Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima,
IEICE Trans. Fundamentals, vol. E97-C, No.06, Jun. 2014, pp.486-494.

３．参考論文

(1) “4 GHz locking range and 0.19 pJ low-energy differential dual-modulus 10/11 prescaler”,
Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima,
IEEE Asian Solid-State Circuit Conf. (A-SSCC), pp.373-376, Nov. 2012.

(2) “The Effect of Supply Voltage Reduction to 5.8-GHz Differential Dual-Modulus Prescaler”
Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima,
IEEE Int. Meeting for Future of Electron Devices, Kansai (IMFEDK), pp.30-31, June 2013.

(3) “37-mW CMOS Voltage-Controlled Oscillators and Dividers for 134-GHz Phase-Locked Loop Synthesizer”
Takeshi Mitsunaka, Kunihiko Iizuka and Minoru Fujishima,
European Microwave Integrated Circuits (EuMIC) , pp.293-296, October 2014.

主論文

Abstract

A study on wireless CMOS receivers for satellite applications is described. In particular, the circuit elements of CMOS down-converter ICs for a broadcasting satellite and a submillimeter receiver such as for radio astronomy are focused. Similarly to common receivers, broadcasting satellite down-converters require lower power consumption, a smaller size and the achievement of the target specifications. In addition, higher reliability under variations in temperature is required because broadcasting satellites are used in open air from the equator to the arctic. However, previous down-converters contained many discrete parts, resulting in issues of not only manual alignment but also temperature drift, time degradation, a large size and high cost. Down-converter ICs with a phase locked loop (PLL) synthesizer were expected to solve these issues. In this study, an integrated CMOS down-converter IC for a broadcasting satellite was described.

In addition, a CMOS PLL synthesizer for satellite applications such as radio astronomy that operates at frequency of over 100 GHz was also described. Furthermore, integrated CMOS circuit elements for a high frequency PLL synthesizer are developed. To realize a CMOS PLL synthesizer operating at frequency of over 100-GHz, a high-speed oscillator and dividers must be developed. In particular, the dividers must operate in a wide frequency range to cover the entire range of operations of the front circuit.

Chapter 2 discusses the techniques used in the integer-N-type PLL synthesizer for a CMOS down-converter IC with a range of 10 GHz and high frequency circuits operating at frequencies exceeding 100 GHz for radio astronomy. A 10-GHz-band CMOS voltage control oscillator (VCO) has a trade-off between low and high VCO gain to realize low phase noise and a wide oscillation range from 9.75 GHz to 11.3 GHz. In addition, a wide range of operation is required to ensure temperature tolerance necessary for open air use. To solve the above the issue, a wide range VCO with the switching varactors was discussed and study results of a 10-GHz band CMOS PLL synthesizer for a broadcasting satellite was described.

In chapter 2, a VCO and dividers for a 134-GHz PLL synthesizer are also discussed. The dividers have injection locked frequency dividers (ILFDs),

which are used in the tuning of the back-gate voltage to increase the operation range of divide-by-two. The developed VCO has a fundamental oscillation frequency range of 131.8 GHz to 134.3 GHz which is controlled by the back-gate voltage. The dividers can cover the entire VCO oscillation range. When the phase frequency detector, charge pump and loop filter are operated in a 10-GHz band, it will be possible to operate the 134-GHz on-chip PLL synthesizer.

Chapter 3 discusses full-differential dual-modulus prescalers in an integer-N-type PLL. Dual-modulus prescalers with a wide locking range, high-frequency operation and a low power based on an ILFD were proposed. They were fabricated in CMOS 130-nm and CMOS 65-nm processes. In this research, the first prescaler fabricated by the CMOS 130-nm process was successfully operated in a range of 4 GHz to 6 GHz indicating its temperature tolerance. The other prescaler fabricated by the CMOS 65-nm process was successfully operated in a range of 22 GHz to 23 GHz, and/or more a wider frequency range. The range of operation and the normalized energy consumption are compared with those of previous prescalers, which showed that good performances were achieved. In addition, the tolerances of phase difference deviation and phase noise degradation are also discussed.

Chapter 4 focuses on the amplifiers and mixer for a 10-GHz band CMOS down-converter IC. To obtain the target frequency range of the 10-GHz band, a low-noise, low current and high-gain RF amplifier and the mixer architecture are described. Satellite applications are constructed in the open air and a constant conversion gain despite variations in the temperature is required. In this research, a temperature-compensated variable-gain amplifier (TC-VGA) is proposed. To maintain a linear output, a constant output 3rd ordered intercept point (OIP3) VGA is also proposed. The amplifiers and mixer are discussed to realize these target specifications.

Chapter 5 gives a conclusion to this research, in which I outline my future works, which include the integration of high-frequency applications. The proposed CMOS down-converter IC for a broadcasting satellite has the potential to be mass-produced and contributed to the sales performance. For sub-millimeter operation with a wide frequency range, CMOS integration guidelines should be obtained.

Acknowledgement

First of all, I would like to express my gratitude to my supervisor, Professor Minoru Fujishima. I have had the support and encouragement of him when I came across difficulties and for many good suggestions in regard to my research and development. I also benefitted a lot from his creatively and his intelligence in my school days.

I would also like to thank other four members of my committee: Professor Takamaro Kikkawa, Professor Hans Jürgen Mattausch, Professor Shuhei Amakawa and Professor Takeshi Yoshida for their valuable suggestions on my dissertation talk and for the time spent reviewing my thesis.

I would also like to thank two assistant professors and a research scientist: Dr. Kyoya Takano, Dr. Mizuki Motoyoshi and Dr. Kosuke Katayama for their great helps and good suggestions in my laboratory works.

My research has been supported by Sharp Corporation and I would like to thank Dr. Kunihiko Iizuka, who gave me the opportunity and good suggestions of this research. I would also like to thank my colleagues in Sharp who have contributed to this work with interactions and technical discussions.

Lastly, I am deeply indebted to my wife Sawako and our children, Kanae and Tatsuya. Without their love and support, I could not have possibly reached this stage of the work.

Thank you.

January 26, 2015
Takeshi Mitsunaka

Contents

Chapter 1. Introduction

1.1 Radio Frequency (RF) Allocation

Radio waves are the public property. In Japan, the Ministry of Internal Affairs and Communications (MIC) allocates radio wave channels [1]. In other countries, government agencies similarly allocate radio wave channels. The allocated channels are used for almost the same purposes in different countries. For example, the radio frequency allocated for Japanese terrestrial television broadcasting services is from 470 MHz to 710 MHz and that for broadcasting and communication satellite services is in a 10-GHz band from 10.7 GHz to 12.75 GHz.

There are many services in the world using radio wave and the frequency range of 30 GHz or lower is particularly crowded. Recently, television broadcasting services, wireless local area networks (W-LAN) and mobile phone services have rapidly expanded and have become an important infrastructure worldwide. To maintain various services using radio waves, it is important to efficiently use allocated radio frequencies.

In Japan, the transition from analog broadcasting to digital broadcasting was in July 2011, which expanded the range of frequencies for other services. At the same time, the frequency range for terrestrial broadcasting service was decreased and rearranged. The frequency range for wireless mobile services was

expanded into the vacant frequency range previously allocated to terrestrial broadcasting. As mentioned above, it is effective to alocate radio frequencies for expanding wireless services. However, it is not easy to relocate radio frequency band at the state level.

Another method of increasing the usability of radio waves is to use higher frequencies than those of millimeter waves such as exceeding 100 GHz. In recent studies, millimeter communication systems using frequencies of around 60 GHz and radar systems using frequencies from 70 GHz to 80 GHz have been developed. However, frequencies exceeding 100 GHz are hardly used except for radio astronomy. The infrastructure, usage instructions, system development, markets and applications must be studied to enable the use of frequencies exceeding 100 GHz.

1.2 Satellite Applications

Satellite applications use a parabolic antenna with a curved surface to receive waves with comparative high frequency. The operating principle of a parabolic antenna is that a point source of an RF signal at the focal point in front of a reflector made of a conductive material is reflected into a collimated plane-wave beam along the axis of the reflector. Conversely, an incoming plane wave parallel to the axis is focused to a point at the focal point. A feed horn is located at the focal point and is connected to the associated RF receiving devices with a low noise block (LNB) down-converter module as shown in Figure 1.1.

An LNB down-converter is a receiving device with local oscillators (LOs) and mixing blocks. An RF signal from the satellite or a cosmic radio wave is converted to an intermediate-frequency (IF) signal by an LO signal. Basically, satellite applications are constructed in open air and directed toward a radio wave source. An LNB down-converter is covered with a packing case with humidity resistance although temperature remains a particularly important issue for commercial satellite applications.

In addition to commercial satellite applications, some research

satellite applications such as radio astronomy have a high frequency LO signal of over 100 GHz. If an integrated oscillator and receiver system operating at frequencies of over 100 GHz is realized, it will contribute to the realization of not only smaller radio astronomy equipment but also various communication systems, sensors and other systems using integrated systems. The realization of a wide operation range at frequencies of over 100 GHz is expected to lead to the development as various systems.

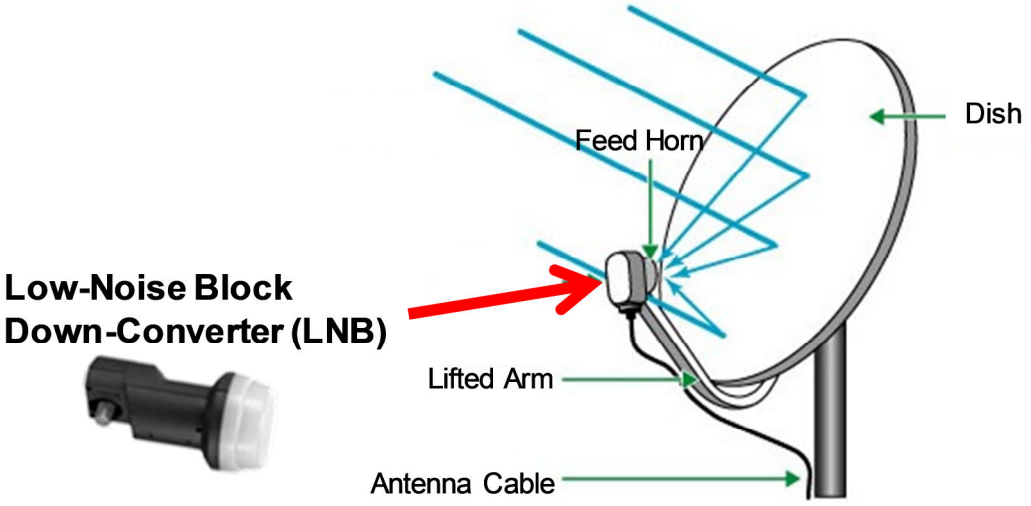


Figure 1.1: Image of the common satellite antenna with a dish, a feed horn and an LNB down-converter.

1.3 Manufacturing Issues of Satellite Applications

The manufacturing issues of satellite applications are described. A 10-GHz band broadcasting satellite down-converter is a receiving device and similarly to other wireless receivers, it requires low power consumption, a small size and a low cost while satisfying various specifications. In addition, broadcasting satellites with a parabolic antenna are used both at the equator and in the arctic, meaning that temperature tolerance is also required. In addition to broadcasting satellites, research satellite applications such as radio astronomy use high-frequency LO signals exceeding 100 GHz. The manufacturing issues of a broadcasting satellite and a high frequency application are described as follows.

1.3.1 Application 1: A 10-GHz Band Broadcasting Satellite

A broadcasting satellite provides a wide range of channels and services. The growing demand for new high-data-rate digital services via satellite, such as high-definition television (HDTV), is having an impact on the markets of developing countries. In the large countries not enough to cover area of terrestrial broadcasting, broadcasting satellites is efficient method for watching television.

A detail broadcasting satellite system is shown in Figure 1.2. A satellite dish antenna receives an RF satellite signal in the 10-GHz band from an artificial satellite. In general, RF satellite signals have two-polarized waves, horizontal and vertical waves. RF signals are reflected on the satellite dish and collected to the feed horn on the lifted arm. A feed horn has an LNB down-converter which translates RF signal to IF signal using LO signals. The frequency values of RF, IF and LO are different from various receiving area or broadcasting providers. Table 1.1 shows the main specifications of LNB chip-set for satellite television.

In the past, the LO signal sources of an LNB down-converter used discrete open-loop dielectric resonator oscillators (DROs), which required not only manual alignment but also a temperature drift, time degradation, large size and cost by many discrete parts. Figure 1.3 (a) is the photograph of previous an LNB down-converter module for a broadcasting satellite and Figure 1.3 (b) is a block diagram of an LNB down-converter module.

To solve above the issues, an LNB down-converter integrated circuit (IC) with a phase locked loop (PLL) synthesizer generated an LO signal had been expected by the manufactures and customers. A PLL synthesizer is an effective part generating a correct LO frequency signal and unnecessary manual alignment. Considering with use in open air, constant operation for temperature variation is required. It means temperature tolerance and wide margin operation under variations in temperature. Amplifiers and mixing block are also similar, wide range operation and constant conversion-gain is required. Temperature tolerance leads to the

high reliability of consumer satellite applications.

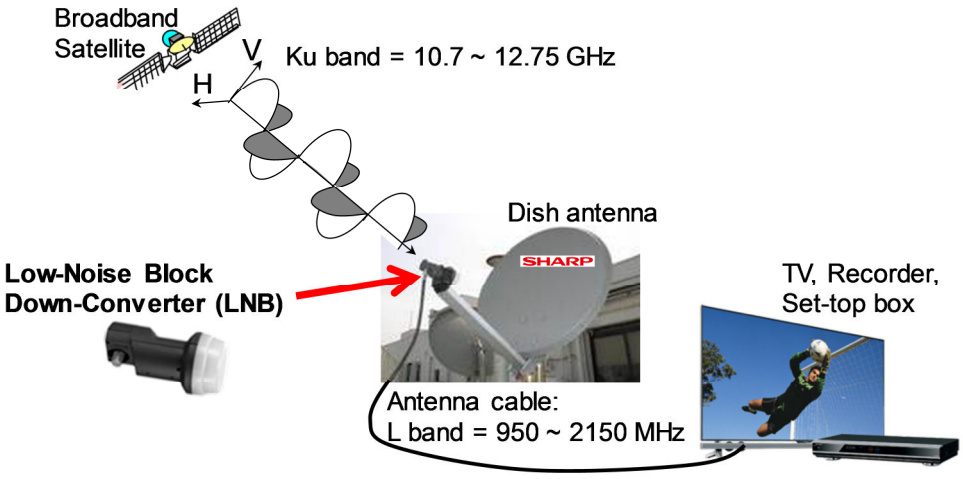
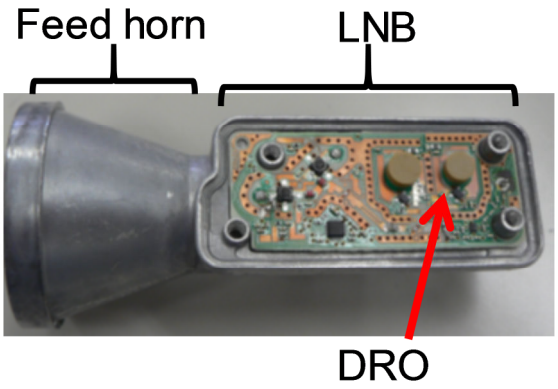


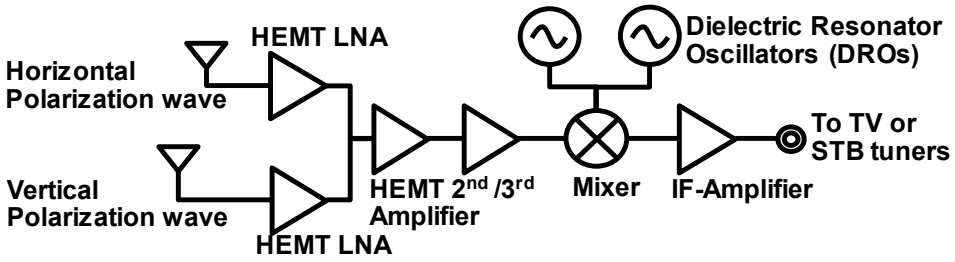
Figure 1.2: Image of the broadcasting satellite system.

Table 1.1: Specifications of an LNB down-converter module for broadcasting satellite

	Universal Band	ABS-S Band	Asian Band	Japan Band
RF: input frequency	10.7 – 12.75GHz	11.7 – 12.75GHz	12.25 – 12.75GHz	11.7 – 12.75GHz
LO frequency	9.75 GHz or 10.6 GHz	10.75 GHz	11.3 GHz	10.678 GHz
IF: output frequency	950 - 2150 MHz	950 - 2000 MHz	950 - 1450 MHz	1022 - 2072 MHz
Conversion gain	55 dB or more	55 dB or more	55 dB or more	55 dB or more
Noise Figure	0.9 dB or less	0.9 dB or less	0.9 dB or less	0.9 dB or less
Main countries adapting	Europe,India, Middle East etc.	North America, China etc.	Australia, South-East etc.	Japan



(a)



(b)

Figure 1.3: Previous broadcasting satellite module. An LNB module photograph (a) and a block diagram (b).

1.3.2 Application 2: A Radio Astronomy over 100-GHz Range

As an example of a current application of radio astronomy, Figure 1.4 shows a photograph of "VERA Iriki" station, which located in Iriki farm of Kagoshima University. According to its website in [2], a number of different sources of radio emissions have been observed, including stars and galaxies, as well as entirely new classes of objects, such as quasars, pulsars and masers.

When the receiver system is focused, LO frequencies generated by a gunn-diode oscillator is used in a down-converter [3] - [4] and a superconductor insulator superconductor mixer (SIS mixer) is used as a mixing block [5] - [6]. To enhance the detection sensitivity when

receiving astronomy wave signals, a gunn-diode oscillator and SIS mixer are operated at an ultra-low temperature of 20 K. Figure 1.5 shows the signal down-converter module used for the radio astronomy system. The LO frequencies are allocated to various frequencies including millimeter and sub-terahertz frequencies.

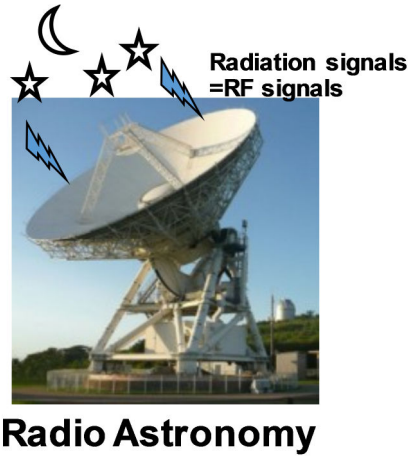


Figure 1.4: Photograph of a satellite antenna for radio astronomy

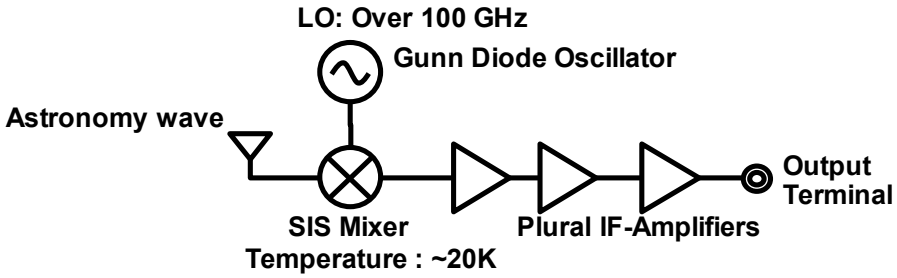


Figure 1.5: Example of LNB integration for the radio astronomy. Gunn-diode and SIS mixer is used in very low temperature.

Similarly to a common receiver system, the LO signal sources are very important parts, that require low phase noise and high frequency accuracy. However, it is difficult to realize CMOS PLL synthesizers with operation above 100 GHz. If they are realized, CMOS systems of not only radio astronomy but also short-range communication systems, sensor systems and other applications are expected. CMOS high-speed circuits such as an oscillator and dividers must be built. In particular, dividers must operate in a

wider frequency range to cover the entire frequency range of the front circuit operation.

1.4 CMOS Down-Converter IC for Satellite Applications

The aim of my research is to implement down-converter ICs for satellite applications. RF integrated circuits in silicon became a reality in the 2000s by using CMOS transistors with unity current gain frequency (f_T) of 10 GHz. Figure 1.6 shows a comparison of CMOS, SiGe BiCMOS processes and III-V compound semiconductors excerpted from ITRS 2011 [7]. The speed of fundamental CMOS transistors is expected to grow steadily in the future. In addition, the merits of CMOS integration are high compatibility with system design using digital circuits, the possibility of mass production, to reduce the cost and device miniaturization. To achieve f_T value of over 600 GHz predicted for the future, we should attempt to design CMOS integration for various high-speed applications.

It is also important to choose an appropriate CMOS process. In general, a CMOS process with ten times the maximum operation frequency (f_{MAX}) at the operating speed of the target application is selected. In this research, there are two target applications. One operates in a 10-GHz band, from 10 GHz to 13 GHz. Target operating frequency of the other applications are 100 GHz or more. Figure 1.7 shows a plot of f_{MAX} for various CMOS processes and selected processes relevant to the two applications. A CMOS 130-nm process is chosen for 10-GHz band applications because f_{MAX} is almost ten times larger than operating frequency. For applications with frequency of exceeding 100-GHz, there are not CMOS processes with f_{MAX} of 1000-GHz, therefore CMOS 65-nm process is selected in this research. In either case, various CMOS performances must be optimized in the building blocks.

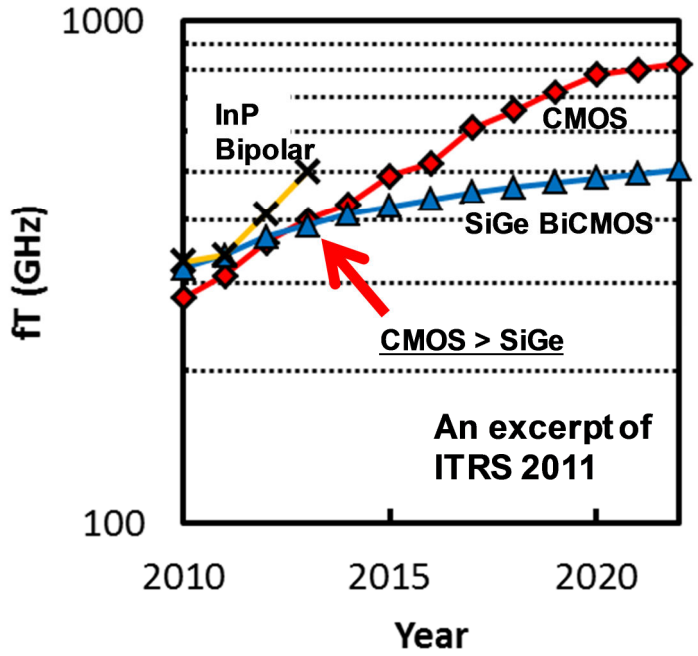


Figure 1.6: Comparison of unity current gain frequency of CMOS, SiGe BiCMOS processes and III-V compound semiconductors excerpted from ITRS 2011.

To implement a CMOS down-converter IC operated in 10 GHz band, various circuit structures must be considered. Figure 1.8 shows a block diagram of the target CMOS down-conversion IC. In this research, amplifiers, a mixing block and an on-chip PLL synthesizer (blue dashed line in Figure 1.7) are focused. In general, the required performances of a CMOS down-converter IC are similar to those of common receivers and include lower power consumption, a small size and a low cost while satisfying the specification. For the applications implemented in CMOS processes, each characteristic target is described as below.

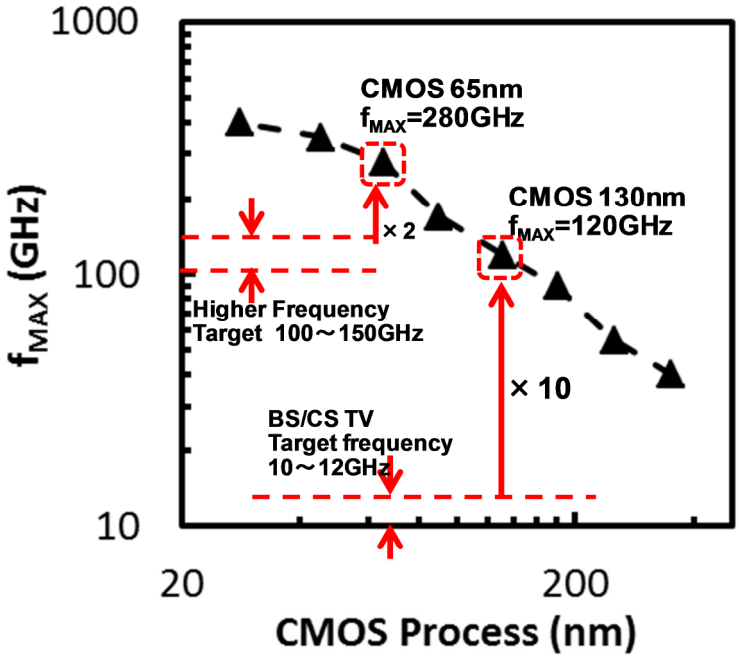


Figure 1.7: Plot of various CMOS process f_{MAX} and selected processes regarding two applications.

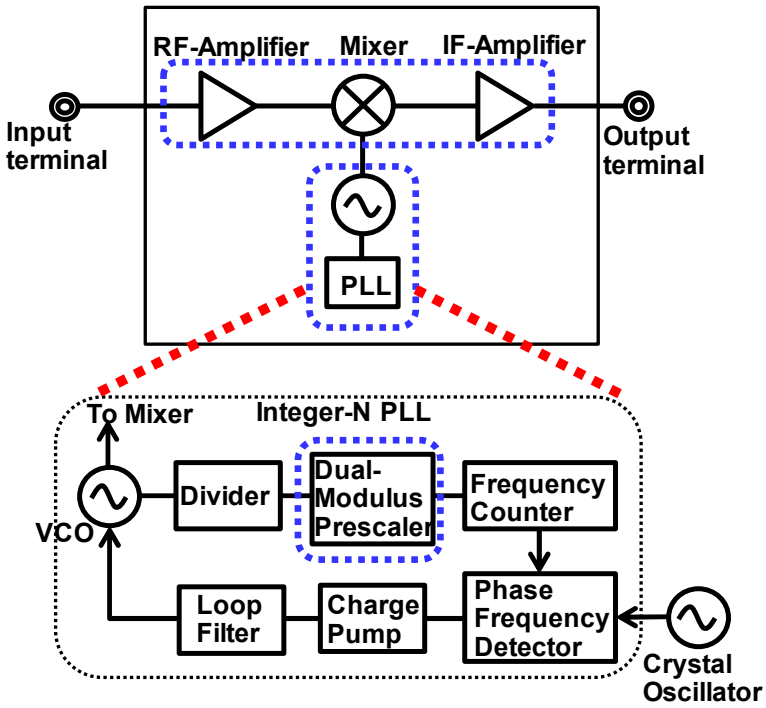


Figure 1.8: Block diagram of a target CMOS down-conversion IC.

1.4.1 10-GHz Band CMOS Down-Converter IC

In a commercial satellite application using a 10-GHz band, from 10 GHz to 13 GHz, broadcasting satellite with a parabolic antenna is constructed in open air from the equator to the arctic, meaning that temperature tolerance is required. In comparison with indoor applications, constant-quality operation over a wide range of environmental conditions is much more importance. When amplifiers and a mixer are designed, operation with a constant gain at different temperatures is important. Naturally, to achieve this target, a low noise, low power consumption, high-speed 10 GHz operation, high gain, high linearity and a variable gain amplifier (VGA) structure with constant the realization of a third-order intercept point (OIP3) are required.

As mentioned in section 1.3.1, a CMOS down-converter IC with a 10-GHz PLL synthesizer that generates various LO signals has been required by the manufacturers and customers. To achieve an on-chip PLL synthesizer in a CMOS down-converter IC for broadcasting satellites, a low power, small area and operation at a wide range of temperature are required. In particular, a dual-modulus prescaler in an integer-N-type PLL synthesizer is essential to improve the range of operation and reduce power consumption. A dual-modulus prescaler can cover the entire PLL operation range at a range of temperatures.

Regarding the target phase noise of an LO signal, Figure 1.8 shows the phase noise values in Astra's basic specifications [8] (dashed line) and the proposed target (solid line) in this research. Astra is the brand name of a number of geostationary communication satellites. The standards in satellite television broadcasting require the use of multi-carrier quadrature phase-shift keying (QPSK) and eight-phase shift keying (8-PSK) modulations. The Astra's phase noise specification was achieved using high-performance DROs, this specification is not suitable for the case of receiving radio waves. Lower phase noise values at low offset frequencies are required when RF signal with QPSK and 8-PSK are

received. Therefore, realistic target values for the phase noise are proposed, which are lower phase noise at low offset frequencies and slight relaxation at high offset frequencies. Simulation tests and field tests were repeatedly performed, and suitability of the proposed phase noise values for the normal operation for practical use were checked. Table 1.2 shows the target specifications of a CMOS down-converter IC for a 10-GHz band broadcasting satellite. Figure 1.9 shows the block diagram of a 10-GHz band broadcasting satellite module, which has two inputs of horizontal and vertical polarization wave antennas, and low noise amplifiers (LNAs) consisting of high-electron-mobility-transistors (HEMTs) to obtain a low noise figure (NF). The target 10-GHz band CMOS down-conversion IC is shown in the red dashed line. The specifications of the overall module in table 1.1 will be achieved using the target 10-GHz band CMOS down-converter IC and low noise HEMTs.

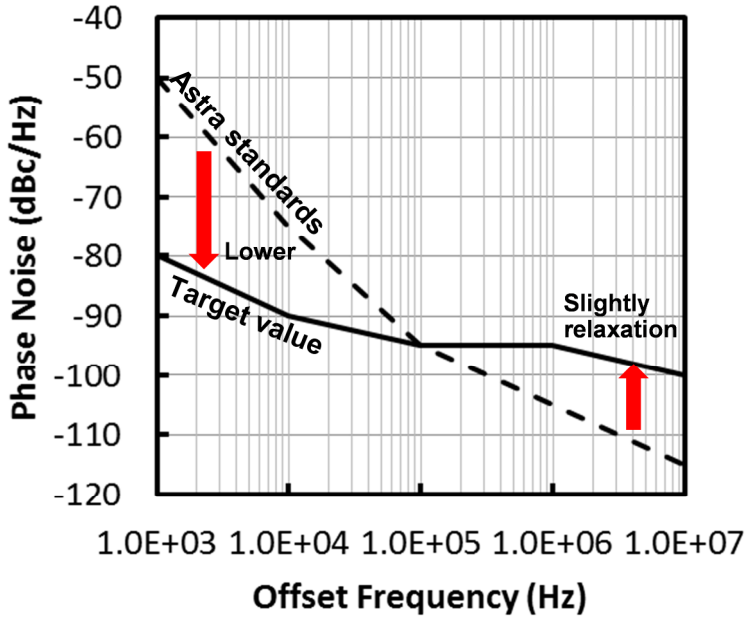


Figure 1.8: Basic specification of phase noise regulated by Astra.

Table 1.2: Target specifications of an LNB down-converter IC for broadcasting satellite

	Target specifications
Process	CMOS 130 nm
Architecture	Direct conversion
Operated Temperature	-30℃～85℃
Chip size	1.5mm×1.5mm or smaller
Supply voltage	3.3 V
IC current consumption	100 mA or less
LO frequency	9.75, 10.6, 10.75, 11.3 GHz
Phase noise	-95dBc/Hz @ 1MHz offset
PLL type	Integer-N-type-PLL
IC conversion gain	40, 36, 32, 28 dB
Gain variation under -30℃~90℃	3dB or less
IC NF	9dB
IC output P1dB	+0dBm

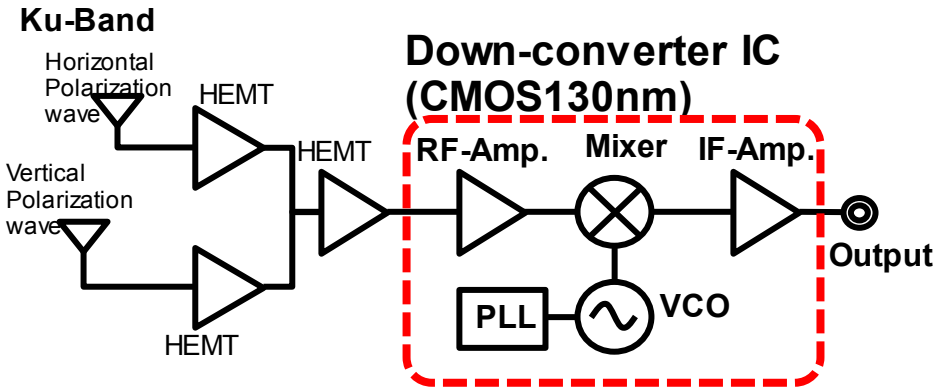


Figure 1.9: Block diagram of a 10-GHz band down-converter for broadcasting satellite

1.4.2 Previous 10-GHz Band Down-Converter ICs

Previous studies on LNB down-converter ICs mainly investigated a voltage-controlled oscillator (VCO), a PLL synthesizer, amplifiers and a mixing block using silicon bipolar technology [9] – [11], SiGe BiCMOS technology [12], CMOS technology [13] – [14] and a SiGe:C BiCMOS process [15]. For the case that the transistor speed is insufficient for a 10-GHz band, the double-conversion architecture was proposed in [9]. The double-conversion architecture has two LO

signals, which oscillated around the frequencies of half the established LO frequencies. There are also two mixing blocks, therefore, the power consumption tends to be increased and the total phase noise of the receiver is deteriorated by double-conversion.

Subsequently, the speed of the silicon bipolar, SiGe, SiGe:C BiCMOS and CMOS processes were improved to sufficient for a 10-GHz band application and the direct-conversion architectures were proposed. The power consumption tends to be decreased by implementing the circuits. In [13], a 10-GHz band mixing block and amplifiers implemented in a CMOS 180-nm process were proposed however their temperature tolerance was not described.

Table 1.3: Previous 10-GHz Band Down-Converter ICs

	[9]	[10]	[12]	[13]	[15]
Process	Silicon Bipolar	Silicon Bipolar	SiGe BiCMOS	180nm CMOS	SiGe:C BiCMOS
Architecture	Double conversion	Direct conversion	Direct conversion	Direct conversion	Direct conversion
Chipsize	4mm× 2.5mm	2mm× 2.3mm	1.7mm× 1.5mm	0.8mm× 1.8mm	1mm× 1.5mm
Supply voltage	3V	3.3V	3.3V	1.8V	5V
C current consumption	180mA	100mA	125mA	75mA	52mA
LO Frequency	4.875GHz 5.3GHz	9.75GHz 10.6GHz	9.75GHz 10.6GHz	w/o PLL	9.75GHz 10.6GHz
Phase noise	-102dBc/Hz @100kHz	-115dBc/Hz @1MHz	-106dBc/Hz @100kHz	w/o PLL	-95dBc/Hz @100kHz
IC conversion gain	33.6dB	34.5dB	33dB	50dB	43dB
IC NF	5.9dB	7.5dB	6dB	4.2dB	6.5dB
IC output P1dB	+5.5dBm	+5dBm	N/A	+9dBm	+7dBm
Published year	2004	2004	2007	2007	2011

1.4.3 Applications with Operation above 100 GHz

Research satellite applications such as for radio astronomy are

operated at a low temperature to increase the sensitivity and receive small signals from cosmic radio waves. A simple CMOS down-converter IC may be not applicable to a radio astronomy. However, it is important to implement a high-performance integrated PLL synthesizer for operation above 100 GHz because it is capable of using ultrahigh-speed transceivers used in radio astronomy, sensors, medical applications and others. Naturally, these applications are used in environments with various temperatures, and therefore the integrated CMOS PLL synthesizer must be operate in a wide frequency range.

The integer-N-type PLL as shown in Figure 1.10 is a common frequency synthesizer. It has a VCO, dividers, a crystal oscillator to provide a reference frequency, a phase frequency detector (PFD), a charge pump (CP) and a loop filter (LF). In this research, VCO and dividers are focused as high frequency circuits in a fundamental straight looped PLL synthesizer with an operation frequency exceeding 100-GHz. In particular, it is important for dividers to cover the entire VCO frequency range. Therefore, they must be designed to have a wider frequency range than the VCO oscillation range. Wide-margin and wide-range operation enable tolerance under temperature variation. Table 1.4 shows the target operation specifications of the VCO and dividers implemented in a CMOS 65-nm process.

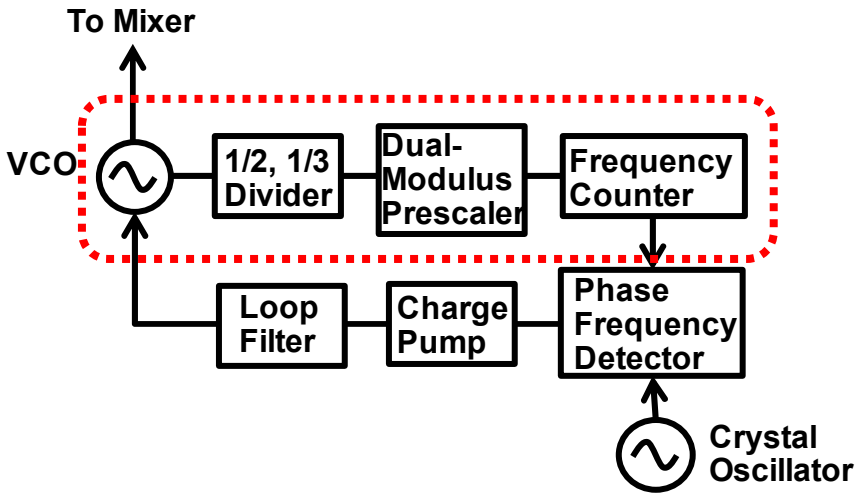


Figure 1.10: Block diagram of an integer-N-type PLL synthesizer.

Table 1.4: Target specifications of the VCO and dividers

	Target specifications
Process	CMOS 65 nm
Supply voltage	1.2 V or less
Operation temperature	Room
IC current consumption	100 mA or less
VCO frequency	100 GHz or more
Division ratio of dividers	2250 (To evaluate samples)

1.4.4 Previous Studies on Integrated High-Frequency Applications

Sub-millimeter and terahertz systems have been extensively studied in various research institutes. A CMOS PLL synthesizer is a key component providing a compact and low-cost signal source in sub-millimeter and terahertz systems. To design CMOS high-speed PLLs, not only a VCO but also dividers, a modulus prescaler and a frequency counter with large division ratios are important circuits. However, it is difficult for dividers to cover high frequency VCO operation. Therefore, CMOS high-speed PLL synthesizers with an operation frequency exceeding 100 GHz including a mixer and off-chip block [16] and an injection-locked frequency tripler (ILFT) [17] were proposed.

In [16], a harmonic mixer was used between the VCO and the divider. An LO signal was supplied by an off-chip multiplier. Therefore, this PLL synthesizer was not a “complete” on-chip circuit. The large size is also issue when using an off-chip device.

In [17], an ILFT was used. A 44 GHz PLL synthesizer was realized and a 44-GHz signal was used with the ILFT as an injected signal. The ILFT output frequency was 132 GHz, three times that of the injected signal. However, the large amount of spurious noise is a concern in an ILFT. Another concern is that 44 GHz interference signals are received by wideband receivers such as those used in radio astronomy.

Table 1.5: Previous high-speed CMOS integrated PLL

	[16]	[17]
Process	CMOS 65nm	CMOS 65nm
LO frequency	156.4 – 159.2 GHz	130 – 133 GHz
Power consumption	24 mW	92 mW
Architecture	Integer-N-type PLL with mixer and off-chip multiplier	Integer-N-type PLL with injection locked frequency tripler
Operated frequency of dividers	1 - 2 GHz	44 GHz
Published year	2012	2012

1.5 Thesis organization

From the following chapters, high frequency CMOS circuits are discussed to realize satellite applications with the operations of 10 GHz and 100 GHz. Broadcasting satellite down-converters operating 10 GHz band require higher reliability under variations in temperature. In addition, high frequency applications such as radio astronomy that operates at frequencies of over 100 GHz require high-speed and to cover the entire range and margin operation of the front circuit.

Chapter 2 discusses the techniques used in the integer-N-type PLL synthesizer for a CMOS down-converter IC with a range of 10 GHz and high frequency VCO and dividers operating at frequencies exceeding 100 GHz for a radio astronomy. A 10-GHz-band CMOS VCO has a trade-off between low and high VCO gain to realize low phase noise and a wide oscillation range from 9.75 GHz to 11.3 GHz. In addition, a wide range of operation is required to ensure the temperature tolerance necessary for open air use. To solve the above the issue, a wide range VCO with the switching varactors was discussed and study results of a 10-GHz band CMOS PLL synthesizer for a broadcasting satellite was described.

In chapter 2, a VCO and dividers for a 134-GHz PLL synthesizer are also discussed. The dividers have injection locked frequency

dividers (ILFDs), which are used in the tuning of the back-gate voltage to increase the operation range of divide-by-two. The developed VCO has a fundamental oscillation frequency range of 131.8 GHz to 134.3 GHz which is controlled by the back-gate voltage. The dividers can cover the entire VCO oscillation range. When the phase frequency detector, charge pump and loop filter are operated in a 10-GHz band, it will be possible to operate the 134-GHz on-chip PLL synthesizer.

Chapter 3 discusses full-differential dual-modulus prescalers in an integer-N-type PLL. Dual-modulus prescalers with a wide locking range, high-frequency operation and a low power based on an ILFD were proposed. They were fabricated in CMOS 130-nm and CMOS 65-nm processes. In this research, the first prescaler fabricated by the CMOS 130-nm process was successfully operated in a range of 4 GHz to 6 GHz indicating its temperature tolerance. The other prescaler fabricated by the CMOS 65-nm process was successfully operated in a range of 22 GHz to 23 GHz, and/or more a wider frequency range. The range of operation and the normalized energy consumption are compared with those of previous prescalers, which showed that good performances were achieved. In addition, the tolerances of phase difference deviation and phase noise degradation are also discussed.

Chapter 4 focuses on the amplifiers and mixer for a 10-GHz band CMOS down-converter IC. To obtain the target frequency range of the 10-GHz band, a low-noise, low current and high-gain RF amplifier and the mixer architecture are described. Satellite applications are constructed in the open air and a constant conversion gain despite variations in the temperature is required. In this research, a temperature-compensated variable-gain amplifier (TC-VGA) is proposed. To maintain a linear output, a constant output 3rd ordered intercept point (OIP3) VGA is also proposed. The amplifiers and mixer are discussed to realize these target specifications.

Chapter 5 gives a conclusion to this research, in which I outline my future works, which include the integration of high-frequency applications. The proposed CMOS down-converter IC for a

broadcasting satellite has the potential to be mass-produced, and contributes to the sales performance. For a sub-millimeter operation with a wide frequency range, CMOS integration guidelines could be obtained.

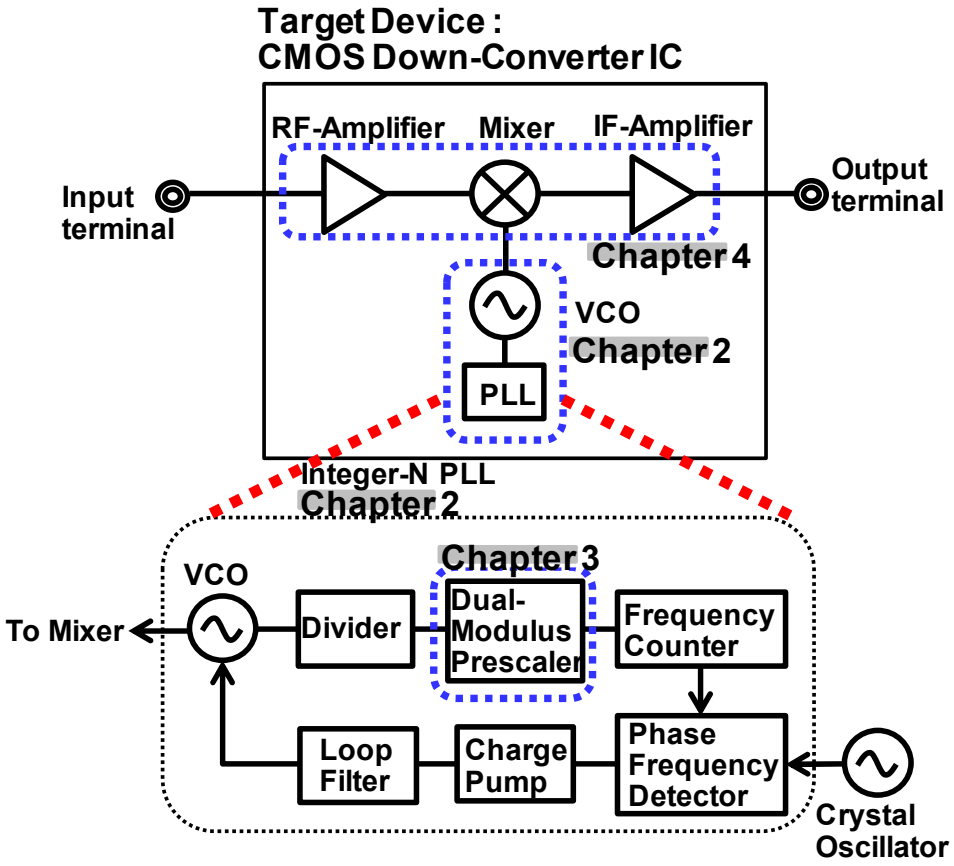


Figure 1.11: Thesis organization: Chapter 2 discusses the techniques used in the integer-N-type PLL synthesizer with a range of 10 GHz and exceeding 100 GHz. Chapter 3 discusses full-differential dual-modulus prescalers. Chapter 4 discusses the amplifiers and mixer in a 10-GHz-band down-converter IC for a broadcasting satellite. Chapter 5 gives a conclusion to this research.

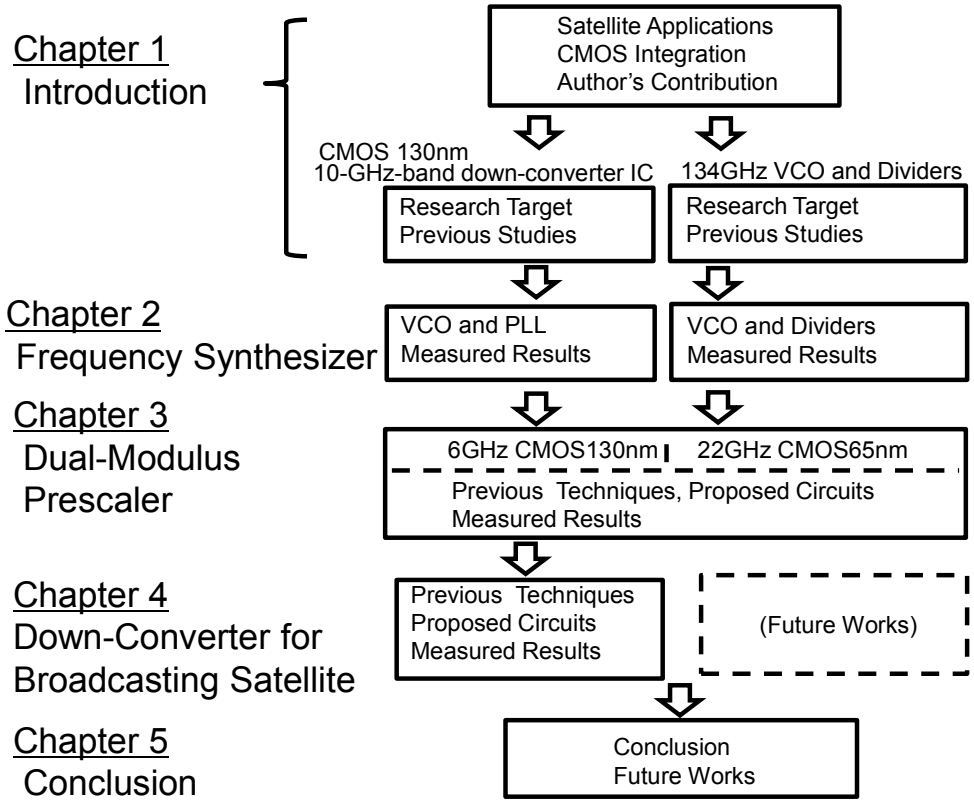


Figure 1.12: Flow chart of my thesis organization.

References of Chapter 1

[1] http://www.tele.soumu.go.jp/j/adm/freq, “The website of the radio frequency allocation by Ministry of Internal Affairs and Communications (MIC)”

[2] http://www.miz.nao.ac.jp/content/facility/vera-iriki-station, “The website of the National Astronomy Observatory of Japan”

[3] Lisa Wray, “IF/LO Systems for Single Dish Radio Astronomy Centimeter Wave Receivers”, NRAO/NAIC Single Dish Summer School, 2003.

[4] Goldsmith, P.F., Dalgarno, A., Erickson, N.R., Fazio, G.G., Harwit, M., Hollenbach, D.J., Koch, D.G., Melnick, G.J., Neufeld, D.A., Schieder, R., Snell, R.L., Stauffer, J., Thaddeus, P., Winnewisser, G.F, "The Submillimeter Wave Astronomy Satellite",in Proc. IEEE International Microwave Symposium (IMS), June 1991, pp.395 - 398.

[5] Qi-Jun Yao, Xue-Song Cao, Xu-Guo Zhang, Jing Li , Sheng-Cai Shi and Ji Yang, "A Compact 500GHz SIS Receiver System for POST", in Proc. Asia Pacific Microwave Conference (APMC), Oct. 2009, pp, 551 - 554.

[6] G.Engargiola, J. Zmuidzinas, K.Y. Lo, "A 492GHz quasi-optical SIS receiver for sub-millimeter astronomy," Rev. Sci. Instrum. 65(6), June 1994, pp.1833 -1838

[7] http://www.itrs.net, “International Technology Roadmap for Semiconductors”

[8] http://www.onastra.com, "The ASTRA website of satellite television"

[9] Tino Copani, Santo A. Smerzi, Giovanni Girlando, Giuseppe Palmisano, "A 12-GHz Silicon Bipolar Dual-Conversion Receiver for Digital Satellite Applications", IEEE J. of Solid-State Circuits, vol.40, No.6, June 2005, pp 1278-1287.

[10] Giovanni Girlando, Tino Copani, Santo A. Smerzi and Giuseppe Palmisano," A Ku-Band Monolithic Tuner-LNB for Satellite Applications", in Proc. IEEE Custom Integrated Circuits Conf. (CICC), Sept. 2004, pp. 613-616.

[11] Tino Copani, Santo A. Smerzi, Giovanni Girlando, Giuseppe Ferla, Giuseppe Palmisano, "A Single-Chip Receiver for Multi-User Low-Noise Block Down-Converters", in Proc. IEEE International Solid-State Circuits Conf. (ISSCC), Feb. 2005, pp.438-608.

[12] A. Maxim, M. Gheorghe and D. Smith, "A Single-Conversion SiGe BiCMOS Satellite TV LNB Front-End Using an Image Reject Mixer and a Calibrated Full-Rate VCO", in Proc. IEEE Custom Integrated Circuits Conf.(CICC) Sept. 2007, pp. 97-100.

[13] Zhiming Deng, Jiashu Chen, Jason Tsai, Ali M. Niknejad, "A CMOS Ku-Band Single-Conversion Low-Noise Block Front-End for Satellite Receivers", in Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June 2009, pp.135-138.

[14] Wenjian Chen, Tino Copani, Hugh J. Barnaby and Sayfe Kiaei, "A 14-GHz CMOS Receiver with Local Oscillator and IF Bandpass Filter for Satellite Applications", in Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, June 2009, pp.123-126.

[15] Praamsma, L., Breunisse, R., van der Heijden, E., Meng, F., Bardy, S., Moreau, F., Wane, S. and Thomas, E., "A low power 9.75/10.6GHz down-converter IC in SiGe:C BiCMOS for Ku-band satellite LNBs",in Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Oct. 2011, pp.211-214.

[16] Wei-Zen Chen, Tai-You Lu, Yan-Ting Wang, Jhong-Ting Jian, Yi-Hung Yang, Guo-Wei Huang, Wen-De Liu, Chih-Hua Hsiao, Shu-Yu Lin and Jung Yen Liao, "A 160-GHz Receiver-Based Phase-Locked Loop in 65 nm CMOS Technology", in Proc. Symposium on VLSI Circuits, June 2012, pp.12-13.

[17] Adrian Tang, David Murphy, Gabriel Virbila, Frank Hsiao, Sai-Wang Tam, Hsing-Ting Yu, , Hsieh-Hung Hsieh, Chewn Pu Jou, Yanghyo Kim, Alden Wong, Alex Wong, Yi-Cheng Wu, Mau-Chung Frank Chang, "D-Band Frequency Synthesis Using a U-band PLL and Frequency Tripler in 65nm CMOS Technology", in Proc. IEEE International Microwave Symposium (IMS), June, 2012, pp.1-3.

Chapter 2. Frequency Synthesizer

2.1 Introduction

The phase-locked loops (PLLs) based frequency synthesizers are essential parts of the wireless or wired transceivers, receivers and other devices. The PLL synthesizers are roughly divided into two types, an integer-N-type and a fractional-N type. In this research, an integer-N-type PLL synthesizer is focused. A typical integer-N-type PLL synthesizer is a feedback circuit, which is controlled integral multiple frequency of reference frequency supplied crystal oscillator or others. A basic structure of an integer-N-type PLL synthesizer consists of some fundamental functional blocks namely, a voltage oscillator (VCO), dividers, a phase frequency detector (PFD), a crystal oscillator as a reference frequency, a charge pump (CP) and a loop filter (LF) with the circuit configuration shown in Figure 2.1. In this chapter, high frequency block of VCO and dividers of dashed line in Figure 2.1 are focused.

In typical CMOS receivers, low power consumption, small area, low cost and the achievement of target specifications are required. In addition for satellite applications, it is important to operate constantly under variations in temperature because they are built in open air all over the world. Therefore, a PLL synthesizer for satellite applications must be designed to operate with wide margin and wide frequency range. In this research, satellite applications

are implemented in low cost CMOS processes therefore various ideas are required.

In this chapter, two PLL synthesizers for a 10-GHz band broadcasting satellite and high frequency band exceeding 100-GHz range are described. In section 2.2, a 10-GHz band CMOS PLL synthesizer for broadcasting satellite is focused. A 10-GHz band CMOS VCO has a trade-off between low VCO gain due to low phase noise and high VCO gain due to wider oscillation range. To overcome the above the issues and realize for the mass-production, previous and proposed techniques and measurement results are described. In section 2.3, a high frequency CMOS VCO and dividers for a 134-GHz PLL synthesizer are focused. Dividers must cover the entire VCO oscillation range therefore wide range operation is required. Including high frequency VCO, previous and proposed techniques and measurement results are described. Section 2.4 concluded in chapter 2.

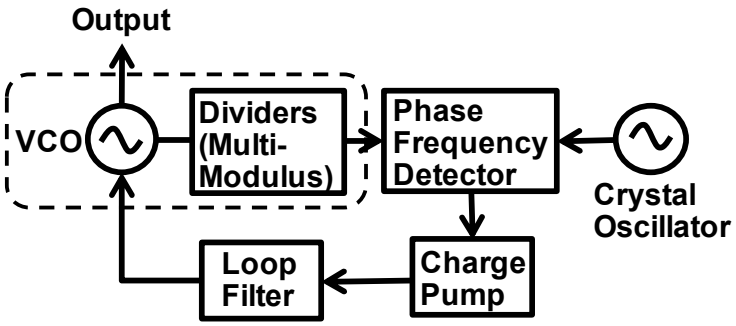


Figure 2.1: Block diagram of a typical integer-N type PLL.

2.2 10-GHz-Band PLL Synthesizer for Broadcasting Satellite

2.2.1 Introduction

A down-converter is used as the receiving device on the satellite dish antenna and it translates radio frequency (RF) signal of the 10-GHz band (10.7 GHz – 12.75 GHz) to an intermediate-frequency

(IF) signal of 1.5-GHz band (950 MHz – 2150 MHz). As mentioned in chapter 1, the local oscillator (LO) of a down-converter uses discrete open-loop dielectric resonator oscillators (DROs), which used to required manual alignment. Recently, to compensate for the temperature drift and the aging effect, fully integrated down-converter ICs [1] – [3] with PLL synthesizers have been implemented. However, they have high power consumption, high implementation costs owing to the SiGe process and do not achieve the target LO frequencies of 9.75 GHz, 10.6 GHz, 10.75 GHz and 11.3 GHz. The target oscillation range as below is 14.7 % however a wider oscillation range is required considering the temperature variation. Therefore, we attempt to achieve a target oscillation range of 20 % to include wider margin.

Table 2.1: Target specification of a 10-GHz band CMOS PLL synthesizer

Parameter	Target Value
Process	CMOS 130 nm
Layout size	1mm × 500um or less
LO frequency	9.75 GHz, 10.6GHz 10.75GHz, 11.3 GHz
Current consumption	50 mA or less
Phase Noise	-80 dBc/Hz @ 1kHz offset -90 dBc/Hz @ 10kHz offset -95 dBc/Hz @ 100kHz offset -95 dBc/Hz @ 1MHz offset -100 dBc/Hz @ 10MHz offset

The target specifications are shown in table 2.1. For a 10-GHz-band PLL synthesizer, low cost and low phase noise are also required. An on-chip inductor is a large passive device therefore 1-inductor VCO is used to control the layout size. However, this means that a high VCO gain is required over a wider oscillation range.

The achievement of target phase noise is also important for a 10-GHz-band down-converter IC. To realize lower phase noise, the VCO gain must be reduced. There is a trade-off between high and

low VCO gains. A useful and convenient structure must be used in a wide range and low phase noise VCO.

2.2.2 10-GHz Band Wide Range Voltage Controlled Oscillator

In general, VCOs can be classified into two types: a ring VCO and an LC-VCO. A ring VCO has the advantages of a small chip area, process scalability and a wide oscillation range however an LC-VCO has extremely high frequency operation, high spectral purity and good phase noise performance. Here, an LC-VCO is chosen for its high-frequency oscillation and low phase noise. Typical high-frequency LC-VCOs consist of cross-coupled NMOS transistors, load inductors and variable capacitors as shown in Figure 2.2.

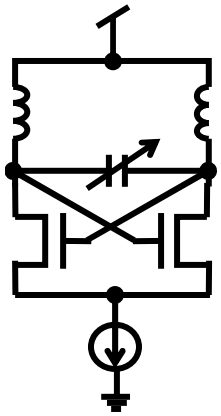


Figure 2.2: Schematic of conventional LC-VCO.

However, in the typical LC-VCO shown in Figure 2.2, the oscillation wave rotates the symmetry around center tap given supply voltage. Therefore, the current consumption is increased by the larger amplitude of oscillation wave. Furthermore, as shown in Figure 2.2, the VCO gain is not controlled. A high VCO gain for a wider range of oscillation and a low VCO gain for low phase noise are required in this case.

To resolve the issues associated with the smaller size, lower current consumption, wider range oscillation and lower phase noise, a complimentary cross-coupled LC-VCO is designed as shown in

Figure 2.3. The peak amplitude of oscillation wave does not exceed the supply voltage. Therefore, the current consumption is suppressed. The VCO consists of thin-gate transistors and its operational voltage is 1.4 V. The supply voltage of the LNB-IC is 3.3 V, therefore a low drop-out regulator (LDO) is implemented to reduce the supply voltage.

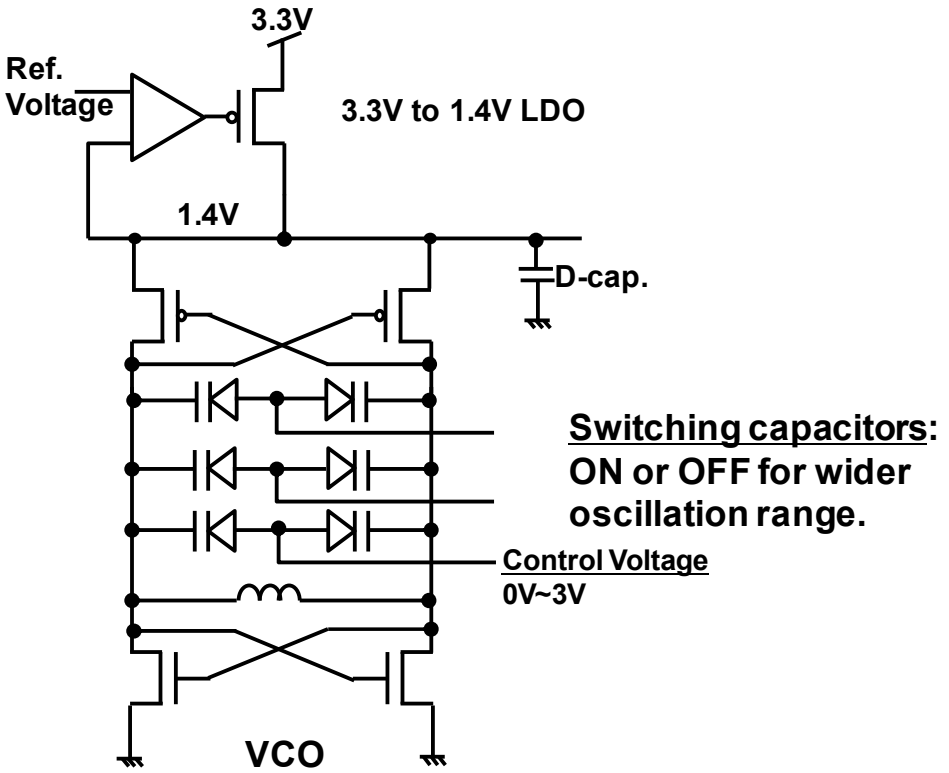


Figure 2.3: Schematics of the complementary LC-VCO and LDO.

The target oscillation frequencies are 9.75 GHz, 10.6GHz, 10.75 GHz and 11.3 GHz. To design the VCO using only a 1-inductor and attain a wide range of oscillation, two-switching capacitors and a varactor diode are implemented as frequency-controlled capacitors. When the VCO is oscillated at a frequency of 9.75 GHz, two switching capacitors are set to "ON" and the capacitance increases. When the VCO is oscillated at a frequency of 10.6 GHz and 10.75 GHz, one switching capacitors is set to "ON" and the other is set to "OFF" and the capacitance is decreased to less than that at an

oscillation frequency of 9.75 GHz. When the VCO is oscillated at a frequency of 11.3 GHz, two switching capacitors are set to "OFF" and the capacitance decreases. To compensate for the oscillation variation in the oscillation frequency due to the variation of temperature, a wider oscillation ratio must be covered. The target oscillation ratio is 20 % (9.45 GHz to 11.6 GHz). Figure 2.4 shows the simulation results for the oscillation range, which covers an oscillation ratio of 23 % (9.3 GHz to 11.8 GHz). As stated above, a 1-inductor LC-VCO with a high VCO gain for a wide range of oscillation frequencies and a low VCO gain for the achievement of low phase noise are proposed.

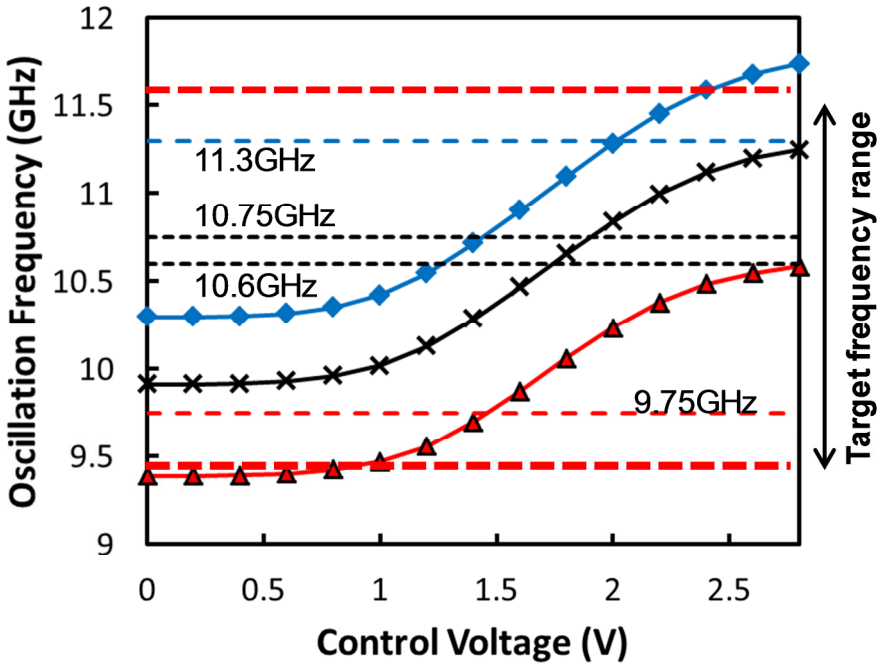


Figure 2.4: Simulated results of the oscillation frequency range as a function of the controlled voltage.

2.2.3 Measurement Results

A die photograph of the mass-production chip including a VCO and a PLL synthesizer is shown in Figure 2.5. A PLL synthesizer has a differential dual-modulus prescaler described in chapter 3. The mass-production chip consists of amplifiers, a mixing block, a

band-gap reference (BGR) and the other circuits implemented in CMOS 130-nm process described in chapter 4. The chip size is 1.1 mm × 1.1 mm including the pads. The layout size of a VCO and a PLL synthesizer is 0.5 mm × 0.3 mm. A current consumption of a VCO and a PLL synthesizer is 45 mA with an LDO, and a total current consumption of a CMOS down-converter IC is 73 mA at the 3.3-V supply voltage.

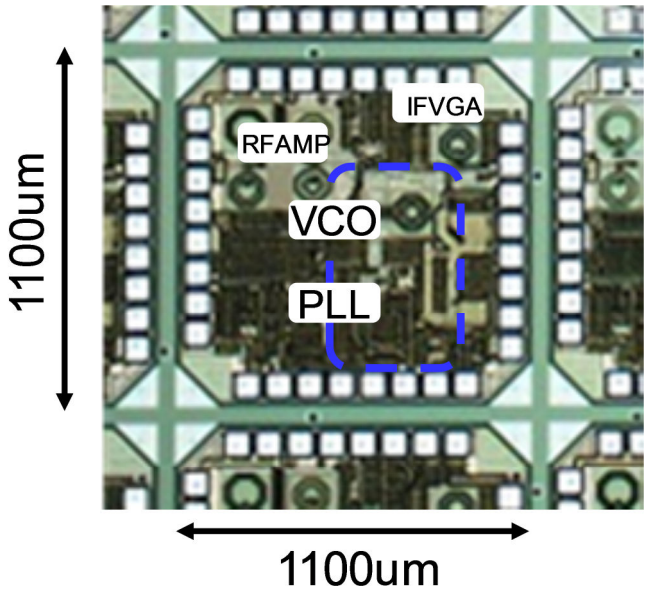


Figure 2.5: Die photograph of a 10-GHz band CMOS down-converter IC.

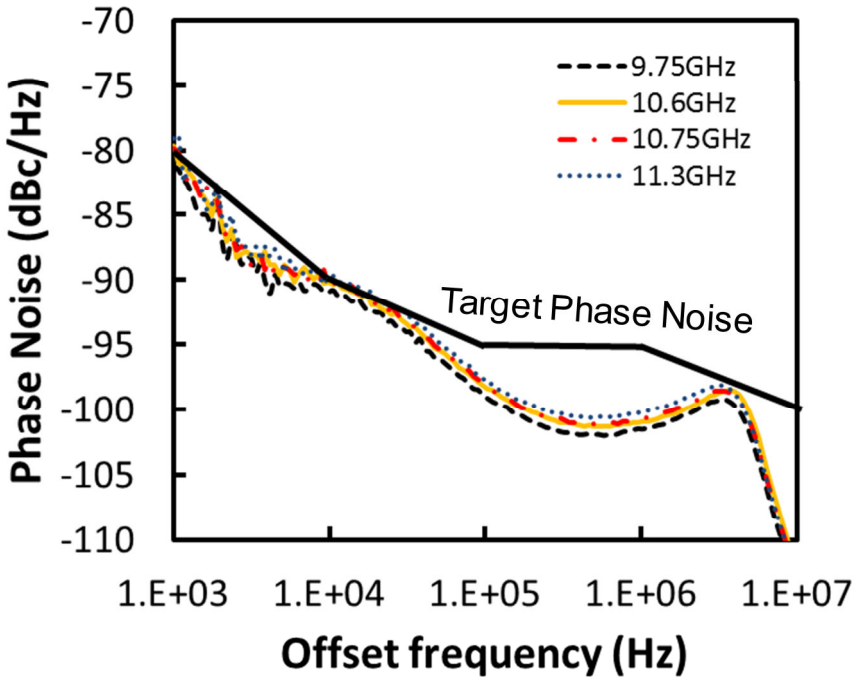


Figure 2.6: Plots of phase noise measurement results of LO frequencies of 9.75 GHz, 10.6 GHz, 10.75 GHz and 11.3 GHz, respectively.

Figure 2.6 shows the plots of phase noise measurement results of LO frequencies of 9.75 GHz, 10.6 GHz, 10.75 GHz and 11.3 GHz, respectively. Table 1.2 shows the target specifications of a 10-GHz band CMOS down-converter IC for broadcasting satellite as mentioned in section 1.4.1. The measured phase noise is achieved target phase noise values in each offset frequency.

Table 2.2: Comparison of the 10-GHz band PLL performance

	[1]	[2]	[3]	This work
Process	Silicon Bipolar	SiGe:C BiCMOS	Silicon Bipolar	CMOS 130 nm
Total Chip size	4 mm × 2.5 mm	1 mm × 1.5 mm	2 mm × 2.3 mm	1.1 mm × 1.1 mm
PLL Current Consumption	180 mA	52 mA	100 mA	45 mA
LO frequency	4.875 GHz, 5.3 GHz	9.75 GHz, 10.6 GHz	9.75 GHz, 10.6 GHz	9.75 GHz, 10.6 GHz, 10.75 GHz, 11.3 GHz
Phase noise	-102dBc/Hz @ 100 kHz	-95dBc/Hz @ 100 kHz	-115dBc/Hz @ 100 kHz	-98dBc/Hz @ 100 kHz
Published year	2005	2011	2004	--

2.2.4 Conclusion of a 10-GHz Band PLL Synthesizer

In this section, a fully integrated 10-GHz-band integer-N-type PLL synthesizer for a broadcasting satellite was presented. In particular, the circuit technique of a 1-inductor VCO was focused. It requires a wide range of operation including temperature tolerance, a low current consumption and the achievement of targets of phase noise and oscillation frequencies.

To overcome a trade-off between high VCO gain for a wide range of operation and low VCO gain for a low phase noise, a 1-inductor VCO has two-switching varactors and a tuning varactor. By setting to the switching varactors, the wide oscillation range of 9.3 GHz to 11.8 GHz could be achieved. This indicates the high VCO gain. In addition, the low phase noise of -98dBc/Hz at 100-kHz offset frequency could be achieved. This indicates the low VCO gain,

therefore, a proposed VCO indicates trade-off issues of a 1-inductor VCO was overcome.

2.3 VCO and Dividers for a 134-GHz PLL Synthesizer

2.3.1 Introduction

Recently, sub-millimeter and terahertz systems have been extensively studied for wireless or wireline communications, radio astronomy, security, sensor systems and medical applications. With the advances in CMOS, it has become realistic to consider high-speed oscillator circuits exceeding 100-GHz operations. Higher oscillation frequencies are limited by the unity maximum available gain frequency (f_{MAX}) of a transistor. To obtain even higher frequencies, push-push oscillator architectures [4] – [5] and fundamental oscillators over 300 GHz [6] have been proposed.

Local oscillator is also the essential parts of ultrahigh-speed receivers not only radio astronomy but also other wireless and wireline communications, security, sensor systems and medical applications, an ultrahigh-speed CMOS multi-phase or quadrature oscillator controlled PLL synthesizer must be studied.

The common frequency synthesizer is an integer-N-type PLL as shown in Figure 2.7, which has a VCO, dividers, crystal oscillator as a reference frequency, PFD, CP and LF. In particular, the dividers must cover entire VCO oscillation range and have large division ratios to compare a reference frequency. Therefore, dividers must operate high frequency and wide frequency range including temperature variation. In this research, a VCO and dividers of high frequency circuits in a PLL synthesizer are focused (dashed line in Figure 2.7). Figure 2.8 shows the block diagram of dividers. Dividers have the divide-by-2, divide-by-3 and dual-modulus prescaler and frequency counter. The target structure is the straight loop PLL synthesizer. Table 2.3 shows the target PLL performance.

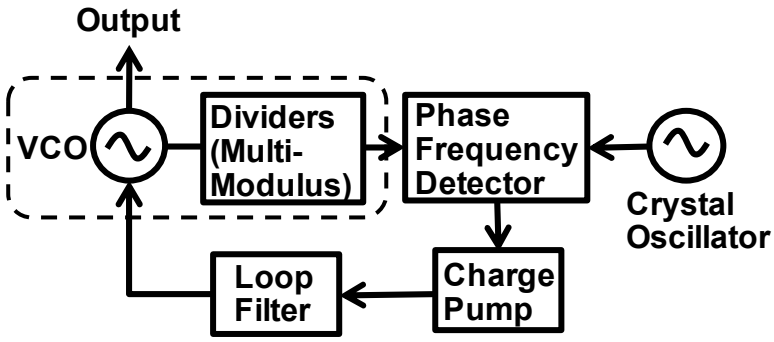


Figure 2.7: Block diagram of the common frequency synthesizer as an integer-N type PLL.

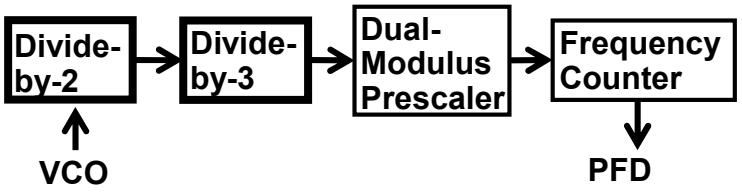


Figure 2.8: Block diagram of dividers for a PLL over 100-GHz operation

Table 2.3: Target performance of a high frequency PLL synthesizer

	Target specifications
Process	CMOS 65 nm
Supply Voltage	1.2 V
Power Consumption	As small as possible
VCO frequnecy	125GHz or higher
Phase noise	As small as possible
Division ratio of dividers	2250 (To evaluate samples)

2.3.2 VCO Circuit Design

To realize the oscillators that operate at frequencies of over 100 GHz, an LC-VCO architecture is described. In typical fundamental

LC-VCO architecture, MOS diodes are used for frequency adjustment. However, the transistor gate-capacitances and other parasitic capacitances are limiting factors preventing higher-frequency oscillation. Generally, MOS diodes with large gate-capacitances limit high oscillating at frequency of over 100 GHz. Therefore, the tuning capacitance architecture with a variable back-gate voltage (V_{BG}) as the VCO control voltage (V_{CNT}) [7] is studied.

Figure 2.9 shows a schematic of the VCO core and buffer circuits. The load capacitance in the VCO is set by a variable V_{BG} and the oscillation frequency is adjusted. Figure 2.10 shows a plot of the results of a gate capacitance simulation for a variable V_{BG} with drain-source and gate-source voltages of 1.2 V using an NMOS transistor with W = 14 μm and L = 65 nm. The gate capacitance is changed from 15.1 fF to 15.5 fF by the variation of V_{BG}. The parasitic capacitances including lines and other capacitances in a 134-GHz VCO are approximately 30 fF, and the total parasitic capacitance varies from 45.1 fF to 45.5 fF. The capacitance variation per center capacitance is approximately 1 %, therefore, therefore, the oscillation frequency variation of 0.5 % is expected by $1/2\pi\sqrt{LC}$, giving an equivalent capacitance variation of nearly 1 %. an oscillation frequency variation of 1% is expected for a VCO, giving an equivalent capacitance variation of nearly 1 %.

Figure 2.11 shows the simulation results of the VCO oscillation frequency at a 1.2-V supply voltage. The simulation results show that the VCO covers the range from 132 GHz to 134 GHz, which is approximately 1 - 2 % of the center frequency. The simulated power consumption of the VCO alone is 12 mW.

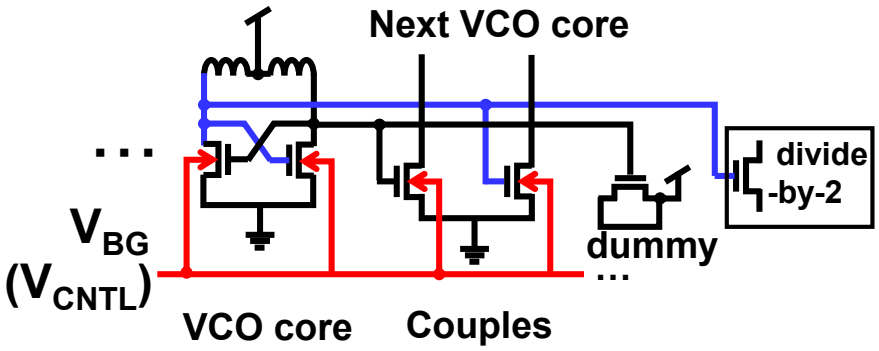


Figure 2.9: Schematic of the VCO core and buffer.

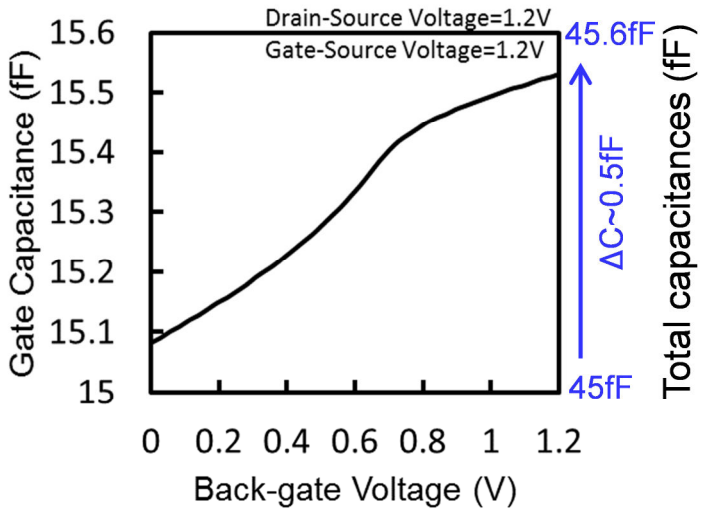


Figure 2.10: Plot of the results of a gate capacitance simulation for a variable V_{BG} with drain-source and gate-source voltages of 1.2 V using an NMOS transistor with W = 14 μm and L = 65 nm

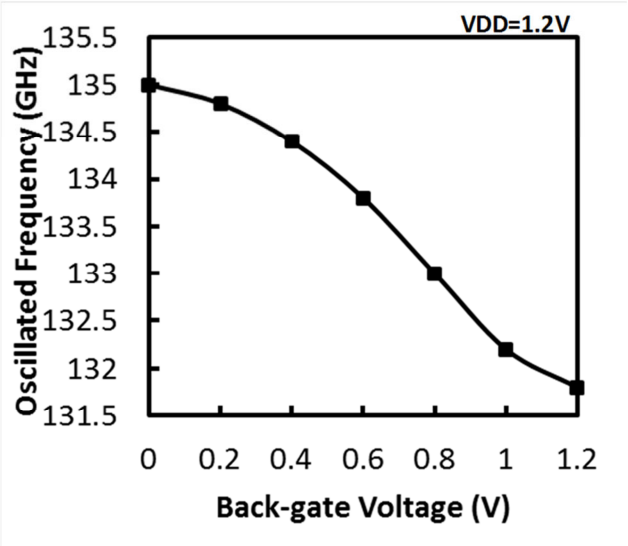
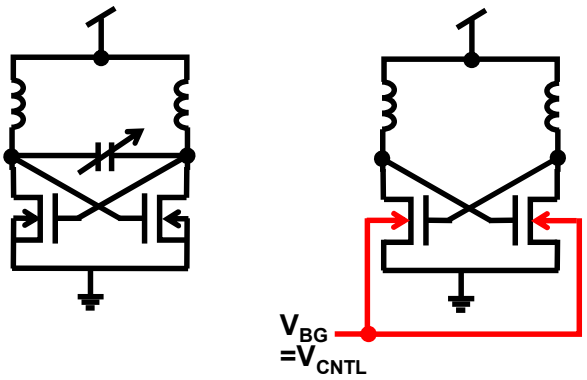


Figure 2.11: Simulation results of the VCO oscillation frequency at a 1.2-V supply voltage

2.3.3 Circuit Design of Divide-by-2 based on LC-VCO

For the correct PLL function, the divide-by-2 divider should cover the entire VCO output frequency range, which is simulated as from 132 GHz to 135 GHz in the previous section.

In general, there are three types of frequency dividers (FDs), static FDs, dynamic FDs and injection locked frequency dividers (ILFDs). An example of the static FDs is a D-flip-flop (DFF) with the Q terminals connected back to the D terminals in reversed polarity. The dynamic FDs use a feedback loop where logic states are stored on a parasitic capacitance for just a short while. Whereas, the ILFDs use an oscillator whose free-running oscillation frequency agrees with the divider output target. When the input frequency around the integer multiples of the resonant frequency of the oscillator is injected, the oscillator is injection-locked to the input signal and divide-by-integer can be achieved through the locking phenomenon. In the three types of FDs, the ILFD is suitable for high frequency operation. In this research, the ILFD based on an LC-VCO as a first divide-by-2 is described.



(a) (b)

Figure 2.12: Schematic of the traditional LC-VCO (a) and LC-VCO controlled the back-gate voltage (b).

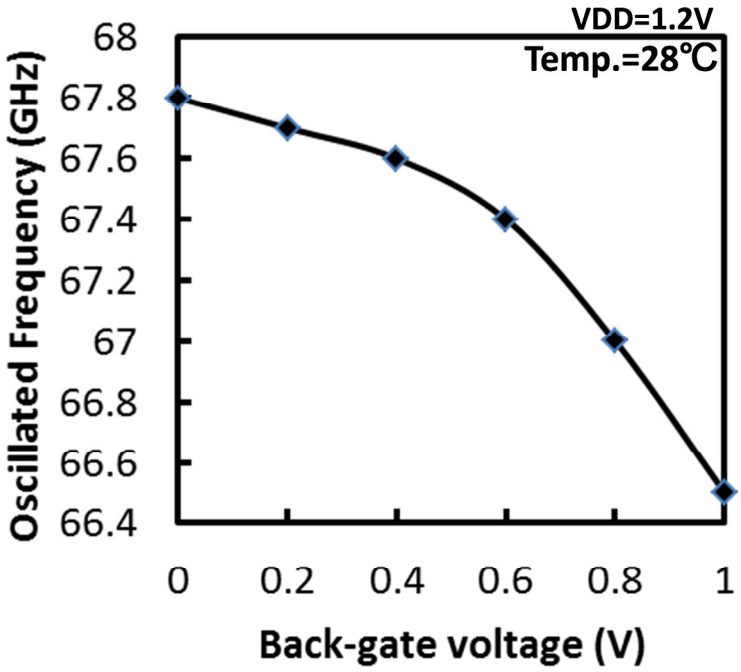


Figure 2.13: Simulation results of the divide-by-2 free-running oscillation frequency.

Figure 2.12 (a) shows a traditional LC oscillator. Its free-running oscillation frequency is equal to $1/2\pi\sqrt{LC}$. In previous section, Figure 2.12 (b) shows a schematic of a differential VCO which change oscillation frequency by changing the back-gate voltage.

Figure 2.13 shows simulation results of the free-running oscillation frequency, which is around a half frequency of 132 GHz to 135 GHz by adjusting inductor size. The target input frequency of divide-by-2 is 132-GHz to 135-GHz operation therefore the free-running oscillation frequency must be adjust to approximately 67.5 - 66 GHz.

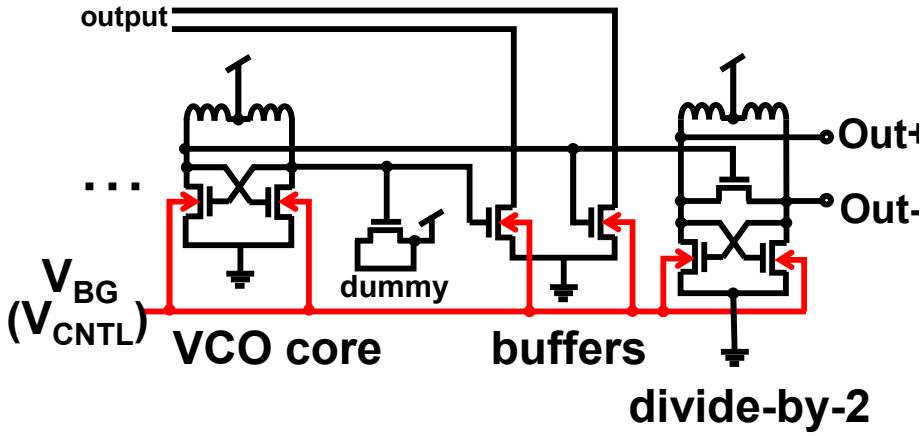


Figure 2.14: Schematic of a 134-GHz fundamental VCO and a divide-by-2 ILFD based on an LC-VCO

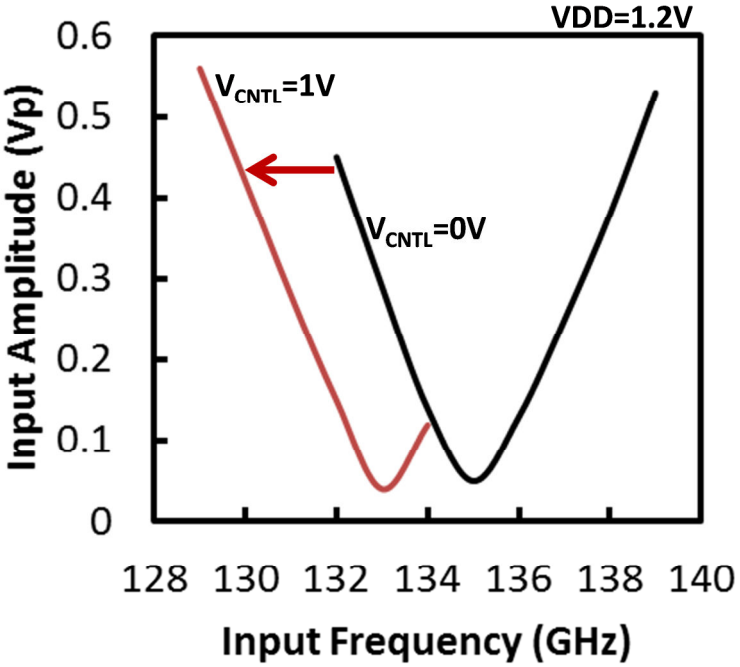


Figure 2.15: Simulation results of the ILFD sensitivities

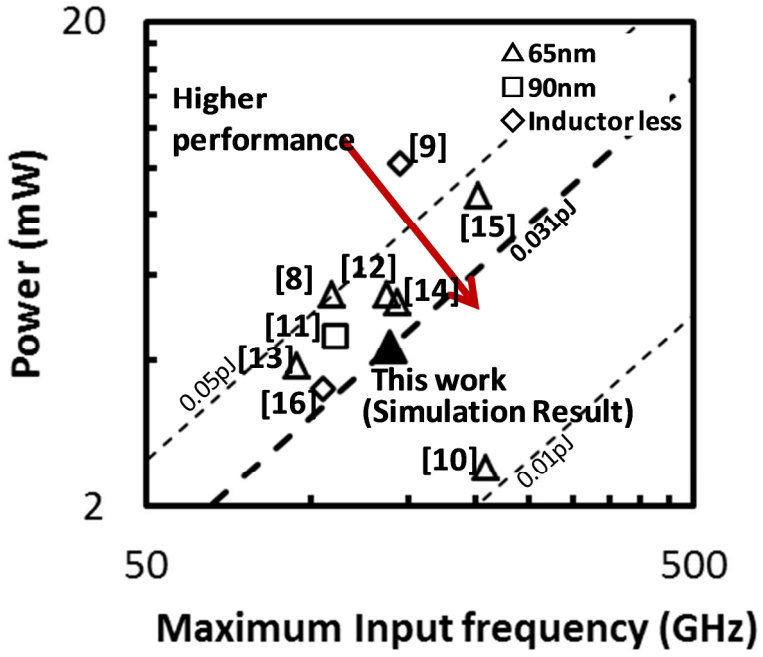


Figure 2.16: Comparison of the energy efficiency

Figure 2.14 shows a schematic of a 134-GHz fundamental VCO and a divide-by-2 ILFD based on an LC-VCO. The ILFD has an NMOS switching-gate transistor connected between cross-coupled pairs. One of the VCO outputs directly connects with the gate terminal of a switching-gate transistor in the ILFD and the other terminal connects with the dummy NMOS transistors with the same gate-capacitance value. The back-gate voltages of the cross-coupled pairs in ILFD take the same control voltage as the VCO. Therefore, proposed ILFD locking range can expand by approximately 2-GHz by using the VCO controlled voltage comparing with a fixed 0-V controlled voltage, as shown in Figure 2.15. The simulation result shows that the divider covers the entire oscillation frequency range of the VCO and contributes the wide operation range.

Figure 2.16 shows the comparison of the energy efficiency of this work with other reported ILFDs. The target energy efficiency (mW/GHz = pJ, power consumption per maximum input frequency)

of the proposed divide-by-2 ILFD compares favorably with the performances of other reported ILFDs.

2.3.4 Measurement Results

The die area of the experimental circuit block including the 134-GHz VCO and dividers is 180 μm × 100 μm implemented in 1P9M 65-nm RF-CMOS process with MIM capacitors and deep N-well structures. A photograph of the die is shown in Figure 2.17. The 134-GHz VCOs have four VCO cores for the multiplier. To measure the output signal of VCOs, a simple transistor buffer is used. Figure 2.18 shows the oscillation spectrum with a frequency of 134.4-GHz and current consumption of 8.5 mA using a one VCO core and 34 mA using four VCO cores at a 0-V control voltage and a 1.2-V supply voltage. The measured amplitude is -59.1 dBm which is used by a buffer output, therefore actual VCO amplitude is expected around 0.9-V peak to peak.

Figure 2.19 shows the plots of the measured phase noise of various control voltages at a 1.2-V supply voltage. The achieved phase noise values are -80 dBc/Hz at 1-MHz offset frequency with the back-gate voltages from 0 V to 0.9 V. The measured phase noises in higher frequency range increase as the control voltage increases to 1.2 V. The result indicates that as the back-gate current increases, thermal noise becomes more dominant than the flicker noise.

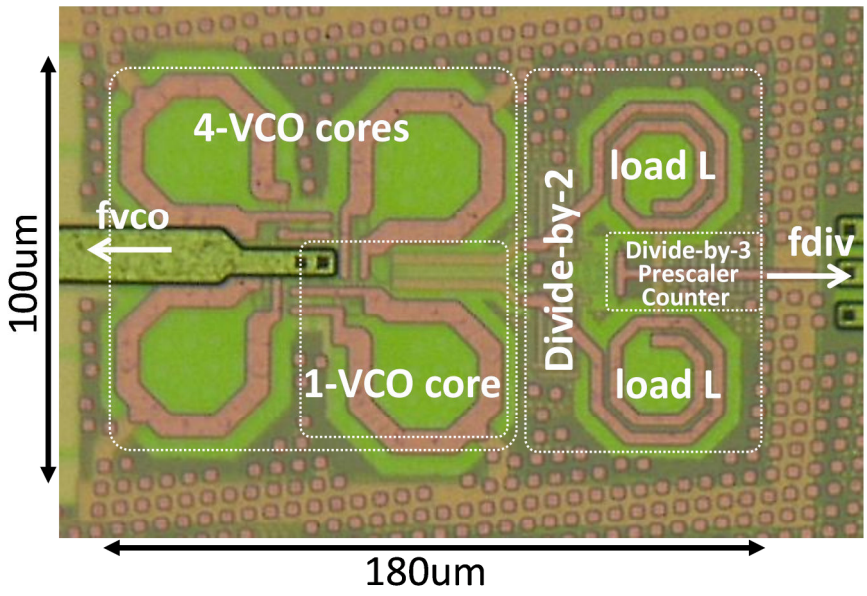


Figure 2.17: IC die photograph of the 134-GHz VCO and dividers.

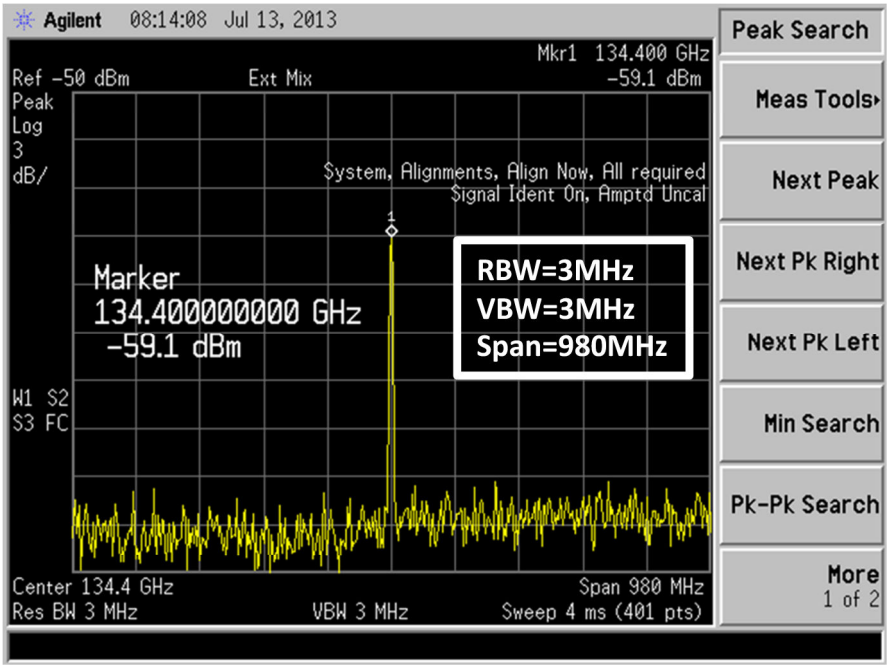


Figure 2.18: Screen shot of the directly spectrum from VCO buffer at 0-V controlled voltage and 1.2-V supply voltage.

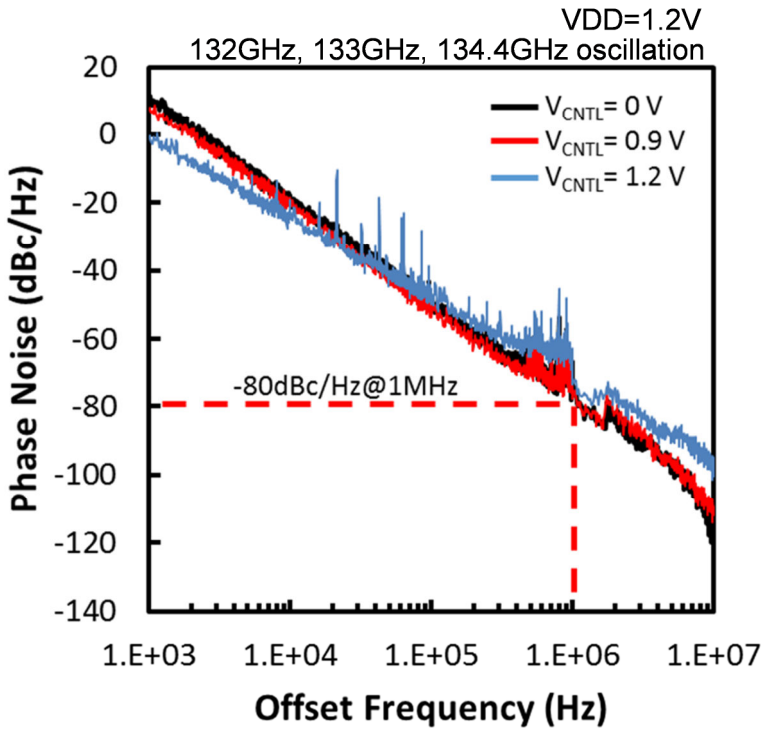


Figure 2.19: Plots of the measured phase noise of various control voltages at a 1.2-V supply voltage.

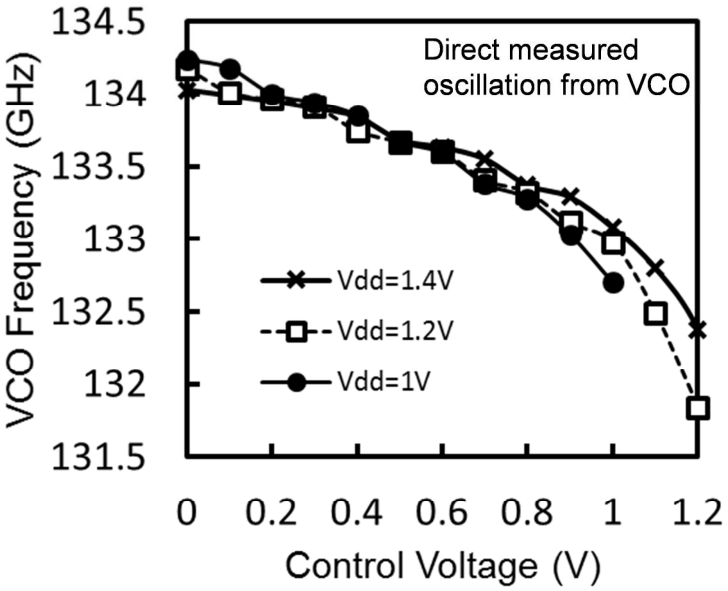


Figure 2.20: Plots of direct measured oscillation frequencies as a function of the control voltage at the various supply voltages.

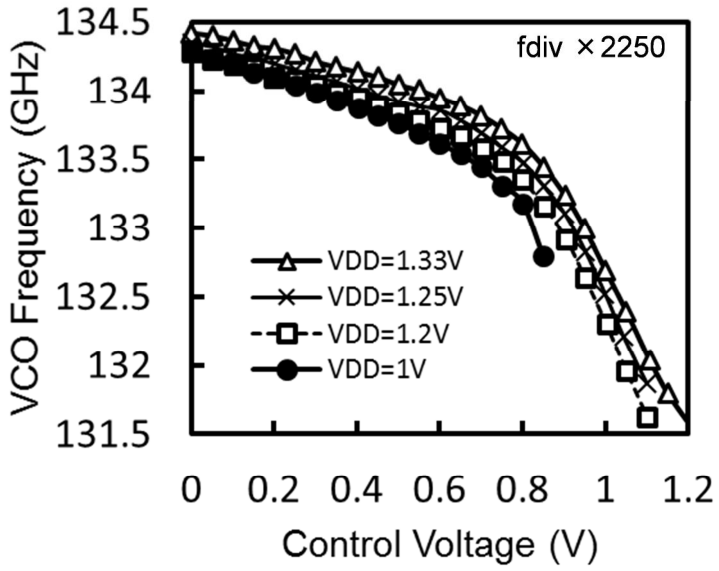


Figure 2.21: Plots of measured oscillation frequencies calculated from output frequency of the dividers as a function of the control voltage at the various supply voltages.

Figure 2.20 shows the plots of directly measured oscillation frequencies of the VCOs as functions of control voltage at supply voltages of 1 V, 1.2 V and 1.4 V. The oscillation ranges of VCOs achieved 132.6 GHz to 134.4 GHz at a 1-V supply voltage and 131.8 GHz to 134.3 GHz at a 1.2-V supply voltage.

The oscillation frequency of the VCOs can be calculated from the output frequency of the dividers. Figure 2.21 shows plots of the oscillation frequencies of the VCOs calculated from the output frequency of the dividers as a function of control voltage at supply voltages of the 1 V, 1.2 V, 1.25 V and 1.33 V. Approximately, the same frequencies in Figure 2.20 and Figure 2.21 can be observed. Therefore, the dividers can operate in the entire oscillation range of the VCOs. In this operation, the total current consumption of the one VCO core and dividers is 37 mA at the 0-V control voltage and a 1-V supply voltage.

These results show that the divider's output signal at 1.34-V supply voltages or higher since the dividers are non-functional. However, the oscillation frequency of the VCOs gradually increases

with the supply voltage. To check the accurate oscillation frequencies of VCOs, we can calculate them from the divider's output frequencies. By these results, a good prospect is now seen in my designing work to operate the 134-GHz on-chip PLL when PFD, CP and LF are designed with 134-GHz VCO and dividers.

2.3.5 Conclusion of a VCO and Dividers for a 134-GHz PLL Synthesizer

In this section, a 37mW CMOS VCO and dividers covering the entire VCO oscillation frequency range for a 134-GHz PLL synthesizer was presented. The dividers have two ILFDs and a divide-by-2 divider was focused. The VCO has a fundamental oscillation range of 131.8 GHz to 134.3 GHz by using the back-gate voltages as a VCO control voltage, which used as a control voltage in divide-by-2. The locking range of divide-by-2 is expanded by the control voltage. The maximum VCO fundamental oscillation frequency of 134.4 GHz was measured. The directly measured VCO oscillation frequencies and calculated frequencies from the measured divider output frequencies are almost equal. This evidences the correct divider function over the entire VCO oscillation range. The VCOs and dividers with a chip core area of 180 μm × 100 μm were implemented in 65-nm CMOS process.

2.4 Conclusion

In this chapter, the CMOS design of integer-N-type PLL, mainly, high speed operation parts of the frequency synthesizers were presented to operate wider operation range.

Firstly, the integer-N-type PLL for CMOS down-conversion IC for a broadcasting satellite was descussed. To achieve a trade-off of the high and low VCO gain, the switching varactors and a tuning voltage varactor were used in a 1-inductor VCO for a 10-GHz-band PLL synthesizer and the target specifications were achieved. A

10-GHz-band PLL synthesizer was implemented in a CMOS 130-nm process. The total chip including amplifiers and a mixer showed 1.1 mm × 1.1 mm.

Next, a 37-mW VCO and dividers for a 134-GHz integer-N-type PLL were descussed. To cover the entire VCO oscillation range, dividers could be increased the operation range by tuning back-gate voltage. The evaluated chip occupies 180 μm × 100 μm implemented in CMOS 65-nm process. A VCO has an oscillation range of 132 GHz to 134.4 GHz and achieves the phase noise values of -80 dBc/Hz at 1-MHz offset frequency. A good prospect is now seen in my designing work to operate the 134-GHz on-chip PLL when PFD, CP and LF are designed with 134-GHz VCO and dividers

References of Chapter 2

[1] T. Copani, S. A. Smerzi, G. Girlando, and G. Palmisano, "A 12-GHz Silicon Bipolar Dual-Conversion Receiver for Digital Satellite Applications", IEEE J. of Solid-State Circuits, Vol. 40, No. 6, June 2005, pp.1278-1287.

[2] P. Philippe, L. Praamsma, R. Breunisse, E van der Heijden, F. Meng, S. Bardy, F. Moreau, S. Wane, E. Thomas, "A low power 9.75/10.6GHz down-converter IC in SiGe:C BiCMOS for Ku-band satellite LNBs", in Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2011, pp.211 – 214.

[3] Giovanni Girlando, Tino Copani, Santo A. Smerzi and Giuseppe Palmisano, "A Ku-Band Monolithic Tuner-LNB for Satellite Applications", in Proc. the IEEE Custom Integrated Circuits Conference (CICC) 2004, pp.613-616.

[4] Daquan Huang, Tim R. LaRocca, Lorene Samoska, Andy Fung, Mau-Chung Frank Chang, "324GHz CMOS Frequency Generator Using Linear Superposition Technique", in Proc, IEEE int. Solid-State Circuit Conf.(ISSCC) Feb. 2008, pp. 476-629

[5] Eunyoung Seok, Changhua Cao, Dongha Shim, Daniel J. Arenas, David B. Tanner, Chih-Ming Hung, Kenneth K. O, "A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna", in Proc, IEEE int. Solid-State Circuit Conf.(ISSCC) Feb. 2008, pp. 472-629

[6] Behzad Razavi, "A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology", IEEE J. Solid-State Circuits, Vol. 46, No. 4, April 2011, pp 894 – 903.

[7] J. Typpo, "A Back Gate Tuned PFET VCO", in Proc. Analog Integrated Circuits and Signal Processing, vol. 30, Issue 3, pp 265-269, March 2002.

[8] L. C. Cho, K. H. Tsai, C. C. Hung, and S. I. Liu, “93.5~109.4GHz CMOS Injection-locked Frequency Divider with 15.3% locking range”, in Proc. Symp. on VLSI Circuits, Jun. 2008, pp. 86–87.

[9] H. Seo, S. Seo, J. Yun, and J. S. Rieh, "A 90-nm CMOS 144 GHz Injection Locked Frequency Divider with Inductive Feedback", J. of Semiconductor Technology and Science, vol. 11, No. 3, Sept. 2011, pp 190-197.

[10] Q. J. Gu, H. Y. Jian, Z. Xu, Y. C. Wu, M. F. Chang, Y. Baeyens and Y. K. Chen, "200GHz CMOS Prescalers with Extended Dividing Range via Time-Interleaved Dual Injection Locking", in Proc. IEEE Radio Frequency Integrated Circuits Symp. (RFIC), Jun. 2010, pp.69 – 72.

[11] K. H. Tsai, L. C. Cho, J H. Wu and S. I. Liu, "3.5mW W-Band Frequency Divider with Wide Locking Range in 90nm CMOS Technology", in Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC), Feb. 2008, pp. 466–628.

[12] B. Y. Lin, K. H. Tsai and S. I. Liu, "A 128.24-to-137.00GHz Injection-Locked Frequency Divider in 65nm CMOS", in Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC), Feb. 2009, pp. 282–283.

[13] P. Mayr, C. Weyers and Ulrich Langmann, "A 90GHz 65nm CMOS Injection-Locked Frequency Divider", in Proc. IEEE Int. Solid-State Circuit Conf. (ISSCC), Feb. 2007, pp. 198–199.

[14] B. Y. Lin and S. I. Liu, "A 132.7-to-143.5GHz injection-locked frequency divider in 65nm CMOS", in Proc. Symp. on VLSI Circuits, Jun. 2009, pp. 230–231.

[15] B. Y. Lin, I. T. Lee, C. H. Wang and S. I. Liu, "A 198.9GHz-to-201.0GHz Injection-Locked Frequency Divider in 65nm CMOS", in Proc. Symp. on VLSI Circuits, Jun. 2010, pp. 49–50.

[16] S. Lim, W. Badalawa and M. Fujishima, "A 110GHz Inductor-less CMOS Frequency Divider", in Proc. Asian Solid-State Circuit Conf. (A-SSCC), Nov. 2009, pp. 61-64.

Chapter 3. Wide Locking Range and Low Energy Differential Dual-Modulus Prescaler

3.1 Introduction

In this chapter, a CMOS dual-modulus prescaler is focused. A typical PLL synthesizer was described in chapter 2, which has both high and low frequency blocks. The VCOs and the frequency dividers are the blocks which operate at high frequencies and consume large power. In addition, wide range and wide margin operation are required in satellite applications because of usage situation under variations in temperature. In general, when the wireless receivers are implemented in CMOS process, the PLL synthesizer consumes a large percentage of the total IC power. It is important to achieve the power reduction of the PLL synthesizer without sacrificing reliability of the achievement of operating frequency and wide margin operation.

Figure 3.1 shows the block diagram of typical integer-N-type PLL synthesizer. Integer-N-type PLL synthesizer is used for a LO signal consisting of a VCO, dividers, a PFD, a CP, a LF and crystal oscillator as a reference frequency. A dual-modulus prescaler is

enclosed by the thick line in Figure 3.1, which requires a higher energy efficiency, lower phase noise and higher speed and wide range operation under variations in temperature. Since the VCO and dividers are differential circuits, the prescaler is also desirable to be a differential circuit, which is much more tolerant of power supply noises. In addition, the differential prescaler should have a wide input phase-shift tolerance since it is difficult to fabricate the differential signal lines with the exactly same length and width in an IC layout. To cover the mismatch of differential signal lines and process variations, the target tolerance of phase-difference deviation from the perfect differential phase-difference, 180 degrees, to be 10 degrees is set. To check the performance of the prescaler, being used as a modulus controller, considerably affects the phase noise and the energy efficiency of the PLL. The limitation of the supply voltage reduction through the measurement results of phase noises and sensitivities of the prescaler under various supply voltages should be also checked.

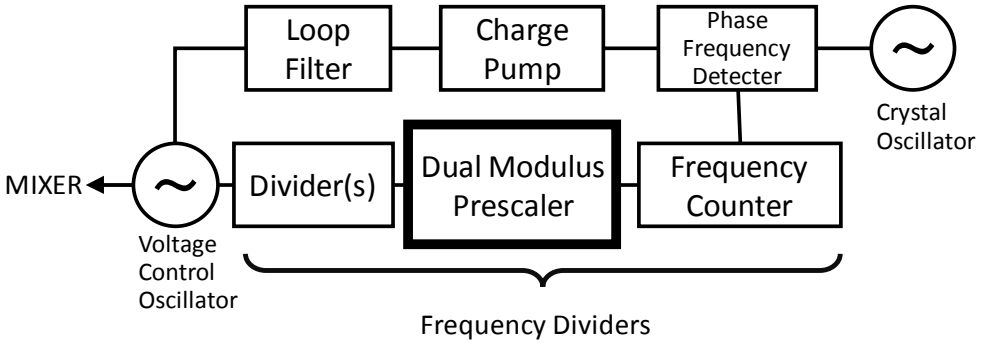
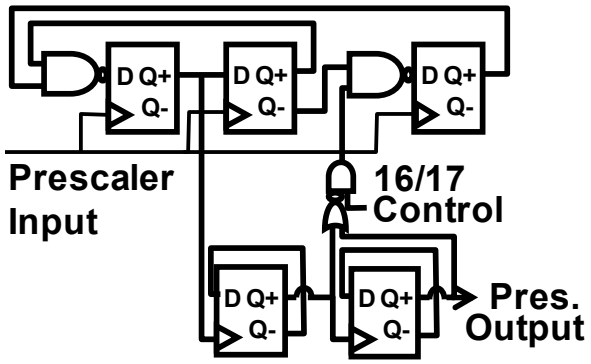


Figure 3.1: Block diagram of typical integer-N-type PLL synthesizer.

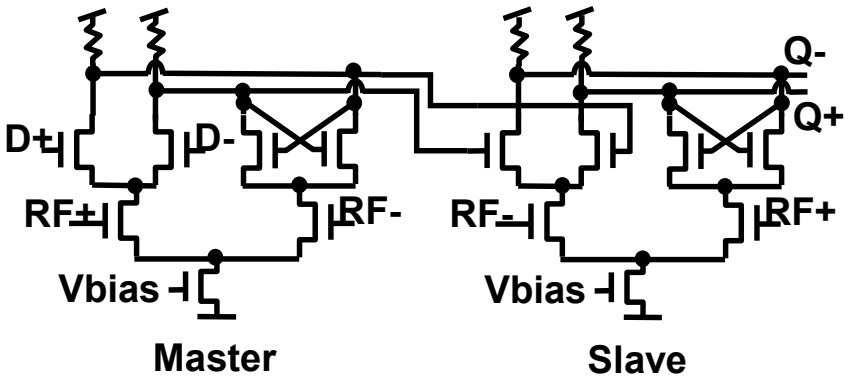
3.2 Previous Modulus Prescaler

A dual-modulus prescaler is the most important circuit in the integer-N-type PLL synthesizers. The prescaler should be energy-efficient and should have a high speed so that it is capable of modulus control from the fixed input frequency. In addition, it should have a wide locking range to cover the process and

temperature variation. A dual-modulus prescaler based on the current-mode logic (CML) has been widely used in PLL synthesizers owing to its wide locking range and high frequency capability [1] - [3]. Figure 2.2 shows an example of a conventional dual-modulus prescaler based on the CML architecture with master-slave configuration [1], (a) shows the block diagram of divide-by-16 or 17, and (b) shows the master-slave D-flip-flop (DFF) in CML architecture. This topology has been widely used in PLL synthesizers owing to its wide locking range and high-frequency operation capability by the differential circuits. Furthermore, they are highly tolerant of the supply voltage noise. However, it has been difficult to meet the increasing demand for lower power consumption, generally. Actually, simulated results in [1], the power consumption is 18.5 mW designed in a CMOS 180-nm process and maximum input frequency is 12.98 GHz.



(a)



(b)

Figure3.2: A typical CML architecture [1], (a) block diagram of divided-by-16/17 and (b) master-slave CML DFF

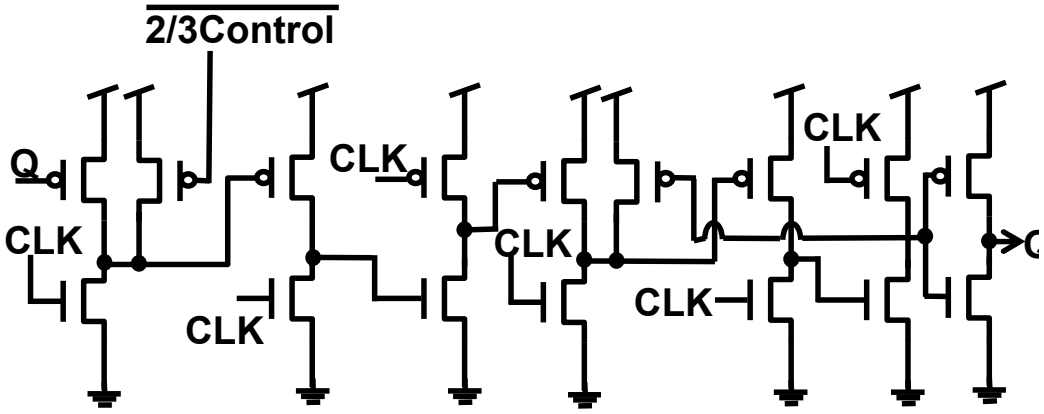


Figure3.3: Example of a TSPC architecture [6]

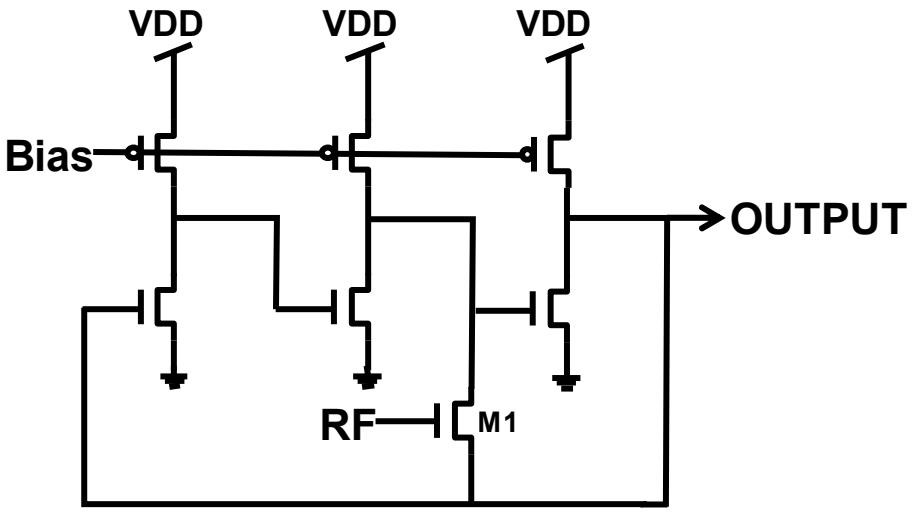
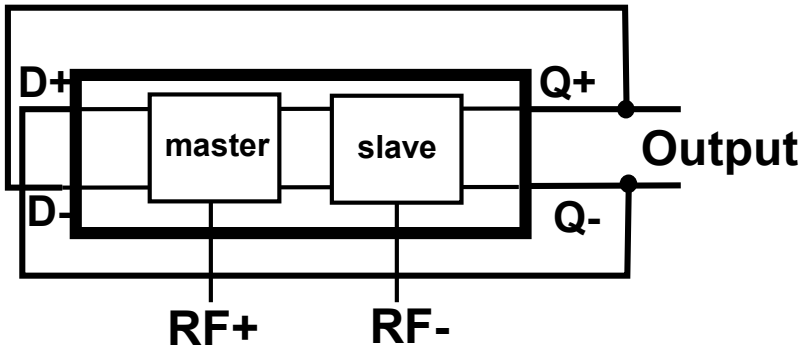
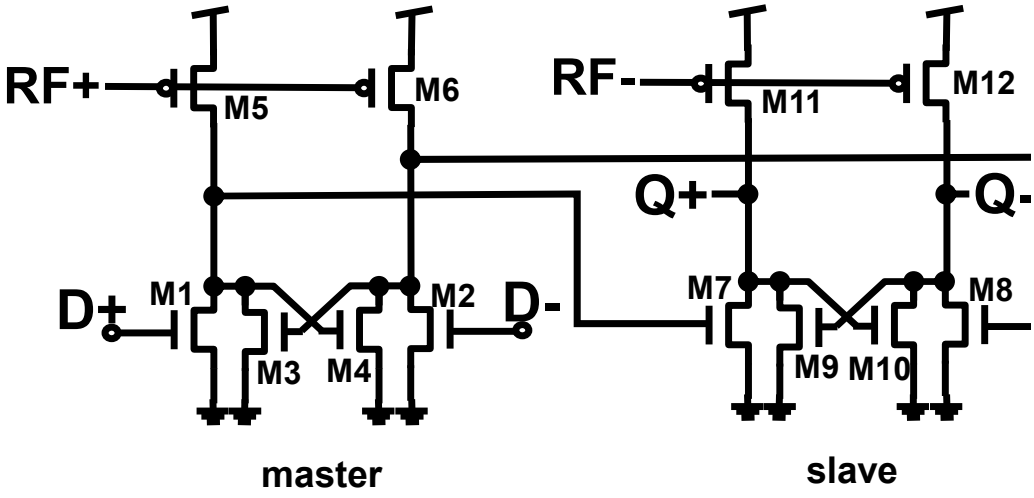


Figure3.4: Schematic of a QDL divider [10]

On the other hand, to reduce the power consumption, modulus-controlled prescalers using injection-locked frequency dividers (ILFDs) have recently been proposed [4] - [9] such as a true single phase clock (TSPC) architecture shown in Figure 3.3. Although they consume less power than the CML architectures, TSPC prescalers cannot accept differential input signals [4] - [8]. For the high-speed and low power operation, there is a system of NMOS transistors used as switching between differential outputs. Figure 3.4 shows a quasi-differential locking (QDL) divider based on the ILFD [10]. Input signals directly modulate the output in a ring oscillator by switching transistor (M1). M1 is inserted between two inverter outputs and used as a quasi-differential output to modulate the oscillation frequency. The architecture using a switch transistor can operate at a low voltage with a wide locking range but is not a fully-differential circuit.



(a)



(b)

Figure 3.5: Simplified block diagram of the divide-by-2 divider (a) and previous latch blocks (b) closed by the thick line in (a) [10].

Figure 3.5 is the differential divider with the master and slave blocks consisting of two sense devices (M1, M2, M7 and M8), a regenerative loop (M3, M4, M9 and M10) and two pull-up devices (M5, M6, M11 and M12) [11]. Since the input transistors, which operate at the fastest speed in the block, are PMOS's and thus have larger gate capacitances, this topology requires larger load driving capability for the preceding block.

A typical VCO based on an LC-VCO is a differential output circuit with hardly any phase-shift mismatch. Since it is difficult to

fabricate the differential signal lines with the exactly same length and width in an IC layout, the dividers and prescalers must tolerate wide phase deviation of its input differential pair. Therefore, the differential dividers with the phase-mismatch tolerance are better than the single-end architectures. However, in previous papers, the phase-shift tolerance is hardly described. Therefore, the phase-shift tolerance of operating a proposed dual-modulus prescaler must be checked.

3.3 Proposed Differential Dual-Modulus Prescaler

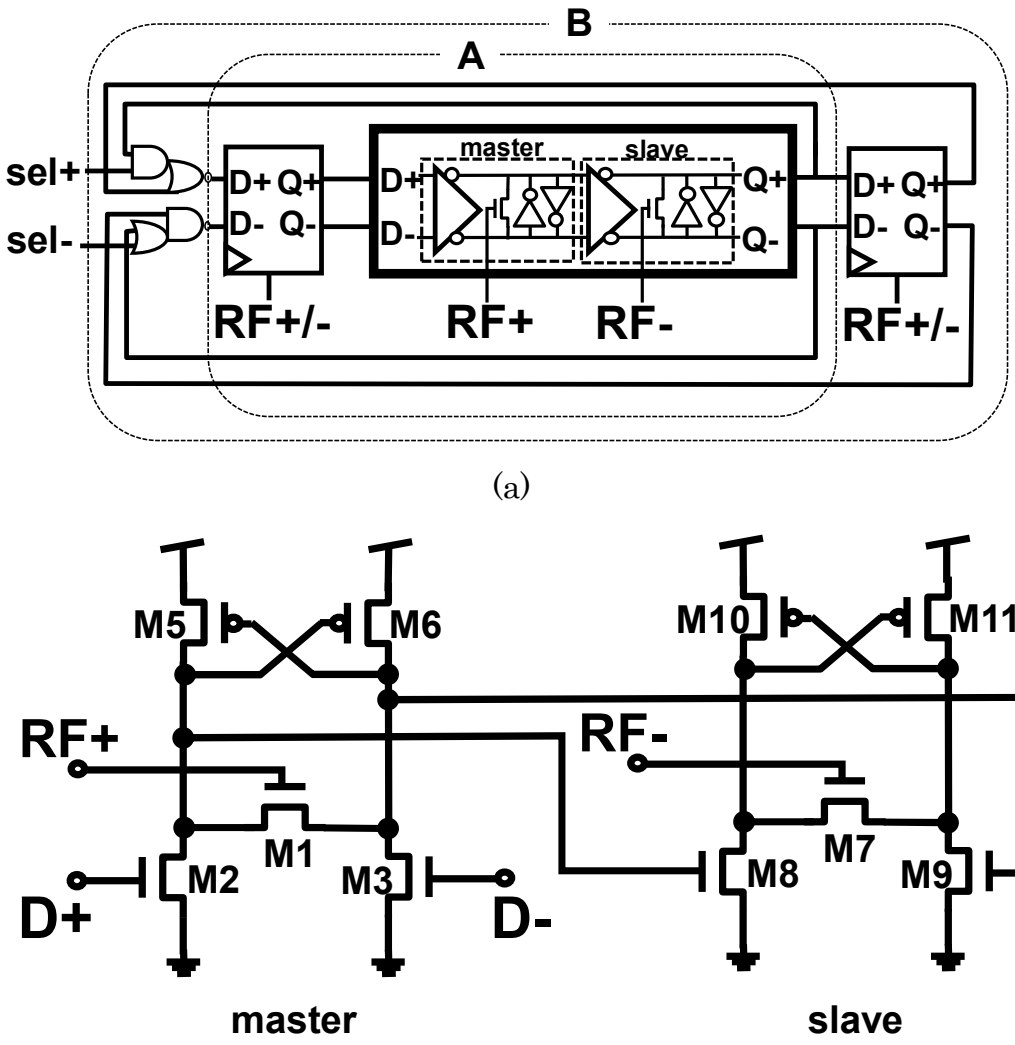
In this research, two satellite applications of a 10-GHz band for broadcasting satellite and a 100-GHz band of high frequency application such as for radio astronomy are focused. Therefore, operated frequencies are different, respectively. For a broadcasting satellite, target frequency is 4 GHz to 6 GHz and the division ratio is 10 and 11, which is implemented in CMOS 130-nm process. For a 100-GHz band application, the operated frequency is 22 GHz to 23 GHz and the division ratio is 11 and 12, which is implemented in CMOS 65-nm process. Both prescalers are same architecture but frequency ranges are different. For the temperature tolerance and wide range operation, wide margin ratio should be required for 100 % or more frequency range as a function of center frequncy. Table 3.1 shows the target specifications of each full differential dual-modulus prescalers.

Table 3.1: Target specifications of two prescalers.

Parameter	For a broadcasting satellite	For a high frequency PLL
Process	CMOS 130 nm	CMOS 65 nm
Operated frequency	4 GHz - 6 GHz	22GHz – 23GHz
Target frequency ratio	100% or more	100 % or more
Phase mismatch tolerance	10 %	‘--

On the basis of the section 3.2 considerations, the fully-differential latch blocks are proposed as shown in Figure 3.6. They are designed the fully-differential dual-modulus 5/6 prescaler based on ILFDs, to achieve a smaller die area, a low power consumption, and a wider locking range by a full-differential architecture. In Figure 3.6 (a), enclosed by dashed line A is a divide-by-4 block created from two-stage differential latch blocks. Enclosed by dashed line B is a divide-by-6 block created from three-stage differential latch blocks. Then a divide-by-5 output is generated by a NAND/NOR block with the divide-by-4 and divide-by-6 blocks. The division ratio is controlled by the modulus control signal "sel+" or "sel-" from a latter cascaded divide-by-2 block. In Figure 3.6 (b), an NMOS switch (M1, M7) is inserted between a differential pair of NMOS's (M2 and M3 or M8 and M9) and between a cross-coupled pair of PMOS's (M5 and M6 or M10 and M11) to inject an input differential signal into the ILFD. Comparing with the conventional single ended ILFDs, [4] - [10], the proposed fully-differential circuit is highly tolerant of supply voltage noise.

To avoid the delay time of the NAND/NOR block, the latch circuit is merged with the NAND/NOR block (enclosed by dashed line C in Figure 3.7(a)) to realize a high-speed latch through modulus control. Figure 3.7 (b) shows a schematic of the proposed latch circuit merged with the NAND/NOR block and master latch block. Figure 3.8 shows the simulation results of the prescaler operation ranges of the single and differential inputs. The operation range of the differential input is two times wider than that of single input.



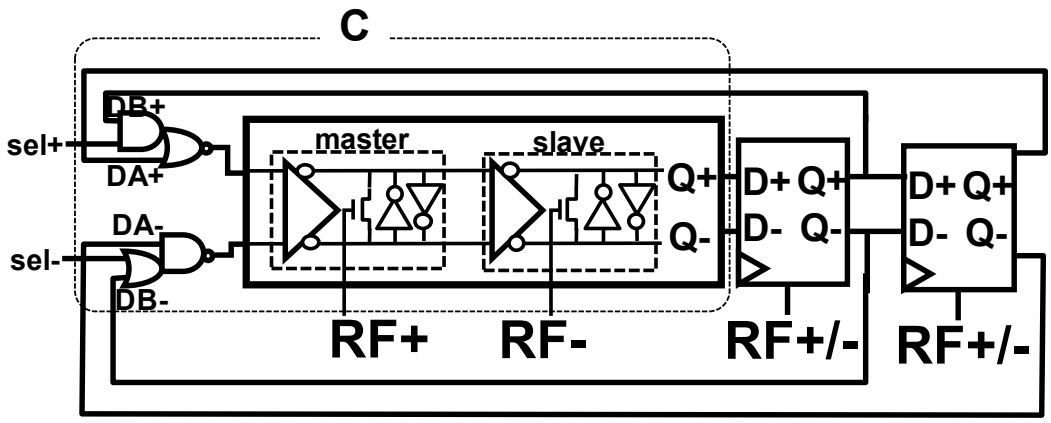
(a)

(b)

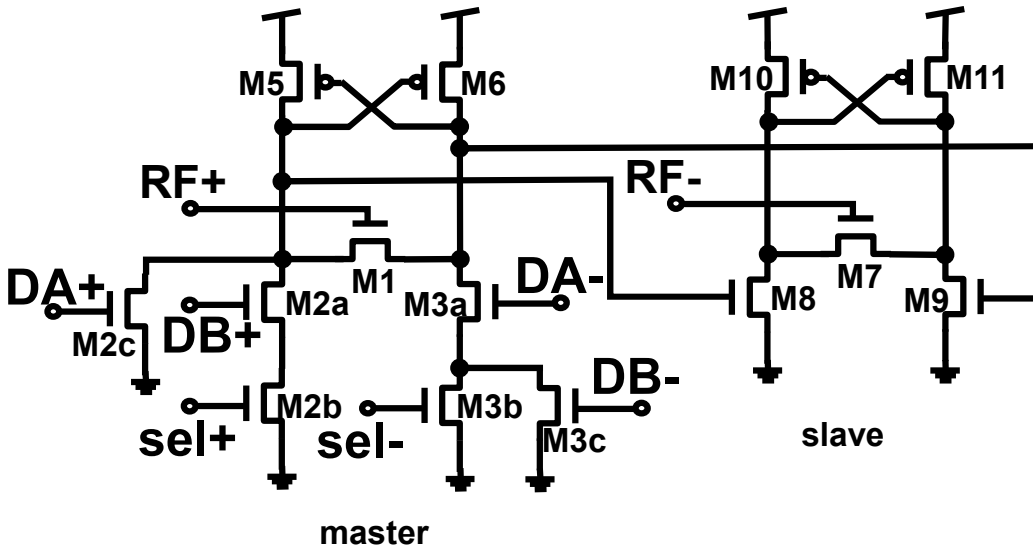
Figure 3.6: Block diagram of a dual-modulus prescaler (a) and proposed latch blocks (b) closed by the thick line in (a).

Figure 3.9 shows the complete block diagram of the proposed differential dual-modulus 10/11 prescaler, which consists of the three-stage latches of merged and simple master-slave blocks with the cascaded divide-by-2 divider. Figure 3.10 (a) shows the divided-by-10 operation and (b) shows the divide-by-11 operations. The divide-by-10 output is generated by using the output of the divide-by-5 block as the input to the cascaded divide-by-2 block in Figure 3.9 (a). On the other hand in (b), the divide-by-11 output is

generated by using the divide-by-5 and divide-by-6 outputs alternately. The division ratio is controlled by the modulus-control signal Cntr+/- from the latter frequency counter.



(a)



(b)

Figure 3.7: Block diagram of a dual-modulus prescaler (a) and proposed latch blocks (b) closed by the thick line in (a).

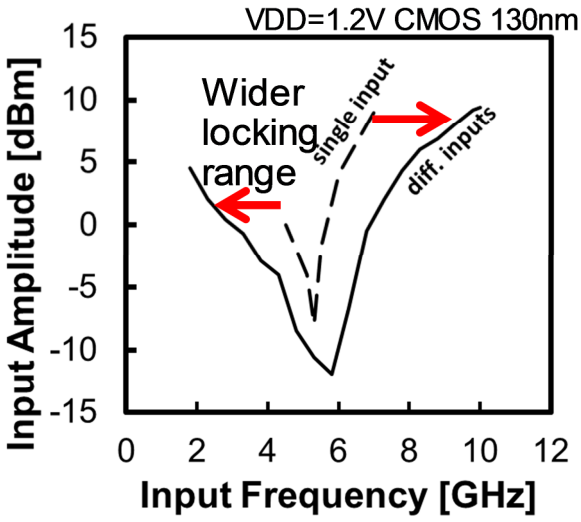


Figure 3.8: Simulated results of the prescaler operation ranges of the single and differential inputs

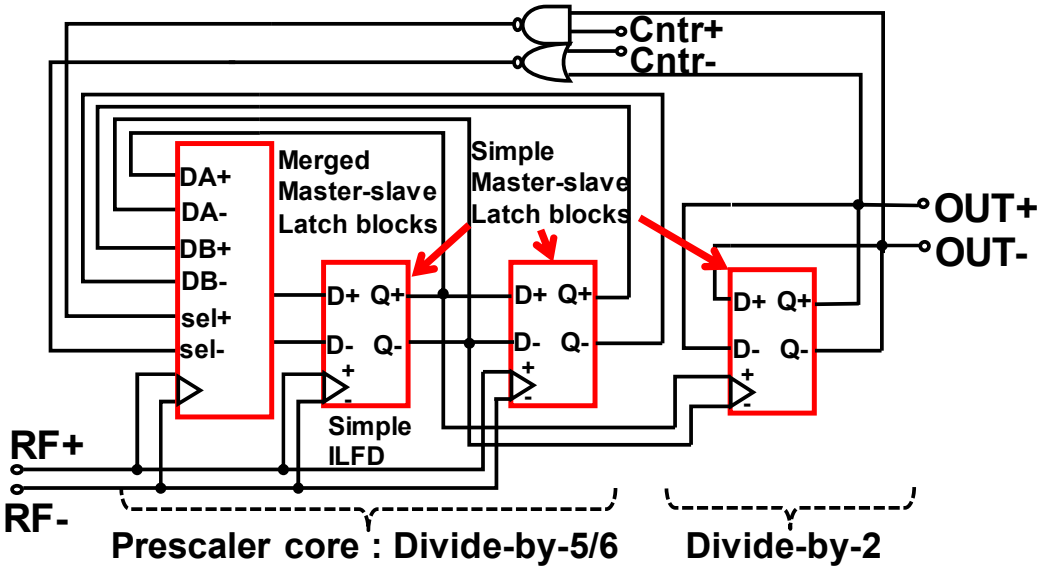


Figure 3.9: Block diagram of a total differential dual-modulus prescaler

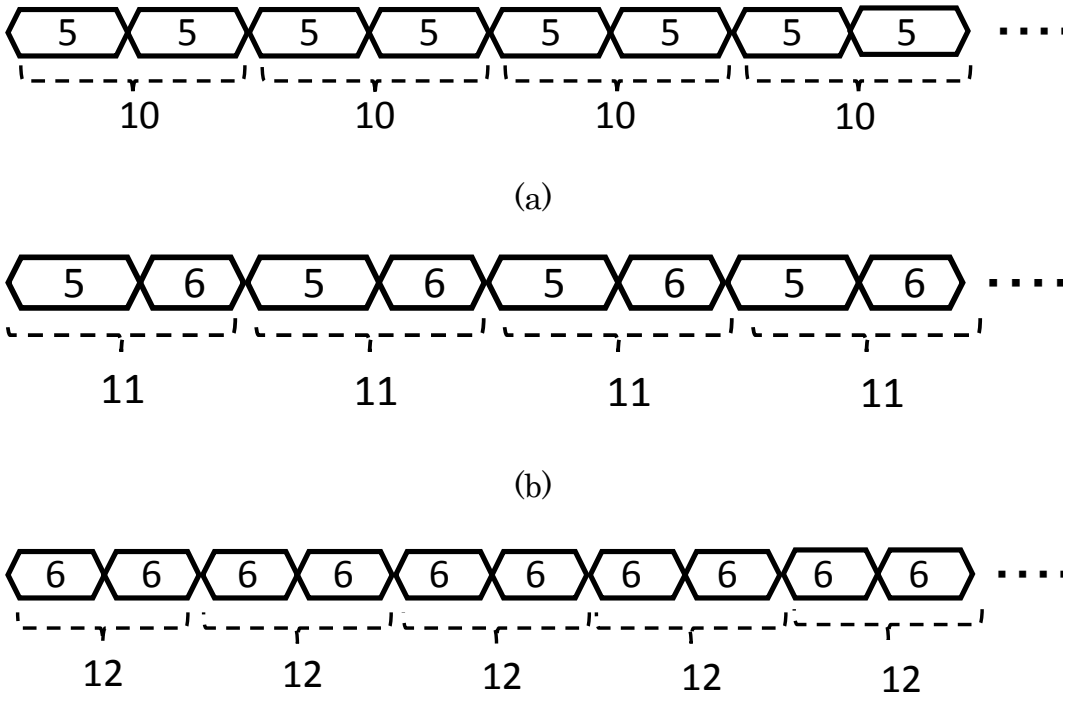


Figure 3.10: Signal timing charts of divide-by-10 (a), divide-by-11 (b) and divide-by-12 (c) operations.

In the case of the differential dual-modulus 11/12 prescaler, the divide-by-11 output is generated by using the divide-by-5 and divide-by-6 outputs, alternately. On the other hand, the divide-by-12 output is generated by using the output of the divide-by-6 block as the input to the cascaded divide-by-2 block, respectively. The division ratio is controlled by the modulus-control signal Cntr+/-. Figure 3.9 (c) shows the concepts of the divided-by-12 operation. To operate as the pulse-swallowing counter, a counter circuit (not illustrated) is implemented after the dual-modulus 10/11 or 11/12 prescaler. The dual-modulus prescaler switches the division ratio of 10 or 11 in a dual-modulus 10/11 prescaler and switches the division ratio of 11 or 12 in a dual-modulus 11/12 prescaler using the feedback signal from a counter circuit.

3.4 Measurement Results

To evaluate the differential dual-modulus prescalers, the test chips including the prescalers are implemented in CMOS 130-nm and 65-nm processes, respectively. Figure 3.11 shows the die photograph of the dual-modulus 10/11 prescaler implemented in CMOS 130-nm process. The core size is 40 µm × 20 µm. Figure 3.12 shows the die photograph of the dual-modulus 11/12 prescaler implemented in CMOS 65-nm process. The core size is 17 µm × 17 µm. In this section, measurement results for the input sensitivity, frequency range, phase-shift variation and impact of the operation from the viewpoints of phase noise measurements are described.

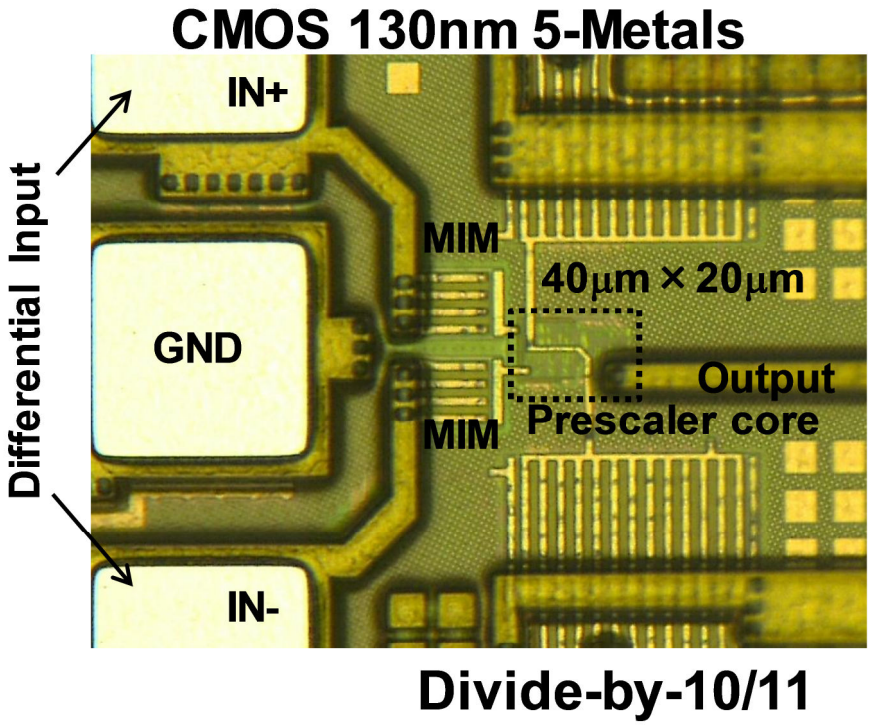


Figure 3.11: Signal timing charts of divide-by-10 (a), divide-by-11 (b) and divide-by-12 (c) operations.

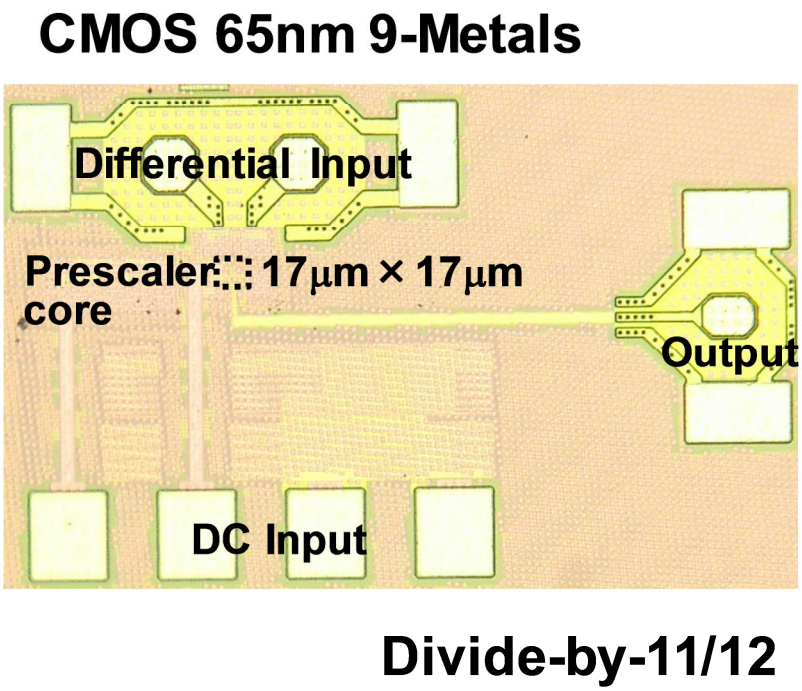


Figure 3.12: Signal timing charts of divide-by-10 (a), divide-by-11 (b) and divide-by-12 (c) operations.

3.4.1 Sensitivity vs. Supply Voltage

Figure 3.13 shows the measurement system. To monitor the output signal, a pair of source follower buffers each with a matching impedance of 50 Ω is implemented and one of the outputs is observed. For the differential input, we mainly used a 4-ports vector-network analyzer (VNA) as the differential signal source, calibrated the phases and amplitudes at the on-wafer probe heads. Otherwise, we used the signal generator and the coaxial balun probe to check the differential input operation. Metal-insulator-metal (MIM) capacitor is used as the input DC-cut without impedance matching. For the input DC-bias voltage of the prescaler, the half supply voltage is used.

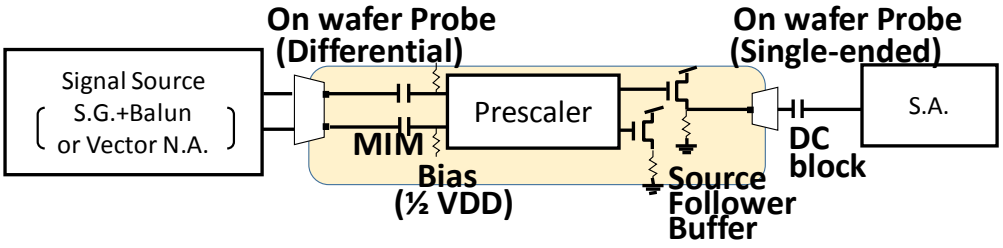
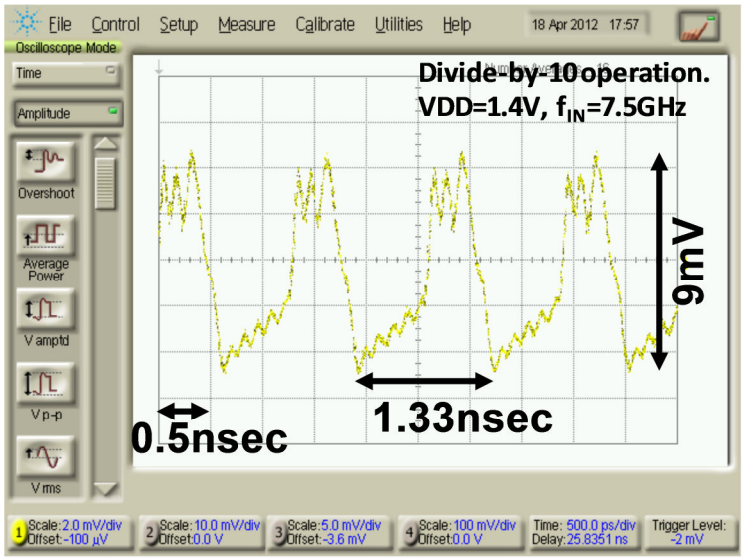
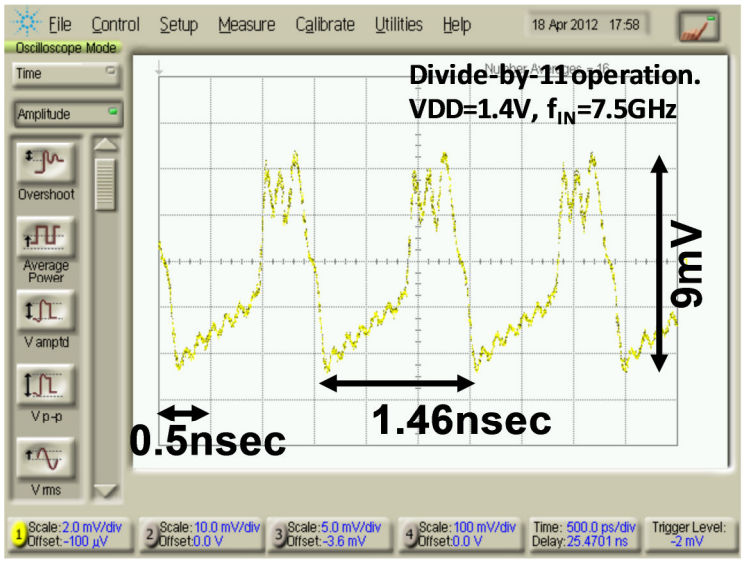


Figure 3.13: Measurement system of prescaler



(a)



(b)

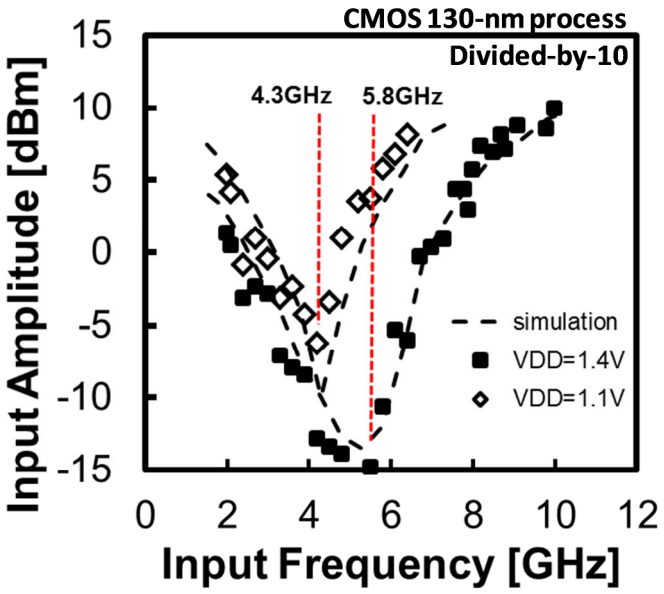
Figure 3.14: Measured output signal waveforms, (a) divided-by-10 operation and (b) divided-by-11 operation.

Figure 3.14 shows the output signal waveform of the dual-modulus 10/11 prescaler implemented in CMOS 130-nm process, which obtained through the source follower buffer for (a) divide-by-10 and (b) divide-by-11 operations at an input frequency of 7.5 GHz with 1.4-V supply voltage and 10-dBm input amplitude. The measured results show the period of (a) 1.33 nsec for divide-by-10 and (b) 1.46 nsec for divide-by-11 operations.

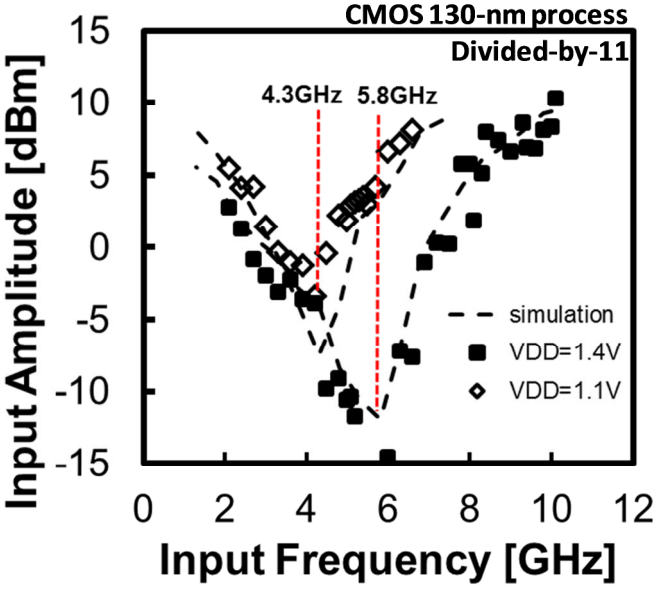
Figure 3.15 shows the plots of simulated and measured input sensitivities as functions of the operating frequency at the 1.4-V and 1.1-V supply voltages for the (a) divide-by-10 operation and (b) divide-by-11 operation implemented in CMOS 130-nm process. The measured sensitivity is defined as the minimum input signal amplitude where no spurious tone is observed in the output spectrum. The minimum operational frequency of the cascade divider is limited to 2.1 GHz and the measurement results show good agreement with the simulation results for both division ratios and supply voltages. At the 1.4-V supply voltages, the sensitivities are highest at 5.8 GHz for both division ratios and the required amplitudes of the input are as small as approximately -12 dBm. The locking range of the proposed dual-modulus 10/11 prescaler is from 2.1 GHz to 10.1 GHz at the 1.4-V supply voltage.

The minimum sensitivity deteriorates when the supply voltage is reduced from 1.4 V. At the 1.1-V supply voltage, the minimum sensitivities are highest at 4.3 GHz for both division ratios, and the required amplitudes of the input are approximately -4 dBm. The locking range of the proposed dual-modulus 10/11 prescaler is from 2.1 GHz to 6.8 GHz at the 1.1-V supply voltage.

Figure 3.16 shows the plots of simulated and measured input sensitivities as functions of the operating frequency at the 1.2-V and 1.0-V supply voltages for the (a) divide-by-11 operation and (b) divide-by-12 operation implemented in CMOS 65-nm process. The shift of the minimum input sensitivity frequencies between the simulated and measured results is approximately 6 GHz and the measured maximum operating frequency is 26 GHz.

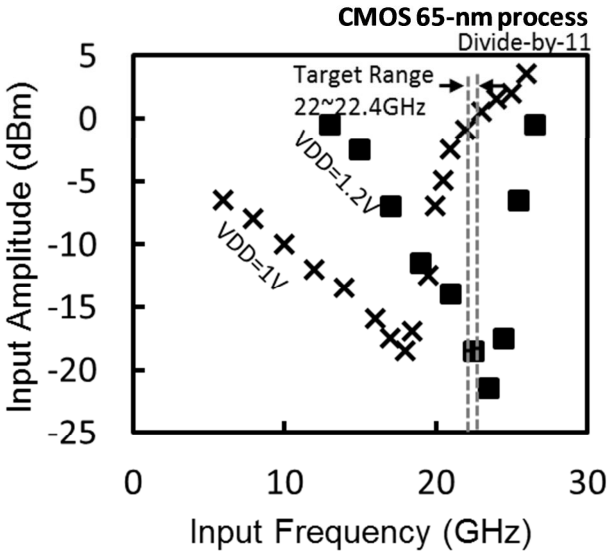


(a)

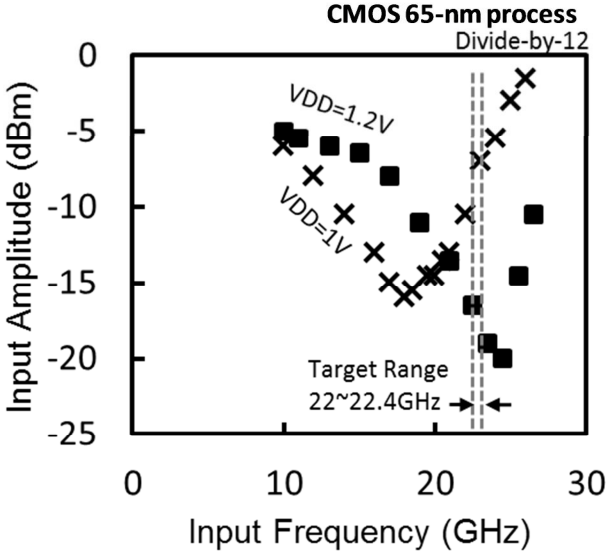


(b)

Figure 3.15: Simulated and measured input sensitivities as functions of the operating frequency for the (a) divide-by-10 operation and (b) divide-by-11 operation.



(a)



(b)

Figure 3.16: Simulated and measured input sensitivities as functions of the operating frequency for the (a) divide-by-11 operation and (b) divide-by-12 operation.

Both Figure 3.16 (a) and (b), the measured operation frequencies increase with the supply voltage. But the signal source of VNA is

limited to 26.5 GHz therefore we could not test higher frequency operation than 26.5 GHz. At the 1.0-V supply voltages, the sensitivities are highest at 17 GHz for both division ratios and the required amplitudes of the input are as small as approximately -16 dBm. The locking range of the proposed dual-modulus prescaler is from 9 GHz to 26 GHz.

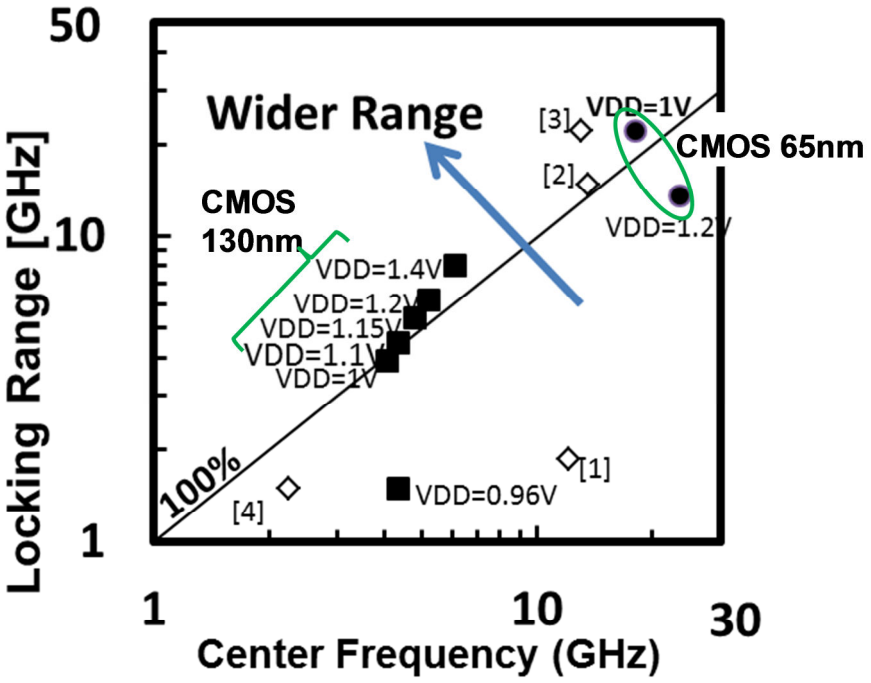


Figure 3.17: Measured locking ranges with minimum and maximum operational frequencies as a function of center frequency for various supply voltages.

As the supply voltage of the proposed dual-modulus prescaler reduces, the power consumption and the operational frequency range decrease. Figure 3.17 shows the locking ranges with minimum and maximum operational frequencies as a function of center frequency for various supply voltages and various types of prescalers with differential topology. The locking range of the proposed dual-modulus 10/11 prescaler implemented in CMOS 130-nm process is from 2.1 GHz to 10.1 GHz and, therefore, the

locking range per center frequency (=$\Delta f/f_{Center}$) is 131 % at 1.4-V supply voltage. The ratio $\Delta f/f_{Center}$ decreases as the supply voltage decreases, however, it is still 104 % at 1.1-V supply voltage. The target frequency range of 100 % is covered at the supply voltage of 1.1 V. The locking range of the proposed dual-modulus 11/12 prescaler implemented in CMOS 65-nm process is from 9 GHz to 26 GHz and, therefore, the $\Delta f/f_{Center}$ is 122 % at 1.0-V supply voltage. The target frequency range of 100 % is covered at the supply voltage of 1.0 V. However, it is 58% at the supply voltage of 1.2 V. The signal source of VNA is limited to 26.5 GHz therefore we could not test higher frequency operation than 26.5 GHz.

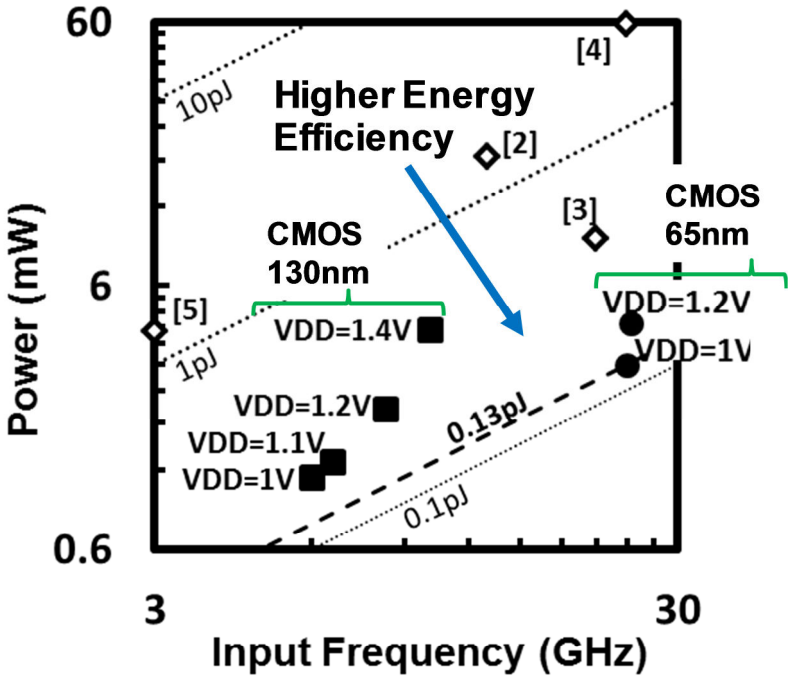


Figure 3.18: Normalized energies at the maximum operational frequencies.

The normalized energy consumption at the maximum operational frequency, which is defined as the power consumption per operating frequency (= mW/GHz, pJ), is shown in Figure 3.18 for various supply voltages and 2-prescalers implemented in CMOS 130-nm

and 65-nm processes. In Figure 3.18, different types of prescalers with a differential topology are also compared. In the operation of the dual-modulus 10/11 prescaler implemented in CMOS 130-nm process, the normalized energy decreases as the supply voltage decreases. The maximum frequency range is 8 GHz at a supply voltage of 1.4 V with a power consumption of 4.06 mW. In this case, the normalized energy consumption is 0.4 pJ. The maximum operational frequency is 6.6 GHz at a supply voltage of 1.1 V with a power consumption of 1.28 mW. In this case, the normalized energy consumption is 0.19 pJ. On the other hand, in the operation of the dual-modulus 11/12 prescaler implemented in CMOS 65-nm process, the maximum operational frequency is 26 GHz at a supply voltage of 1.0 V with a power consumption of 3.1 mW. In this case, the normalized energy consumption is 0.13 pJ. As shown in Figure 2.16, the proposed dual-modulus 11/12 prescaler implemented in CMOS 65-nm process achieved the minimum normalized energy consumption. The proposed dual-modulus prescalers cover the wide frequency range over 100 % and also achieved lower normalized energy operation compared with the conventional differential prescalers.

3.4.2 Sensitivity vs. Supply Voltage

The differential prescaler has a wide input phase-shift tolerance since it is difficult to fabricate the differential signal lines with the exactly same length and width in an IC layout. The target tolerance of phase-difference deviation is 10 degree from the perfect differential phase-difference. For the phase-shift measurement by various phase-shift inputs, we used 4-ports VNA as the various phase-shift signal sources, which calibrated the phases and amplitudes at the on-wafer probe heads. Figure 3.19 shows the simulation results of sensitivities for various phase deviations with divide-by-11 operation at 1.4-V supply voltage. The minimum sensitivity is achieved at approximately 5.8 GHz for the various phase-differences and the operational frequency range remains approximately the same for the phase-difference from 90 to 270

degrees (-90 to 90 degrees).

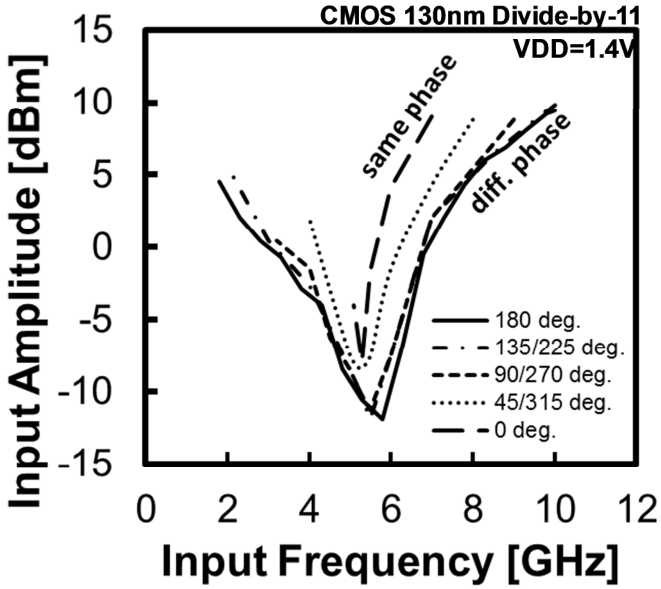
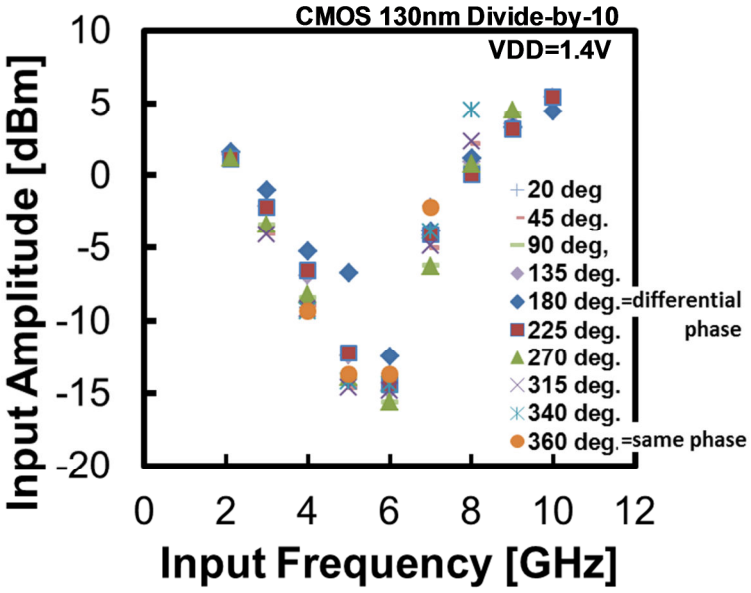


Figure 3.19: Simulated sensitivity of the various phase difference inputs at the 1.4-V supply and divided-by-11 operation.

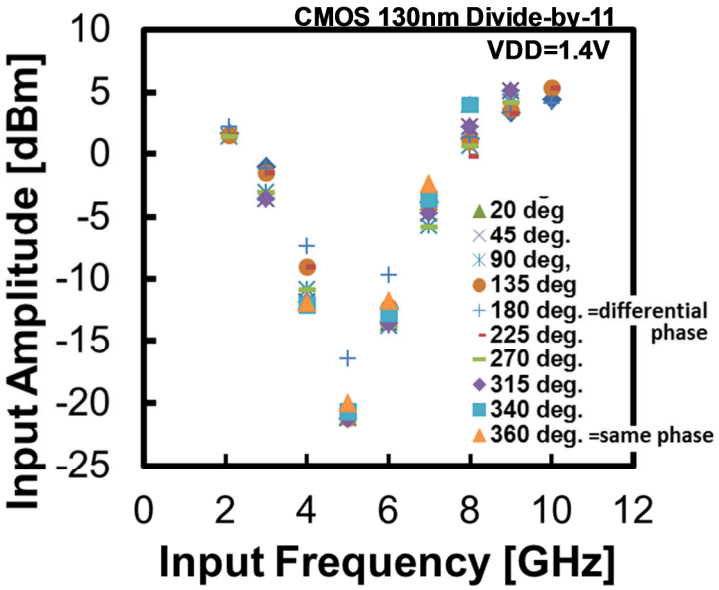
Figure 3.20 shows the measured sensitivities for various phase-differences at 1.4-V supply voltage for (a) divide-by-10 operation and (b) divide-by-11 operation. The measured minimum sensitivity takes place approximately at 5.8 GHz and the operational frequency range remains approximately the same for the phase-difference from 90 to 270 degrees as the simulation results in Figure 3.20.

Figure 3.21 shows the locking range as a function of various phase-differences between the differential input pair. The locking range of the perfect differential input pair (180-degree difference) is from 2.1 GHz to 10.1 GHz and is the widest among the various phase-differences. This 8-GHz locking range at 180-degree phase-difference remains approximately the same over the phase-difference from 90 to 270 degrees. However, the measured locking range decreases as the phase deviation increases and reaches the narrowest range from 4 to 8 GHz at 0 or 360 degrees of phase-difference. According to the measurement results, the proposed prescaler achieves the target tolerance of phase-difference

deviation with an enough margin.



(a)



(b)

Figure 3.20: Measured sensitivities of the various phase-shift mismatches at the 1.4-V supply voltage for (a) divide-by-10 and (b) divide-by-11 operations.

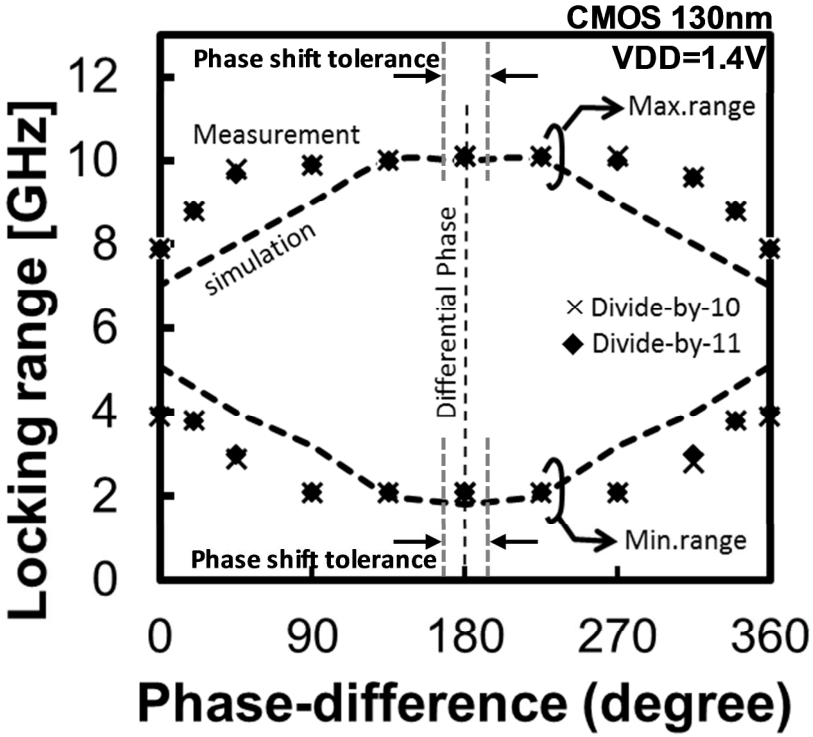


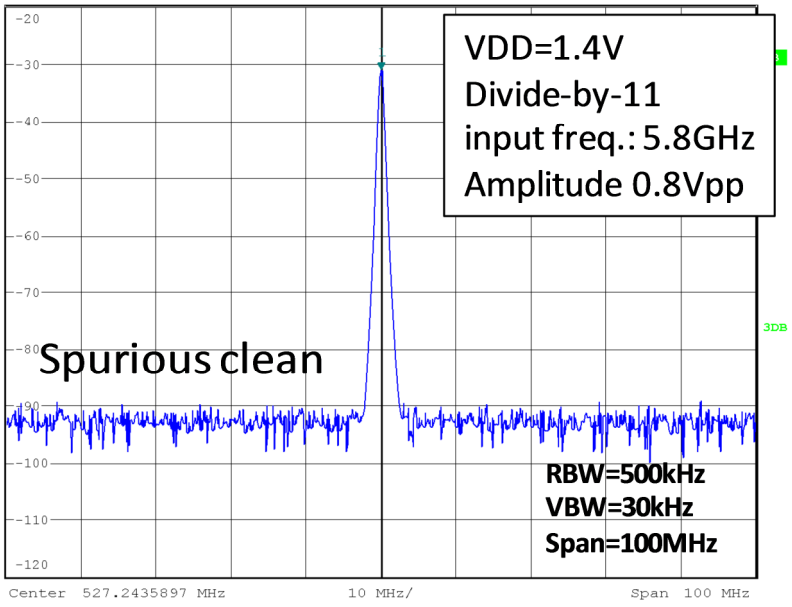
Figure 3.21: The locking range as a function of center frequency at the various phase shifts.

3.4.3 Impact of the Quasi- and Non- Locking Operations

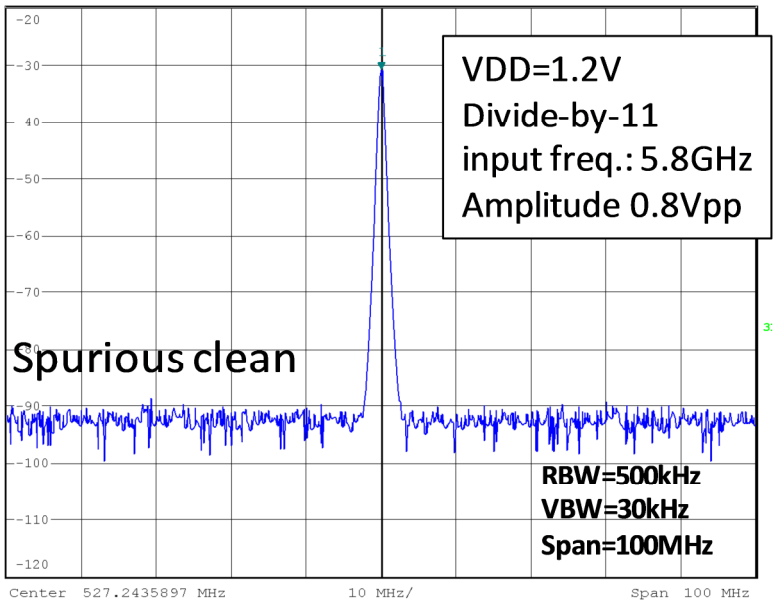
A dual-modulus prescaler in PLL using LO signal is expected to operate without many spurious noises nor large phase noises. Figure 3.22 shows the measured spectrums of output signals, where (a) is for 1.4-V, (b) is for 1.2-V, (c) is for 1.1-V and (d) is for 0.96-V supply voltage, respectively. The noise floors of spectrum in (a) and (b) are clean indicating the full-locking operations. On the other hand, the noise floor of spectrum in (c) has some spurious noises indicating the quasi-locking operation. The noise floor of the spectrum for 0.96-V supply voltage in (d) has many spurious noises indicating non-locking operation.

Figure 3.23 shows the phase noise measurement results under the various supply voltages at 5.8 GHz input operations, where (a) is for divide-by-10 operation and (b) is for divide-by-11 operation. The

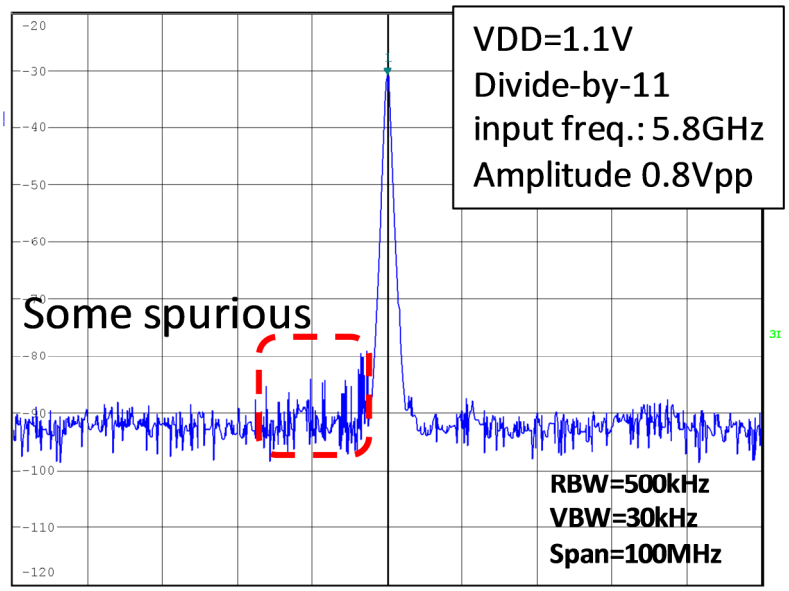
phase noise rapidly increases as the supply voltage decreases from 1.2 V to 1.1 V. Furthermore, the phase noise increases for both division ratios and reaches the worst at 0.96-V supply voltage.



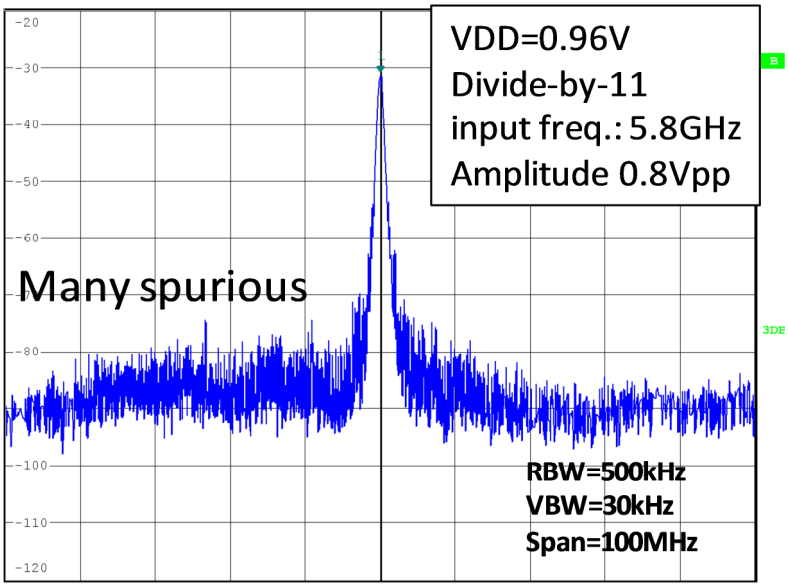
(a)



(b)

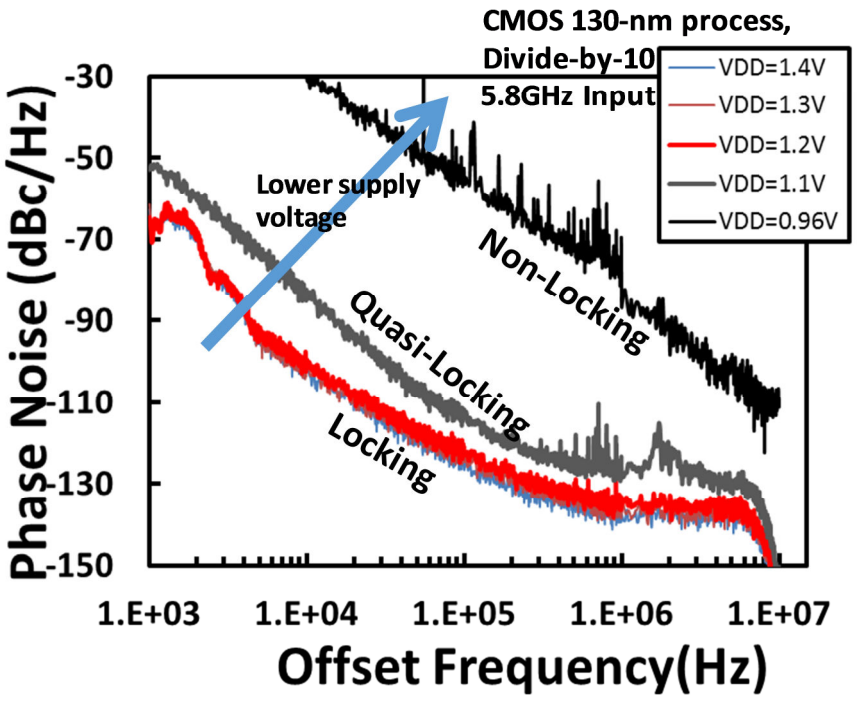


(c)

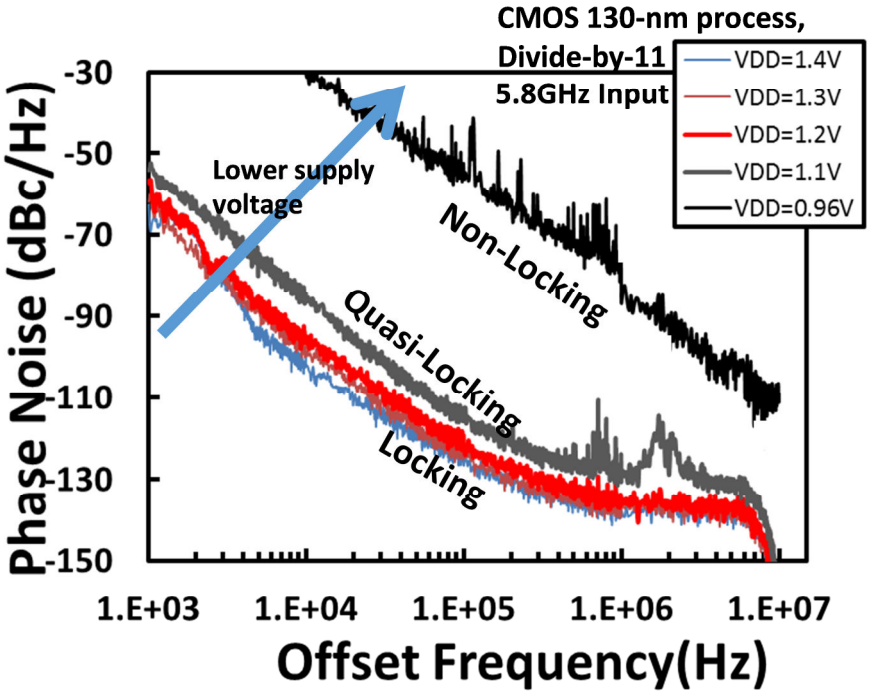


(d)

Figure 3.22 Measured spectrum of proposed prescaler implemented in CMOS 130-nm process for divide-by-11 operation at (a) 1.4-V, (b) 1.2-V, (c) 1.1-V and (d) 0.96-V supply voltage



(a)



(b)

Figure 3.23: Measured phase noise of (a) divide-by-10 and (b) divide-by-11 operation at various supply voltage.

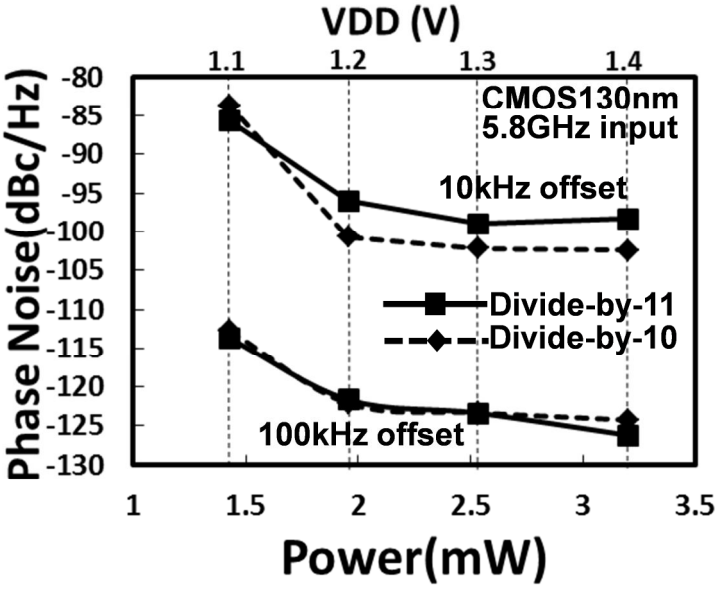


Figure 3.24: Comparison of the phase noise of the various supply voltages at 10-kHz and 100-kHz offsets.

The measurement results of spectra and phase-noise indicate that the quasi-locking operation occurs for 5.8 GHz and 800 mVp-p input frequency at a 1.1-V supply voltage, where the phase noise of 1-MHz offset has some tones due to the quasi-locking operation. The non-locking operation increases many spurious tones in the output spectrum and the worst phase noises.

The phase noises of 10-kHz and 100-kHz offset as a functions of power consumption are shown in Figure 3.24. In the dual-modulus 10/11 prescaler operations, the power consumption decreases in proportional to the square of the supply voltage. However, the measurement results at 1.1-V supply voltage show the larger phase noise than at higher supply voltages due to the quasi- and non-locking operations.

3.5 Conclusion

A differential dual-modulus prescaler based on an ILFD architecture was presented. The three-stage differential latches

using the ILFD and a cascaded differential divider were implemented in a CMOS 130-nm and 65-nm processes. The prototype chip core occupies 40 μm × 20 μm in a CMOS 130-nm process and 17 μm × 17 μm in a CMOS 65-nm process. The proposed prescaler implemented in CMOS 130-nm process can operate divide-by-10 and divide-by-11 operations and the prescaler implemented in CMOS 65-nm process can operate divide-by-11 and divide-by-12 operations.

In the proposed prescaler implemented in a CMOS 130-nm process, the normalized energy consumptions of 0.4 pJ (=mW/GHz) at a 1.4-V supply voltage and 0.24 pJ at a 1.2-V supply voltage could be achieved. Furthermore, in the proposed prescaler implemented in a CMOS 65-nm process, the normalized energy consumption of 0.13 pJ at a 1.0-V supply voltage could be also achieved.

To evaluate the tolerance of phase-difference deviation of the input pair from the perfect differential phase-difference, 180 degrees, the operational frequency range for various phase-differences was measured. The proposed prescaler implemented in CMOS 130-nm process achieves an operational frequency range of 2.1 GHz - 10 GHz as far as the input phase-difference deviation is less than 90 degrees. However, the range of operational frequency decreases as the phase-difference deviation exceeds 90 degrees, finally reaching the range of 3.9 GHz - 7.9 GHz at 180 degrees of phase-difference deviation.

In addition, to verify the fully-locking operation, the spurious noise and the phase noise degradation while reducing the supply voltage were checked. The sensitivity analysis of the prescaler for different supply voltages can explain the above degradation of spectral purity. Spurious noise arises and the phase noise degrades with decreasing supply voltage due to the quasi- or non-locking operation. We verified that the fully-locking operations from 1.4-V to 1.2-V supply voltage meet the requirement operations. The wide range operation and wide margin structure could be achieved in this proposed full-differential dual-modulus prescaler.

References of Chapter 3

[1] Evan Eschenko and Kamran Entesari, “A Low Noise 13 GHz Power Efficient 16/17 Prescaler with Rail to Rail Output Amplitude” in Proc. Midwest Symposium on Circuit and Systems (MWSCAS) 2007, pp. 427 – 430.

[2] Yanping Ding and Kenneth K. O, “A 21-GHz 8-Modulus Prescaler and a 20-GHz Phase-Locked Loop Fabricated in 130-nm CMOS”, IEEE J. Solid-State Circuits, vol. 42, no. 6, JUNE 2007, pp 1240 – 1249..

[3] Hans-Dieter Wohlmuth and Daniel Kehrer, “24GHz Dual-Modulus Prescaler in 90 nm CMOS", in Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS), 2005, pp 3227 - 3230.

[4] Ahmdd MlRael, “A 5 GHz, 1.5 Volt and very low-power CMOS frequency synthesizer for wireless communications", in Proc. Midwest Symposium on Circuit and Systems (MWSCAS) 2002, pp III-536 –539.

[5] Ram Singh Rana, “Dual-Modulus 127/128 FOM Enhanced Prescaler Design in 0.35-µm CMOS Technology”, IEEE J. Solid-State Circuits, vol. 40, no. 8, AUGUST 2005, pp 1662 – 1670.

[6] M.Vamshi Krishna, M.A.Do, C.C.Boon, K.S.Yeo and Wei Meng Lim. “A 1.8-V 6.5-GHz Low Power Wide Band Single-Phase Clock CMOS 2/3 Prescaler”, in Proc. Midwest Symposium on Circuit and Systems (MWSCAS) 2010, pp. 149 – 152.

[7] Joonhee Lee and Seonghwan Cho, “A 470-µW Multi-Modulus Injection-Locked Frequency Divider with Division Ratio of 2, 3, 4, 5 and 6 in 0.13-µm CMOS”, in Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC) 12-3, November, 2007, pp. 332 – 335.

[8] Zhiming Deng and Ali M. Niknejad, “The Speed–Power Trade-Off in the Design of CMOS True-Single-Phase-Clock Dividers”, IEEE J. Solid-State Circuits, vol. 40, no. 11, Nov. 2010, pp 1662 – 1670

[9] Xiaopeng Yu, Jianjun Zhou, Xiaolang Yan, Wei Meng Lim, Do, A.V. and Kiat Seng Yeo, “Sub-mW Multi-GHz CMOS Dual-Modulus Prescalers Based on Programmable Injection-Locked Frequency Dividers”, in Proc. Radio Frequency Integrated Circuits (RFIC) Symposium, 2008, RTU1D-3, pp.431-434.

[10] K. Yamamoto and M. Fujishima, “A 44-μW 4.3-GHz Injection-Locked Frequency Divider With 2.3-GHz Locking Range”, IEEE J. of Solid-State Circuits, vol. 40, pp. 671-677, March 2005.

[11] Behzad Razavi, Kwing F. Lee and Ran H. Yan, “Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS”, IEEE J. Solid-State Circuits, vol. 30, no. 2, pp.101 - 109 1995.

Chapter 4. Amplifiers and a Mixing Block for a Broadcasting Satellite

4.1 Introduction

In many areas of the world, the broadcasting satellite provides a wide range of channels and services. The growing demand for new high-data-rate digital services via satellite, such as high-definition television (HDTV), is having an impact on the markets of developing countries.

A broadcasting satellite system is shown in detail in Figure 4.1. The dish antenna receives an RF satellite signal in 10-GHz band (10.7 GHz – 12.75 GHz) from a satellite. A low-noise block (LNB) down-converter set on the dish antenna converts the RF signal in 10-GHz band to an IF signal in 1.5-GHz band (950 MHz – 2150 MHz). As I mentioned in chapter 1, the LO signals used discrete open-loop DROs, which required manual adjustments of oscillation frequencies. Recently, to relax the temperature drift and the aging effect, fully integrated down-converter ICs with PLLs have been proposed with a silicon bipolar or SiGe BiCMOS process [1] - [2]. A satellite antenna is built in open air all over the world, therefore down-converter IC is operated with constant conversion gain under variations in temperature. In this research, the target temperature ranges set from -30 degree to 90 degree. On other hand, it is

important to meet the specifications of conversion gain, noise figure (NF), linearity and power consumption at the 10-GHz band operation. The down-conversion ICs of a broadcasting satellite use relatively expensive silicon bipolar or SiGe BiCMOS processes.

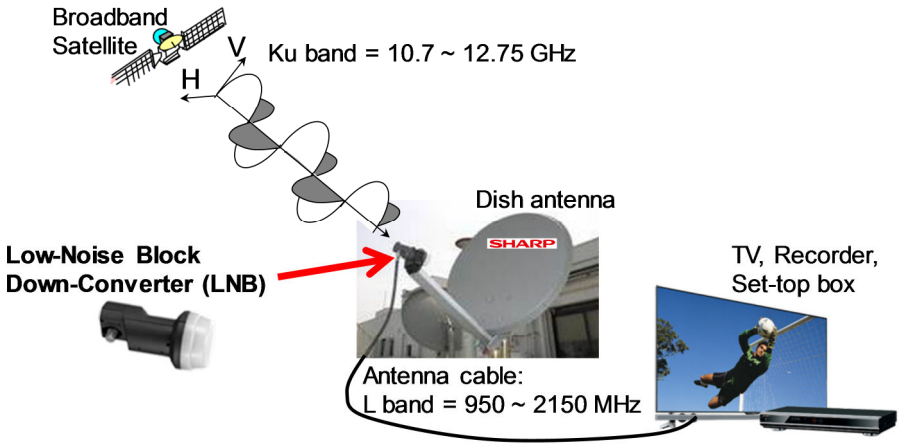


Figure 4.1: Simplified broadcasting satellite configration.

In this chapter, the realization of the fully integrated down-converter IC for a broadcasting satellite using a low-cost CMOS 130-nm process is described. Figure 4.2 shows the block diagram of an LNB module using CMOS down-converter IC with amplifiers and a mixing block (enclosed by a dashed blue line). The LNB module has two RF input terminals of horizontal and vertical waves. The module selects the horizontal or vertical wave of satellite signals and amplifies the selected signal using the first LNA (LNAH or LNAV) and the second LNA (LNA2) fabricated with a high-electron mobility transistor (HEMT) process. The first LNAs and the second LNA have low NFs, therefore 0.9 dB of the total target NF is realized when 9 dB of a CMOS down-converter is achieved.

To realize a CMOS down-converter IC for mass-production, integrating an RF-amplifier (RF-AMP), a mixer and an IF variable gain amplifier (IF-VGA) are focused. In addition, a temperature compensated variable gain amplifier (TC-VGS) is also described for realizing constant conversion gain. Table 4.1 summarizes the target specification of CMOS down-converter IC for mass-production. The

variable step conversion gains of 42 dB, 38 dB, 34 dB and 30 dB, 9 dB or less of NF, an output third-order intercept point (OIP3) exceeding +10 dBm for all gain setting and constant conversion gain under variations in temperature are important specifications.

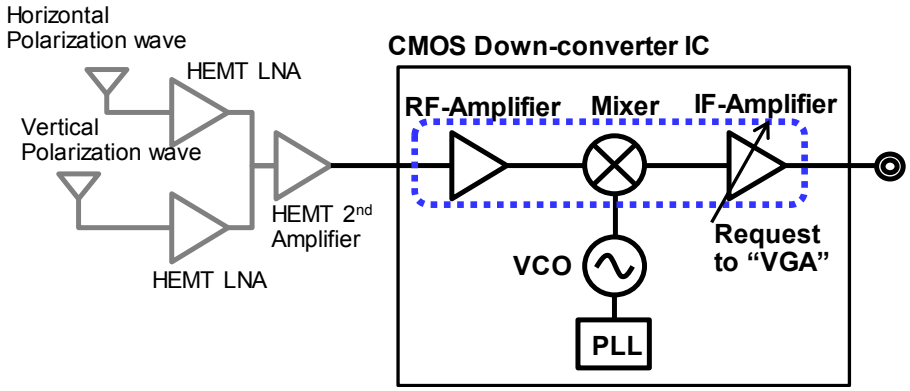


Figure 4.2: Simplified block diagram of LNB down-converter with a CMOS down-converter IC

Table 4.1: Target specification of CMOS down-converter IC

Parameter	Target specifications
Process	CMOS 130 nm
Architecture	Direct-Conversion
Supply voltage	3.3 V
IC current consumption	50 mA or smaller
IC input frequency	10.7 GHz – 12,75 GHz
IC output frequency	950 MHz – 2150 MHz
Conversion gain	42, 38, 34, 30 dB adjustable (4dB step gain set in manufacturer)
Gain variation under -30℃ to 90℃	3dB or less
IC NFssb	9dB
Output IP3	+10dB @ 75Ω load
S22	< -10 dB @ 75Ω load

4.2 RF-Amplifier and Mixer

4.2.1 Previous Techniques ~Noise-Canceling LNA~

CMOS LNAs are used in various integrated receiving systems. Common CMOS receiver require LNAs with sufficiency large gain, low NF, adequate linearity and source impedance matching $Z_{IN} = R_S$ with operating frequency.

The noise-canceling architecture [3] - [6] is proved to be effective for improving the NF of conventional wide-band LNAs. Figure 4.3 shows the basic single-to-differential noise-canceling LNA [4]. The common-gate (CG) FET (M_1) stage realizes a wideband impedance matching $Z_{IN}=1/gm_{M1}$, whereas the common-source (CS) FET (M_2) stage senses the voltage signal and noise across the input source. For $Z_{IN} = R_S$, the input noise voltage is $I_{n,i} \times R_S$ due to the noise current $I_{n,i}$ of the impedance matching CG FET (shown in Figure 4.3 (a)). The noise voltage of the output node, Voutp is

$$\mathrm{Voutp}_{,n} = I_{n,i} \times R_1 \quad \cdots (4.1)$$

and the noise voltage of the output node, Voutm, is

$$\mathrm{Voutm}_{,n} = I_{n,i} \times R_S \times gm_{M1} \times R_2 \quad \cdots (4.2)$$

therefore the noise cancellation condition in Figure 4.3 (a) is

$$\mathrm{Voutp}_{,n} = \mathrm{Voutm}_{,n}$$

from (4.1) and (4.2),

$$\mathrm{R}_1 = gm_{M1} \times R_S \times R_2 \quad \cdots (4.3)$$

On the other hand, the signal voltage at node Voutp and Voutm have opposite sign in Figure 4.3 (b). The circuit is employed to cancel the noise and distortion due to the CG FET. The CG FET and CS FET produce differential outputs with the common-mode noise. In this way, the noise canceling LNA can achieve wideband, low-NF and single-to-differential signal conversion.

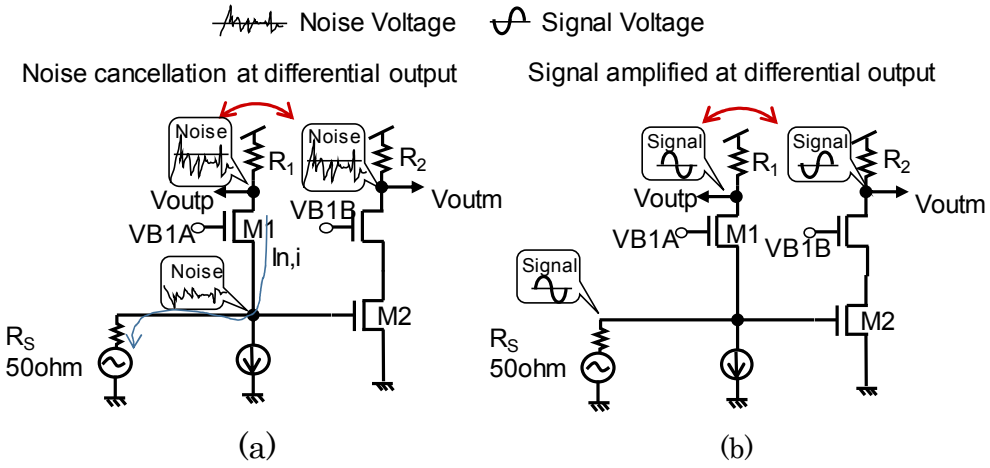


Figure 4.3: Basic noise-canceling CMOS LNA
(a) noise and (b) signal voltages at nodes, Voutp and Voutm.
(Single-to-differential. Bias not shown)

4.2.2 Previous Techniques ~Mixer~

The "BLIXER" was proposed for achieving a higher-frequency operation [6]. BLIXER is a merged current-commutating mixer with a single-to-differential noise-canceling LNA as shown in Figure 4.4. To operate a higher frequency, the real part of the impedance of all RF nodes is kept low, and the voltage gain is not created at RF but in a baseband after the mixing stage where capacitive loading is not harmful. Both the CG and the CS side have now two cascode (or mixer) transistors, which are periodically switched on and off, with LO frequency. In [6], BLIXER achieves high-frequency operation (~7 GHz) without on-chip inductors fabricated by CMOS 65-nm process.

I first tried the architecture of BLIXER to RF-AMP and mixer with a CMOS 130-nm process, however, I found by simulations that I cannot reach the 10-GHz band target performance. Figure 4.5 shows the simulated results of conversion gain and NF, where output frequency is 950 MHz and LO frequency is RF - 950 MHz, R_1 and R_2 are 100 Ω and 25 Ω, respectively. Since the output is in

L-band, (not the baseband), and gate capacitance of CS FET, the extracted capacitances of on-chip wires and package bonding wires are large, the investigated BLIXER is limited to less than 4-GHz frequency range because of 3-dB attenuation. In addition, the simulated conversion gain was lower than our target value (~27 dB). Therefore, I had to come up with another idea to increase the upper frequency limit and the conversion gain of RF-AMP and the mixer in addition to the use of BLIXER. The target value of RF-AMP and mixer is shown in table 4.2.

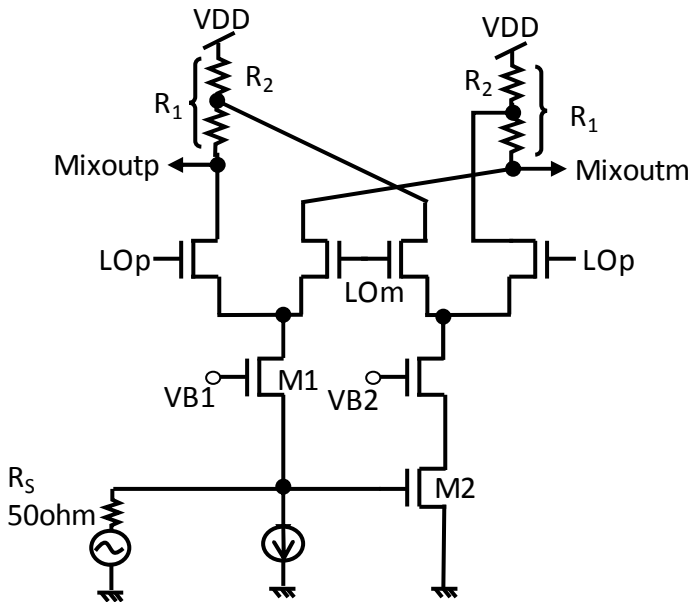


Figure 4.4: Schematic of BLIXER
(Single-to-differential. Bias not shown).

Table 4.2: Target values of RF-AMP and mixer.

Parameter	Value
RF signal input	10.7 GHz – 12.75 GHz
LO Frequencies	Low Band: 9.75 GHz High Band; 10.6 GHz
IF signal output	950 MHz – 2150 GHz
Conversion Gain	27 dB
SSB Noise Figure	9 dB
Input IP3	-15 dBm @ 50 Ω load
S11	-6 dB @ 50 Ω load
Process	CMOS 130 nm
Current Consumption	< 30 mA @ 3.3 V or less

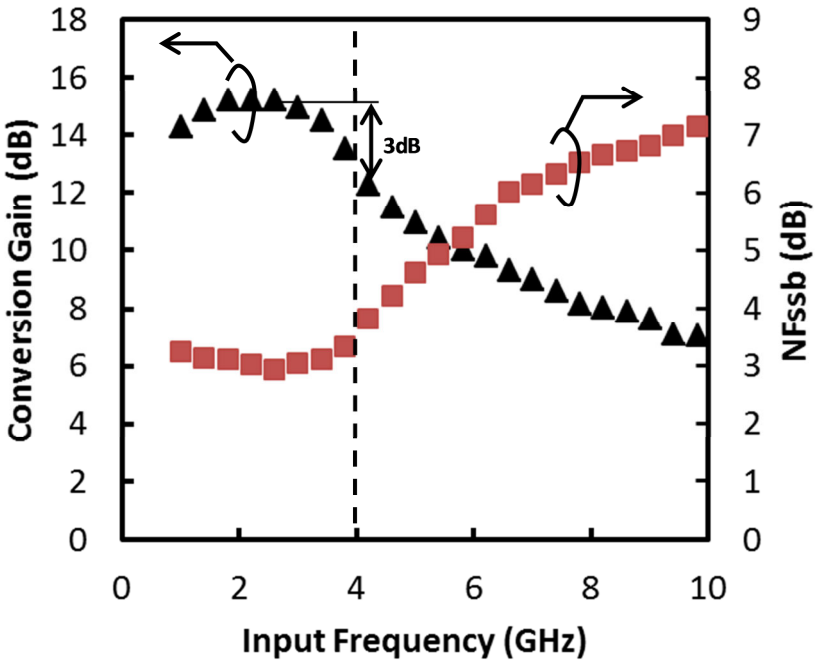


Figure 4.5: Simulated conversion gain and NF of investigated BLIXER, where output frequency is 950 MHz and LO frequency is RF - 950 MHz, R_1 and R_2 are 200Ω and 50Ω, respectively.

4.2.3 Noise Canceling LNA with LC Ladder Filter

To increase the upper frequency limit, a noise canceling LNA with an inductor load and an LC ladder filter for an input-matching network is proposed. An LC ladder filter has the characteristic similar to a transmission line, and the gain flatness in the pass-band improves as the number of sections increases. Instead of using MIM capacitors for the LC filter, we employed the gate capacitances of CS FETs resulted in a topology of a distributed amplifier [7], which can cover a wider frequency range than a conventional amplifier. The basic distributed amplifier consists of a pair of transmission lines with characteristic impedances connecting the inputs of several transistors. In this implementation, the CS FETs (M2a, M2b and M2c) consist a part of the distributed amplifier and CG FET (M1) is used as an impedance matching device.

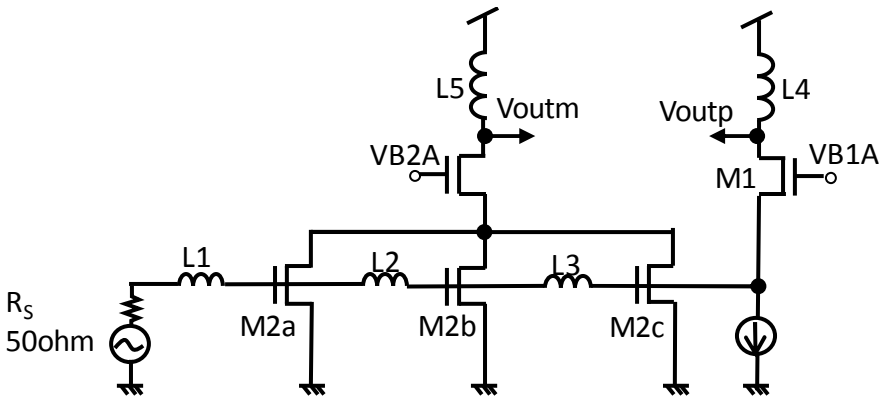


Figure 4.6: Schematic of noise-canceling RF-AMP with a fifth order L-C ladder filter

Figure 4.6 shows the proposed RF-AMP with the operating frequency range in the 10-GHz band. The proposed RF-AMP has a distributed amplifier with a fifth order LC ladder filter covering the 10-GHz band, and a CG FET with 50-Ω impedance matching. To increase the upper limit frequency to the 10-GHz band, we adopted

an LC ladder filter of 20-GHz frequency bandwidth. The CS FETs are connected in parallel, and the drains are connected to a single cascode transistor to reduce the Miller effect. The inductance of L1 is adjusted by the die position and the wire-bond length in a quad flat-pack no lead package (QFN). The inductances of L2 and L3 are adjusted with the post layout simulations. The overall gain of the distributed amplifier in the pass-band is proportional to the summation of trans- conductances.

4.2.4 Current Re-using RF-Amplifier and Mixer

To decrease the power consumption, it is effective to decrease the current consumption in a down-conversion IC because the IC supply voltage is only 3.3 V. The internal LDO does not make the clock noise compared with the DC-DC converter therefore an RF-AMP and a mixer in down-converter IC are supplied suitable voltage of 2.8 V and 1.4V from internal LDOs.

To decrease the current consumption, it is wasteful to arrange an RF-AMP and a mixer in a cascaded line. To decrease total current consumption, the current re-using technique is considered as the two-stage cascade circuits [8] - [9]. The AC-GND capacitor is implemented between the first and the second stage circuits, the current of the first and the second stage circuits is common used.

Figure 4.7 shows the proposed schematic of an RF-AMP and a mixer. The circuit generates a 27-dB voltage gain in the 10-GHz band using the inductor loads and trans-conductance stages in a Gilbert cell mixer. Moreover, a current-reusing structure to reduce the supply current consumption is implemented, which has a Gilbert cell mixer cascaded on RF-AMP. Since the supply voltage of the single conversion front-end IC is kept stable at 3.3 V using an external voltage regulator, to reduce the total current consumption. The on-chip LDO generates a 2.8-V supply voltage to the circuit. The voltage of the AC-GND node is adjusted to half of the supply voltage. The total current consumption of the RF-AMP and mixer block is 11 mA with 2.8-V supply voltage according to our simulation results.

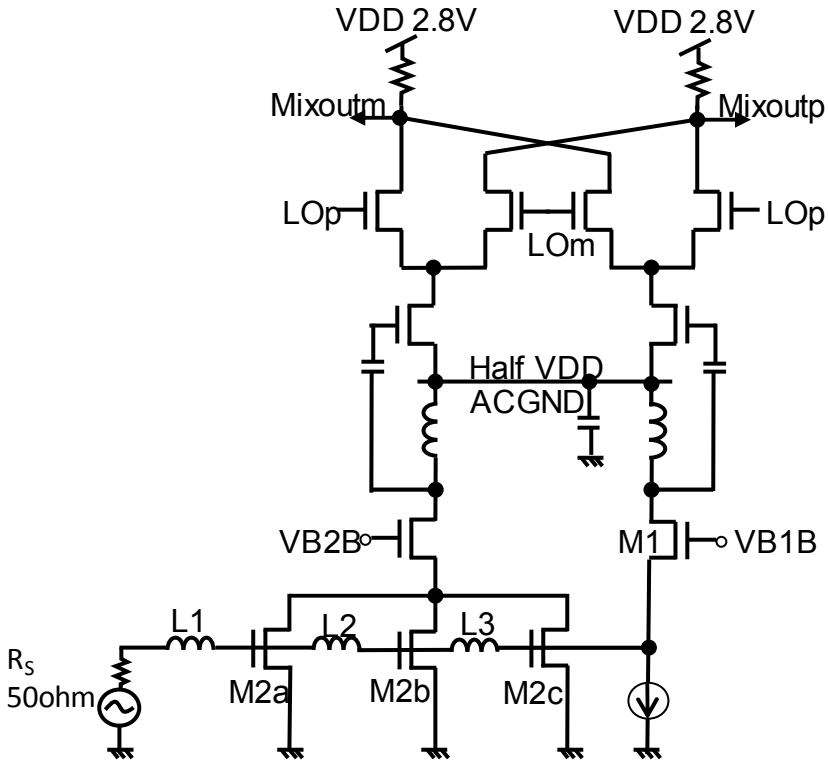


Figure 4.7: Schematic of our proposed RF-AMP and mixer (Single-to-differential. Bias is not shown)

4.3 IF-Amplifier

4.3.1 Target Specification

In a CMOS down-converter IC, a variable gain amplifier (VGA) structure is requested by LNB suppliers. A fixed conversion gain of a CMOS down-conversion IC is set when installed in a satellite antenna. The RF signal strength is different depending on the receiving location therefore LNB suppliers often must adjust the gain setting for a place of shipment. Furthermore, a constant output-3rd intercept point (OIP3) under various gain conditions is also requested. If an OIP3 is reduced in the low gain device, the receiving condition is deteriorated and a broadcasting satellite is

un-received.

In addition, a fixed conversion gain structure under the severe temperature variation is required once LNB suppliers often must adjust the gain setting. An LNB down-converter is the receiving device used in open air under the cold and hot weather areas. Therefore, the target gain variation of 3 dB or less from -30 degrees to 90 degrees is planned. Figure 4.8 shows the block diagram of the proposed IF-amplifier, which has a differential to single (D2S) buffer, a temperature-compensated VGA (TC-VGA) and a constant OIP3 VGA.

Table 4.3 shows the target specification of an IF-VGA in a CMOS down-conversion IC.

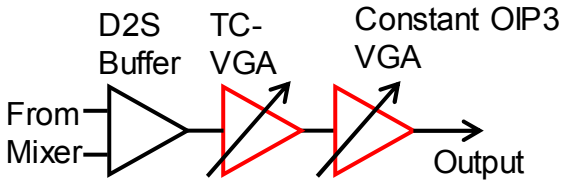


Figure 4.8: Block diagram of the proposed IF-amplifier, which has a D2S buffer, a TC-VGA and a constant OIP3 VGA.

Table 4.3: Target values of IF-VGA.

Parameter	Value
IF signal output (L-Band)	950 MHz – 2150 MHz
Conversion Gain	15 dB, 11 dB, 7 dB, 3 dB
Gain variation at -30℃ to +90℃	3 dB or less
OIP3	+10 dB or more @ all gain settings
S22	-10 dB @ 75 Ω load
Process	CMOS 130 nm
Current Consumption	< 30 mA @ 3.3 V or less

4.3.2 Conventional VGA

The conventional VGAs operating from 950 MHz to 2150 MHz are designed using current steering circuits with analog bias control [8] - [11] as shown in Figure 4.9 (a) or digital control [12] - [13] as shown in Figure 4.9 (b). For these configurations, the distortion components produced at the transconductor stage are constant against gain variation and thus the IF-VGAs follow the constant input-3rd intercept point (IIP3) principle. When a VGA is expected to receive a desired signal A together with large interfered signal B as shown in Figure 4.10, LNB suppliers decrease the gain setting during manufacturing assuming. The desire signal (A→C) and the 3rd distortion of interfered signal (E → F) when gain reduces. However the pair (desired, distortion) of (A, E) to (C, F) does not improve even if a VGA gain is decreased.

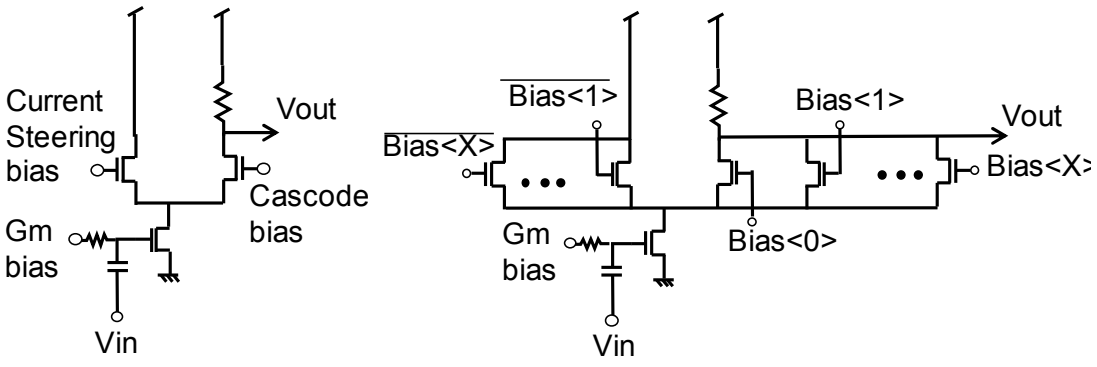


Figure 4.9: Schematics of current steering VGAs with analog bias control (a), and digital bias control (b).

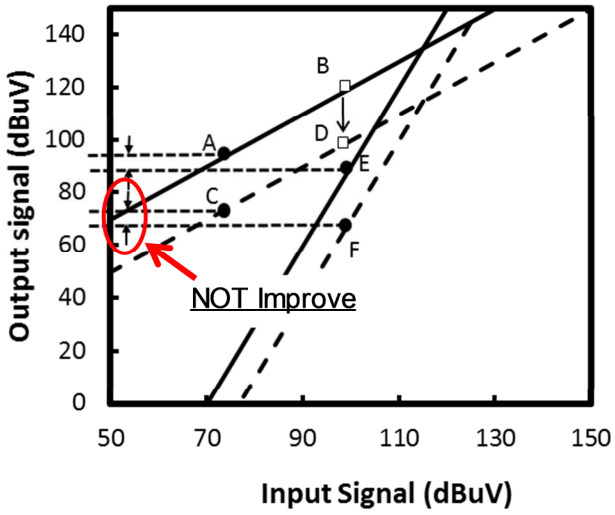


Figure 4.10: Plots of desired and 3rd distortion signals with current steering structures.

4.3.3 Gate-Width Controlled CMOS VGA

Conventional CMOS VGAs using a current-steering structure did not have a constant OIP3 property and the IF output signal was distorted upon receiving a 10-GHz band signal with large amplitude. In [14], the concept of a gate-width-controlled CMOS RF-amplifier was proposed, which is applicable to a CMOS down-converter IC in an LNB down-converter. A constant OIP3 property is shown in Figure 4.11, the desire signal (A' → C') and the 3rd distortion of interfered signal (E' → F'). The difference of (C', F') is wider than (A', E').

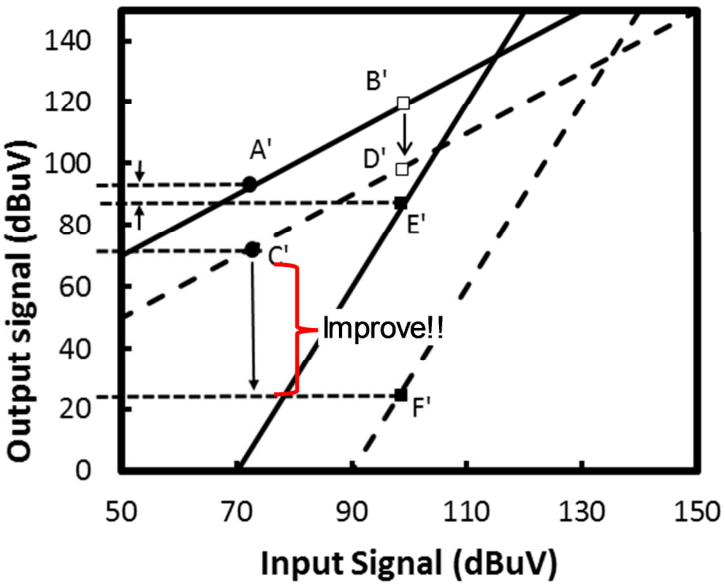


Figure 4.11: Plots of desired and 3rd distortion signals with a constant OIP3 property.

To analyze the nonlinearity of IF-VGA, the basic Shockley MOS model is used for the drain current in the saturation region using the α-power square-law model,

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^{\alpha} \quad \cdots(4.4)$$

Here, μ, C_{OX}, W, L, V_{GS} and V_{TH} denote the carrier mobility, gate oxide capacitance, gate width, gate length, gate-source voltage and threshold voltage, respectively. Also, we define the overdrive voltage V_{OD} as $V_{OD} = V_{GS} - V_{TH}$. By taking derivatives of (5.4), we have

$$gm = \frac{1}{2}\alpha\mu C_{OX}\frac{W}{L}V_{OD}^{\alpha-1} \quad \cdots(4.5)$$

$$gm' = \frac{1}{2}\alpha(\alpha-1)\mu C_{OX}\frac{W}{L}V_{OD}^{\alpha-2}$$

and

$$gm'' = \frac{1}{2}\alpha(\alpha-1)(\alpha-2)\mu C_{OX}\frac{W}{L}V_{OD}^{\alpha-3} = \frac{\alpha(\alpha-1)(\alpha-2)I_{DS}}{V_{OD}^{3}} \quad \cdots$$

(4.6)

The gain of the amplifier, Gain, is described as a function of gm and R_L as

$$\text{Gain} = \text{gm} \cdot \text{R}_\text{L} = \frac{\alpha I_{DS} R_L}{V_{OD}}. \qquad \cdots(4.7)$$

The transfer function can then be expressed as a Taylor series around the bias point,

$$\text{I}_\text{DS} = \text{gm} \cdot \text{V}_\text{OD} + \frac{1}{2}\text{gm}' \cdot \text{V}_{OD}^2 + \frac{1}{6}\text{gm}'' \cdot \text{V}_{OD}^3 + \ldots$$

Then the peak signal IIP3 is given by

$$\text{IIP3}_\text{peak} = \sqrt{\frac{4\text{gm}}{3\text{gm}''/6}} = \sqrt{\frac{8\text{gm}}{\text{gm}''}} = \frac{2V_{OD}\sqrt{2}}{\sqrt{(\alpha-1)\,|\,\alpha-2\,|}}$$

and the RMS voltage IIP3 is given by

$$\text{IIP3rms} = = \frac{2V_{OD}}{\sqrt{(\alpha-1)\,|\,\alpha-2\,|}} \qquad \cdots(4.8)$$

The RMS voltage OIP3 is obtained from (4.7) and (4.8) as

$$\text{OIP3}_\text{rms} = = \frac{2\alpha \cdot I_{DS} R_L}{\sqrt{(\alpha-1)\,|\,\alpha-2\,|}} \qquad \cdots(4.9)$$

The equations (4.7) and (4.9) indicate that we can realize the values of variable gain and constant OIP3 by adjusting the overdrive voltage V_{OD} through changing the gate width while maintaining the bias current I_{DS} constant.

Figure 4.12 shows these results by comparing calculation and simulation results using simple single-ended transistor models, where α and $I_{DS} \times R_L$ are 1.3 and 0.75 V, respectively. The gap of about 6 dB in OIP3 arises from the nonlinearity of the output impedance (75 Ω). Since $I_{DS} \times R_L/2$ is 0.375 V with 75-Ω matching, the maximum achievable output 1-dB compression point (P1dBout) is calculated as 3 dBm. Therefore, OIP3 is about 12 dBm at 75 Ω. This effect is not included in the simple model (4.4).

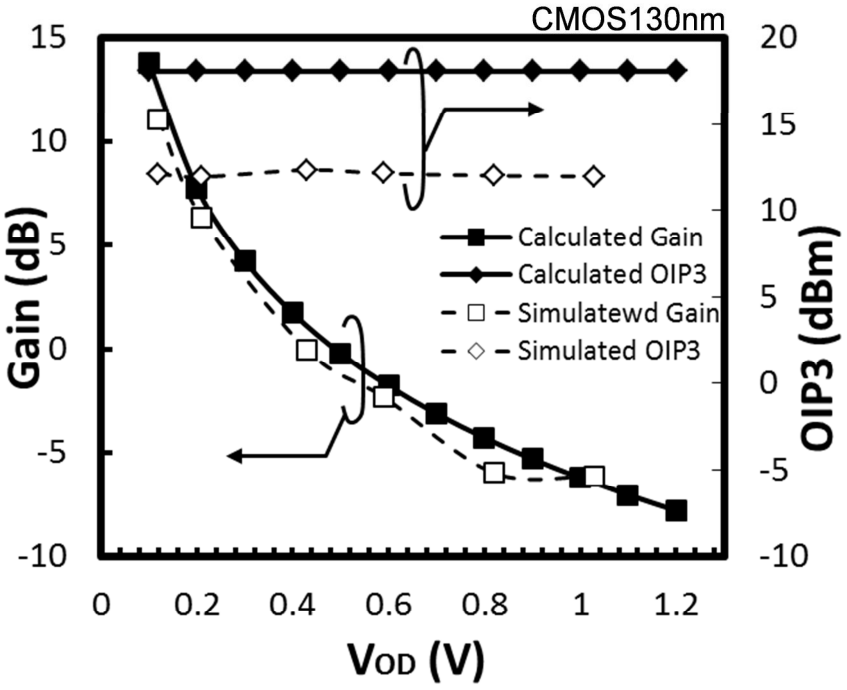


Figure 4.12: Plots of calculation and simulation results using simple single-ended transistor models

The proposed digitally controlled CMOS IF-VGA is shown in Figure 4.13, where the block diagram is shown in (a), the first amplifier in (b) and the second amplifier in (c).

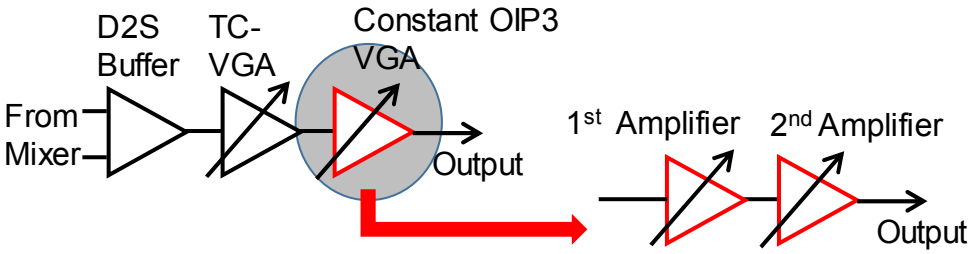
The differential signal from the mixer output is converted to a single-end signal in the differential to single-end (D2S) buffer. If the differential signal from the mixer has the phase-shift or the amplitude difference, the D2S buffer generates a DC-offset or a second harmonic. However, since the phase-shift and the amplitude difference are marginal, the DC-offset and second harmonic have a negligible impact on the single conversion front-end operation.

The voltage of $I_{DS} \times R_L$ of the first amplifier is set to 0.66 V and the second amplifier is set to 0.75 V. In these cases, the calculated values of OIP3 of the single transistors are 22.5 dBm on the first amplifier and 23.5 dBm on the second amplifier with 75-Ω matching. Therefore, if $I_{DS} \times R_L$ is larger than 0.75 V, the nonlinearity of the transistors has a negligible impact on the OIP3 of the IC.

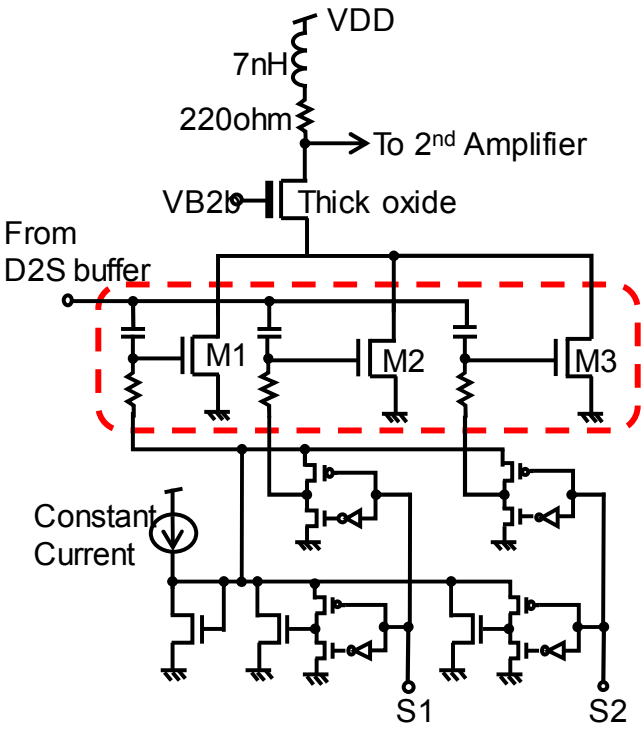
By turning the switch transistors on and off digitally, the effective

gate width W of the transconductance is controlled. Our target gain step is approximately 4 dB. In the case of maximum gain, all the switches are on. To decrease the gain, the number of on switches is decreased. To maximize the voltage headroom of the transconductance transistor using thin-oxide devices with smaller gate capacitances, thick-oxide transistors are used as cascode devices. With this technique, the voltage of 2.8-V supply voltage by the on-chip LDO can be used to increase V_{DS} for higher OIP3.

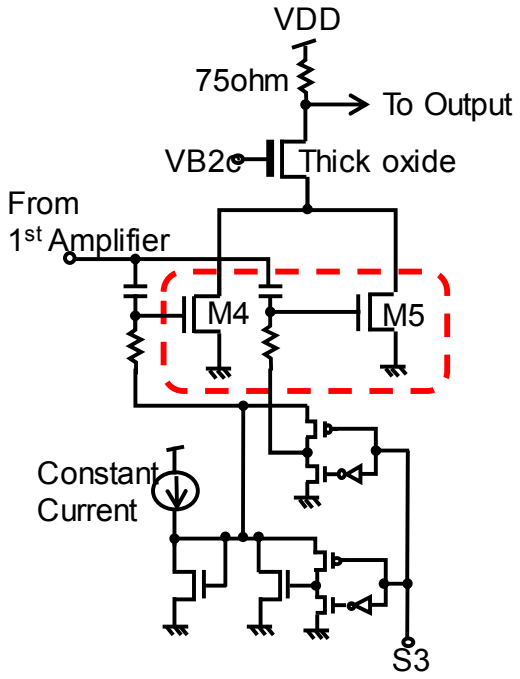
Figure 4.14 shows the simulation results of the proposed digitally controlled IF-VGA, the flatness of OIP3 is maintained for various gain setting at the output frequency of 1.5 GHz



(a)



(b)



(c)

Figure 4.13: Block diagram of a constant OIP3 VGA (a) and schematics of the first amplifier (b) and the second amplifier (c).

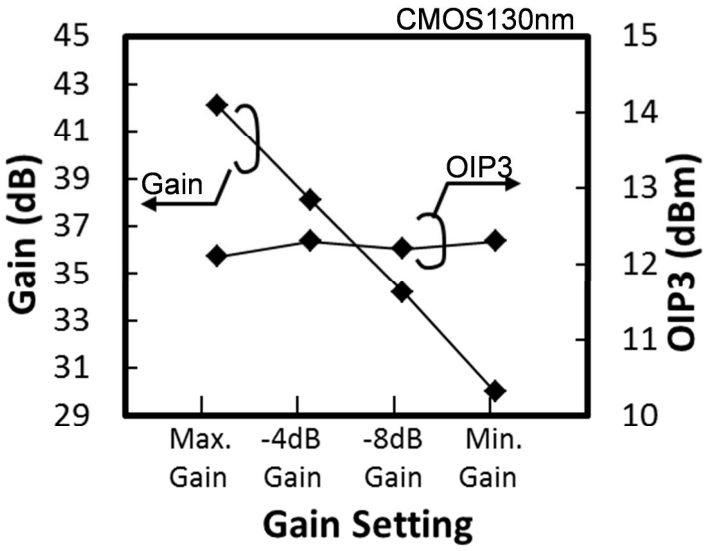
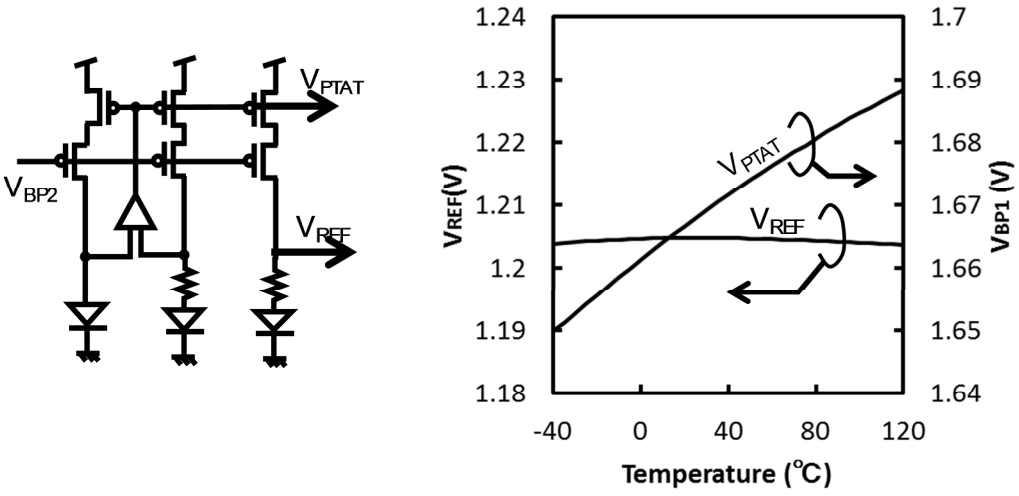


Figure 4.14: Simulated results of OIP3 and Gain for various gain conditions

4.3.4 TC-VGA

The gain of a common open-loop CMOS amplifier is followed by a temperature variation because the transconductance of an NMOS transistor has a temperature coefficient. The gain variation from -30 degrees to 90 degrees is 3 dB or less, and only a constant-gm bias circuit is insufficient to achieve the target specification. Therefore, a temperature compensated VGA is proposed. Figure 4.15 (a) shows a schematic of a conventional band-gap reference (BGR) circuit, which produces an output voltage that is traceable to fundamental constants due to temperature variation. The temperature coefficient of the diode is independent of the temperature and equal to about -2 mV/K. This linear decrease in the voltage of the diode referred to as being complementary to absolute temperature (CTAT). If a voltage that is proportional to absolute temperature (PTAT) is added to the CTAT voltage, the sum of the voltages will be independent of temperature. Figure 4.15 (b) shows the simulation results of the sum voltages of CTAT and PTAT voltages, which is used as a reference voltage (V_{REF}).



(a) (b)

Figure 4.15: Schematic of the conventional BGR circuit (a) and simulation results of V_{REF} and V_{PTAT} (b).

Figure 4.16 shows the schematic of a TC-VGA circuit core consisting of the current-steering VGA. By adjusting bias voltages between a VB2A and a VB2B, the amplifier's gain is adjusted by current control. The voltages of VB2A and VB2B are determined by V_{REF} and the PTAT voltage V_{PTAT}. At low temperature, the current of the transistor M2A is decreased to decrease the gain. Conversely at high temperature, the current of the transistor M2A is increased to increase the gain.

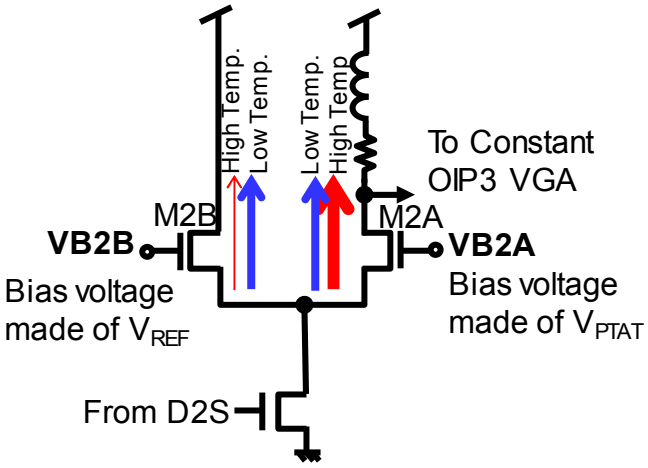


Figure 4.16: schematic of a TC-VGA circuit core consisting of the current-steering VGA.

4.3.5 Measurement Results

A CMOS down-conversion IC are implemented in a 1P5M 130-nm RF-CMOS process with MIM capacitor and deep N-well structure. In the fabricated IC, the proposed circuits (an RF-amplifier, a mixer and an IF-VGA), occupies 0.9 mm × 0.5 mm die area and consumes a current of 27 mA with 2.8-V supply voltage. A 2.8-V supply voltage is generated by an on-chip LDO. A die photograph is shown in Figure 4.17.

Figure 4.18 shows the measured conversion gain versus input RF frequencies. Figure 4.18 (a) shows the conversion gain at the 9.75-GHz LO frequency for the RF input frequency from 10.7 GHz to 11.7 GHz. Figure 4.18 (b) shows the conversion gain at the 10.6-GHz

LO frequency for the RF input frequency from 11.7 GHz to 12.75 GHz. In the target specifications, the variable gain range is from 30 dB to 42 dB, the gain step is about 4 dB, and the gain flatness of the desired frequency band is 3 dB.

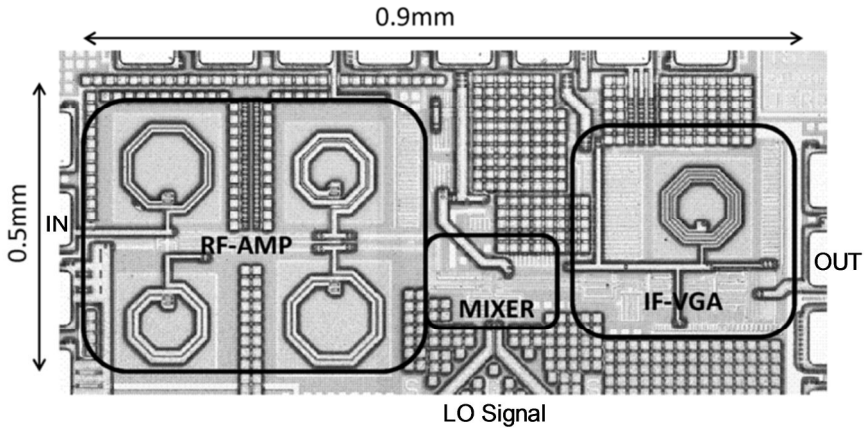


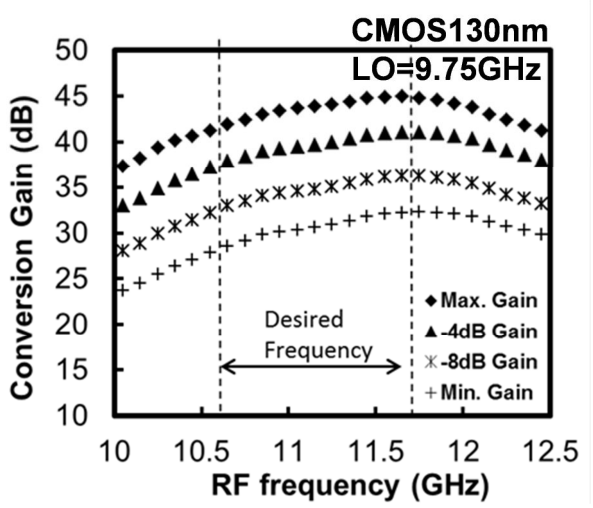
Figure 4.17: Die photograph of an RF-amplifier, a mixer and an IF-VGA

Figure 4.19 shows the plot of the conversion gain under variations in temperature at the gain setting of 30 dB and the 9.75-GHz LO frequency for the RF input frequency from 10.7 GHz to 11.7 GHz. The gain variation of 3 dB or less is achieved under variations in temperature from -30 degrees to 90 degrees.

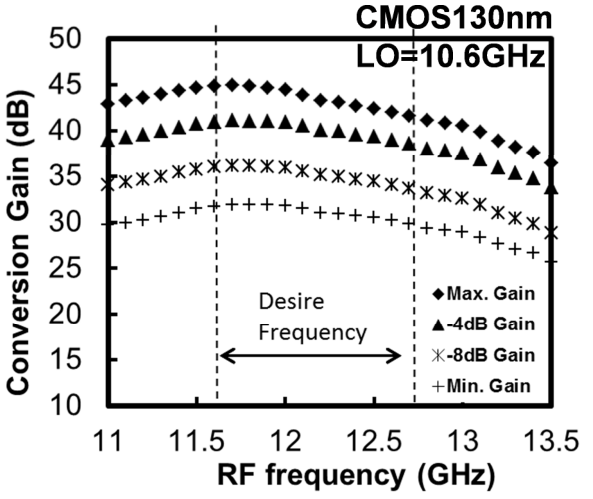
Figure 4.20 shows the measured OIP3 for various gain settings at the output frequency of 1.5 GHz and the LO frequency of 9.75 GHz. The constant OIP3 of 11 dBm is achieved under variations in conversion gains from 30 dB to 42 dB.

Figure 4.21 shows the measured single side-band noise figure (NFssb) versus IF output frequency for various gain settings. Figure 4.21 (a) shows the NFssb at the LO frequency of 9.75 GHz and Figure 4.21 (b) shows the NFssb at the LO frequency of 10.6 GHz. The NFssbs of below 9 dB are achieved under variations in conversion gains. Note that the maximum gain results in the worst NFssb of 9 dB. This is attributed to the low dynamic range of our NF meter.

Figure 4.22 shows the measured S11 (Figure 4.22 (a)) and S22 (Figure 4.22 (b)) versus frequency. Measured S11 is –7 dB or less and S22 is –17 dB or less. A comparison of the 10-GHz band integrated receiver block performance with previously published results is shown in Table 4.4.



(a)



(b)

Figure 4.18: Plots of measured gain versus input RF frequencies, at the 9.75-GHz LO (a) and the 10.6-GHz LO (b) frequencies.

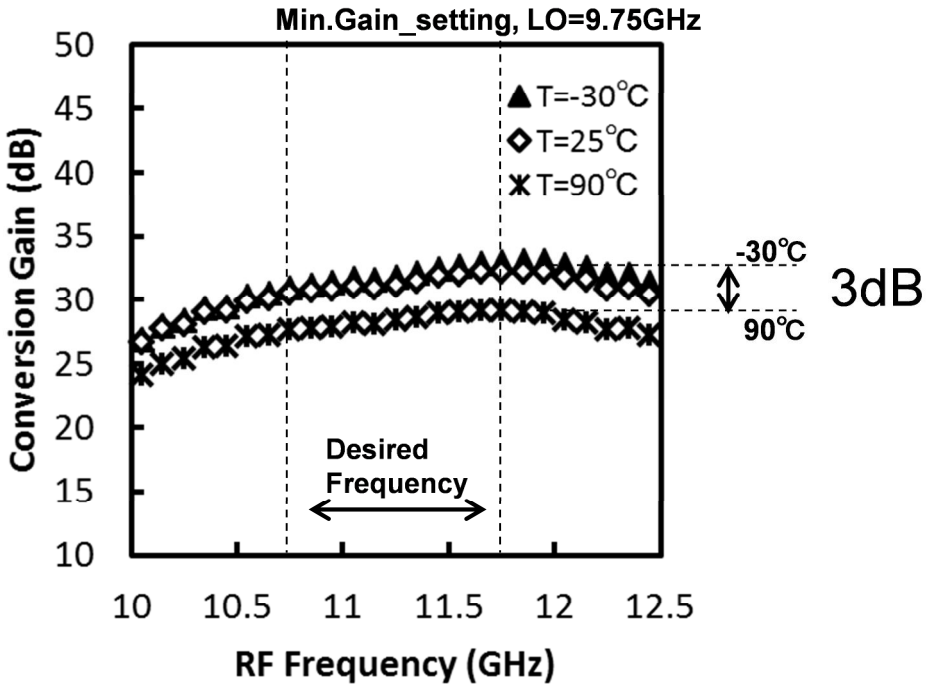


Figure 4.19: Plots plot of the conversion gain set to 30 dB under variations in temperature, and the 9.75-GHz LO frequency for the RF input frequency from 10.7 GHz to 11.7 GHz

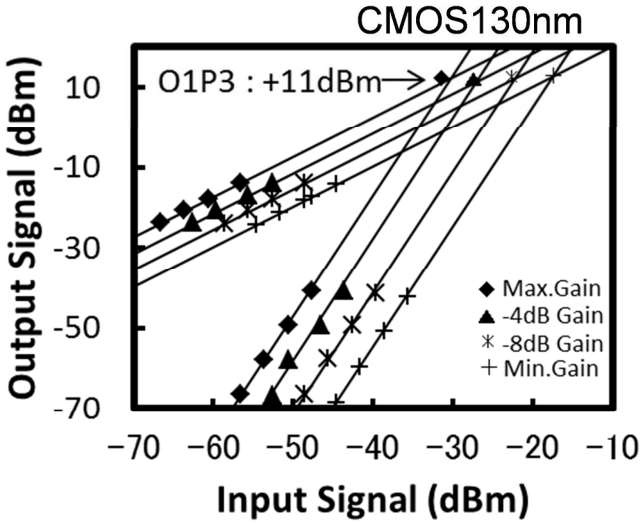
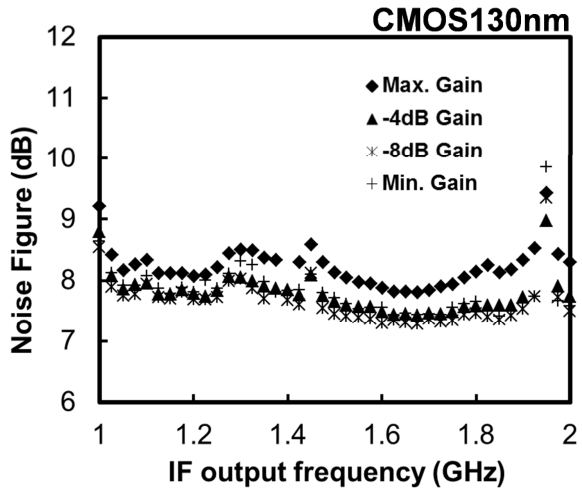
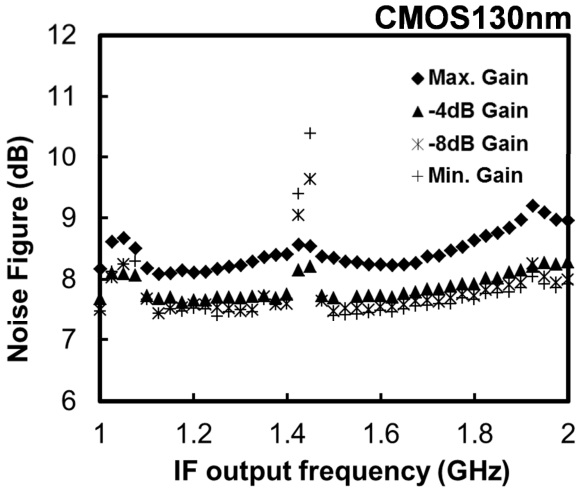


Figure 4.20: Plots of measured OIP3 under variations in conversion gains

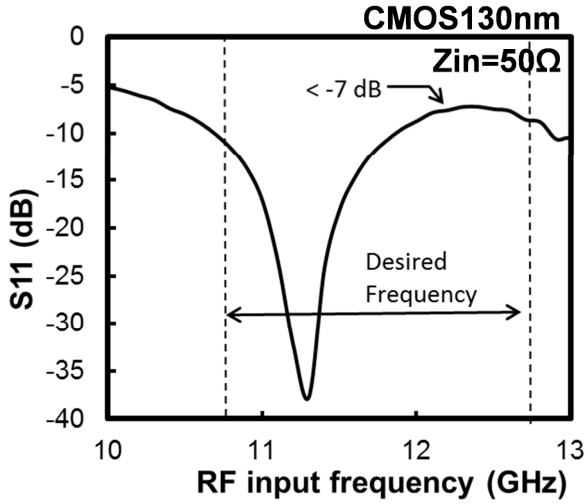


(a)

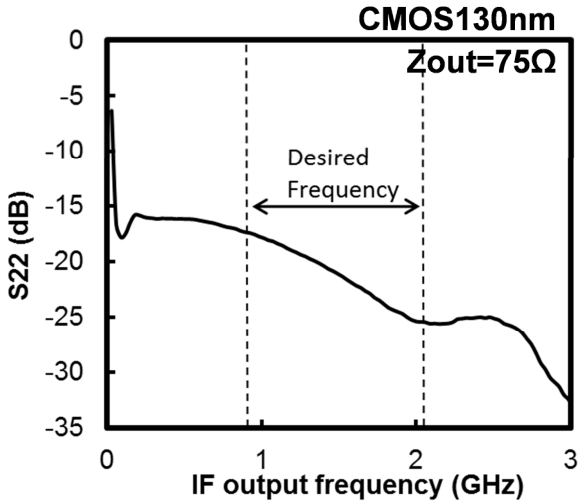


(b)

Figure 4.21: Plots of measured NFssbs versus IF frequencies, at the 9.75-GHz (a) and the 10.6-GHz (b) LO frequencies.



(a)



(b)

Figure 4.22: Plots of the measured S11 (a) at the 50-Ω impedance, and S22 (b) at the 75-Ω impedance

Table 4.4: Comparison of the 10-GHz band integrated receiver block (RF-AMP, mixer and IF-AMP) performance

	[1]	[15]	This work
Technology	0.8 μm BJT	0.18 μm CMOS	0.13 μm CMOS
Current / voltage	38 mA / 3.3 V	75 mA / 1.8 V	27 mA / 2.8 V
Conversion gain	34 dB	50 dB	42, 38, 34, 30 dB
Gain variation -30℃~ 90℃	4 dB	4 dB	3 dB
SSB Noise Figure	9 dB	4.2 dB	9 dB
OIP3	15 dBm	17 dBm	11 dBm
Die area	4×2.5mm (w/ PLL)	0.9× 1.8mm	0.9× 0.5mm

4.4 Conclusion

To realize the CMOS down-converter IC for broadcasting satellite with the lower current consumption, a constant OIP3 VGA structure at all gain setting and constant gain variation from -30 degrees to 90 degrees, a 10-GHz band noise-canceling LNA, a current reusing RF-amplifier and a mixer, a constant OIP3 IF-VGA and a temperature compensated VGA (TC-VGA) were proposed. These circuits are implemented in CMOS 130-nm process and total current consumption is 27 mA at 2.8-V supply voltage.

To operate a 10-GHz band RF-amplifier and a mixer using CMOS 130-nm process, a noise-cancelling LNA with the distributed amplifier using the LC-ladder filter was proposed. Furthermore, the current re-using RF-amplifier and mixer were proposed for lower current consumption. The on-chip LDOs generate a 2.8-V supply voltage and a 1.4-V AC-GND voltage to these circuits. The total

current consumption of the RF-amplifier and mixer is 11 mA with 2.8-V supply voltage according to the simulation results.

To obtain a constant OIP3 VGA at all gain setting, a digitally controlled gate width VGA was proposed. By turning the switch transistors on and off digitally, the effective gate width of the transconductance is controlled. 4-dB gain step and +11 dBm OIP3 at all gain setting were achieved.

To realize the constant gain under variations in temperature, a TC-VGA was proposed. It is current steering VGA which has bias voltages compared with a PTAT voltage and a temperature constant voltage. To realize a proposed CMOS down-converter IC with an RF-amplifier, a mixer and an IF-VGA, 3-dB gain variation under the temperature of -30 degrees to 90 degrees was proposed for a mass-production broadcasting satellite.

References of Chapter 4

[1] T. Copani, S. A. Smerzi, G. Girlando, and G. Palmisano, "A 12-GHz Silicon Bipolar Dual-Conversion Receiver for Digital Satellite Applications", IEEE J. of Solid-State Circuits, Vol. 40, No. 6, June 2005, pp.1278-1287

[2] P. Philippe, L. Praamsma, R. Breunisse, E van der Heijden, F. Meng, S. Bardy, F. Moreau, S. Wane, E. Thomas, "A low power 9.75/10.6GHz down-converter IC in SiGe:C BiCMOS for Ku-band satellite LNBs", in Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011, pp.211-214.

[3] F. Bruccoleri, E.A.M. Klumperink, B. Nauta, "Noise Cancelling in Wideband CMOS LNAs", in Proc. IEEE International Solid-State Circuits Conference (ISSCC) 2002, 24.6, pp.406-407.

[4] Bruccoleri F., Klumperink, E.A.M. and Nauta, B. "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling", IEEE J. of Solid-State Circuits, Vol. 39, Feb. 2004 pp. 275-282

[5] Wei-Hung Chen, Gang Liu, Boos Zdravko, and Ali M. Niknejad. "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation", IEEE J. of Solid-State Circuits, Vol. 43, May. 2008 pp. 1164-1176

[6] Blaakmeer, S.C., Klumperink, E.A.M., Leenaerts, D.M.W., Nauta, B. "The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology", IEEE J. of Solid-State Circuits, Vol. 43, Dec. 2008 pp. 2706-2715.

[7] Brian M. Ballweber, Ravi Gupta and David J. Allstot, “A Fully Integrated 0.5?5.5-GHz CMOS Distributed Amplifier”, IEEE J. of Solid-State Circuits, Vol. 35, Feb. 2000, pp. 231-239.

[8] Jianhong Xiao, IuriMehr, Jose Silva-Martinez: “A High Dynamic Range CMOS Variable Gain Amplifier for Mobile DTV Tuner”, IEEE J. Solid-State Circuits, vol.42, No.2, Nov. 2007, pp.292-301.

[9] Weinan Gao, Kendal Hess, Ray Rosik, Mark Santini, Mats Lindstrom, Jason McFee and Jacek Czajka, “A Fully Integrated Dual Broadband Direct Conversion Tuner Chip for Digital Satellite TV Applications”, in Proc. IEEE Custom Integrated Circuits Conference (CICC) 2005, pp.353-356.

[10] Vincent Leung, Lawrence Larson and Prasad Gudem, “Digital-IF WCDMA Handset Transmitter IC in 0.25μm SiGe BiCMOS”, in Proc. IEEE International Solid-State Circuits Conference (ISSCC) 2004, pp.182-521.

[11] Larry Connell, Neal Hollenbeck, Mike Bushman, Dan McCarthy, Steve Bergstedt, Ron Cieslak, Jim Caldwell, “A CMOS Broadband Tuner IC”, in Proc. IEEE International Solid-State Circuits Conference (ISSCC) 2002, pp. 324-529.

[12] M. Koutani, H. Kawamura, S. Toyoyama and K. Iizuka: “A Digitally Controlled Variable-Gain Low-Noise Amplifier With Strong Immunity to Interferers”: IEEE J. Solid-State Circuits, vol.42, No.11, pp.2395-2403. Nov. 2007.

[13] Fei Song, Huailin Liao, Jiang Chen, Le Ye, Huaizhou Yang, Junhua Liu, Jinshu Zhao and Ru Huang: “A 1.8-V CMOS Direct-Conversion Tuner for Mobile DTV Applications” in Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC) 2008, pp. 353-356.

[14] K. Iizuka, M. Koutani, T. Mitsunaka, H. Kawamura, S. Toyoyama, M, Miyamoto, and A. Matsuzawa: “RF Variable-Gain Amplifiers and AGC Loops for Digital TV Receivers”, IEICE Trans. Electronics, VOL. E91-C, No.6, pp.854 ? 861, Jun. 2008.

[15] Zhiming Deng, Jiashu Chen, Jason Tsai, Ali M. Niknejad: “A CMOS Ku-Band Single-Conversion Low-Noise Block Front-End for Satellite Receivers”, in Proc. Radio Frequency Integrated Circuits (RF-IC) Symposium 2009, pp. 135-138.

Chapter 5. Conclusion

5.1 Research Outcome

In the beginning of this research, the outline of satellite applications, the significance of CMOS down-converter IC, the target specifications and the manufacturing issues were introduced. The satellite antennas are constructed in open air. In particular, a down-converter for a broadcasting satellite requires higher reliability under variations in temperature. In this study, a constant conversion gain and a wide range of operations was focused on a broadcasting satellite. In addition, a CMOS PLL synthesizer for satellite applications such as radio astronomy that operates at frequency of over 100 GHz was described. It will be capable of using ultrahigh-speed transceivers used in not only radio astronomy but also sensors and medical applications. Figure 5.1 shows a block diagram of a CMOS down-converter IC and main subjects in each chapter.

In chapter 2, the techniques used in the integer-N-type PLL synthesizer for a CMOS down-converter IC with a range of 10-GHz and high-frequency circuits operating at frequencies exceeding 100-GHz were described. In a 10-GHz-band down-converter IC for a broadcasting satellite, each circuit requires a small size, a low noise

and low power consumption. In addition, a higher reliability of operation is required to ensure the temperature tolerance necessary for open air. In this study, a 1-inductor VCO with switching varactors could achieve a wide range of operation and a low phase noise for solving the trade-off issues.

In a 100-GHz-band on-chip PLL synthesizer, a VCO and dividers for a 134 GHz PLL synthesizer were described. The dividers have ILFDs which are used in the tuning of back-gate voltage to increase the operation range of divide-by-two. The developed LC-VCO has a fundamental oscillation range of 131.8 GHz to 134.3 GHz, which is controlled by the variable back-gate voltage. The dividers can cover the entire VCO oscillation range. When the PFD, CP and LF are operated, it will be possible to operate the 134-GHz on-chip PLL synthesizer..

In chapter 3, CMOS full-differential dual-modulus prescalers in integer-N-type PLLs were described. In the integer-N-type PLL, the dual-modulus prescalers must operate a low power consumption, high-frequency and a wide frequency of locking range. In this research, the first prescaler fabricated by in the CMOS 130-nm process was successfully operated in a range of 4 GHz to 6 GHz indicating its temperature tolerance. The other prescaler fabricated by the CMOS 65-nm process was successfully operated in a range of 22 GHz to 23 GHz, and/or more a wider frequency range. The 100 % or more of operation range and the normalized energy consumption of 0.13 pJ were compared with those of previous prescalers, which showed that good performances were achieved. In addition, the tolerance of phase-difference deviation, the spurious noise and the phase noise degradation while reducing the supply voltage were checked to achieve the higher reliable prescaler,. The range of operational frequency decreases as the phase-difference deviation exceeds 90 degrees, finally reaching the range of 3.9 GHz - 7.9 GHz at 180 degrees of phase-difference deviation. A spurious noise arises and the phase noise degrades with decreasing supply voltage due to the quasi- or non-locking operation. The wide range operation and wide margin structure could be achieved in this proposed full-differential dual-modulus prescaler.

In chapter 4, CMOS amplifiers and mixer were described for a mass-production down-converter IC in a broadcasting satellite. To obtain the target frequency range of the 10-GHz band, a low-noise, low current and high-gain RF amplifier and the mixer architecture are described. Satellite applications are constructed in the open air and a constant conversion gain despite variations in the temperature is required. In this research, a TC-VGA is proposed. To maintain a linear output, a constant OIP3 IF-VGA is also proposed. The amplifiers and mixer were discussed to realize these target specifications. In particular, the achievement of target specification and 3 dB gain variation under the temperature of -30 degrees to 90 degrees were achieved and could be mass-produced. A wide range and high reliability of operation under variations in temperature could be contributed..

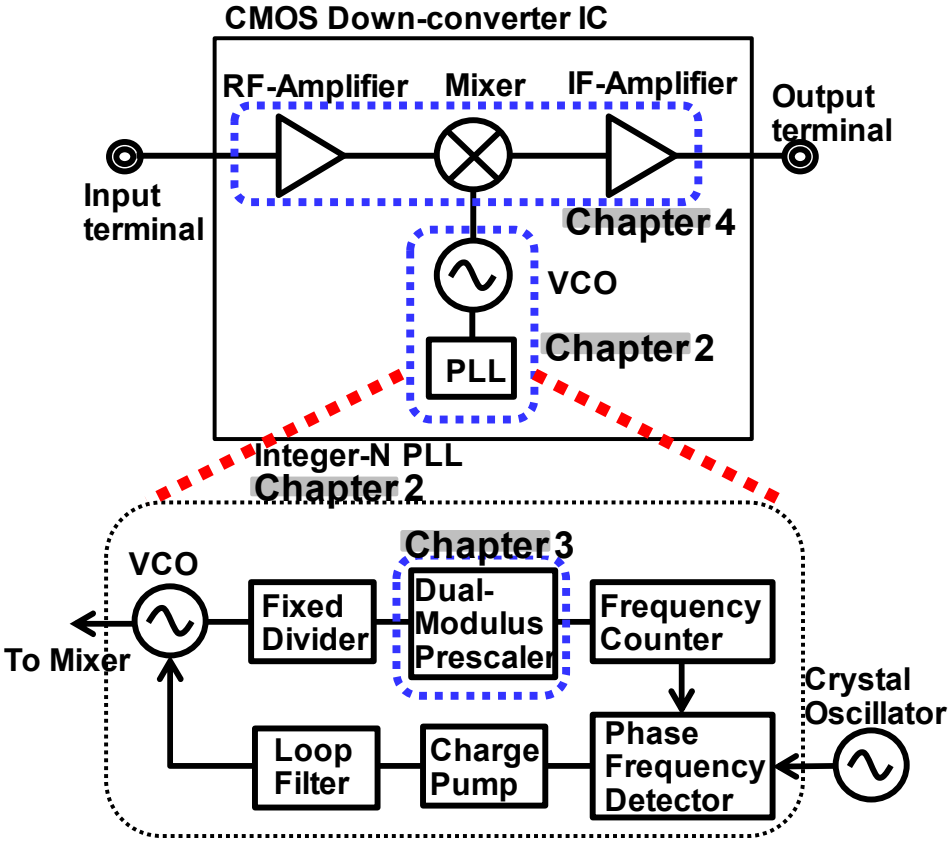


Figure 5.1: Block diagram of a CMOS down-converter IC

5.2 Author's Contribution

By studying 10-GHz-band CMOS circuits for a down-converter IC with temperature tolerance, a "single-type" LNB down-converter using a highly reliable CMOS down-converter IC for a broadcasting satellite was realized. The total shipment of the LNB down-converter using the CMOS down-converter IC studied in this research has reached to 20 million in FY 2013 and has contributed to our corporate performance.

A single-type LNB down-converter has a one-input and one-output system. The LO frequencies in a developing CMOS down-converter IC are limited to 9.75 GHz, 10.6 GHz, 10.75 GHz and 11.3 GHz. There are some types of LNB down-converter systems for various receiving areas. Now, our team is developing the CMOS "PLL-IC" for a different type of LNB down-converter, which has different LO frequencies of 9.71 GHz to 12.2 GHz, as shown in Figure 5.2. In a CMOS PLL-IC system, the amplifiers and mixer are not required but a PLL synthesizer is required. The CMOS VCO and PLL circuits proposed in this research can be used and improved in the CMOS PLL-IC being developed. Furthermore, our team plans to develop a "twin-type" LNB down-converter, as shown in Figure 5.3. A twin-type LNB down-converter has a two-input and two-output system. The detailed target specifications must be improved. However, the proposed CMOS amplifiers and mixer including the proposed CMOS VCO and PLL circuits will be contributed by this research.

In addition, by studying CMOS circuits operating at frequencies exceeding 100 GHz, such as these used radio astronomy, sensors and medical applications, a high-frequency VCO and dividers for a 134 GHz PLL synthesizer can be realized. A VCO has a 2 % oscillation range by the tuning back-gate voltage, and a divide-by-2 divider also has a wide range of operation by the tuning back-gate voltage. The proposed dividers could cover the entire VCO oscillation range, and it will be possible to operate the 134-GHz PLL synthesizer is expected by using low-frequency circuits such as a PFD, a CP, an LF. In high-frequency CMOS circuits, a wide margin

and a wide range of operation could be realized.

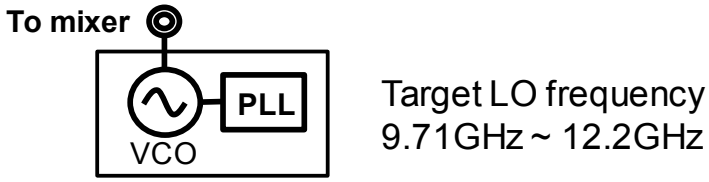


Figure 5.2: Block diagram of a PLL-IC

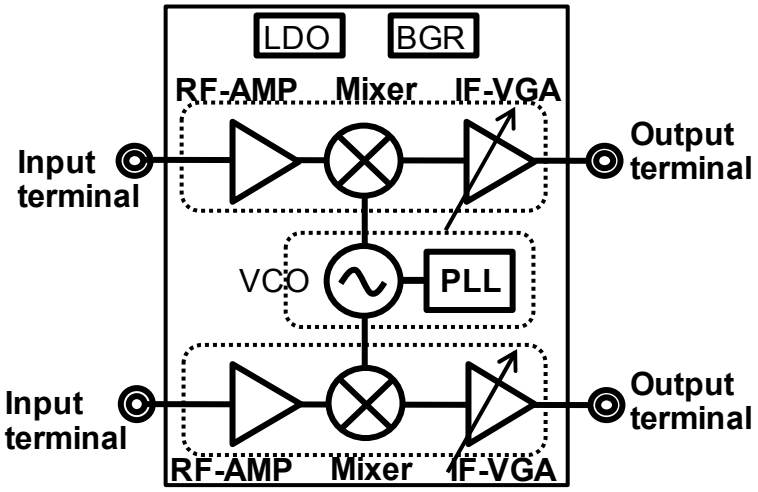


Figure 5.3: Block diagram of a "twin-type" CMOS down-converter IC

5.3 Summary of this research

In the manufacture of common wireless receivers, there are many manufacturing requests, namely, small size, low power consumption, low noise and the achievement of target specifications. In addition to the manufacturing issues for satellite applications, a wide margin and a wide range operation are required because the satellite applications are used in open air worldwide from the equator to the arctic. Therefore, high reliability with temperature tolerance should be realized. In high-frequency applications such as radio astronomy, high-frequency operating circuits at frequencies exceeding 100 GHz

must be developed. In this research, CMOS circuits in satellite receivers using the 10-GHz band and over 100-GHz band were studied. In particular, wide-margin, wide-range and constant-gain operation under variations in temperature was mainly described.

In this study, a 10-GHz band 1-inductor VCO with switching varactor, full-differential dual-modulus prescalers based on ILFD, high-frequency LNA and current re-using mixer, temperature-compensated VGA, constant OIP3 VGA and other circuits were studied. These circuits have many general manufacturing issues of common wireless receivers, which are smaller size, low-noise-phase VCO, lower power consumption and to achieve the target specifications. In addition, satellite applications have unique issues of wider margin, wider range and constant gain operation under temperature variations. In the 100-GHz band, a 134 GHz VCO and dividers were focused. To provide these issues, 1-inductor VCO with switching varactor, wide-operating-range dividers and temperature-compensated VGA were proposed and realized. The system construction with highly reliable satellite applications could be realized.

5.4 Future Works

A CMOS down-converter IC for a single-type LNB down-converter was achieved in the mass-production stage. The development of other type 10-GHz-band PLL-IC and twin-type down-converter IC has been taken over by other team members. Recently, the author has been planning to continue research on applications requiring frequencies exceeding 100 GHz as below.

1. A fundamental 134-GHz VCO and dividers for integer-N-type PLL synthesizer was realized however author could not operate a complete PLL at frequencies of exceeding 100 GHz. Now, one target is to realize the on-chip CMOS PLL at frequencies of exceeding 100 GHz.
2. Analyses from the view point of higher and wider oscillation frequencies have not been carried out. The author is planning

to improve the VCO design for operating in a higher and wider oscillation range. We would like to develop a push-push technique and multi-VCOs..

3. To realize many sub-terahertz applications, not only oscillation circuits but also mixer and amplifier circuits should be realized. The author is planning to study mixer circuits operating at frequencies of exceeding the CMOS maximum frequency.
4. In this study, an example of a higher frequency application exceeding 100 GHz is shown in radio astronomy, however, sub-terahertz applications have many possibilities, such as high-data-rate communications, microwave sensors and medical applications. We are planning to study practicable systems and investigate their probable applications in the future.

公表論文

[1] Takeshi Mitsunaka, Yusuke Kishino, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima, “9 dB NF and +11 dBm OIP3 CMOS Single Conversion Front-End for a Satellite Low-Noise Block Down-Converter” IEICE Trans. Fundamentals, vol. E97–A, No.01 Jan. 2014, pp.101-108.

URL
http://search.ieice.org/bin/summary.php?id=e97-a_1_101&category=A&lang=E&year=2014&abst=

[2] Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima, “8-GHz Locking Range and 0.4-pJ Low-Energy Differential Dual-Modulus 10/11 Prescaler” ” IEICE Trans. Fundamentals, vol. E97-C, No.06, Jun. 2014, pp.486-494.

URL
http://search.ieice.org/bin/summary.php?id=e97-c_6_486&category=C&lang=E&year=2014&abst=

参考論文

[1] Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima, "4 GHz locking range and 0.19 pJ low-energy differential dual-modulus 10/11 prescaler", in Proc. IEEE Asian Solid-State Circuit Conf. (A-SSCC), pp.373-376, Nov. 2012.

URL
http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6570803&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxpls%2Fabs_all.jsp%3Farnumber%3D6570803

[2] Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka and Minoru Fujishima, "The Effect of Supply Voltage Reduction to 5.8-GHz Differential Dual-Modulus Prescaler", in Proc. IEEE Int. Meeting for Future of Electron Devices, Kansai (IMFEDK), pp.30-31, June 2013.

URL
http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6602226&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxpls%2Ficp.jsp%3Farnumber%3D6602226

[3] Takeshi Mitsunaka, Kunihiko Iizuka and Minoru Fujishima “37-mW” CMOS Voltage-Controlled Oscillators and Dividers for 134-GHz Phase-Locked Loop Synthesizer”, in Proc. European Microwave Integrated Circuits (EuMIC) , pp.293-296, October 2014.

URL
http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=6997850
&searchWithin%3Dp_Authors%3A.QT.Mitsunaka%2C+T..QT.