広島大学学位請求論文

Study of NAND Flash Memory Cells

NAND 型フラッシュメモリセルの研究

2013 年

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Abstract

This paper presents the device technologies of NAND Flash memory to realize low bit cost and high reliability.

First, planar (two-dimensional) NAND Flash memory cells are discussed. Four types of NAND Flash memory cells of the LOCOS (LOCal Oxidation of Silicon) isolation cell, the SA-STI cell (Self-Aligned Shallow Trench Isolation cell) with FG wing, the SA-STI cell without FG wing, and SWATT cell (Side WAll Transfer Transistor cell) have been proposed and developed. By using these proposed memory cell, NAND Flash memory cell has been scaled down over 20 years to achieve small memory die size, high performance, and high reliability.

The LOCOS isolation cell is developed. A small memory cell size of 1.13 μm^2 per bit has been achieved in 0.4 μm technology (unit cell size $6*F^2$, F: Feature size). In order to realize the small cell size, narrow 0.8 μm LOCOS isolation is realized with Field Through Implantation (FTI) technique. A negative bias of -0.5 V to the P-well of the memory cell is applied during programming to improve isolation.

The SA-STI cell with FG wing is developed. The extremely small cell size of $0.31um^2$ has been achieved for the 0.25um design rule (cell size $5*F^2$). To minimize the cell size, a floating gate is isolated with shallow trench isolation (STI) and a slit formation by a novel SiN spacer process, which has made it possible to realize a 0.55um-pitch isolation at a 0.25um design rule. A tight Vt distribution width (2.0V) in 2Mbit memory cell array is achieved due to a good uniformity of the channel width in the SA-STI cells.

The SA-STI cell without FG wing is developed. The SA-STI technology results in a small cell size of ideal $4*F^2$, 67% from LOCOS isolation cell without dimension scaling. The key technologies to realize a small cell size are (1) Feature size width (F) Shallow Trench Isolation (STI) to isolate neighboring bits and (2) a floating gate that is self-aligned with the STI, eliminating the floating-gate wings. Even though the floating-gate wings are eliminated, a high coupling ratio of 0.65 can be obtained by using the side-walls of the floating gate to increase the coupling ratio.

The scaling challenges of the SA-STI cell are investigated over 2X~0X nm generations for NAND flash memories. The scaling challenges are categorized to 1) narrow Read Window Margin (RWM) problem, 2) structural challenge, and 3) high field (5~10 MV/cm) problem. First, 1) the narrow RWM is investigated by extrapolating physical phenomena of FG-FG coupling interference, etc. The RWM is degraded not only by increasing programmed Vt distribution width, but also by

increasing Vt of erase state mainly due to large FG-FG coupling interference. However, RWM is still positive in 1Z nm (10nm) generation with 60% reduction of FG-FG coupling by air-gap process. For 2) structural challenge, very narrow 5nm FG width/space has to be controlled. For 3) high field problem, by using WL air-gap, high field problem can be mitigated. Therefore, the SA-STI cell is expected to be able to scale down to 1Z nm (10nm) generation, with the air gap of 60% reduced FG-FG coupling interference.

A SWATT cell has been proposed for a high performance and reliable multi-level cell (MLC) NAND Flash memory. With the SWATT cell, a relatively wide threshold voltage (Vth) distribution of 1.1V is allowed for MLC in contrast to a narrow 0.6 V distribution width in conventional cell. During read, the Transfer Transistors of the unselected cells work as pass transistors. So, even if the Vth of the unselected floating gate transistor is higher than the control gate voltage of Vpass_read, the unselected cell is in the ON state. As a result, wide Vth distribution width can be allowed. Then, the programming speed can be faster because the number of program/verify cycles can be reduced.

Second, three-dimensional (3D) NAND Flash memory cell technologies are discussed.

The 3D DC-SF (Dual Control gate with Surrounding Floating gate) NAND flash cell has been proposed. The DC-SF cell consists of a surrounding floating gate with stacked dual control gates. With this structure, high coupling ratio, low voltage cell operation, and wide Program/Erase window (9.2 V) can be obtained. Moreover, negligible FG-FG coupling interference (12 mV/V) is achieved due to the control-gate shield effect. As a result, the DC-SF NAND flash cell can overcome the problems of SONOS-based 3D NAND flash.

An advanced DC-SF cell process and operation schemes have been developed. In order to improve performance and reliability of DC-SF cell, new Metal Control Gate Last (MCGL) process has been developed. The MCGL process can realize a low resistive tungsten (W) metal word-line, a low damage on tunnel oxide/IPD (Inter-Poly Dielectric), and a preferable FG shape. And also, new read and program operation schemes have been developed. In new read operation, the higher and lower $V_{pass\text{-}read}$ are alternately applied to unselected control gates (CGs) to compensate lowering FG potential to be a pass transistor. And in new program scheme, the optimized V_{pass} are applied to neighbor WL of selected WL to prevent program disturb and charge loss through IPD.

Third, reliabilities of NAND flash memory cell are discussed.

Program/Erase (P/E) cycling degradation and data retention characteristics of NAND Flash were studied in the two P/E schemes. The data retention characteristics have been drastically improved by applying a bi-polarity uniform P/E scheme which uses uniform Fowler-Nordheim tunneling over the whole channel area both during program and erase. It is clarified experimentally that the detrapping of electrons from the gate oxide to the substrate results in an extended retention time of erase state. An uniform P/E scheme also guarantees a wide cell threshold voltage window even after 1 million write/erase cycles.

Read disturb characteristics of NAND flash were investigated. It is clarified that Flash memory cell programmed and erased by uniform Fowler-Nordheim(FN) tunneling has ten times as long read disturb time as the conventional one. This difference of data retentivity is due to decreasing the oxide leakage current by bi-polarity FN tunneling stress. And also, this improvement in read disturb is more remarkable, according as the gate oxide thickness decreases.

Novel negative Vt shift phenomena in inhibit cell during programming have been analyzed in 2X~3X nm SA-STI cells. The negative Vt shift is caused in an inhibit cell when along-WL adjacent cell is programming. The magnitude of the negative shift becomes larger in case of higher program voltage, lower field oxide height, slower program speed of the adjacent cell, and high Vt of victim cell. The experimental results suggest that the mechanism of negative Vt shift is attributed to hot holes that are generated by FN electrons injection from channel/junction to the control gate (CG). This phenomenon will become worse with cell size scaling since hot hole generation is increased by increasing electron injection due to narrower floating gate space.

At the end of this thesis, the future NAND Flash device technologies and its reliabilities are discussed.

The planar SA-STI cell is facing critical scaling limitations in 1Y-1Z nm generations. A severe FG-FG coupling interference is major root cause of critical scaling limitation. On the other hand, 3D NAND cell has been intensively developed. 3D NAND cell can be realized extremely small cell size with more than 32 stacked cells. 3D cell has a potential to realize over 64 stacked cells. Then the 3D cell would replace the planar SA-STI cell, and would be continuously scaled down effective cell size next 10 years.

The reliability of planar NAND flash cell has been degraded, as the memory cell scaling. The important reliability aspects of P/E cycling and data retention are trade-off relationship. Future target of P/E cycling and data retention for each applications will be compromised as <1K P/E cycling and <1 year data retention with system solutions.

Acknowledgement

I would like to express my special thanks to Professor Takamaro Kikkawa, Hiroshima University for invaluable guidance and continuous encouragement. I am also grateful to Professor Shin Yokoyama, Professor Seiichiro Higashi, all of Hiroshima University, for their advice and support as the qualifying examination committee members.

I would like to thank Professor Fujio Masuoka, Mr. Kiyoshi Kobayashi, Mr. Shinichi Tanaka, Mr. Masaki Momodomi, Professor Riichiro Shirota, Professor Shigeyoshi Watanabe, Dr. Koji, Sakui, Professor Fumio Horiguchi, Mr. Kazunori Ohuchi, Dr. Junichi Matsunaga, Dr. Akimichi Hojo, Dr. Hisakazu Iizuka for their continuous encouragement ever since I joined Research & Development center in Toshiba Corporation.

I am grateful to colleagues of mine at Toshiba Corporation for their contributions. Without their help, this work could not have been successful. I especially thank Mr. Ryouhei Kirisawa, Dr. Kazuhiro Shimizu, Mr. Yuji Takeuchi, Mr. Hiroshi Watanabe, Dr. Gertjan Hemink, Mr. Shinji Sato, Dr. Tooru Maruyama, Mr. Kazuo Hatakeyama, Professor Hiroshi Watanabe, Professor Ken Takeuchi, and Mr. Tomoharu Tanaka. I appreciate Mr. Ryozo Nakayama, Mr. Akira Goda, Mr. K. Narita, Mr. E. Kamiya, Mr. T. Yaegashi, Ms. K. Amemiya, Mr. Toshiharu Watanabe, Dr. Fumitaka Arai, Dr. Tetsuya Yamaguchi，Ms. Hideko Oodaira, Dr. Tetsuo Endoh，Mr. Susumu Shuto, Mr. Hirohisa Iizuka，Mr. Hiroshi Nakamura, Dr. Toru Tanzawa, Dr. Yasuo Itoh, Mr. Yoshihisa Iwata, Mr. Kenichi Imamiya, Mr. Kazunori Kanebako, Mr. Kazuhisa Kanazawa, Mr. Hiroto Nakai, Mr. Takehiro Hasegawa, Dr. Katsuhiko Hieda, and Dr. Akihiro Nitayama, Mr. Koichi Fukuda, Mr. Seiichi Mori for their fruitful discussion.

I would like to thank Dr. Sungwook Park, Dr. Sungjoo Hong, Dr. Seok Hee Lee, Dr. Seokkiu Lee, Dr. Seaung Suk Lee, Dr. Sungkye Park, Mr. Gyuseog Cho, Mr. Jongmoo Choi, Mr. Yoohyun Noh, Mr. Hyunseung Yoo, Dr. EunSeok Choi, Mr. HanSoo Joo, Mr. Youngsoo Ahn, Mr. Byeongil Han, Mr. Sungjae Chung, Mr. Keonsoo Shim, Mr. Keunwoo Lee, Mr. Sanghyon kwak, Mr. Sungchul Shin, Mr. Iksoo Choi, Mr. Sanghyuk Nam, Mr. Dongsun Sheen, Mr. Seungho Pyi, Mr. Jinwoong Kim, Mr. KiHong Lee, Mr. DaeGyu Shin, Mr. BeomYong Kim, Mr. MinSoo Kim, Mr. JinHo Bin, Mr. JiHye Han, Mr. SungJun Kim, Mr. BoMi Lee, Mr. YoungKyun Jung, Mr. SungYoon Cho, Mr. ChangHee Shin, Mr. HyunSeung Yoo, Mr. SangMoo Choi, Mr. Kwon Hong, Mr.

SungKi Park, Ms. Soonok Seo, Mr. Hyungseok Kim, for their warm considerations ever since I joined Research & Development division in the SK Hynix Inc.

I would like to thank Mr. Eli Harari, Mr. Sanjay Mehrotra, Dr. George Samachisa, Dr. Jian Chen, Mr. Tuan D. Pham, Mr. Ken Oowada, Dr. Hao Fang, Dr. Khandker Quader, for their continuous encouragement and fruitful discussion since SanDisk-Toshiba joint development started on 1999.

I would like to thank Dr. Kirk Prall, the late Mr. Andrei Mihnea, Mr. Frankie Roohparvar, Dr. Luan Tran, and Mr. Mark Durcan for their continuous encouragement since I joined Micron Technology, Boise, ID, USA on 2003.

I would like to thank Mr. Krishna Parat, Dr. Pranav Kalavade, Dr. Mark Bauer, Dr. Nile Mielke and Dr. Stefan K. Lai, for their continuous encouragement and fruitful discussion since Intel-Micron joint development started.

I would like to thank Mr. Angelo Visconti, Ms. Silvia Beltrami, Ms. Gabriella Ghidini, Dr. Emilio Camerlenghi, Mr. Roberto Bez, Mr. Giuseppe Crisenza, and Mr. Paolo Cappelletti for their continuous encouragement and fruitful discussion during performing Numonyx-Hynix joint development.

I would like to thank Dr. T.-J. Brian Shieh, Dr. Alex Wang, Dr. Travis C.-C.Cho, Ms. Saysamone Pittikoun, Mr. Yoshikazu Miyawaki, Mr. Hideki Arakawa, Mr. Stephen C. K. Chen, for their continuous encouragement and support since I joined Powerchip Semiconductor Corp, Hsinchu, Taiwan.

Finally I would like to express my heart-felt thanks to my wife, Miho Aritome and my son, Santa Aritome who have continuously supported me with their love.

CONTENTS

Chapter 1
Introduction

1.1 Background

Recent progress in computers and mobile equipments requires further efforts in developing higher density and higher reliability nonvolatile semiconductor memories. A breakthrough in the field of nonvolatile memories was the invention of the Flash EEPROM (Electrically Erasable and Programmable Read Only Memory) [l]. The Flash EEPROM has many advantages in comparison with other nonvolatile memories. Therefore, the Flash EEPROM explosively accelerated the development of higher density EEPROM's.

In 1987, a NAND structured cell was proposed by F. Masuoka et al. [2]. This structure can reduce the cell size without scaling of device dimension. The NAND structure cell arranges a number of bits in series, as shown in Fig.1.1.1 [2]. The conventional EPROM cell has one contact area per two bits. However, for a NAND structure cell, only one contact hole is required per two NAND structure cells (NAND string). As a result, the NAND cell can realize a smaller cell area per bit than the conventional EPROM.

Table 1.1.1 shows the history of NAND Flash memory, based on technical papers from 1987 to 1997. During 10 years from first NAND flash paper on 1987, all of the fundamental and important NAND flash technologies were established, such as uniform program and uniform well erase method [9][12][13], bit-by-bit verify[15][21], ISPP (Incremental Step Pulse Program) [25][26][29], Self-aligned STI cell [22][51][54], shield bit-line scheme [21], page programming [7][8], block erase, etc. After that, NAND flash production started to tremendously expand. The overall NAND market is expected to hit $30 billion in 2013. This thesis is based on research during developing NAND Flash devices from 1987 to present.

Table 1.1.1 History of NAND Flash (~1997)

Year		Authors	Ref	Conference/Journal
1984	Flash Memory, 1st paper	F. Masuoka, et.al	[1]	IEDM 1984
1987	NAND-type Flash memory, 1st paper	F. Masuoka, et.al	[2]	IEDM 1987
1988	NAND-type Flash memory	R. Shirota, et al	[3]	VLSI 1988
	drain-FN program	M. Momodomi, et al	[4]	IEDM 1988
1989	4Mb NAND-type Flash memory	Y.Itoh, et al /M. Momodomi, et al	[5][6]	ISSCC1989/JSSC
	page program	M.Momodomi, et al/Y. Iwata, et al	[7][8]	CICC1989/JSSC
1990	Well erase reliability	S. Aritome, et al	[9]	IRPS 1990
	4Mbit tight Vt distribution	T.Tanaka, et al /M. Momodomi,et al	[10][11]	VLSI 1990/JSSC1991
	Well erase	R. Kirisawa, et al	[12]	VLSI 1990
	Bi-polarity program/erase	S. Aritome, et al	[13]	IEDM 1990
	Double patterning	R. Shirota, et al	[14]	IEDM 1990
1992	bit-by-bit verify	T.Tanaka, et al	[15]	VLSI 1992
1993	Reliability of Flash	S. Aritome, et al	[16]	Poceeding of IEEE
	0.4um 64Mb cell technology	S. Aritome, et al	[17][18]	SSDM 93/ JJAP
1994	SILC	H. Watanabe, et al	[19]	VLSI 1994
	Cycling and Data Retention Reliabilit	S. Aritome, et al	[20]	IEICE
	Intelligent program, shield BL schem	T.Tanaka, et al	[21]	JSSC
	Self-Aligned STI cell (SA-STI cell)	S. Aritome, et al	[22]	IEDM 1994
1995	32Mb NAND	K. Imamiya, et al /Y. Iwata, et al	[23][24]	ISSCC1995/JSSC
	32Mb NAND with Increment Step Program Pulse (ISPP), self-boost	K.D. Suh,et al	[25][26]	ISSCC1995/JSSC
	Read disturb, SILC	S. Satoh, et al	[27][28]	ICMTS1995/ED
	Increment Step Program Pulse (ISPI	G.J. Hemink, et al	[29]	VLSI 1995
	double Vt Select gate	K. Takeuchi, et al	[30][31]	VLSI 1995/JSSC
	SWATT cell	S. Aritome, et al	[32][33]	IEDM 1995/ ED
1996	128Mb MLC	T.S. Jung, et al	[34][35]	ISSCC 1996/JSSC
	64Mb	J.K.Kim, et al	[36][37]	VLSI1996/JSSC
	SILC	G.J. Hemink, et al	[38]	VLSI 1996
	on-chip ECC	T.Tanzawa, et al	[39][40]	VLSI1996/JSSC
	Booster Plate	J.D. Choi, et al	[41]	VLSI 1996
	High speed NAND	D.J. Kim, et al	[42]	VLSI 1996
	SILC in STI	H. Watanabe, et al	[43]	IEDM 1996
	Shared Bit Line	W.C. Shin, et al	[44]	IEDM 1996
1997	nonvolatile virtual DRAM using NANI	T.S. Jung, et al	[45][46]	ISSCC 1997/JSSC
	3-level cell (1.5bit/cell)	T. Tanaka, et al	[47]	VLSI 1997
	Multi pagecell	K. Takeuchi, et al	[48][49]	VLSI 1997/JSSC
	Parallel program	H.S.Kim,et al	[50]	VLSI 1997
	0.25um SA-STI cell	K. Shimizu, et al	[51]	IEDM 1997
	Program Disturb	S. Satoh, et al	[52]	IEDM 1997
	Triple-poly booster gate	J.D. Choi, et al	[53]	IEDM 1997

Applications of flash memory are becoming quite wide due to non-volatility, fast access, and robustness. Flash memory application can be classified into two major markets. One is for code storage applications, such as PC BIOS, cellular phone and DVD. NOR-type cell is best suitable for this market due to its fast random access speed. The other is for file storage applications, such as Digital Still Camera (DSC), Silicon Audio, smartphone, and tablet PC. Requirements for file storage memory are low bit cost, high reliability (program/erase cycling endurance and data retention characteristics), high speed programming and erasing, low power consumption, as shown in Fig.1.1.2 [54].

Most important requirement for file storage applications is the low bit cost. Cost of memory device is mainly determined by the die size of memory chip and fabrication process cost (mainly depreciation of investment on factory). Then it is very important to combine small die size with simple fabrication process. In order to reduce the die size,

reduction of unit memory cell size is most important as scaling feature size. Ideal memory cell size is $4*F^2$ (F; Feature size), because both X and Y directions determined by Line (F) and space (F). However, in Flash memory cell size, it was difficult to realize $4*F^2$ cell due to wide (>2*F) isolation width of LOCOS and Floating gate wing.

Recently, in order to scale down NAND Flash memory cell further to be lower bit cost, several three-dimensional (3D) NAND flash cells have been proposed [55]-[60]. 3D cell has stacked several cells vertically to decrease effective cell size. However, these 3D cells have used the charge trap (CT) type flash cell which stores charges in SiN layer, then they have several intrinsic disadvantages, such as slow erase speed, small data retention margin [61], and charge spreading issues [62]. They would cause degradation of data-retention characteristics and poor Vt distribution of cell state. As these problems are related to charge trap nitride, floating gate type 3D NAND flash is required instead of charge trap nitride.

The other important requirement for file storage applications is “high reliability”, as shown in Fig.1.1.2. A high voltage (>20V) is applied to control gate to make Fowler-Nordheim (FN) tunneling current on the tunnel oxide. The electric field in tunnel oxide become over 10MV/cm, which is normally caused oxide breakdown in other semiconductor devices. This means Flash memory uses a breakdown-like operation in normal program and erase. Due to applying a high field, tunnel oxide has degraded, such as electron/hole trap, interface state generation, and Stress Induced Leakage Current (SILC). Major reliability degradation aspects of flash memory are related on this tunnel oxide degradation by program and erase cycling. Even if tunnel oxide is degraded, a stored data has to be sustained in memory cells for long time, as non-volatile memory. Data retention time after program and erase is a key of NAND flash reliability.

In addition, read disturb and program disturb are also an important reliability phenomena in NAND flash [13]. During read and program operation, pass voltages are applied to unselected WLs in the NAND string. Several kinds of disturb stress are applied to unselected cell in cell array. Read disturb and program disturb is caused in these unselected cell in string in cell array.

Reliability specifications for NAND Flash are depended on applications, such as digital still camera, MP3 players, SSD (solid state disk) for PC, SSD for data server, etc. Target specifications of NAND flash are generally as follows.

Program and Erase cycles (P/E cycles) ; 1K~100K cycles

Data Retention ; 1~10 years

Read cycles ; 1E5 ~ 1E7 times

Number of page program time (NOP); 1 time for 2~4 bits/cell, 2~8 times for 1bit/cell

In order to guarantee specification of NAND, every effort has been made on device, process, operation, circuit, etc. This thesis is based on these efforts to the reliability during development NAND Flash.

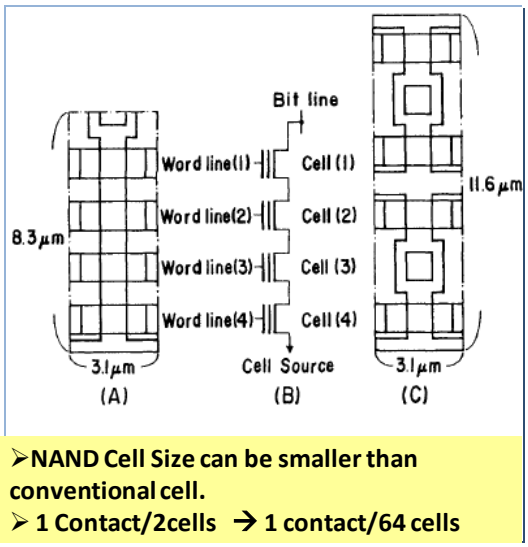

Fig1.1.1 Comparison between (A) NAND cell and (C) conventional NOR flash cell. (B) shows equivalent circuit of the NAND structure cell having 4 bits [2].

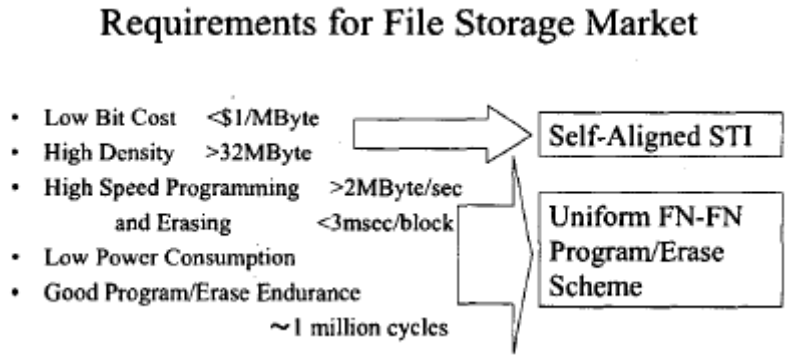

Fig.1.1.2 Requirements for file storage markets [54].

1.2 Research Objectives

The objective of this research is to study the NAND Flash memory device technology for a low bit cost and high reliability. Investigation focuses on the scaling of NAND flash memory cell and improvement of NAND flash reliabilities, because they are most important requirements for file storage devices.

Layout of NAND Flash memory cell is simple that parallel word lines (WL) are perpendicular to parallel bit lines (BL). WL pitch is normally 2*F, (F; Feature size), which is limited by lithography, however, BL pitch is normally 3*F or more. This is because isolation width is needed 2*F or more to prevent relatively high (~8V) punch through between NAND cell channels (strings) during program. Then, it is crucial to scale down isolation width, in order to scale down memory cell size to satisfy requirement of low bit cost.

Another important technology for low bit cost is Multi Level Cell (MLC), which is stored multi logical bit in physical single memory cell. To implement MLC, cell threshold voltage (Vt) setting margin of each logical states (read window margin) have to be wide enough. As scaling down of NAND Flash memory cell, cell Vt setting margin (read window margin) is degraded because of many physical phenomena, such as FG-FG capacitive coupling, RTN, etc. Then it is important to clarify scaling limitation factors of NAND Flash cell. And also, it is important to research preferable cell structure to realize wider read window margin.

Other important requirement is high reliability. Reliability of Flash memory is attributed to data retention or read disturb after program/erase cycling endurance. Program and erase operation schemes have an impact on reliability of Flash memory cell. Then, many program/erase schemes are proposed to satisfy requirement of reliability and performance. Then it is very important to clarify cell degradation mechanism and best scheme of program/erase in order to achieve requirement of reliability and performance.

Corresponding to these motivations, this research has the following concrete objectives:

1) Investigate the scaling scenario of NAND flash memory cell.
2) Develop a practical framework of scaling down of NAND flash memory cell.
3) Develop the advanced LOCOS isolation technology to scale down NAND Flash memory cell.
4) Develop the advanced STI isolation technology to be suitable to NAND Flash memory.
5) Develop the low cost of NAND Flash process flow.

6) Analyze the scaling limitation of NAND flash cell and propose solutions to overcome the scaling limitation.
7) Develop the new structure of NAND Flash memory cell to be suitable MLC (Multi Bit Cell).
8) Develop new 3-dimensional NAND memory cell to be extremely scalable and highly reliable NAND Flash memory.
9) Investigate the reliability of NAND Flash on several program and erase schemes, in order to clarify the dependence of program and erase scheme.
10) Investigate the new disturb phenomena to optimize operation of NAND Flash cell.
11) Define the future NAND Flash memory cell technologies.

In general, the scaling of memory cell is always facing the technical and physical limitations. In order to make a break-through over these limitation, new technologies are required. However, there was no such technology to break-through to scale down NAND flash memory cell.

For reliability of NAND Flash, there was no comparison data among several program and erase schemes to determine proper operation scheme.

Therefore, the significance of this research in terms of engineering resides in the following points;

1) The practical framework of NAND flash cell scaling was developed.
2) NAND Flash memory cell technologies are developed over 10 generations.
3) Cell size of NAND Flash memory with LOCOS isolation is minimized by using FTI process.
4) The Self-Aligned STI cell (SA-STI cell) technology with FG (Floating Gate) wing is developed.
5) The Self-Aligned cell (SA-STI cell) technology without FG wing is developed. This cell was used long time over ten years, and became de-fact standard.
6) The scaling limitation of SA-STI cell is clarified based on extrapolate physical phenomena.
7) The Side Wall Transfer Transistor cell (SWATT cell) is proposed to have wide read window margin for MLC.
8) 3-dimensional Floating Gate (FG) NAND Flash of DC-SF cell (Dual Control gate and Surrounding Floating Gate cell) is proposed and investigated to be candidate of future high density and high reliable NAND Flash memory.
9) Suitable operation schemes of DC-SF cell are proposed.
10) It is clarified that reliability of NAND Flash cell is depended on program/erase

schemes. Uniform program and uniform erase scheme is most preferable to obtain both high reliability of high performance.

11) New negative Vt shift phenomena is observed for the first time, and analyzed the mechanism.

1.3 Chapter Organization and Overview

This thesis is organized as shown in Fig.1.3.1.

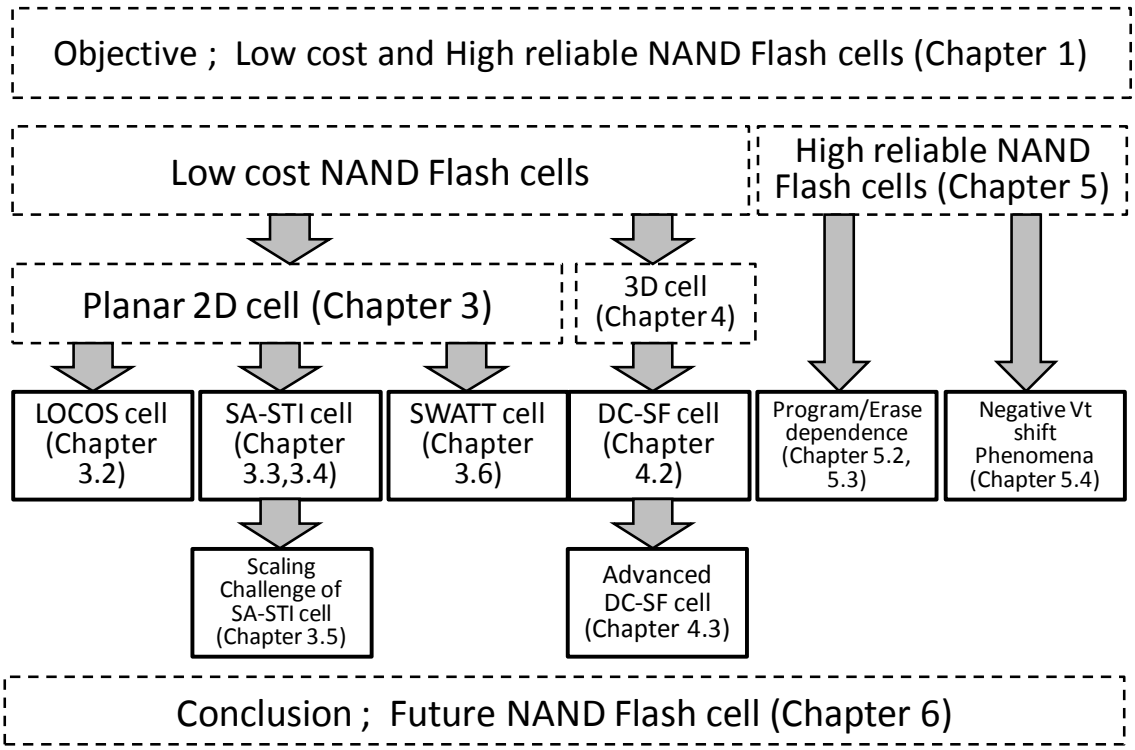

Fig.1.3.1 Structure of this thesis

Chapter 2 presents a basic structure and operations of NAND Flash memory. The structures of single cell and NAND cell array are described. And the key of NAND cell scaling is discussed. Cell operations of read, program, and erase are introduced. And then MLC NAND cell technology is discussed to realize low cost NAND.

In Chapter 3, planar 2-dimentional NAND flash memory cell technologies are discussed. First, LOCOS isolation cell technologies are presented (Chapter 3.2). The LOCOS isolation width can be minimized with improving device performance by field through implantation technique (FTI) after LOCOS formation. Next, Self-Aligned STI cell with FG wing is discussed. In order to reduce aspect ratio of cell structure, FG wing

is applied. And then, Self-Aligned STI cell without FG wing is discussed. This cell has been used from 90nm generation cell to present cell (2Y nm cell), as a de-fact standard. After that, the scaling challenges of Self-Aligned STI cell are discussed. The read window margin is seriously degraded from 1X nm generation, and read window margin of 1Y/1Z nm memory cell can be implemented by reducing FG-FG coupling effect. And also, the Side Wall Transfer Transistor cell (SWATT cell) is described. Due to side-wall transfer transistor, Vt read window margin can be greatly improved. Then, fast programming speed can be expected.

The 3-dimentional (3D) NAND Flash cells are presented in Chapter 4. After describing motivation and history of 3D NAND Flash, Dual Control gate and Surrounding Floating Gate cell (DC-SF cell) is presented. Advantages and performance of the DC-SF cell are discussed. After that, Advanced DC-SF cell technologies are presented. The advanced process and new read/program scheme can greatly improve performance and reliability of the DC-SF cell.

Chapter 5 describes reliability aspect of NAND Flash cell. It is clarified that the uniform program and uniform erase technology has several advantages in NAND Flash reliability by comparing program/erase endurance, data retention and read disturb characteristics in several program and erase schemes in chapter 5.2 and 5.3. And newly observed negative Vt shift phenomena during programming is described in chapter 5.4.

Conclusion based on this research and discussions about the future NAND Flash cell trends are described in Chapter 6. The perspectives on future NAND Flash technologies are also discussed.

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Chapter 2
Principle of NAND Flash Memory

2.1 NAND Flash Device and Architecture

2.1.1 NAND Flash Memory Cell Architecture

Fig.2.1.1 shows single cell architecture of Flash memory [2.1]. The single cell has Nch MOS transistor with poly-silicon floating gate (FG). FG is electrically isolated by tunnel oxide and Interpoly Dielectric (IPD). Charge is stored in FG, and potential of FG is controlled by Control Gate (CG) voltage with capacitive coupling. Fig.2.1.2 shows NAND string structure [2.2]. NAND string consist of 32 cells (typical) and two select transistors (SGD, SGS). 32 cells are connected in series. SGD and SGS connect at drain and source to isolate from Bit Line (BL) and Source Line (SL).

Fig.2.1.3 shows a top view of NAND Flash memory cells. One NAND string consists of 32 series-connected stacked gate memory transistors and two select gate transistors. The entire memory array is formed by straight active area lines (horizontal lines) and straight gate lines (vertical lines). This simple cell structure enables easy fabrication of memory cells, which have small feature size. The memory cell is located at an intersection of the two cross lines. Thirty-two memory transistors are arranged between two select transistors, so that both the bit-line and source-line contacts are arranged every 34 vertical lines.

Fig.2.1.4 shows array architecture of NAND Flash cell. Page size is typically 2K~16KByte (2~16KByte cells + ECC code). Page size is increasing for enhancing performance of read and program. The original page size was 512Byte+ECC code [2.3]-[2.6]. And it increased to have steps of 512B → 2KB → 4KB → 8KB or 16KB. Page size will be increased for future because more higher performance will be required. Block is basically : page x 2 x 32 cells = 128K~256KByte cell (physical). And Read and Program is performed per page. And Erase is performed per block.

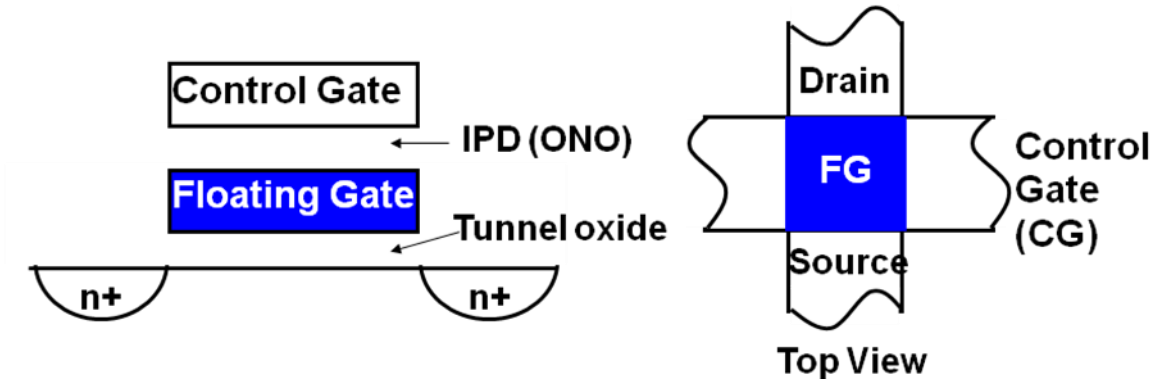


Fig.2.1.1 Single Cell Architecture of floating gate flash memory. Nch MOS transistor with poly-silicon floating gate (FG). FG is electrically isolated by tunnel oxide and Interpoly Dielectric (IPD). Charge is stored in FG.

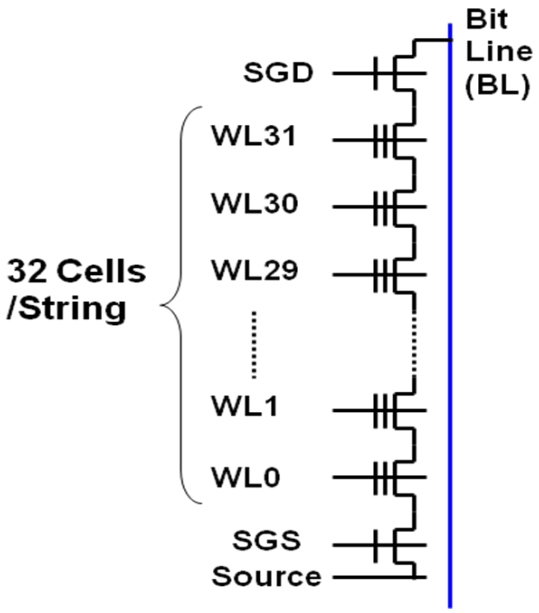


Fig.2.1.2 NAND String Architecture. NAND string consist of 32 cells (typical) and two Select transistor (SGD, SGS). 32 cells are connected in series. SGD and SGS connect at drain and source to isolate from Bit Line and source line.

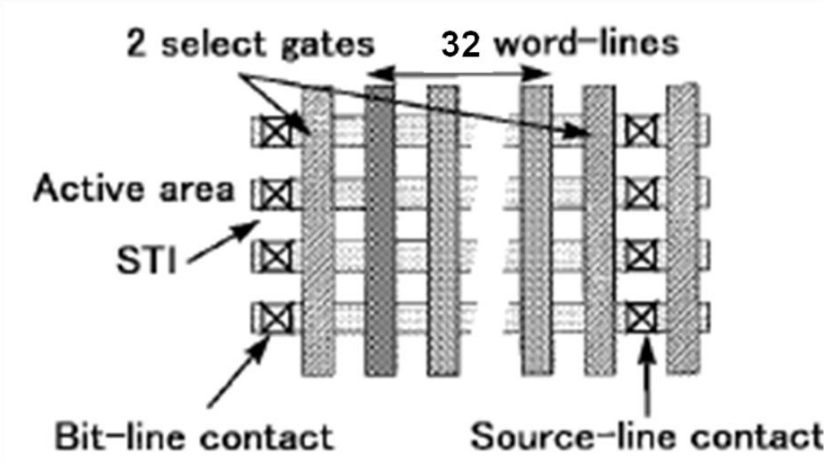


Fig.2.1.3 Top-view schematic of NAND flash memory cells.

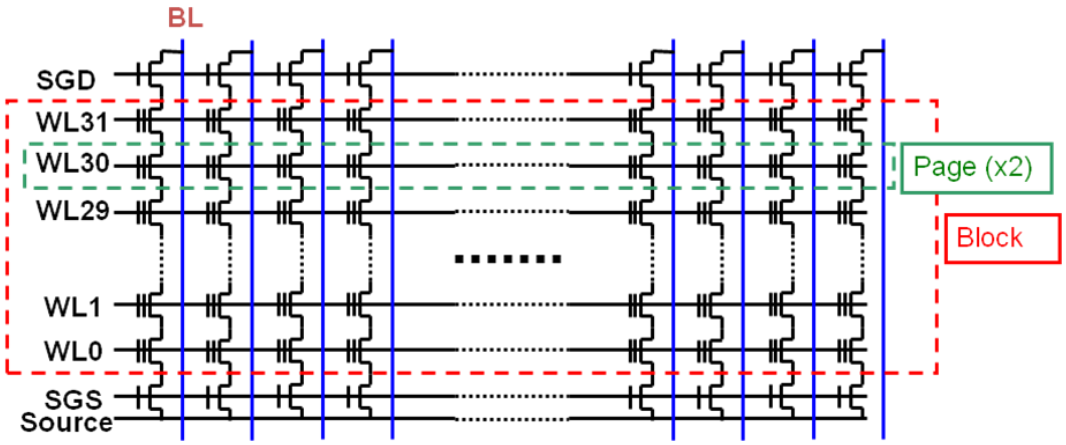


Fig.2.1.4 Array Architecture. Page size is typical 2K~16KByte (2~16KByte cells + ECC code). Block size : page x 2 x 32 cells = 128K~256KByte cell (physical). Read and Program : per page, Erase : per block

2.1.2 Memory cell scaling

Most important requirement for NAND flash memory is low bit cost, which can be attained with small cell size. NAND Flash cell can make small cell size without scaling feature size, as shown in Fig.1.1.1 [2.2] in chapter 1, because one contact area is shared by more than 8 cells in comparison with one contact area/2 cells of NOR flash. Fig.2.1.5 shows the single cell layout of NAND flash cell with LOCOS isolation cell (chapter 3.2). The line/space pitch of word line (WL) is ideal 2*F (F; feature size), however the line/space pitch of bit line (BL) is 3*F because of limitation of LOCOS isolation. Requirement for isolation of NAND flash cells are severer than other device due to high

voltage operation during programming. Required items are 1) punch through and junction breakdown of bit line contact, 2) CG field transistor Vt, 3) SG field transistor Vt. The Shallow Trench Isolation (STI) technology could solve these isolation issues (Chapter 3.3 and 3.4). The STI can reduce isolation width from 2*F to F**,** so cell size can be scaled down to ideal $4*F^2$.

The effective cell size can be reduced by MLC(Mu1ti-level Cell) scheme. Therefore, small physical cell size of $4*F^2$ combined with MLC can drastically reduce the bit cost. However, in order to realize MLC cell, Vt distribution setting (Read Window Margin; RWM) have to have enough margin. As scaling down memory cell size, many physical phenomena have an impact to degrade RWM, as described in Chapter 3.5. One important physical phenomenon is the FG-FG coupling [2.7] that is caused Vt shift by programming neighbor cells. Vt distribution width become wider. The other physical phenomena to have an impact on RWM are Random Telegraph Noise (RTN), Electron Injection Spread (EIS), string resistance which are described in Chapter 3.5. Except for RWM degradation, there are several problems. Fig.2.1.6 shows the scaling problems of Self-Aligned STI cell (SA-STI cell). They are also described in Chapter 3.5.

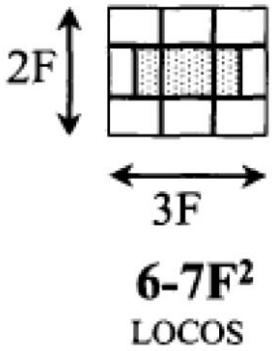


Fig.2.1.5 Layout of NAND Flash memory cell with LOCOS isolation.

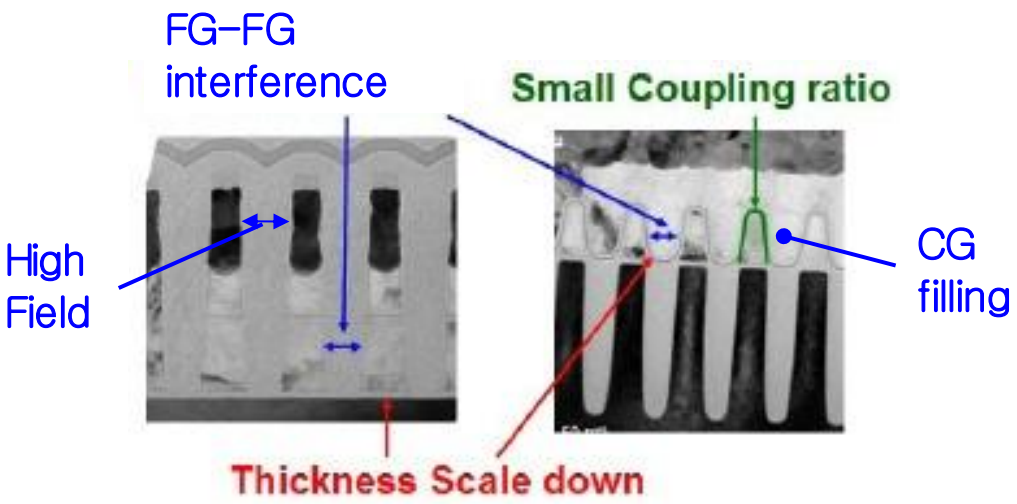


Fig.2.1.6 Cross sectional TEM photograph of Self-Aligned STI cell (SA-STI cell) and the major obstacles in scaling down the NAND Flash.

2.1.3 Peripheral Device

The peripheral transistors for NAND flash memory device are listed in Fig.2.1.7. The types of peripheral transistors are depended on circuit requirement. Fig.2.1.7 is typical case of transistors list. Thick gate oxide of 25~40nm is used for a high voltage transistor. Low voltage transistor has thin gate oxide (~9nm) which is the same as tunnel oxide in memory cell. In order to realize low process cost, it is important that peripheral Tr is fabricated without increasing process steps.

The scaling of high voltage transistor (HV Tr) is also one of the important challenge for NAND Flash memories. The size scaling of high voltage transistor (HV Tr) is required for placing HV Tr and isolation on certain determined cell pitch. There are two critical location of HV Tr scaling. One is the row decoder/ word line driver, HV Tr + isolation width have to be in one string pitch basically. The other loaction is the bit-line selector area. Small area of HV Transistor can make small area of bit line selector.

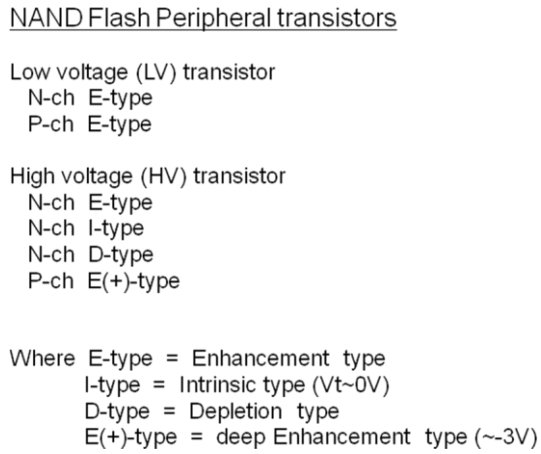


Fig.2.1.7 List of peripheral transistors in NAND Flash memories.

2.2 Cell Operation

2.2.1 Read Operation

Fig.2.2.1 shows basic read operation of single cell. Data (0 or 1) is judged by cell current (Icell) flow “ON” or not flow “OFF” during Vgate=0V applied. Erased state has positive charge in FG. Programmed state has negative charge in FG.

Read operations are performed in page units, as shown in Fig.2.2.2. A page corresponds to a row of cells and is accessed by a single wordline. VpassR (~6V) is applied to unselected wordline to be as a pass transistor. Random Read speed (tR) is normally 25usec for SLC, 60usec for MLC. However, tR is becoming longer as a cell scaling because of decreasing Icell.

Read disturb problem is mainly caused in unselected cells where VpassR is applied to CG and channel is 0V. It is the weak electron injection mode, then cell Vt is gradually increased.

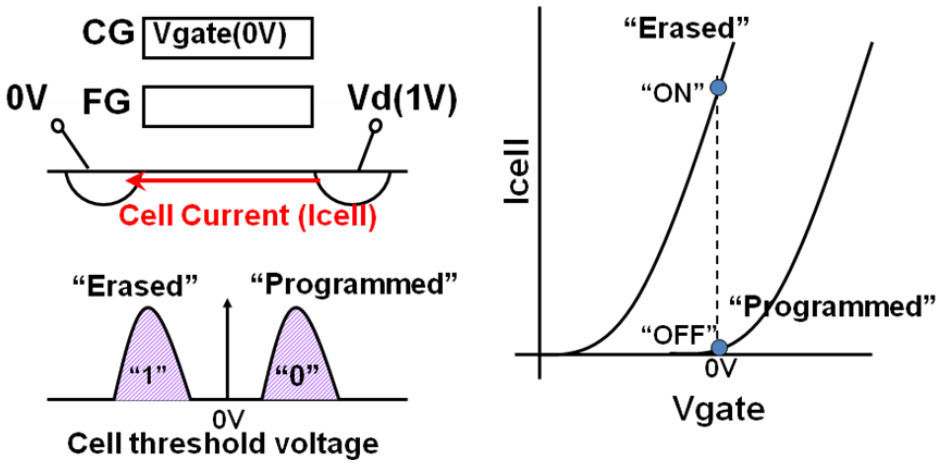


Fig.2.2.1 Single Cell Read. Erased : Positive charge in FG. Icell "ON". Programmed : Negative charge in FG. Icell "OFF".

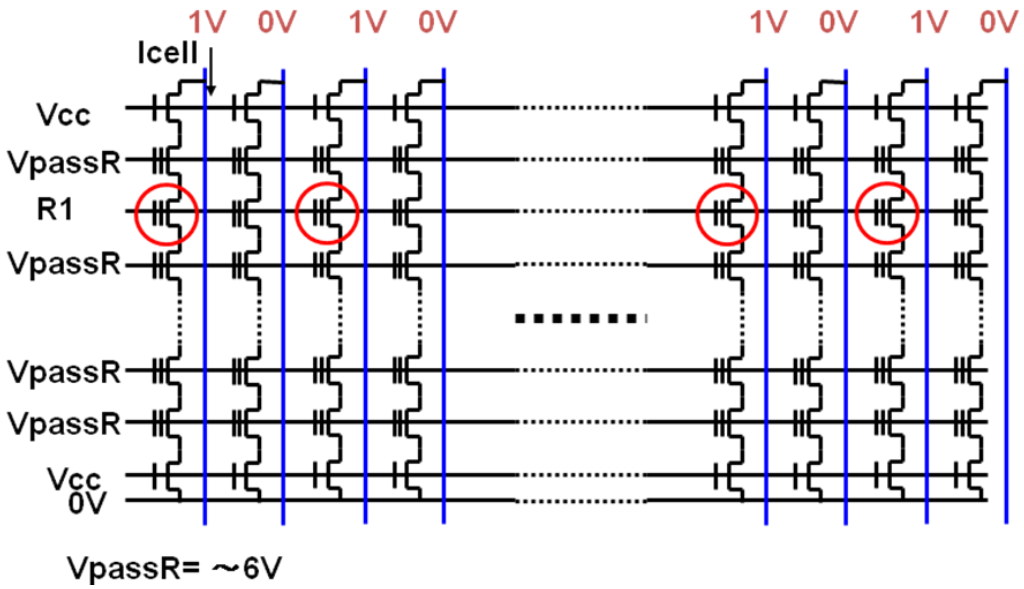


Fig.2.2.2 Array Cell Read. Page Read : 2~16KByte at the same time. Random Read speed, tR : 25usec for SLC, 60usec for MLC.

2.2.2 Program and Erase Operation

Several program and erase schemes were considered to use NAND flash memory product, as shown in Fig.2.2.3. There are only two ways of electron injection to Floating Gate (FG), such as Channel Hot Electron injection (CHE) and Fowler-Nordheim (FN) channel injection. And also, there are only two ways of electron ejection from FG, such as Drain/Source FN ejection or Channel FN ejection. Four schemes of programming

and erase operations are possible by combination of these ways of injection and ejection. First one is the NOR type flash program/erase scheme. CHE injection is used for programming, and Source FN ejection is used for erase. Second one is the new NOR type flash program/erase scheme [2.8]. CHE injection is used for programming, and channel FN ejection is used for erase. Third one is the old program/erase scheme for NAND flash [2.9][2.10]. Drain FN ejection is used for programming, and channel FN injection is used for erase. Fourth one is the NAND type flash program/erase scheme [2.8][2.11][2.12]. Channel FN injection is used for programming, and channel FN ejection is used for erase. Power consumption and scalability are worse in CHE and Drain/Source FN ejection schemes due to large current flow. However, reliabilities of each schemes was not well known. They had to be analyzed because reliabilities were difficult to predict.

The program/erase schemes of NAND flash memory product was decide to use uniform program/erase scheme in Fig.2.2.3 [2.8][2.11][2.12]. Detail program and erase operation are described in following.

The program operation of NAND Flash cell is performed by applying high voltage Vpgm to control gate (CG) while keeping substrate/source/drain 0V, as shown in Fig.2.2.4. Electrons are injected to the floating gate (FG) by Fowler-Nordheim (FN) tunneling mechanism through the tunnel oxide. Vt of cell has a positive shift. Erase operation is performed by applying high voltage Vera to substrate (P-well), while keeping CG 0V. Electrons in FG are ejected to substrate through tunnel oxide. Vt has a negative shift.

Fig.2.2.5 shows a typical program characteristic. Higher program voltage (Vpgm) or longer program pulse width can be faster programming.

Fig.2.2.6 shows array cell program scheme. At first, the programming starts at the source side cells. Vpgm are applied to the control gate of the selected cells while Vpass are applied to the control gates of the unselected cells. These unselected cells act as pass transistors and make the boosting voltage in channel to prevent from boosting mode program disturb, as described in chapter 2.2.4. A 0V is applied to the bit line and then electrons are injected from the bit-line (channel) to floating gate by the electric field between the bit line and the floating gate of the selected cell. The threshold voltage of the selected cell is pushed up into the enhancement mode of approximately 2 V. In the case of program inhibit mode, the bit line is raised to Vcc. The voltage of Vcc-Vt (Vt of select Tr) is transferred to the channel of cell strings. Then Vpass are applied to the control gate of the unselected CGs to make the boosting voltage in the channel of unselected string. No electrons are injected from the channel(Vboost) to the floating

gate, because the electric field between the bit line and the floating gate is insufficient to initiate tunneling. The threshold voltage of the selected cell remains at -3 V. After programming the cells connected with CG0 (WL0), the programming of the cells connected with CG1 (WL1) starts. Vpgm are applied to the control gate of the selected cell (CG1) and Vpass is applied to the control gate of the unselected cell (CG0, CG2-31). 0V or Vcc are applied to bit line as corresponding with data. Subsequently, the programming continues from the source side cell to the bit-line side cell successively. Typical programming time per page, including the data load sequence, is 200usec for SLC, 800~1600usec for MLC.

Incremental step pulse programming (ISPP) achieves fast program performance under process and environmental variations while keeping a tight programmed cell *Vt* distribution [2.13][2.14][2.15]. Fig.2.2.7 shows Vpgm waveform of ISPP program. Vpgm has stepped up by each pulse. ISPP scheme suppresses process variations issues effectively by allowing fast programmed cells to be programmed with a lower program voltage and slow program cells to be programmed with a higher program voltage. After an initial 15.5 V program pulse, each subsequent pulse (if required) is incremented in 0.5 V steps up to 20 V, for example. Since sufficiently programmed cells are automatically switched to the program inhibit state in the verification step, easily programmed cells are not affected by the higher program voltages. A 1 V program pulse increment is approximately as effective as five pulses without the increment. Thus, ISPP has the effect of increasing pulse width [2.16] without actually increasing the program time by dynamically optimizing program voltage to cell characteristics. Through program pulse/verify cycles, programmed cell *Vt* is maintained to within 0.6 V by using 0.5V ISPP step as shown in Fig.2.2.8 [2.13]. With ISPP, a page is typically programmed within 2~6 program pulses/verify cycles for SLC (~300 usec*)*. The constant 16.5 V program voltage device of Fig.2.2.8 has the tightest *Vt* distribution (~0.5V), however program verify cycles are larger of 11~37 cycles. This means 2~16 times slower programming speed. Then ISPP provides an optimum combination of both a tight *Vt* distribution and a fast program time.

By effectively adjusting to process and environment variations, ISPP maintains consistent program performance which helps improve the yield of the device. Marginal cells that were previously out-of-spec when conditions were varied are brought within-spec with ISPP. However, ISPP is able to compensate for cell-by-cell variations that can exist within a die.

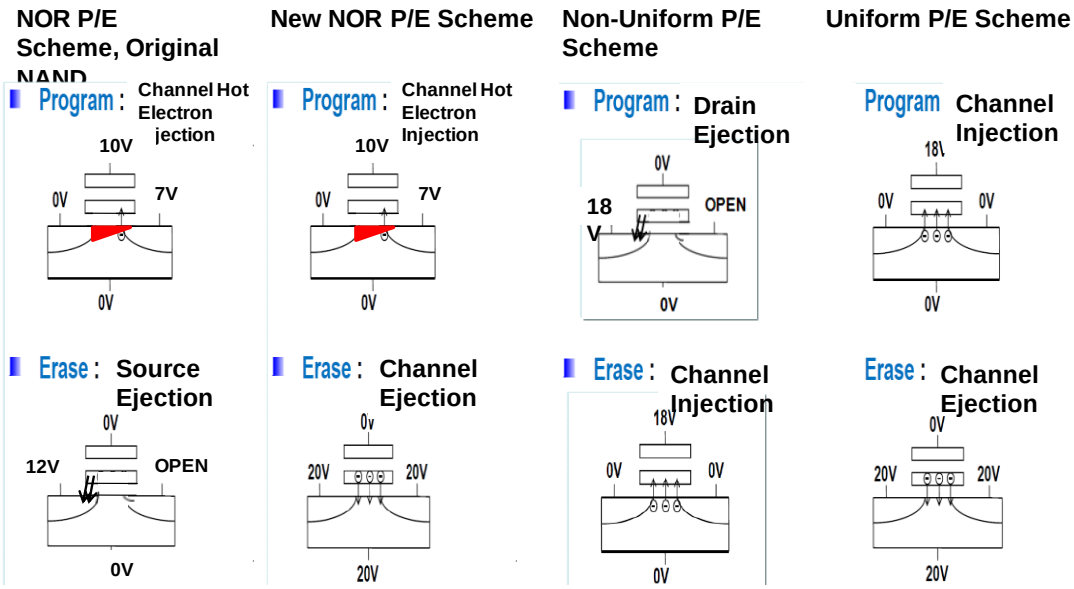


Fig.2.2.3 Program and Erase schemes of NOR and NAND Flash cells.

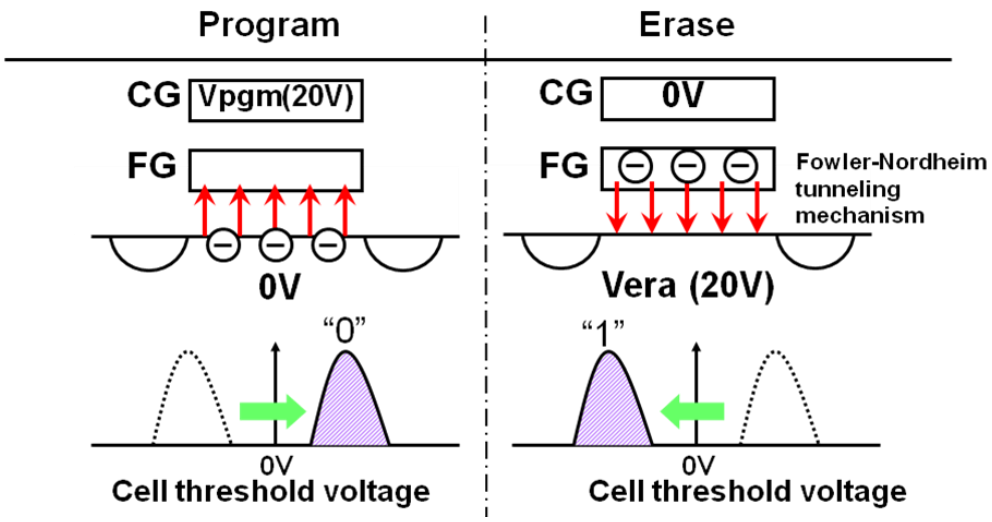


Fig.2.2.4 Single Cell Program and Erase. Program : Injected electron to the FG through tunnel oxide. Erase : Ejected electron from the FG

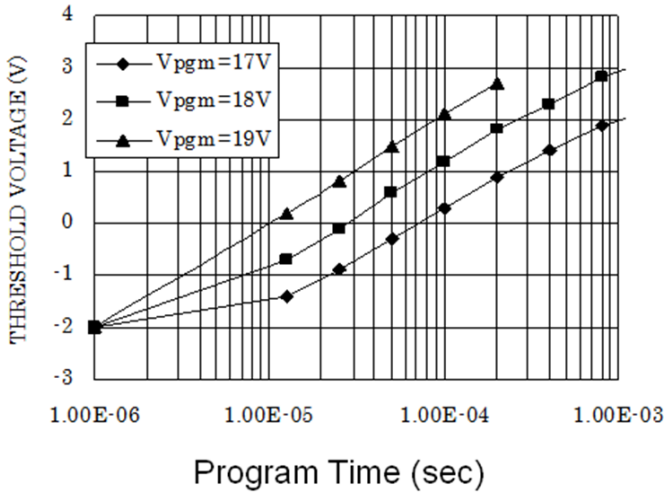


Fig.2.2.5 Program Characteristics. High Program/Erase voltage can be faster operation. Program speed; 200usec for SLC, 800usec for MLC. Erase speed, tera : 2~3msec.

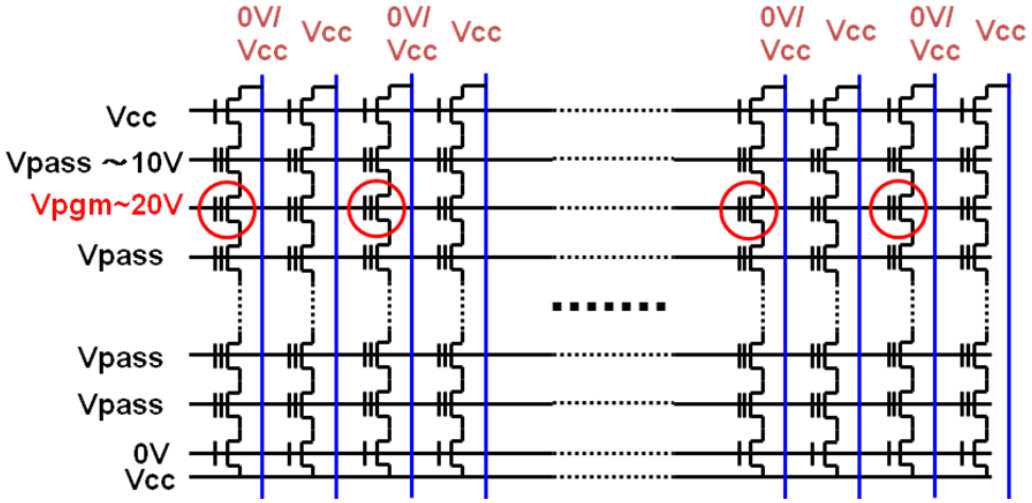


Fig.2.2.6 Array cell program. Page Program : 2~16KByte at the same time. Page Program should be done once. (Prohibit Partial page program). Program speed, tprog : 200usec for SLC, 800~1600usec for MLC. Sequential page program in block (Prohibit random page program).

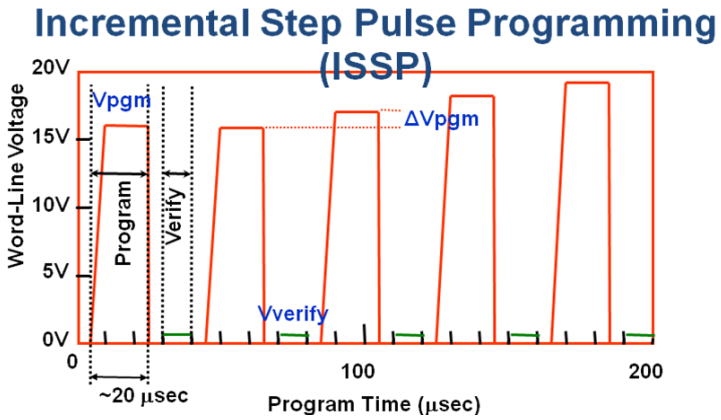


Fig.2.2.7 Incremental Step Pulse Programming (ISSP) waveform. ISPP is used for page program to make a tight cell Vt distribution. Degradation of tunnel oxide can be mitigated due to relaxed maximum electric field in tunnel oxide during program.

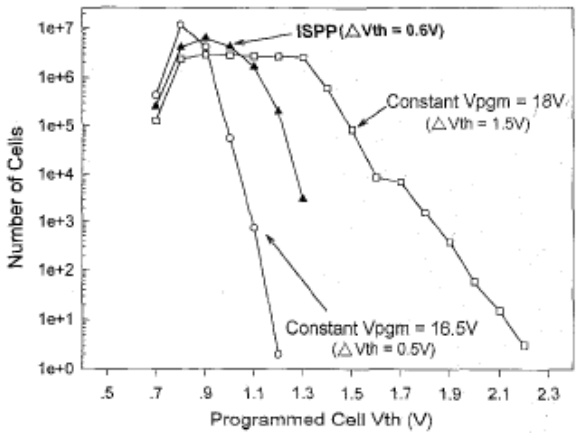


Fig.2.2.8 Comparison of programmed cell threshold voltage distribution in devices with ISPP and without ISPP (constant voltage programming with 16.5 and 18 V).

The erase operations can be performed in block units, as shown in Fig.2.2.9. The wordlines of selected blocks are grounded and the wordlines of unselected blocks are floating. A high erase pulse (~20V) is then applied to the p-well. In the selected blocks, the erase voltage creates a large (~20V**)** potential difference between the p-well and the control gates. This causes FN tunneling of electrons from the floating gate into the p-well, resulting in a typical cell threshold voltage shifts negative. Since over-erasure is not a concern in NAND flash, cells are normally erased to -3 V. Also, the low erased cell threshold voltage provides additional margin against upward threshold voltage shifts that arise from program/erase cycling, program disturb, read disturb and Vt shift by FG-FG coupling (chapter 3.5).

Fig.2.2.10 shows the typical erase characteristics. Cells can be erased to -3V by applying 17~18V, 1msec erase pulse width.

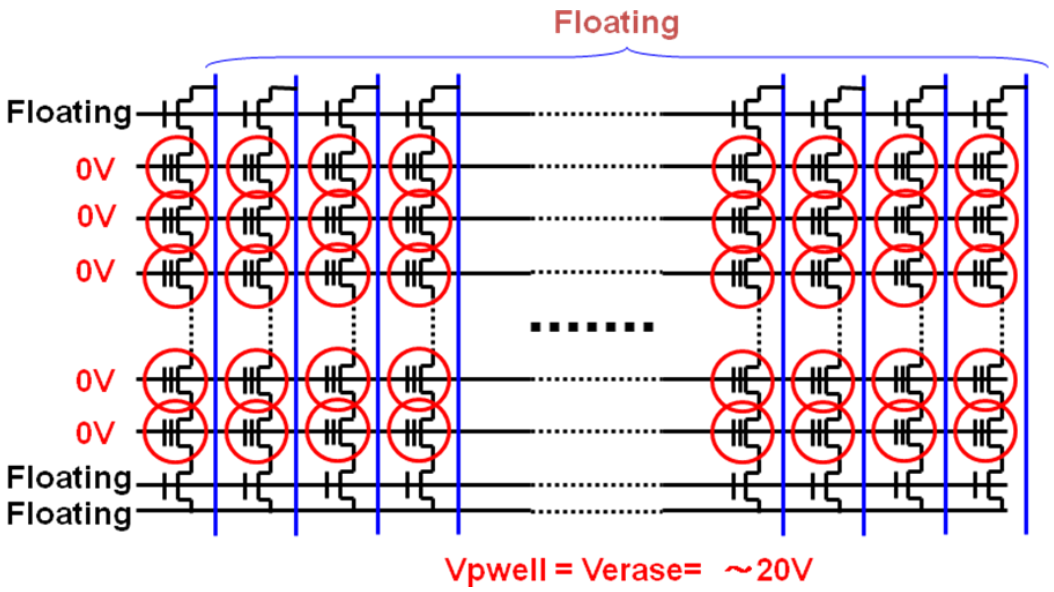


Fig.2.2.9 Array Cell Erase Block Erase : 128~256KByte (2KBytex2x32) erased at the same time. Erase speed, terase : 2~3msec with erase verify.

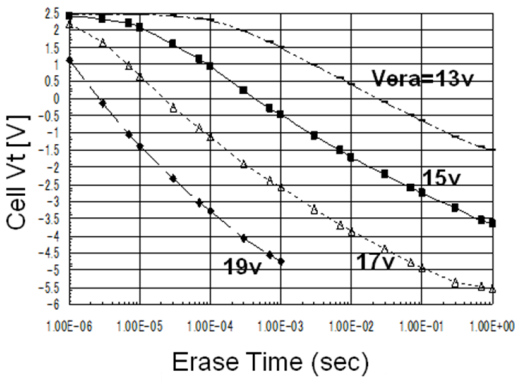


Fig.2.2.10 Erase Characteristics. High Erase voltage can be faster operation. Erase speed, tera : 2~3msec

2.2.3 Program and Erase Dynamics

The device model is described for program and erase dynamics [2.17].

A. Calculation of Tunnel Current

The tunneling current density through the tunnel oxide is approximated by the well-known Fowler-Nordheim equation [2.18], [2.19].

$$J_{tun} = \alpha E_{tun}^2 \cdot (\exp(-\beta/E_{tun})) \qquad (1)$$

where E_{tun} is the electric field in the tunnel oxide, and α and β are constants. The tunnel oxide field E_{tun} is given by

$$E_{tun} = \frac{|V_{tun}|}{X_{tun}} \qquad (2)$$

where V_{tun} is the voltage drop across the oxide and X_{tun} is the thickness. V_{tun} can be calculated from a capacitive equivalent circuit of the cell.

B. Calculation of V_{tun}

In order to gain insight into the basic device operation, a simplified equivalent circuit, shown in Fig.2.2.11, is used. In Fig.2.2.11, C_{pp} is the interpoly capacitance, C_{tun} is the thin oxide capacitance between the floating gate and the substrate. Q_{fg} is the stored charge on the floating gate. V_{tun} can be expressed for an electrically neutral floating gate in terms of simple coupling ratios

$$|V_{tun}|_{write} = V_g * K_w \qquad (3)$$

where

$$K_w = C_{pp}/(C_{pp}+C_{tun}) \qquad (4)$$

and

$$|V_{tun}|_{erase} = V_{well} * K_e \qquad (5)$$

Where

$$K_e = 1- C_{tun}/(C_{pp}+C_{tun}) \qquad (6)$$

The coupling ratios K_w and K_e denote the fraction of the applied voltage that appears across the tunnel oxide. Note that (3) and (5) are applicable only when $Q_{fg} = 0$. During program operation buildup of negative stored charge of the floating gate will reduce the tunnel-oxide voltage according to

$$|V_{tun}|_{write} = V_g * K_w + Q_{fg}/(C_{pp}+C_{tun}) \qquad (3')$$

In the ERASE operation, the initial negative stored charge on the floating gate will increase the tunnel-oxide voltage according to

$$|V_{tun}|_{erase} = V_{well} * K_e - Q_{fg}/(C_{pp}+C_{tun}) \qquad (5')$$

at the end of the erase operation when positive charge is built up on the floating gate, the last term in (5') will reduce the tunnel-oxide voltage.

C. Calculation of *Threshold Voltages*

The initial threshold voltage of the cell, corresponding to $Q_{fg} = 0$ is denoted by V_{ti}. Stored charge shifts the threshold according to the relation

$$\Delta Vt = - Q_{fg}/ C_{pp}$$

Using (3') and (5') for Q_{fg} at the end of the program/erase pulse, the cell's threshold voltages are

$$V_{tw} = V_{ti} – Q_{fg}/C_{pp} = V_{ti} + V_g * (1 - V_{tun}'/(K_w*V_g)) \quad (8)$$

$$V_{te} = V_{ti} – Q_{fg}/C_{pp} = V_{ti} - V_{well} * (K_e/K_w - V_{tun}'/(K_w*V_{well})) \quad (9)$$

Here V_{tw} is the threshold of a programmed cell, and V_{te} is the threshold of an erased cell. V_g and V_{well} are the program/erase pulse amplitudes, respectively, and V_{tun}' is the tunnel-oxide voltage at the end of the pulse. Assuming that the program/erase pulse is sufficiently long, the thin-oxide field will be reduced to below about $1x10^7$ V/cm, when tunneling practically "stops". An approximation of V_{tun}' can be calculated from (2), and substituted in (8), (9) to give the approximate programming window of the cell and its dependence on cell parameters and programming voltage. Typical results are shown in Fig.2.2.12 [2.17].

In order to maximize the cell window at a given tunnel oxide thickness and program/erase voltage, the coupling ratios should approach unity. Both coupling ratios can be increased by reducing C_{tun} and increasing C_{pp}. At a given tunnel-oxide thickness, this is usually achieved by minimizing the thin oxide area and adding extra poly-poly overlap area on the sides of the cell transistor. Typical coupling ratios are about 0.6.

Fig.2.2.13 shows the calculated and measured results for the program operation [2.17]. The threshold voltage as a function of program pulse amplitude are shown. The simulation results fit the measured data closely. And we can see write pulse amplitude and Vt has linear relationship $\Delta Vt = \Delta Vpgm$ in same pulse width. This is important in case of considering ISPP and Vt window setting.

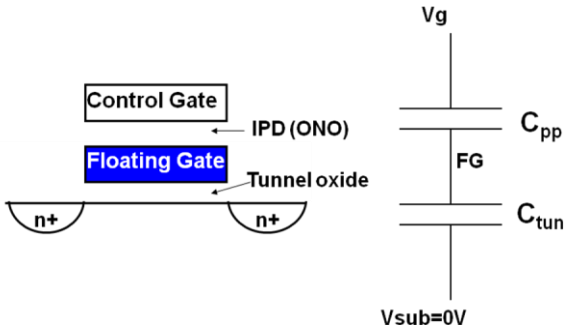


Fig.2.2.11 A simplified capacitive equivalent circuit of the NAND flash cell.

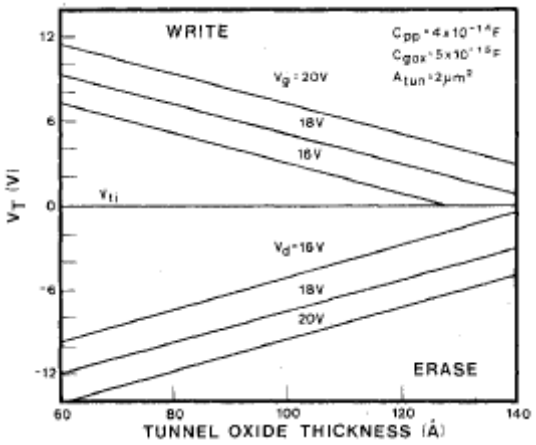


Fig.2.2.12 Program/Erase threshold window versus tunnel oxide thickness, calculated with the approximation of (8), (9), assuming that V_{tun}' = l x 10^7 * X_{tun} at the end of the operation.

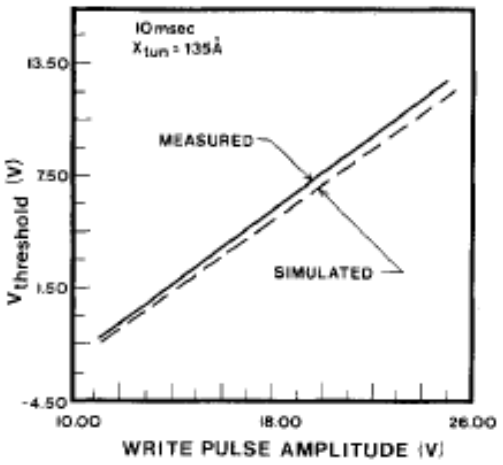


Fig.2.2.13 Measured and simulated threshold voltage as a function of program pulse amplitude, for a fixed program time.

2.2.4 Program Boosting Operation

Program Disturb is a phenomenon that the threshold voltage (Vt) of unselected cell is increased during program operation. The basic program disturb modes are shown in Fig.2.2.14. There are two modes of program disturb. One is “Vpass mode” in selected NAND string, which bit-line (BL) and cell channel are 0V. Vpass (~10V) is applied to control gate (word line) while 0V applied to source and drain (channel). This condition is a weak electron injection mode to FG, then Vt is increased, specially in case of higher

Vpass. The other is “boosting mode” in unselected NAND string. The program voltage Vpgm is applied to control gate, while channel is the boosting voltage. The boosting voltage (~8V) is generated by Vpass voltage of unselected word lines in string. The “boosting mode“ is also in weak electron injection mode. Vt of memory cell is increased, especially in the case of high Vpgm and lower Vpass (lower boosing voltage). As indicated in Fig.2.2.14, Vt distribution tail is mainly increased in L0 or L1 states in MLC Vt setting due to higher tunnel oxide field.

Figure 2.2.15 [2.20] shows program disturb data depended on Vpass. In case of higher Vpass (14~18V), Vt shift of Vpass mode is increased. On the other hand, in case of lower Vpass (~10V), Vt shift of boosting mode is increased. The middle of Vpass voltage (10~14V) have to be used due to small Vt shift (small program disturb). Normally the range of available Vpass voltage is called “Vpass window”, indeed, Vpass region where Vth shift by disturbs does not cause incorrect operation.

There are several program boosting schemes for Multi-level NAND flash cells. Fig.2.2.16 shows three basic boosting schemes. First one is conventional Self-Boosting (SB) scheme. SB scheme is mainly used for SLC (1bit/cell) device. Second one is Local self-boosting scheme [2.14]. The boosting voltage (Vboost) can be increased because adjacent WL cell cut off due to applied 0V. Then program disturb of boosting mode can be improved due to reducing voltage difference between CG (Vpgm) and channel (Vboost). Third one is Erase-Area Self-Boosting scheme (EASB). EASB was widely used for MLC (Multi bit cell) to obtained higher boosting voltage. The reason why higher boosting voltage can be obtained is separated erased cells and programmed cell in string. Due to page program order, source-side cells from selected WL have already been programmed. Boosting efficiency is lower in source side cells. However, drain-side cells from selected WL are still erased state. Boosting efficiency of drain side cells is higher than source-side due to lower cell Vt. Then it is very effective to obtain high Vboost by cutting off boosting node between drain-side and source-side cells. As NAND flash cell scaling, the boosting voltages make higher electric field in source/drain area. Higher electric field generate hot electron and hot hole, and they are unexpectedly injected to FG. In order to relax high electric field, The self-boosting scheme is becoming more advanced and complicate scheme for each generation NAND flash.

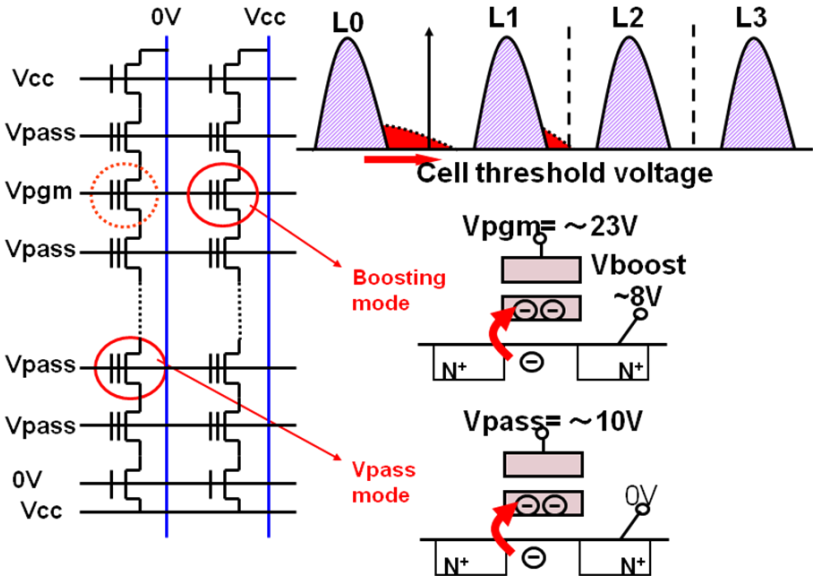


Fig.2.2.14 Program Disturb of NAND Flash cells. Weak electron injection mode is caused in unselected cell. There are Boosting mode and Vpass mode. "Self-boosting" scheme for unselected string is used. The channel in unselected string has boosted up to Vboost~8V.

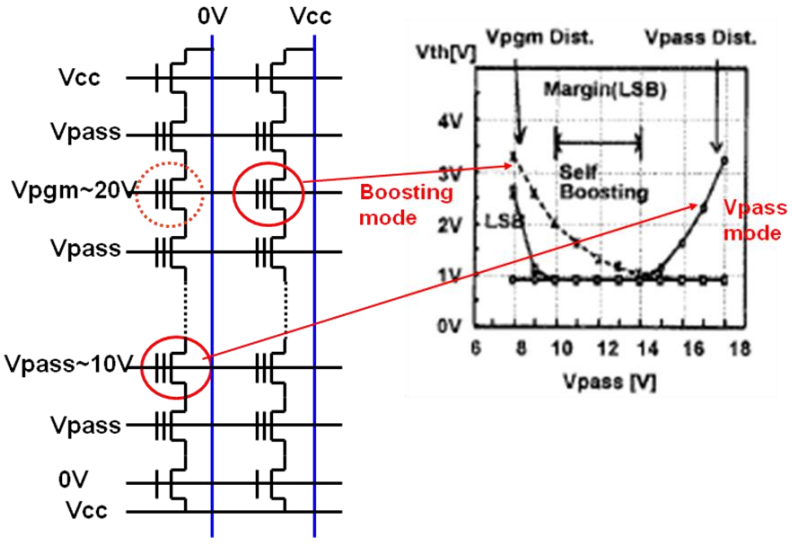


Fig.2.2.15 Vt shift of program disturb, Self-booting. Vpass mode dominates in higher Vpass. Boosting mode dominates in lower Vpass due to low Vboost. Vpass window is between Vpass mode and boosting mode.

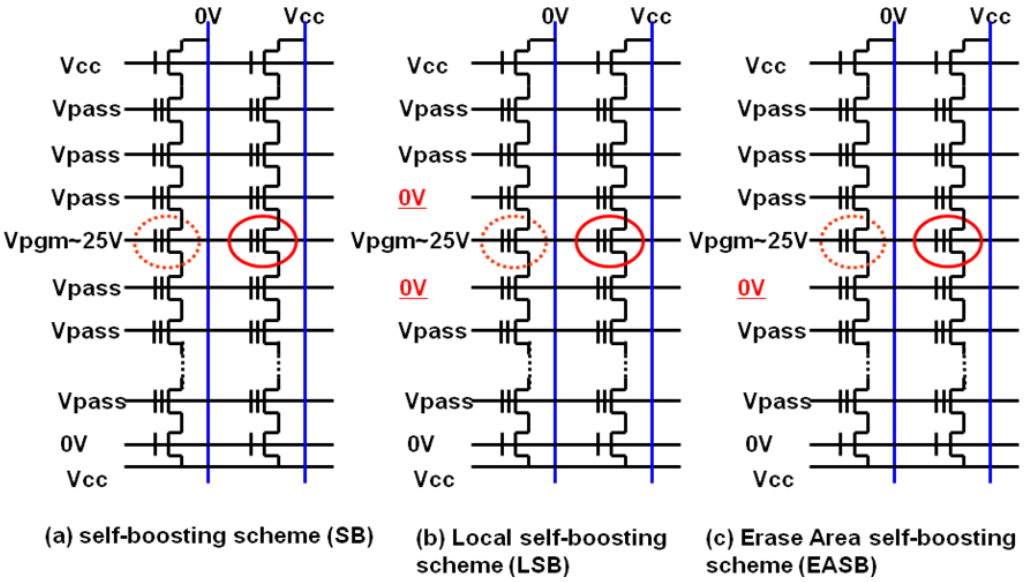


Fig.2.2.16 Self-boosting Schemes. (a) self-boosting scheme (SB), (b) Local self-boosting scheme (LSB) , (c) Erase Area self-boosting scheme (EASB).

2.3 Multi-Level Cell (MLC cell)

2.3.1 Read Window Margin (Cell Vt setting)

Fig.2.3.1 shows Vt distribution setting image of SLC (Single Level Cell) and MLC (Multi-Level Cell, 2bits/cell). SLC has a wider cell Vt window margin, then SLC has a better program and read performance, and also a better reliability than MLC. As described in Chapter 2.2.1 Read operation, the unselected cells have to be pass transistor during reading. Therefore, all cell Vt distributions have to be lower than VpassR, as shown in Fig.2.3.1. This is one of limitation of cell Vt setting.

Fig.2.3.2 shows Read Vt window of MLC cells. Vt window is defined by right side edge of erase Vt distribution and left side edge of L3 Vt distribution, after programmed all pages in string (block). Two programmed Vt distributions of L1 and L2 should be inside of Vt window. And Read Window Margin (RWM) is defined as shown in Fig.2.3.2. As scaling down of memory cell size, RWM has degraded due to increasing impact of many inevitable physical phenomena. Major reliability issues might happen due to narrow cell Vt window margin.

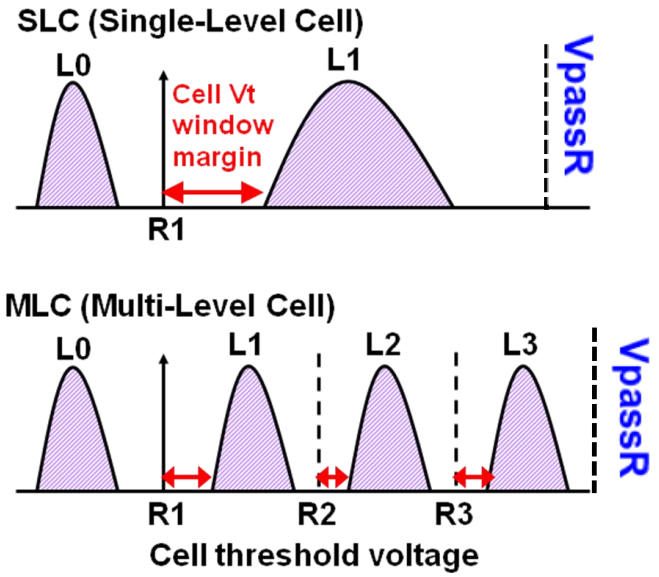
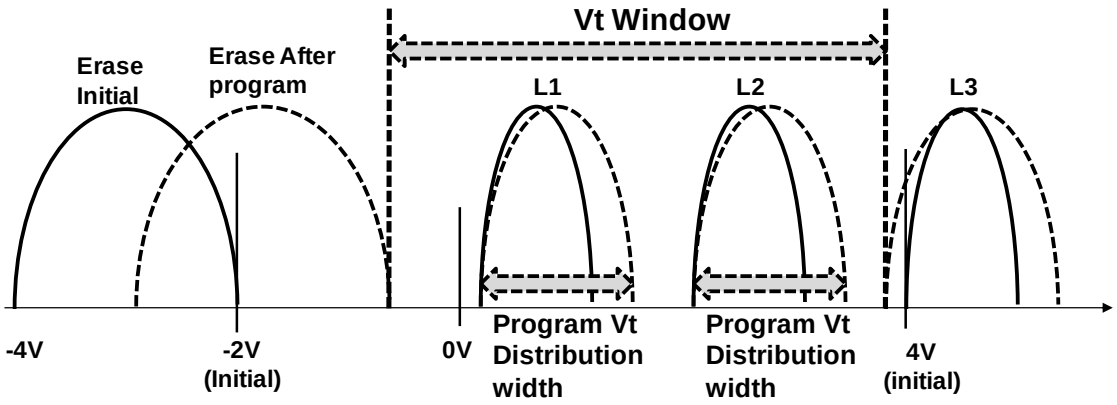


Fig.2.3.1 Cell Vt distribution of SLC and MLC.



Read Window Margin (RWM) = (Vt Window) – 2*(Program Vt Distribution width)

Fig.2.3.2 Read Vt window of MLC NAND cell.

2.4 Summary of Chapter 2

The principle of NAND flash memory has been described in this chapter.

NAND flash device and architecture were shown. NAND flash cell string have series connected floating gate cells with two select transistors. Due to sharing contact area by 2 strings (32 cells x 2), the effective cell size can be reduced. And requirements for scaling down NAND flash cell are also described as scaling of x-direction and y-direction. And then, basic cell operation of NAND flash cells are described, such as

read, program, and erase. Finally, basic concept of MLC read window margin have been explained.

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Chapter 3
NAND Flash Memory Devices

3.1 Introduction

In order to realize low bit cost of NAND Flash memory, the scaling down of memory cell size is most important. In this chapter, NAND Flash memory cell and its scaling technologies are discussed. NAND Flash technology road map and NAND Flash memory cell scaling trend are shown in Figure 3.1.1 and Figure 3.1.2, respectively. Production of NAND Flash was started 0.7um technology on 1992. The LOCOS (LOCal Oxidation of Silicon) isolation was used. It was difficult to scale down of LOCOS isolation width beyond 0.8um width, because junction breakdown voltage and punch-through voltage were degraded as scaling down due to boron diffusion from isolation bottom by LOCOS oxidation process. Then new FTI process (Field Through Implantation process) was developed, as described in chapter 3.2. Due to FTI process, technology node could be scaled down to 0.35um technology, as shown 1) LOCOS cell scaling in Fig. 3.1.1.

Next, Self-Aligned Shallow Trench Isolation cell (SA-STI cell) with Floating Gate (FG) wing had been developed, as described in chapter 3.3. Due to STI, isolation width could be scaled down to 50% (0.8um to 0.4um) and then cell size could be scaled down to 67% (1.2um to 0.8um) in the same design rule, as shown 2) STI cell w/ FG wing in Fig.3.1.1. And also, isolation capability was much improved because of deep isolation of STI. Furthermore, reliability of tunnel oxide was improved due to no STI edge corner in tunnel oxide.

After that, SA-STI cell without FG wing had been developed, as described in chapter 3.4. By using this cell structure, high coupling ratio could be obtained due to large capacitance of IPD using FG side wall, as shown 3) SA-STI cell in Fig.3.1.1. This SA-STI cell has been extensively used for long time of more than 10 years, over 7 generations of NAND Flash product.

The SA-STI cell has a very simple structure, and layout allows for the formation of a very small cell size with bit-line and word-line pitch of 2*F, where F refers to the

minimum feature on the technology. The cell size become ideal $4F^2$, as shown in Fig.3.1.2.

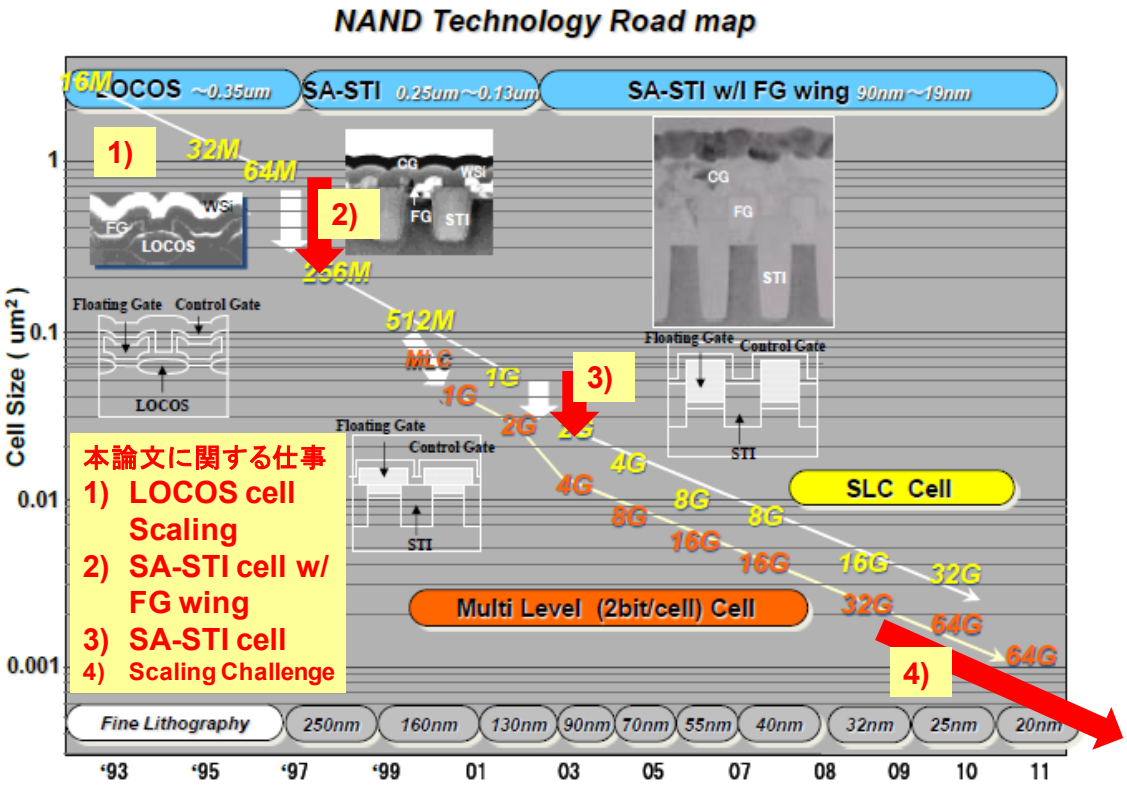

Fig.3.1.1 NAND Technology Roadmap. (modified from [3.1.1].)

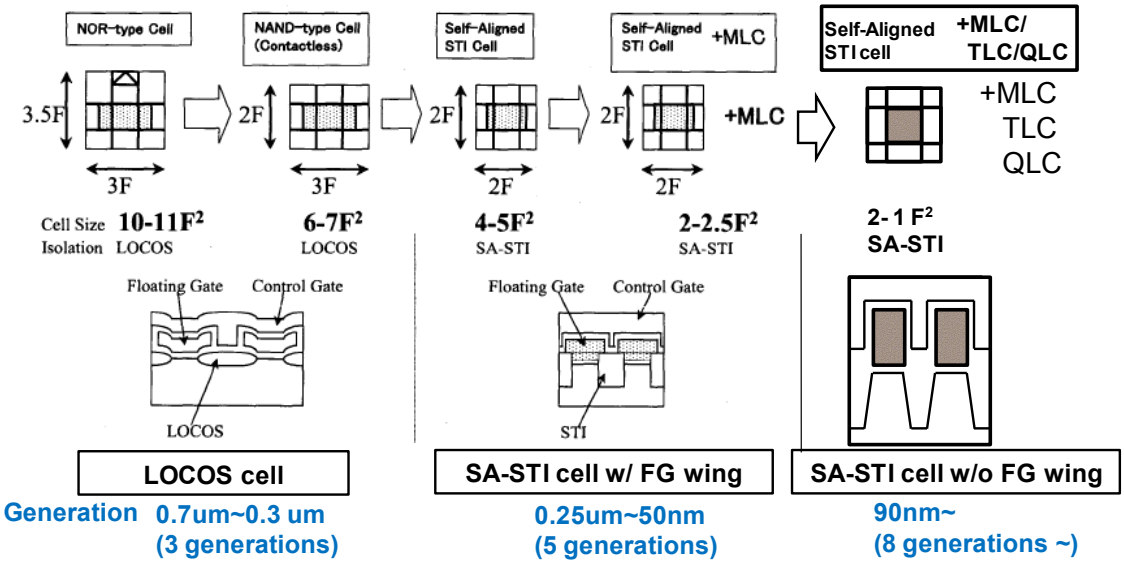

Fig.3.1.2 Scaling trend of planar FG NAND Flash memory cell.

The scaling challenges of the SA-STI cell are discussed beyond 20nm feature sizes, as described in chapter 3.5. The key challenges include the read window margin, structure and high field limitation. For read window margin problem, cell Vt distribution width become wider due to many physical phenomena, such as Floating gate capacitive coupling interference, program electron injection spread, random telegraph signal noise (RTN), etc. For structure limitation, the control gate can no longer be wrapped around the floating gate. This is due to the physical thickness of the IPD, which becomes comparable with the distance between neighboring floating gates. For high field problem, during programming, the electric field between WL and WL (word line) become high (>5MV/cm) as scaling WL dimension.

In chapter 3.6, a Side-WAll Transfer-Transistor (SWATT) cell are discussed for a multi-level NAND Flash memory cell. By using a new SWATT cell, a wide threshold voltage (Vth) distribution could be obtained.

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3.2 LOCOS cell

Abstract ; A small NAND-structure cell of 1.13 μm^2 per bit has been developed in 0.4 μm technology. The chip size of a 64 Mb NAND electrically erasable and programmable read only memory (EEPROM) using this cell is estimated to be 120 mm^2, which is 60% of a 64 Mb DRAM die size. In order to realize the small cell size, 0.8 μm width field isolation is used with Field Through Implantation (FTI) technique. A negative bias of -0.5 V to the P-well of the memory cell is applied during programming. In addition, a bit-by-bit intelligent writing technology allows a 3.3 V data sensing scheme which can suppress read disturb to 1/1000 in comparison with the conventional 5 V scheme. As a result, it is expected that with this technology, 10^6 write and erase cycles can be achieved and that the tunnel oxide can be scaled down from 10 nm to 8 nm.

3.2.1 Introduction

It has been expected that a high-density flash memory [3.2.1][3.2.2] will replace magnetic disk memory [3.2.3][3.2.4] because it has numerous advantages such as small

cell size, fast access time, and low power dissipation [3.2.5]-[3.2.11]. However, in order to replace the magnetic disk, several requirements must be satisfied. The first and most important is low bit cost, which can be attained with small cell size and reduction of the number of fabrication steps. The second item is high reliability, which is related to the write/erase endurance and data retention. The target specification of reliability is 10-year long data retention time after 1 million write/erase cycles. The other items are high-speed programming (1μs/Byte), small block size (4k Byte) and single 3.3 V power supply.

A NAND-structure electrically erasable and programmable read only memory (EEPROM) had proposed [3.2.12]-[3.2.15]. This structure reduces the cell size without scaling of the device dimension. The operation method for the NAND cell had also developed. A bi-polarity Fowler-Nordheim tunneling write/erase method [3.2.14][3.2.16] can be used. This method achieves high reliability, high-speed programming and small sector size. Moreover, a new bit-by-bit verify sequence [3.2.17] results in a tight distribution of cell threshold voltage after writing. As a result, 3.3 V single power supply operation is possible. Therefore, the NAND EEPROM is the most promising candidate to replace magnetic disk memory.

In chapter 3.2, an advanced NAND-structure cell is described to produce 64Mbit EEPROMs [3.2.18][3.2.19]. A small cell size of 1.13μm^2, including the select-transistor and drain contact area, was obtained under a 0.4μm design rule. The key technology in obtaining small cell size is the bit-line isolation technology, which uses the field through isolation (FTI) process and a negative bias to the p-well during the write operation. Read disturb can be ensured for more than 10 years even after 1 million write/erase cycles.

3.2.2 Advanced NAND-Structure Cell

A. Scaling of NAND-structure cell

The NAND-structure cell [3.2.12]-[3.2.16] arranges a number of bits in series. The current EPROM cell has one contact area per two bits. However, for the NAND-structure cell, only one contact hole is required per two NAND structure cells. As a result, the NAND-structure cell realizes a smaller cell area per bit than the current EPROM.

Figure 3.2.1 compares the top view of the advanced 0.4μm NAND-structure cell with that of the 0.7μm conventional one. Figure 3.2.2 shows the cross-sectional view of

the NAND-structure cell. This NAND-structure cell has 16 memory transistors arranged between two select transistors in series. The word-line pitch is 0.8μm (line/space =0.4μm/0.4μm). The bit-line pitch can be reduced to 1.2μm by using 0.8μm field isolation technology. Figure 3.2.3 shows the cross-sectional view of the NAND-structure cell SEM photograph after the self-aligned stacked etching process. The floating gates are made of first-layer polysilicon (phosphorus-doped). The control gates are made of second-layer polysilicon (phosphorus-doped polysilicon/tungsten-silicide). The process technology is summarized in Table I.

As the design rule of the word line is scaled, it becomes apparent that the NAND-structure cell has such advantages as scaled down gate length of the memory cell in comparison with the NOR-type Flash memory cell, because the NAND-structure cell is punch-through free since there is no voltage difference between the drain and source during programming and erasing. Moreover, the NOR-type Flash memory cell has a large gate-drain overlap region, because the source/drain impurity concentration must be high enough for hot-electron injection. However, the NAND-structure cell has a very small gate-drain overlap region because the impurity concentration of the diffusion layer can be less than $10^{18}cm^{-3}$. As a result, the gate length of the NAND-structure cell can be smaller than that of the NOR-type Flash memory cell.

With respect to scaling in the bit-line direction (bit-line pitch), isolation technology is very important, as discussed in the next section of 3.2.3.

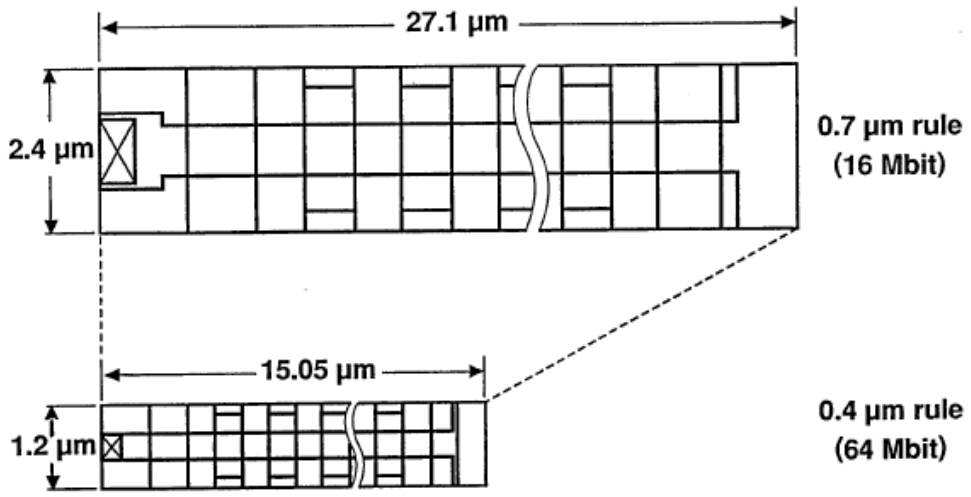

Fig.3.2.1. Top view of an advanced 0.4-μm-rule NAND-structure cell in comparison with that of a 0.7um rule cell. This NAND-structured cell has 16 memory transistors arranged in series between two select transistors. Word-line and bit-line pitches are 0.8μm (L/S=0.4μm/0.4μm) and 1.2μm, respectively. The cell size is $1.13\mu m^2$, including

the select transistors and the drain contact area.

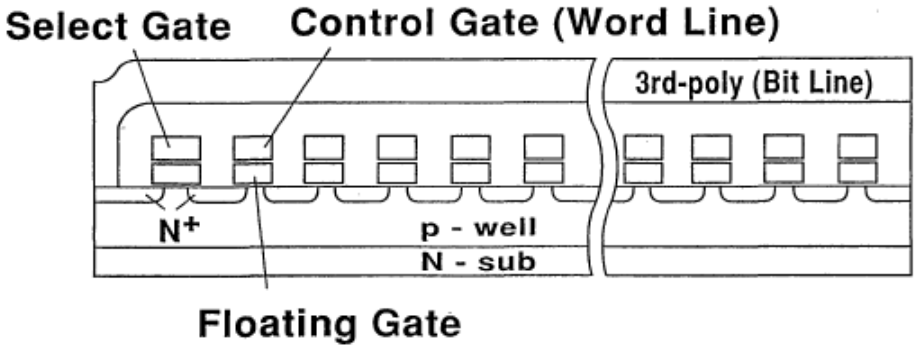

Fig.3.2.2. Cross-sectional view of an advanced NAND-structure cell

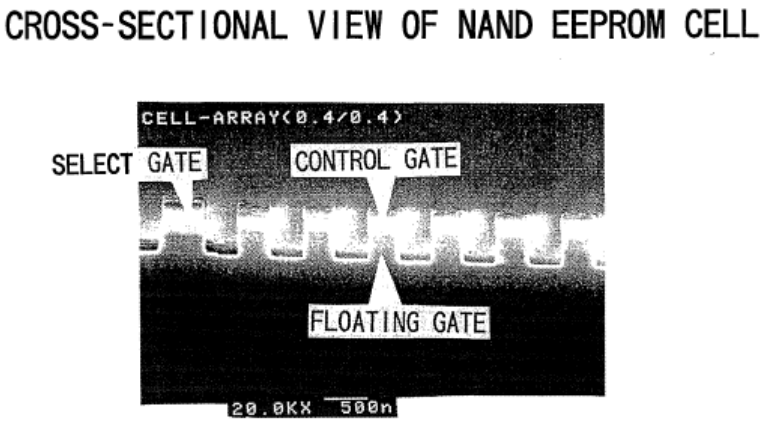

Fig.3.2.3. Cross-sectional SEM photograph of NAND-structure cell after the self-aligned stacked etching process.

Table I. Process technology.

Process	double well CMOS triple-poly-silicon technology 1 layer-metal	
Cell	cell size W/L tunnel oxide interpoly dielectric	$1.13\ \mu m^2$ $0.4/0.4\ \mu m$ 80 Å ONO 200 Å (effective)
Peripheral	L poly N-ch P-ch	$0.8\ \mu m$ $0.8\ \mu m$

B. Operation of *NAND-structure cell*

The operating conditions are shown in Table II. During writing, 18 V is applied to the selected control gate while the bit lines are grounded, electrons tunnel from the substrate to the floating gate, resulting in a positive threshold voltage shift. If a voltage of 7 V is applied to the bit line, tunneling is inhibited, and the threshold voltage remains the same. The negative bias to the p-well is effective in preventing the parasitic field transistor from turning on, as will be discussed in the next section. During erasing, 20 V is applied to both the p-well and the substrate while keeping the bit lines floating and all the selected control gates grounded. Electrons tunnel from the floating gate to the substrate, and the threshold voltage of the memory cells becomes negative.

The reading method is also shown in Table II. Zero volt is applied to the gate of the selected memory cell, while 3.3 V (Vcc) is applied to the gates of the other cells. Therefore, all of the other memory transistors, except for the selected transistor, serve as transfer gates. A cell current flows if an selected memory transistor is in the depletion mode. On the other hand, cell current does not flow if the memory cell is programmed to be in the enhancement mode.

Table II. Operation conditions.

	Write	Erase	Read
Bit line	0/7 V	open	1.5 V
Select gate	7 V	20 V	3.3 V
Control gate 1	7 V	0 V	3.3 V
Control gate 2	18 V (selected)	0 V	0 V
⋮		⋮	
Control gate 16	7 V	0 V	3.3 V
Select gate	0 V	20 V	3.3 V
Source	0 V	open	0 V
P-well	−0.5 V	20 V	0 V
N-sub	3.3 V	20 V	3.3 V

3.2.3 Isolation Technology

For the NAND EEPROM, high-voltage field isolation technology is important to reduce the bit-line pitch. The isolation between the bit lines must satisfy two requirements, as shown in Fig.3.2.4. One is the punch-through or the junction breakdown voltage of the bit-line junction area. During programming, 7 V is applied to the bit line to prevent electron injection in cells that should remain in the erased state. Zero volt is applied to a bit line which is connected to a cell that should be programmed. The punch-through voltage between neighboring bit-line junctions must be higher than

7 V, as well as the bit-line junction breakdown voltage. Another requirement is a high threshold voltage of the parasitic field transistor. During programming, the selected control gate is biased with a high voltage of 18 V which may easily turn on the field transistor between neighboring bits (Table II).

In order to avoid bit-line junction breakdown/punch-through and to prevent the field transistor from turning on, the Field Through Implantation process (FTI process) and p-well negative bias method have been developed [3.2.18][3.2.19], as shown in Fig.3.2.5. In the FTI process, the boron ions (160 keV, le13 cm^{-2}) are implanted to form a field stopper after LOCOS fabrication. The field oxide thickness at field-through implantation is 420 nm. The punch-through voltage and the threshold voltage of the parasitic transistor increase without decreasing the junction breakdown voltage, because the lateral diffusion of the boron stopper impurity is decreased in comparison with the conventional field stopper implantation before LOCOS fabrication. A negative p-well bias prevents punch-through and increases the threshold voltage of the parasitic field transistor.

Figure 3.2.6 shows the breakdown voltage between two neighboring bit-lines as a function of the bit-line contact distance. The breakdown voltage is ensured to be higher than 7V, in the case of a negative-biased p-well. Figure 3.2.7 shows the threshold voltage of the parasitic field transistor. By using the FTI process, the threshold voltage of the 0.8μm field transistor becomes more than 28 V. Moreover, a negative bias of -0.5 V is applied to the p-well to increase the threshold voltage of the parasitic field transistor (Vtf). In comparison with a zero-biased p-well, Vtf is increased to more than 30 V. Therefore, the field width margin is increased from 0.05μm to 0.15μm. As a result, a very small bit-line pitch of 1.2μm can be realized.

The FTI process also reduces the body effect of the cell transistors, because the boron impurity concentration under the channel region of the cell transistors and the select transistor become lower. The decrease of the body effect results in an increased cell current. Figure 3.2.8 shows the cell current of a NAND cell as a function of the cell gate length. The cell currents were measured at the nearest cell from the bit-line contact side, which has the smallest cell current among all cells because that cell should be strongly influenced by the body effect due to the series resistance of the other cells. The threshold voltage of the selected cell is -1V and -3V, the threshold voltage of the unselected cells, which connected in series, is from 0.5 to 1.5 V. In the case of the FTI process, the cell current is larger than in the conventional case.

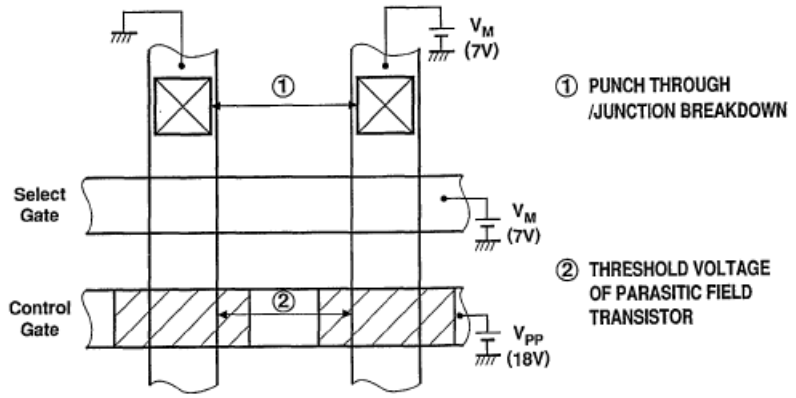

Fig.3.2.4. Isolation between two neighboring bit lines: (1) punch-through or junction breakdown in the bit-line contact area, (2) the threshold voltage of the parasitic field transistor.

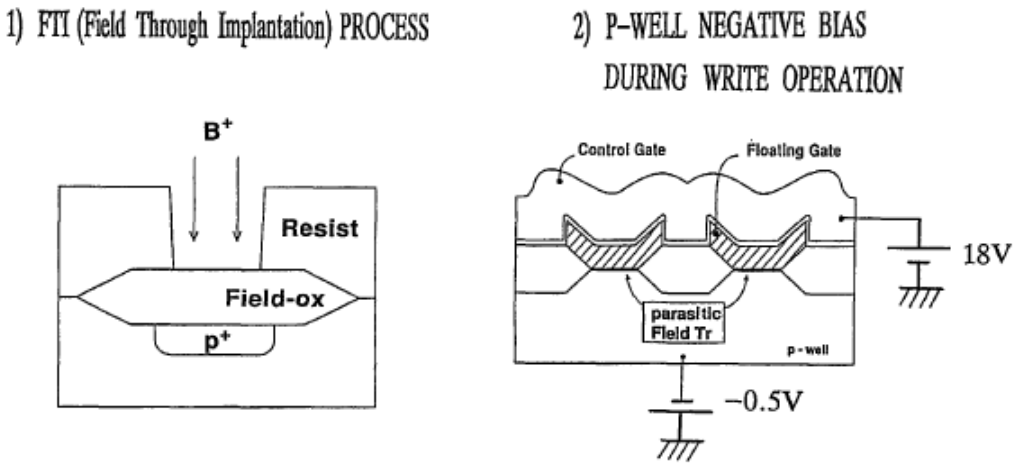

Fig.3.2.5. The 0.8-μm-wide high-voltage field isolation technology

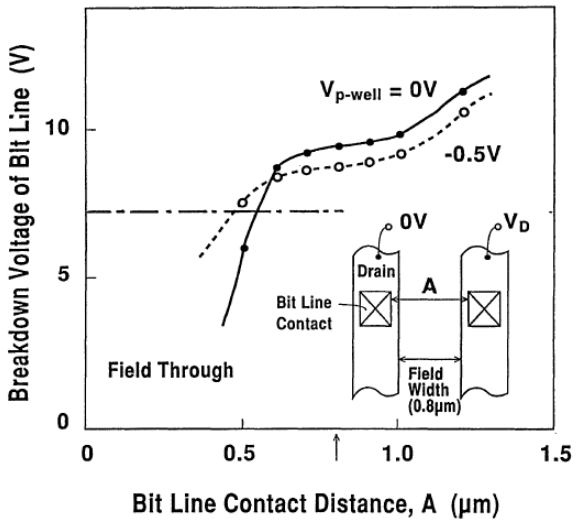

Fig.3.2.6. The punch-through voltage of the bit-line junction. The punch-through voltage is higher than 7V at a 0.8μm bit-line contact distance.

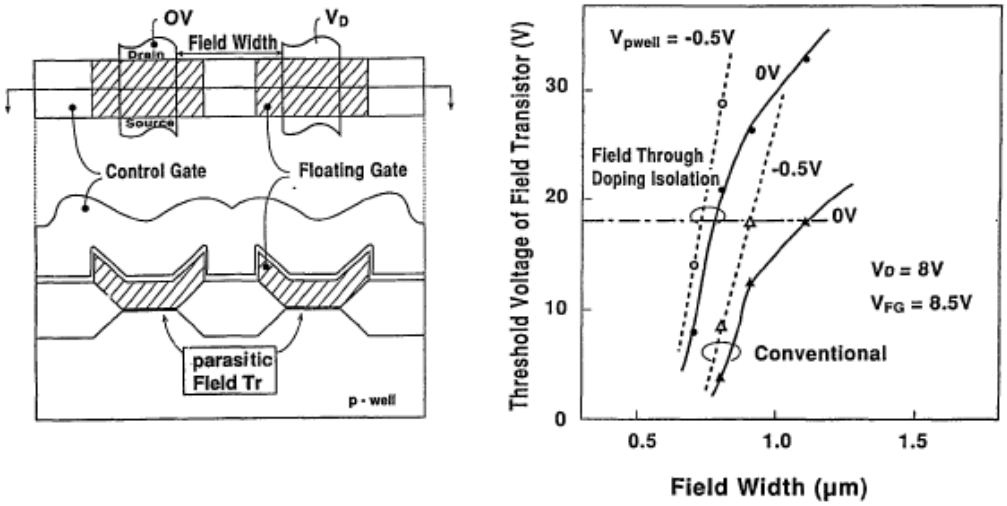

Fig.3.2.7. The threshold voltage of the parasitic field transistor as a function of the field width. By using a field-through-implantation process (FTI process), the threshold voltage of a 0.8μm field transistor becomes higher than 28 V when -0.5 V is applied to the p-well.

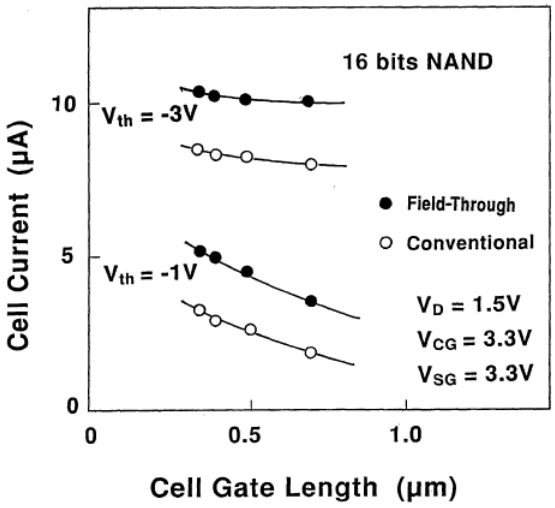

Fig.3.2.8. The cell current during a read operation using both the field-through-implantation (FTI) process and the conventional process. The cell current of the FTI process is larger than that of the conventional process due to the suppression of boron diffusion to the channel region.

3.2.4 Reliability

Figure 3.2.9 shows the program and erase cycling endurance characteristics of a NAND cell with 8- and 10-nm-thick tunnel oxide using the bipolarity write/erase method [3.2.14][3.2.18]. This method guarantees a wide cell threshold window of as large as 4 V, even after 1 million write/erase cycles. In the 8 nm tunnel oxide cell, window narrowing can hardly be seen due to the small number of electron traps in the 8 nm tunnel oxide.

Read disturb occurs as a weak programming mode. When a certain positive voltage is applied to the control gate during read operation, a small Fowler-Nordheim tunneling current flows from the substrate to the floating gate. Unfortunately, the tunnel oxide leakage currents, which are induced by the program and erase cycling stress, degrade the read disturb of the memory cell, as shown in Fig.3.2.10. In order to suppress the read disturb, the applied gate voltage must be lowered. A reduction of the gate voltage from 5 V to 3.3 V allows the downscaling of the tunnel oxide from 10 nm to 8 nm (Fig.3.2.11). Sensing at 3.3 V can be performed by a bit-by-bit verified programming scheme [3.2.17], which results in a written cell threshold voltage between 0.5V and 1.8V.

Even for an 8nm tunnel oxide thickness, read disturb suppression can be ensured for more than 10 years even after 10^6 W/E cycles, as presented is Fig.3.2.11. By scaling down the tunnel oxide thickness from 10 nm to 8 nm, the program voltage can be reduced from 21 V to 18 V, which allows the design of more compact peripheral circuits such as row decoders and sense amplifiers.

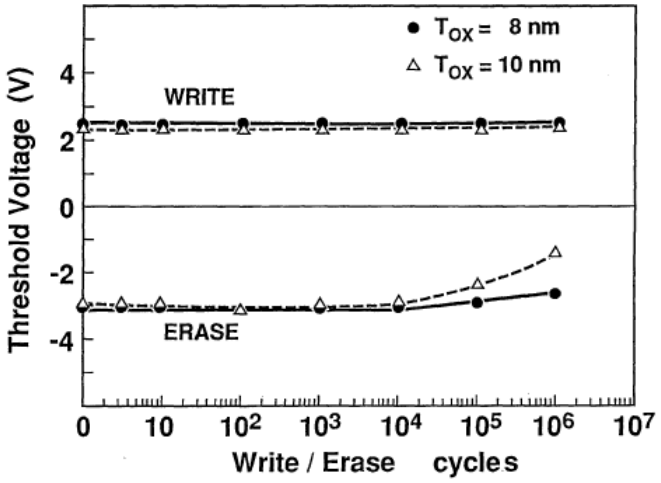

Fig.3.2.9. Program and Erase cycling endurance characteristics. The threshold voltage is defined as the control gate voltage which flows a drain current of 1μA with a

drain-source voltage of 1.5V. For an 8 nm tunnel oxide, write; Vcg=18V, 0.1ms, and erase; Vp-well=20V, 1ms. For a 10nm tunnel oxide, write: Vcg=20.4V, 0.1msec, erase; Vp-well=22.7V, 1msec. Window narrowing is not almost observed up to 1 million write/erase cycles.

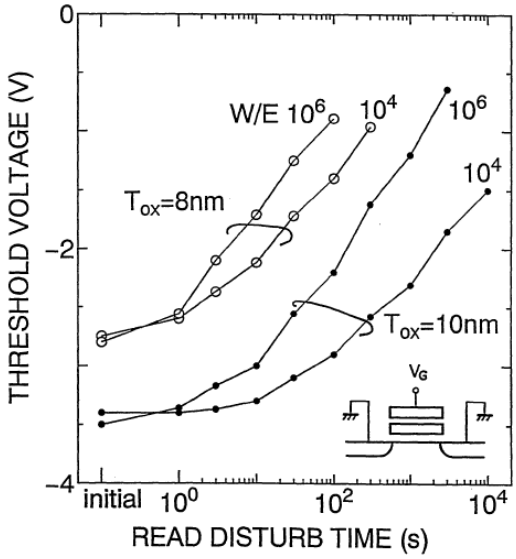

Fig.3.2.10. The read disturb characteristics of a NAND Flash cell with 8 and 10nm tunnel oxide thickness. The voltage of control gate (V_G) is 9V. The threshold voltage is measured under the same condition as in Fig.3.2.9.

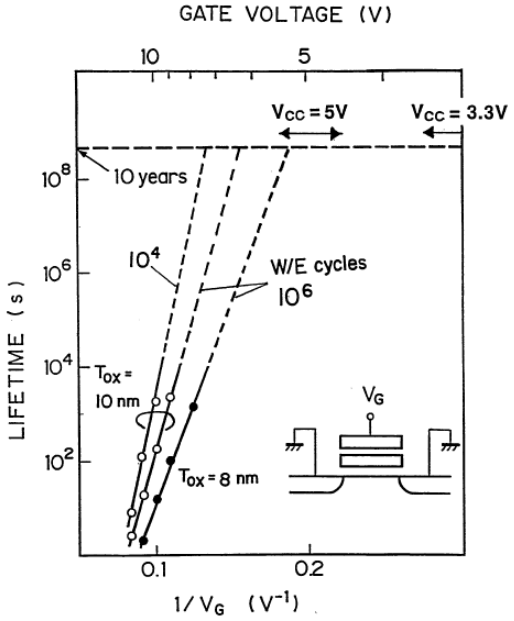

Fig.3.2.11. The read disturb time is defined as the time at which Vth reaches -1.0 V during the applied gate voltage stress. Even if 8 nm tunnel oxide thickness is used, the

read disturb time is far more than 10 years when a 3.3+/-0.3 V supplied voltage (Vcc) is used.

3.2.5 Summary

A 1.13μm^2 memory cell for a 64 Mbit NAND EEPROM has been successfully developed using 0.4 μm technology. High-voltage field isolation technology realizes a very small bit-line pitch of 1.2μm. The tunnel oxide thickness can be scaled down from 10 nm to 8 nm, and 3.3V operation is possible using a bit-by-bit verify programming method. This technology is suitable for realizing a low-cost and highly reliable memory chip, which may lead to the replacement of hard disk memories in the near future.

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3.3 Self-Aligned STI cell (SA-STI cell) with FG wing

Abstract ; A novel high density $5*F^2$ (F; Feature size) Self-Aligned Shallow Trench Isolation cell (SA-STI cell) technology is described to realize a low cost and high reliability NAND flash memories. The extremely small cell size of $0.31um^2$ has been obtained for the 0.25um design rule. To minimize the cell size, a floating gate is isolated with a shallow trench isolation (STI) and a slit formation by a novel SiN spacer process, which has made it possible to realize a 0.55um-pitch isolation at a 0.25um design rule. Another structural feature to the cell and its small size is the borderless bit-line and source-line contacts which are self-aligned with the select-gate. The proposed NAND cell with the gate length of 0.2um and the isolation space of 0.25um shows a normal operation as a transistor without any punch-through. A tight distribution of the threshold voltages (2.0V) in 2Mbit memory cell array is achieved due to a good uniformity of the channel width in the SA-STI cells. And also, the peripheral low voltage CMOS transistors and high voltage transistors can be fabricated at the same time by using the self-aligned STI process. The advantages are (1) The number of process steps is reduced to 60% in comparison with a conventional process, and (2) high reliability of the gate oxide is realized even at high voltage transistors because a gate electrode does not overlap the trench corner. Therefore this SA-STI process integration combines a small cell size (a low cost) with a high reliability for a manufactuable 256Mbit and lGbit flash memory.

3.3.1 Introduction

The high-density flash memories [3.3.1]-[3.3.4] have been receiving much attention for application to the silicon files used in digital still cameras and handheld computer devices as a portable mass storage. One of the most important factors in the mass storage memory is the low bit cost which can be attained by a shrinkage of a cell size and reduction of the number of fabrication steps.

This section describes a novel high density $5*F^2$ (F: feature size) NAND STI cell technology [3.3.5] and peripheral transistors devices [3.3.6] which has been developed for a low bit-cost flash memories. The three key technologies to minimize the cell size have been introduced as shown in Fig.3.3.1. The Self-Aligned shallow trench isolation cell (SA-STI cell) has a high coupling ratio with a thick floating gate [3.3.7]. However, its high aspect ratio of the gate space has made it difficult to control the planarization

process of the trench isolation by chemical mechanical polishing (CMP). To overcome this problem, a stacked floating gate structure is applied. A first thin poly-Si gate is self-aligned with the active area of the cells to control the channel width precisely. A global planarization by CMP process is very controllable due to the reduction of the gate space aspect. A second poly-Si gate is formed on the first poly-Si gate to achieve a high coupling ratio (>0.6) of the cells. The second poly-Si gate is patterned with spacing of 0.15um by a novel SiN spacer process. This process has made it possible to realize 0.55um-pitch isolation. Another feature of integration to the cell and its small size is the borderless bit-line and source-line contacts which are self-aligned with the select-gate. By the above technologies, an extremely small cell size of 0.31um^2 has been obtained for the 0.25um design rule.

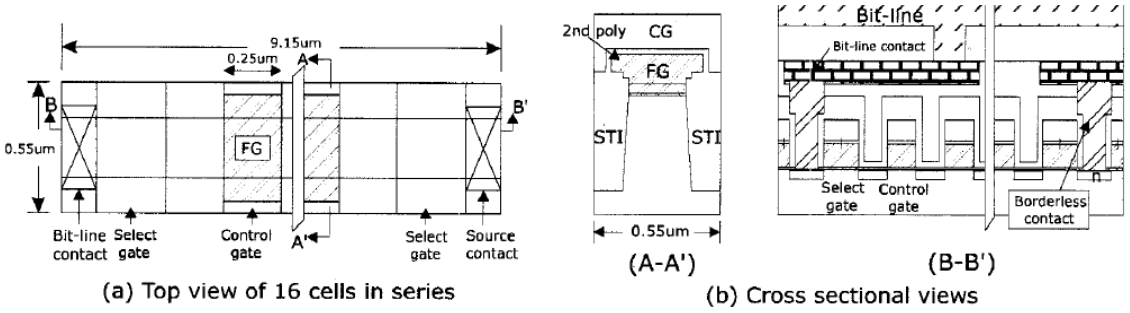


Fig.3.3.1 Schematic view of the proposed NAND STI cells : (a) top view of 16 NAND cells in series (b) cross sectional views of A-A' and B-B' in (a), respectively. Three key technologies to achieve 5*F^2 (F:feature size) cell size has been introduced. (1) A stacked floating gate structure has been applied in order to reduce the gate space aspect. A 1st poly-Si gate is self-aligned with the active area. A 2nd poly-Si gate is formed over the exposed 1st gate to achieve a high coupling ratio (>0.6) of the cells. (2) The 2nd poly-Si gate has been patterned with spacing of 0.15um by a novel SiN spacer process. This process has made it possible to realize 0.55um-pitch isolation. (3) The borderless bit-line and source-line contacts which are self-aligned with the select-gate can eliminate a space between the contacts and the gate.

3.3.2. Fabrication process flow

The process flow of the proposed SA-STI cell with FG wing is outlined in Fig.3.3.2. The active area is isolated by the STI formation using a self-aligned mask of a first thin poly-Si gate (a). After CVD SiO_2 deposition and planarization by CMP, the second poly-Si gate is deposited on the exposed first poly-Si layer, resulting in the

stacked floating gate structure (b). The second poly-Si layer is striped with spacing of 0.15um which is less than a design rule by a novel SIN spacer process as follows. A SiN mask is patterned at spacing of 0.25um, and a 50nm-thick spacer SIN is then deposited. By etching the SiN mask back, a stripe mask pattern with 0.15um space is obtained (c). A SEM micrograph in Fig.3.3.2 shows the patterned second poly-Si gate. After removal of the SiN mask, an inter-poly dielectric (ONO) and the control gate are successively deposited (d). The control gate and the floating gate are continuously patterned, followed by deposition of a barrier SiN layer and an interlayer. The SiN layer covering the control gate prevents a short circuit between the gate and the borderless contacts. Finally, a doped poly-Si is filled with in the bit-line contact and source-line contact, and etched back, followed by the metallization. Fig.3.3.3 and Fig.3.3.4 show the cross-sectional SEM micrographs of the $5*F^2$ memory cell array with a cell size of $0.31um^2$ using 0.25um design rule. The key process parameters are listed in Table I.

Figure 3.3.5 shows the schematic view of SA-STI cell and peripheral transistor. The comparison between a novel process and a conventional process is schematically shown in Fig.3.3.6. The number of fabrication steps of the process is reduced to about 60%. The memory cells and the peripheral transistors can be formed simultaneously without additional process steps.

First, a retrograde well profile is formed by a high energy ion implantation. Each implantation is carried out for a well formation, a field punch-through stopper, and a channel threshold adjustment. Next, 40nm-thick gate oxides for the high voltage transistors and 9nm-thick gate oxides for the cells and the low voltage transistors are formed, and then 1st poly-Si layer for the floating gate and a SiN layer are successively deposited, as shown in Fig.3.3.6(a). The shallow trench, which is self-aligned with the 1st poly-Si layer, is etched, followed by SiO_2 filled-in, planarization by CMP, as shown in Fig.3.3.6(b). After the SiN mask removal and 2nd poly-Si layer deposition, the 2nd poly-Si layers are patterned with a 0.15um-space by a SiN spacer process. The stacked poly-Si structure acts as the floating gate of the cells and the gate electrode of the peripheral transistors. Then, ONO of an inter-poly dielectric is deposited, as shown in Fig.3.3.6(c).

Next, a WSi polycide layer for the control gate of the cell is deposited, and then the polycide layer, ONO, the stacked poly-Si layer are continuously patterned, as shown in Fig.3.3.6(d). The peripheral gate electrode is also patterned with the cell. The polycide layer in the peripheral transistors is partially removed for a gate contact formation.

Finally, interconnections and peripheral contacts are formed by a dual damascene process. Fig.3.3.7 shows the cross-sectional SEM micrographs of the cell and the

peripheral gate. The main device parameters of peripheral devices are also summarized in Table 1.

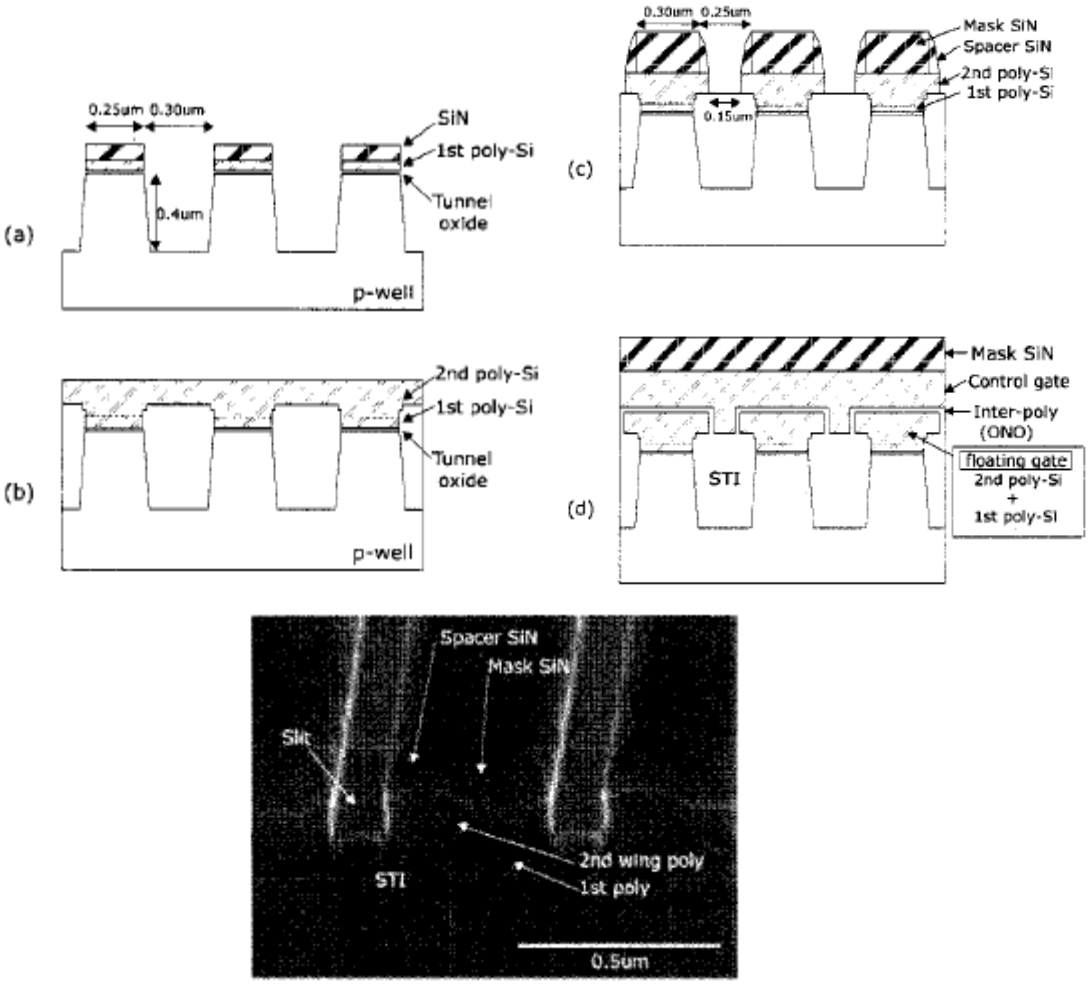


Fig.3.3.2 Process flow of the proposed SA-STI cell with FG wing. (a) Trench etching, (b) LPCVD SiO2 fill-in and planarization by CMP, 2nd poly-Si gate deposited, (c) floating gate formation by SiN spacer process, (d) ONO and the control gate formation. SEM micrograph shows 2nd poly-Si patterned by SiN spacer process.

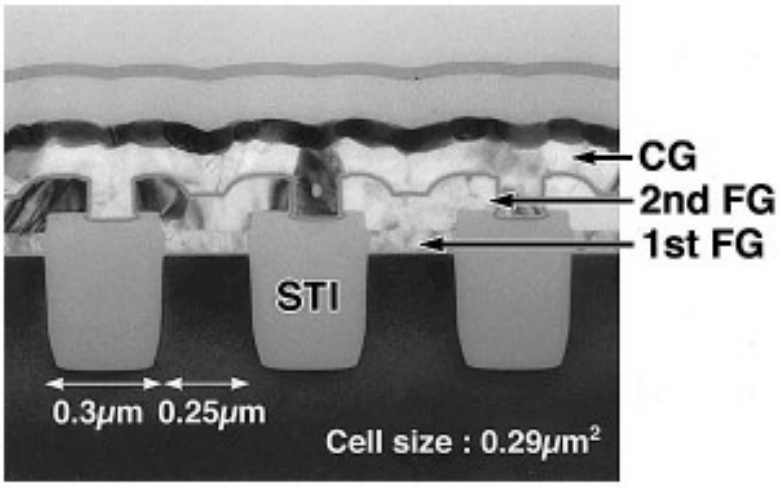


Fig.3.3.3 Cross sectional SEM micrographs of the cell, parallel to the control gate.

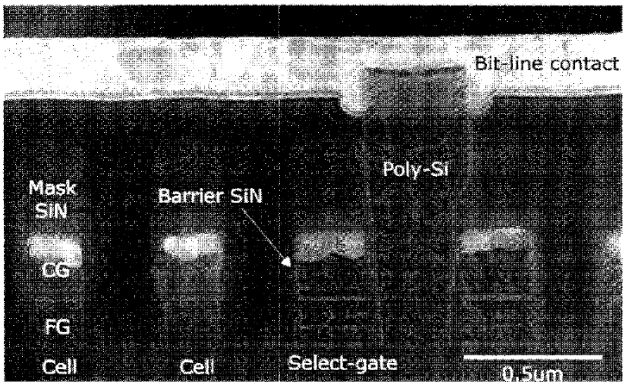


Fig.3.3.4 Cross sectional SEM micrographs of the cell, parallel to the bit line.

Table.1 The main device parameters.

Technology		
0.25um Double Well CMOS		
Self-Aligned Shallow Trench Isolation		
Cell	Tunnel Oxide	9.0nm
	Gate Length	0.25um
	Channel Width	0.25um
	Cell Size	0.31um^2
Peripheral		
High Voltage	Gate Oxide	40.0nm
Low Voltage	Gate Oxide	9.0nm
NMOS Effective Gate Length		0.28um
PMOS Effective Gate Length		0.38um

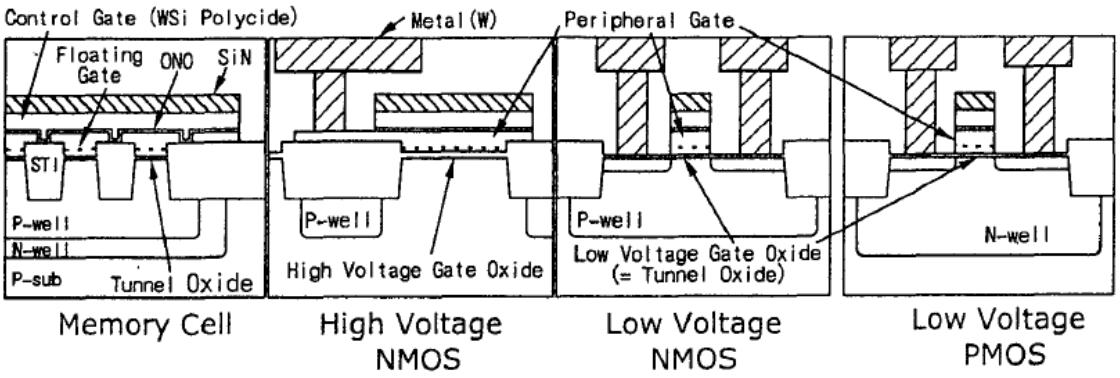


Fig.3.3.5 The schematic view of proposed flash memory.

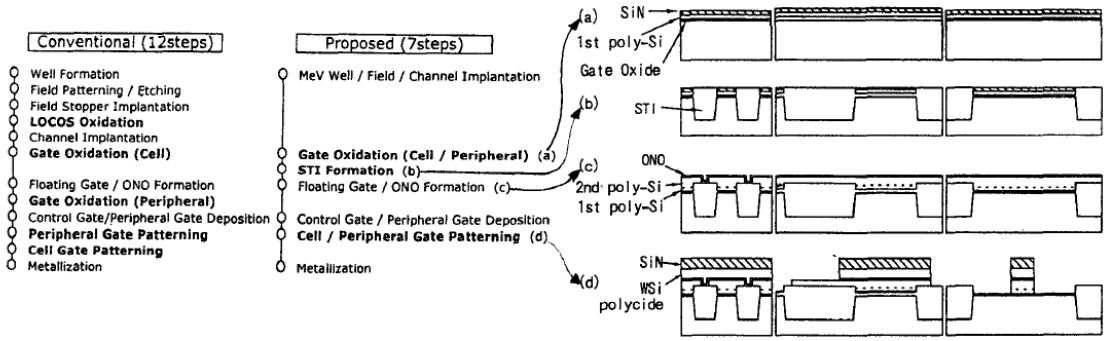
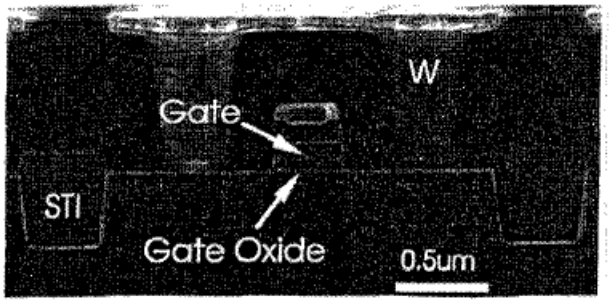
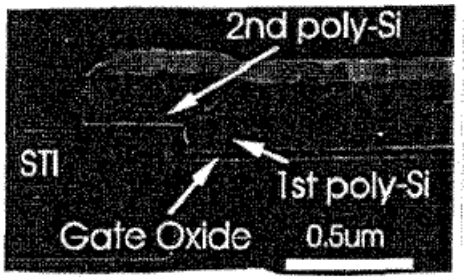


Fig.3.3.6 The process sequence of proposed self-aligned STI.



(a)



(b)

Fig.3.3.7 Cross-sectional SEM micrographs. (a) SEM micrograph of peripheral transistor. (b) SEM micrograph of peripheral gate electrode. The gate electrode is self-aligned with STI.

3.3.3 Characteristics of SA-STI with FG wing cell

Fig.3.3.8 shows a bit-line junction breakdown characteristics as a function of the isolation width. There occurs no field punch-through between the bit-line contacts at the STI width of up to 0.25um with an implantation of Boron for the field stopper. Moreover, the 0.4um-thick STI field oxide results in a high threshold voltage(>30V) of the parasitic field transistor between the neighboring bits. Fig.3.3.9 shows that the threshold voltage of the cell transistors shows a weak dependence on the channel width because no Boron atoms implanted for the field stopper diffuses into the channel region from the trench bottom. From these results, the STI cell is very suitable for scaling of the isolation pitch.

Fig.3.3.10 shows that no anomalous hump is observed in the sub-threshold characteristics of the wide channel transistors with W=10 um since the floating gate never overlap the STI corners. In case of the NAND cell transistors, the maximum drain voltage of Vcc is applied only in the read operation. Fig.3.3.11 shows the Id-Vg characteristics of the cell transistors with various gate lengths at Vd=Vcc(2.5V). There is a sufficient margin at the gate length of 0.2um for device operation. These results enable a 0.2um-rule NAND STI cell with the cell area of $0.31um^2$. In the proposed STI cells, Fower-Nordheim tunneling can achieve a fast programming (20usec) by applying 17V to the control gate and a fast erasing (2msec) by applying 18V to p-well, as shown in Fig.3.3.12. Fig.3.3.13 shows the TDDB characteristics of the tunnel oxides. Since Q_{BD} in the stripe capacitors with trench edges is almost the same as that in the flat capacitors without trench edges, the process damages into the tunnel oxides during the STI fabrication steps are negligibly small. Therefore, the endurance characteristics of the STI cells are excellent as shown in Fig.3.3.14. The threshold voltage window narrowing has not been observed up to l million cycles.

A threshold voltage distribution of programmed and erased cells are evaluated by measuring 2Mbit cell array, as shown in Fig.3.3.15. Both the programming and the erasing are performed by Fowler-Nordheim tunneling of electrons. A tight distribution of about 2.0V is realized though the programming and the erasing are carried out by one pulse without verification, because of a good uniformity of the channel width in the memory cell by using the self-aligned STI structure.

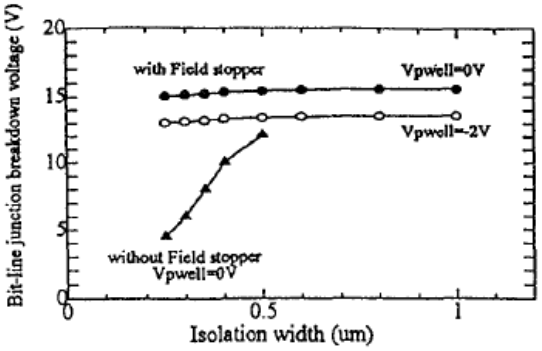


Fig.3.3.8 A punch-through voltage of the bit-line junctions, which is isolated by STI. There is no punchthrough at less than 15V which is the junction breakdown voltage using Boron Field stopper implantation.

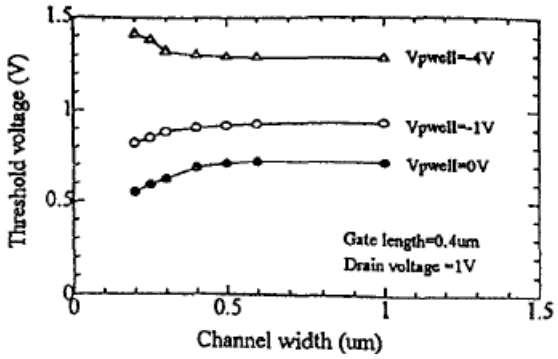


Fig.3.3.9 A threshold voltage as a function of the channel width. The STI cells show a weak dependence on the threshold voltage by the change of the channel width. Therefore, the STI cell is suitable for scaling of the isolation pitch.

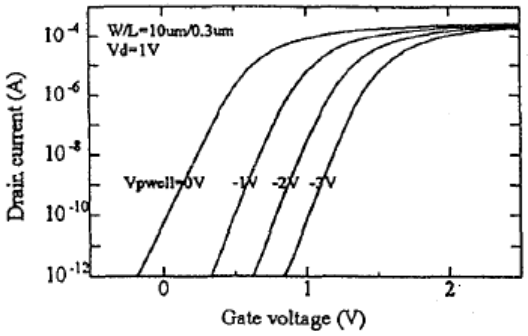


Fig.3.3.10 Id-Vg characteristics of the wide cell transistors with various voltages of p-well. No anomalous hump is seen in the subthreshold characteristics since the floating gate never overlap the STI comers.

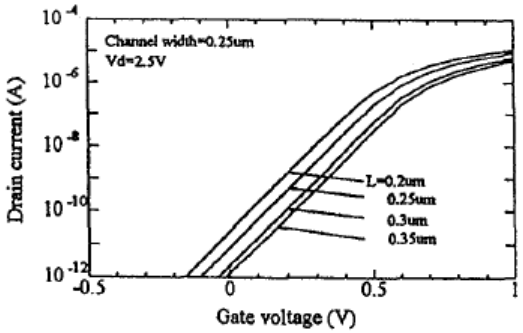


Fig.3.3.11 Id-Vg characteristics of the short channel cell transistors at Vd=2.5V which *is* applied in the read operation. There is a sufficient margin at the gate length of 0.2um for device operation.

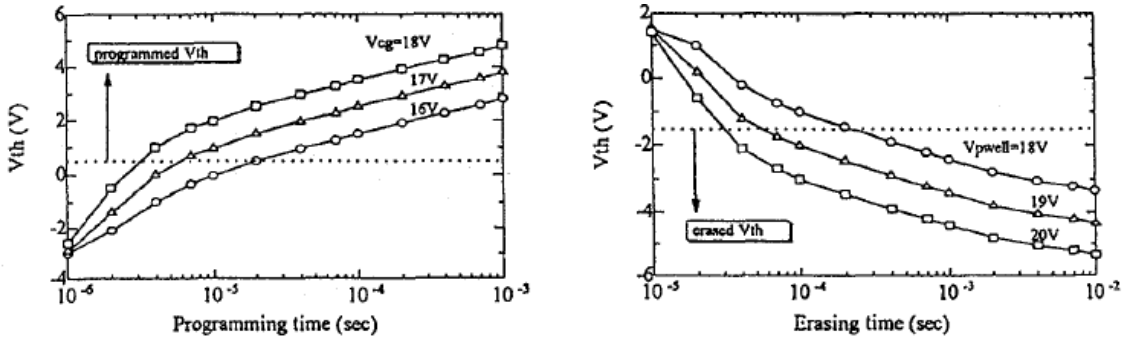


Fig.3.3.12 Prognmming and erasing characteristics of the SA-STI cells. Fast programming (20usec) and erasing (2msec) can be accomplished by Fowler-Nordheim tunneling, applying 17V to the control gate during programming and 18V to p-well during erasing, respectively.

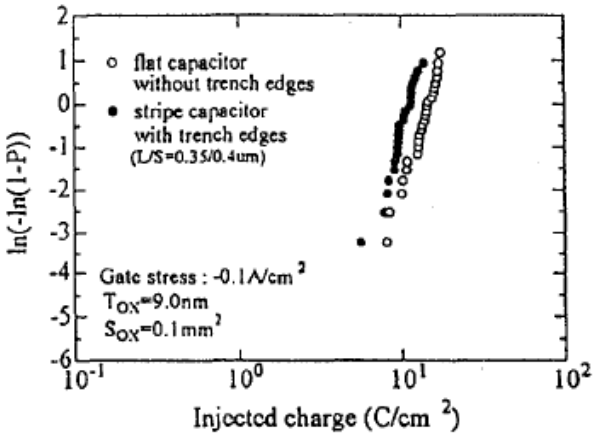


Fig.3.3.13 TDDB characteristics of the tunnel oxide in the STI stripe capacitor and a flat capacitor. The process damages into the tunnel oxides during the STI fabrication steps are negligibly small.

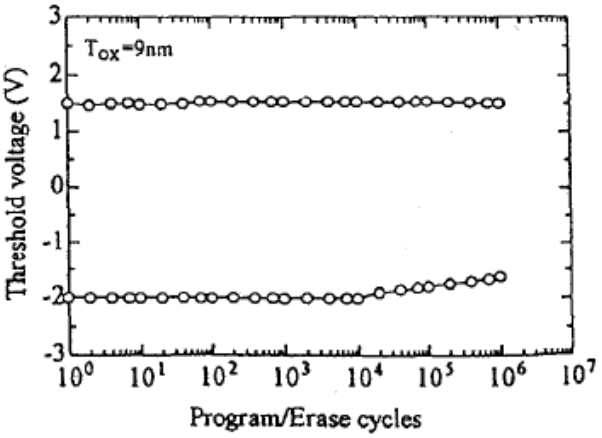


Fig.3.3.14 The program and erase cycling endurance characteristics of the STI cell. The threshold voltage window narrowing has not been observed up to 1 million cycles.

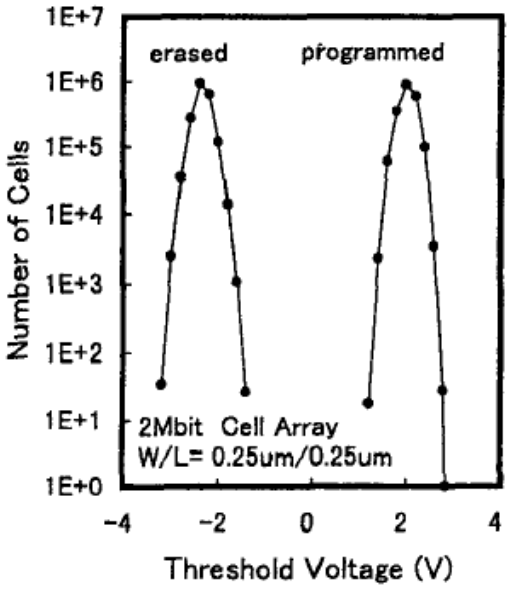


Fig.3.3.15 A cell threshold voltage distribution in one program and one erase pulse (no verify). Programming and erasing are carried out by 17V, 10usec and 18V, lmsec, respectively.

3.3.4 Characteristics of peripheral devices

Fig.3.3.16 shows sub-threshold characteristics of low voltage peripheral transistor as a function of the well voltage. No hump is observed in sub-threshold region because of avoiding to overlap the gate electrodes with the STI corners.

Fig.3.3.17 shows a junction breakdown voltage and a threshold voltage of a parasitic field transistor. The isolating ability of the STI is greatly higher than that of LOCOS. Furthermore, the breakdown voltage is higher than a demand (>22.5v with an enough margin. Therefore, the self-aligned STI process is suitable to the peripheral transistor as well as to the memory cell.

Fig.3.3.18 shows the TDDB characteristics of the gate oxides in the high voltage transistors. The evaluated lifetime of the gate oxide is sufficiently long. The result implies that the process damages into the gate oxides are negligibly small.

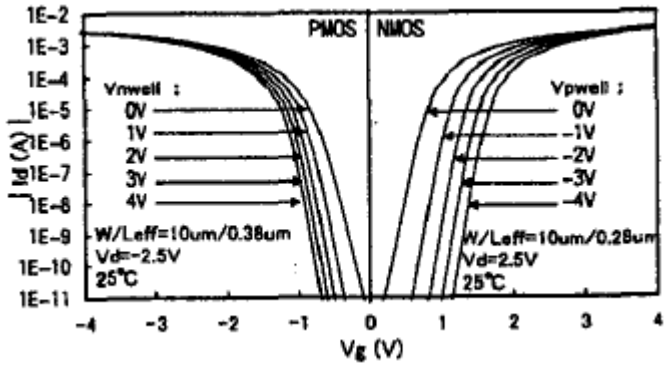


Fig.3.3.16 A subthreshold characteristics of the peripheral transistors (NMOS and PMOS) as a function of well voltage.

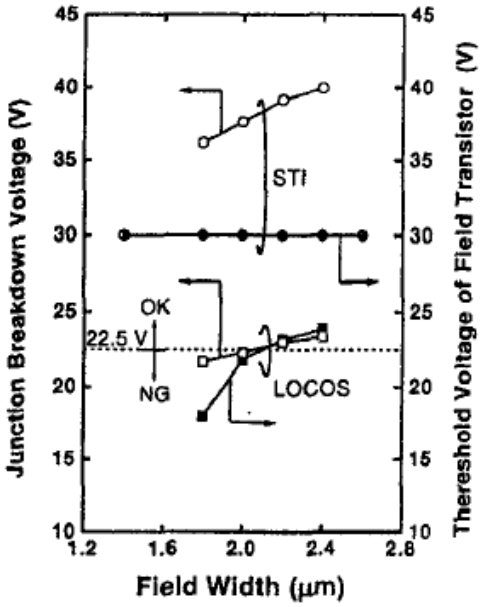


Fig.3.3.17 A punch-through voltage and threshold voltage of parasitic field transistor for high voltage isolation.

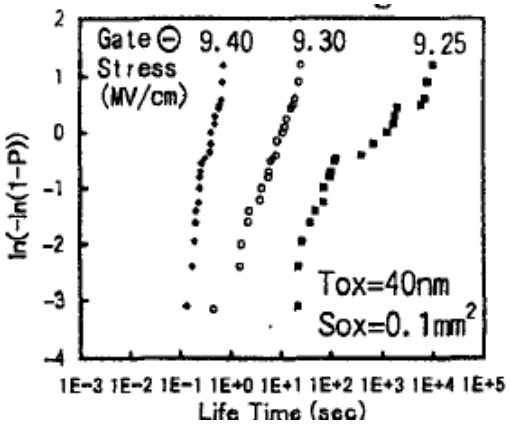


Fig.3.3.18 TDDB characteristics of the high voltage gate oxide as a function of applied gate electric field at negative gate voltage.

3.3.5 Summary

A 0.31um^2 SA-STI cell with FG wing and peripheral integration process have been successfully developed using 0.25um design rules. This technology makes it possible to realize reliable memory cell and peripheral devices with a simple process. Therefore, the proposed SA-STI cell with FG wing is suitable for a low cost flash memories of 256Mbit and lGbit for mass storage applications [3.3.8][3.3.9].

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3.4 Self-Aligned STI cell (SA-STI cell) without FG wing

Abstract ; An ultra high-density NAND-structured memory cell, using a new Self-Aligned Shallow Trench Isolation (SA-ST1) technology, has been developed for a high performance and low bit cost Flash memory. The SA-STI technology results in an extremely small cell size of 0.67 um^2 per bit by using 0.35um design rule, 67% without dimension scaling. The key technologies to realize a small cell size are (1) 0.4um width Shallow Trench Isolation (STI) to isolate neighboring bits and (2) a floating gate that is self-aligned with the STI, eliminating the floating-gate wings. Even though the floating-gate wings are eliminated, a high coupling ratio of 0.65 can be obtained by using the side-walls of the floating gate to increase the coupling ratio. Using this self-aligned structure, a reliable tunnel oxide can be obtained because the floating gate does not overlap the trench corners, so enhanced tunneling at the trench corner is avoided. Therefore, the SA-STI cell combines a low bit cost with a high performance and a high reliability, such as the fast programming (0.2usec/byte), fast erasing (2msec), good program/erase endurance (>1 million cycles), and excellent read disturb characteristics (>10 years). The process technologies and the device performance of the SA-STI cell are described. The SA-STI technology can be used to realize NAND flash memories of 256Mbit and beyond.

3.4.1 Introduction

It has been expected that a high density flash memory [3.4.1] will replace magnetic disk memory, because it has numerous advantages such as small cell size, fast access time, and low power dissipation. However, in order to replace the magnetic disk, several requirements must be satisfied. The first and most important is low bit cost, which can be attained with small cell size and reduction of the number of fabrication steps. The second item is high reliability, which is related to the program/erase endurance and data retention. The other items are high-speed programming, small block size and single 3V power supply.

A NAND-structure Flash memory had been proposed [3.4.1]. This NAND structured cell reduces the cell size without scaling of the device dimension. We have also developed the operation method for the NAND cell. A bi-polarity Fowler-Nordheim tunneling write/erase method [3.4.2] can be used. This method achieves high reliability, high-speed programming and small sector size. Therefore, the NAND Flash is the most promising candidate to replace magnetic disk memory.

In this section, a novel Self-Aligned Shallow Trench Isolation (SA-ST1) cell technology are described for a high performance and low bit cost NAND structure Flash memory[3.4.3]. A small cell size of 0.67um^2, including the select transistor and drain contact area, was obtained under a 0.35um design rule, in comparison with 1.13um^2 LOCOS cell [3.4.4]. The key technology in obtaining small cell size is the bit-line isolation technology, which uses the Shallow Trench Isolation (ST1) process. This technology also realizes a high reliability and a high performance.

3.4.2 SA-STI cell structure

Figure 3.4.1 compares the cross sectional and top view of the SA-STI cell with that of the conventional LOCOS cell. This NAND structure cell has 16 memory transistors arranged between two select transistors in series. The word-line pitch is 0.7um. The bit-line pitch can be reduced to 0.8um by using 0.4um STI technology. As a result, the cell size of SA-STI cell is about 60% of that of the conventional LOCOS cell [3.4.4].

In general, as the isolation width between the memory cells is reduced, the coupling ratio is reduced due to the decreased floating-gate wing area. However, In the SA-STI cell, even if a very tight 0.4um width isolation is used, a high coupling ratio of 0.65 can be obtained because the 0.3um high side wall (H) of the floating gate is used to increase the coupling ratio, as shown in Fig.3.4.2. Table 1 shows major cell parameters.

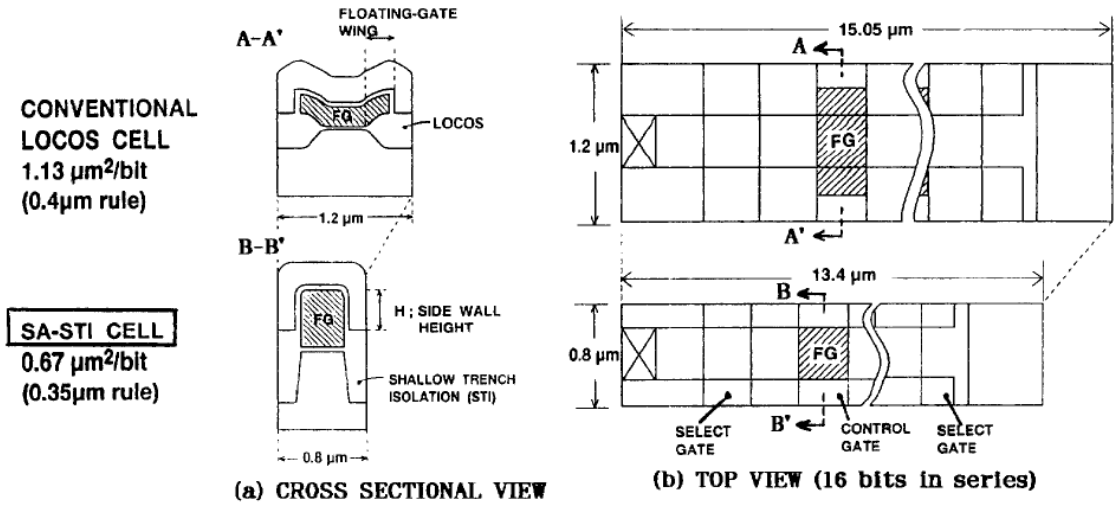

Fig.3.4.1 (a) The cross sectional and (b) top view of the Self-Aligned Shallow Trench Isolation cell (SA-STI cell) in comparison with that of the conventional LOCOS cell.

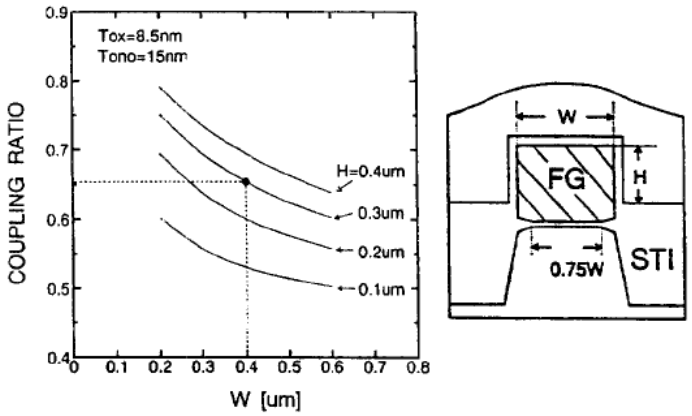

Fig.3.4.2 The coupling ratio of the SA-STI cell as a function of the gate width (W). A high coupling ratio of 0.65 can be obtained because the 0.3um high side wall (H) of the floating gate is used.

Table 1. Memory cell parameter.

Cell size	0.67 μm² (including select Tr etc.)
Gate Length	0.35 μm
Gate Width	0.4 μm
Trench Isolation Width	0.4 μm
Tunnel Oxide	8.5 nm
Interpoly Dielectric	ONO 15 nm (effective)
Programming Time	0.195 μsec/byte
Erase Time	2 msec/sector
	2 msec/chip

3.4.3 Fabrication Process

The fabrication of the SA-STI cell is simple and uses only conventional techniques, as shown in Fig.3.4.3. First, a stacked layer of the gate oxide, the floating gate poly-silicon and the cap oxide is formed. Next, the trench isolation region is defined by patterning these three layers, followed by the trench etching, as shown in Fig.3.4.3(a) and filling with LP-CVD SiO_2, as shown in Fig.3.4.3(b). Subsequently, the LP-CVD SiO_2 is etched back until the side-wall of the floating gate poly-silicon is exposed. After that, the inter-poly dielectric (ONO) (Fig.3.4.3(c)) and the control-gate poly-silicon are formed (Fig.3.4.3(d)), followed by the stacked gate patterning. In this process, the floating gate and STI patterning are carried out by the same mask, so the number of fabrication steps for the SA-STI process can be decreased with about 10% in comparison with that for a conventional LOCOS process. Figure 3.4.4 shows cross-sectional SEM photograph of SA-STI cell.

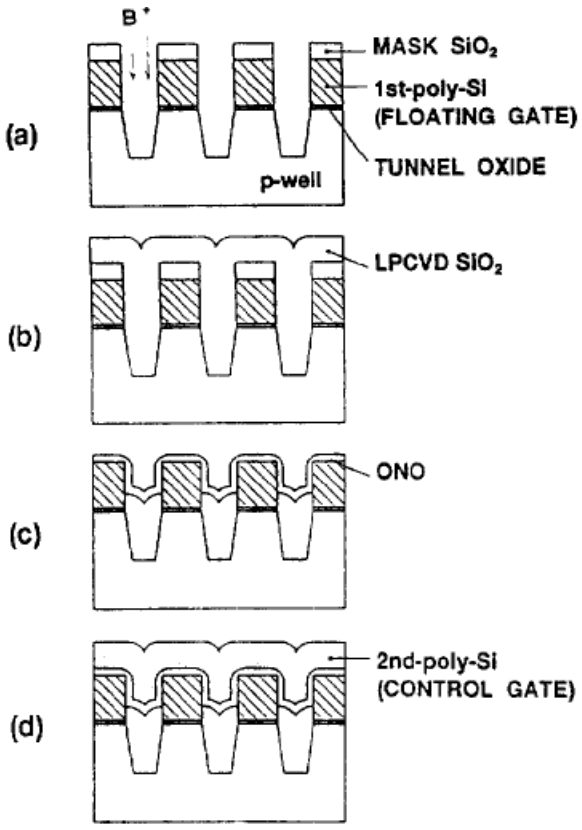

Fig.3.4.3 The process sequence of the SA-STI process. (a)Trench etching, B+ implantation. (b)LP-CVD SiO_2 fill-in, (c)Oxide etch-back and ONO formation, (d)Control gate formation. The floating gate and STI patterning are carried out by the same mask, so the number of fabrication steps for the SA-STI process can be decreased with about 10% in comparison with that for a conventional LOCOS process.

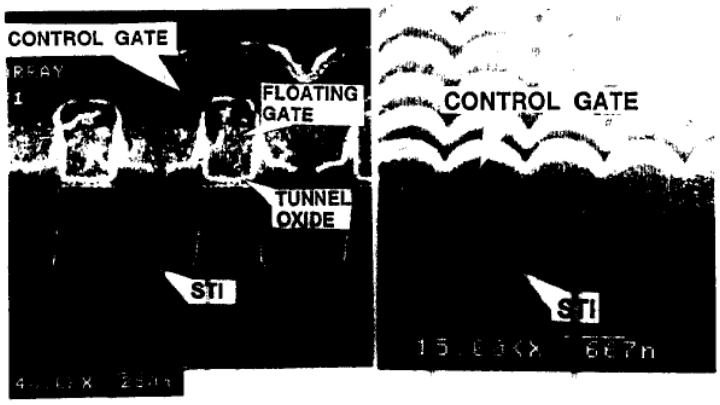

Fig.3.4.4 Cross-sectional SEM photograph of the SA-STI cell.

3.4.4 Shallow Trench Isolation (STI)

In the case of LOCOS isolation, the punch-through of the bit-line junctions occurs at a 0.5um isolation width, as shown in Fig.3.4.5. However, in the case of STI. the punch-through and junction breakdown voltage are higher than 15V even at a 0.4um isolation width, as shown in Fig.3.4.5. Furthermore, the 0.7um thick STI field oxide results in a high threshold voltage (>30V) of the parasitic field transistor between the neighboring bits. As a result, a very tight 0.8um bit-line pitch can be realized by using STI.

Figure 3.4.6 illustrates the leakage of n+-p junction for STI and LOCOS. The leakage current of STI is comparable to that of LOCOS.

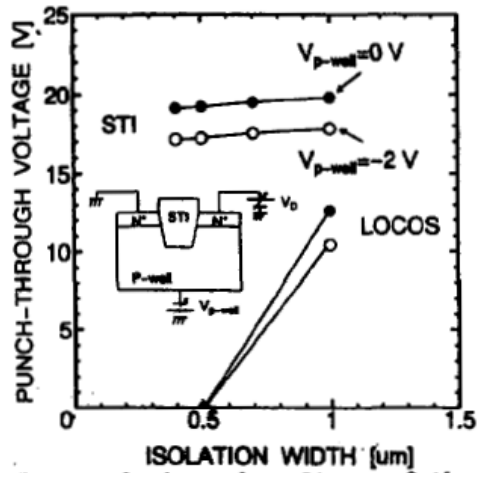

Fig.3.4.5 The punch-through voltage of the bit-line junction, which is isolated by Shallow Trench Isolation (STI), in comparison with LOCOS isolation. The punch-through is higher than 15V. which is high enough to realize a 0.4 um trench isolation.

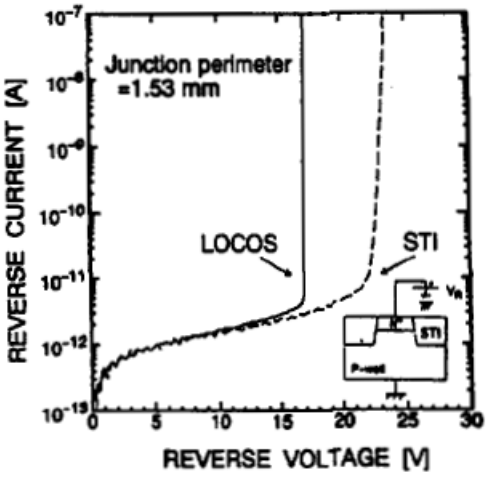

Fig.3.4. 6 Junction leakage current of STI and LOCOS. The junction leakage current of STI is comparable to that of LOCOS.

3.4.5 SA-STI cell Characteristics

Figure 3.4.7 shows the sub-threshold characteristics of the SA-STI cell with 0.4um channel width. Anomalous sub-threshold characteristics (hump) cannot be seen as a result of SA-STI structure.

Figure 3.4.8 shows the program and erase characteristics of SA-STI cell. The fast programming (100usec/512byte) and fast erasing (2msec) can be accomplished by Fowler-Nordheim tunneling, applying a positive voltage of 17V to the control gate during programming and 17V to the p-well during erasing, respectively, as shown in Fig. 3.4.8.

The TDDB characteristics of the tunnel oxide in the SA-STI process are almost the same as that in the LOCOS process, as shown in Fig.3.4.9, because the floating gate does not overlap the trench edges. Therefore, the endurance characteristics of the SA-STI cell are comparable with that of the conventional LOCOS cell, as shown in Fig.3.4.10. The SA-STI cell guarantees a wide cell threshold window as large as 3V, even after 1 million write/erase cycles. Furthermore, read disturb characteristics can be ensured for more than 10 years even after 1 million write/erase cycles, as shown in Fig.3.4.11.

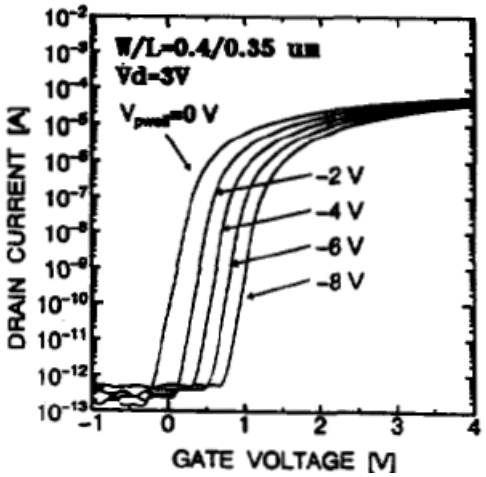

Fig.3.4.7 The sub-threshold characteristics of the SA-STI cell with various substrate (p-well) bias conditions. Anomalous sub-threshold characteristics (hump) cannot be seen because the floating-gate dose not overlap the trench comer.

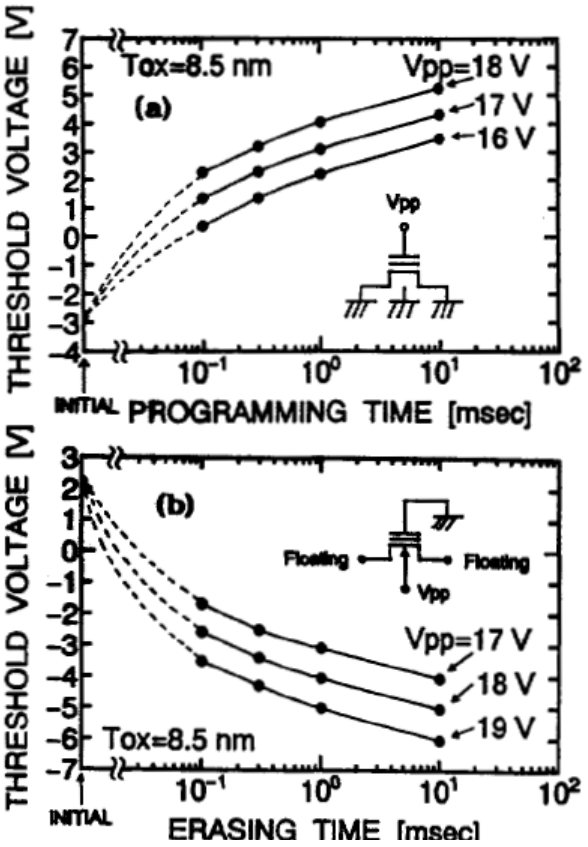

Fig.3.4.8 (a) The program and Erase characteristics of the SA-STI cell. The fast programming (100usec) and erasing (2msec) can be accomplished by Fowler-Nordheim tunneling over the channel area, applying a positive voltage of 17V to the control gate during programming and 17V to the p-well during erasing, respectively.

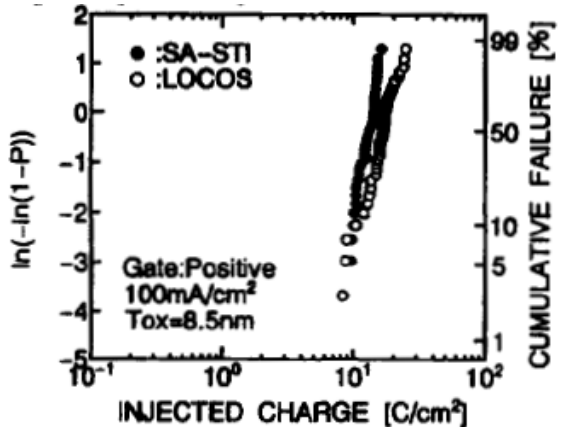

Fig.3.4.9 The TDDB characteristics of the 8.5nm thick tunnel oxide. The TDDB characteristics in the SA-STI process are almost the same as that in the LOCOS process.

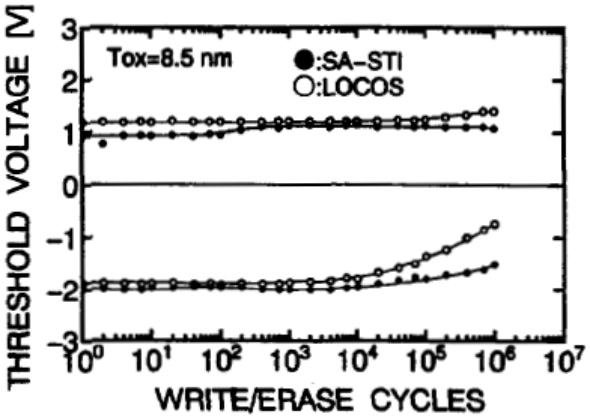

Fig.3.4.10 The endurance characteristics of the SA-STI cell and the LOCOS cell. In the SA-STI cell, window narrowing has not been observed up to 1 million write/erase cycles.

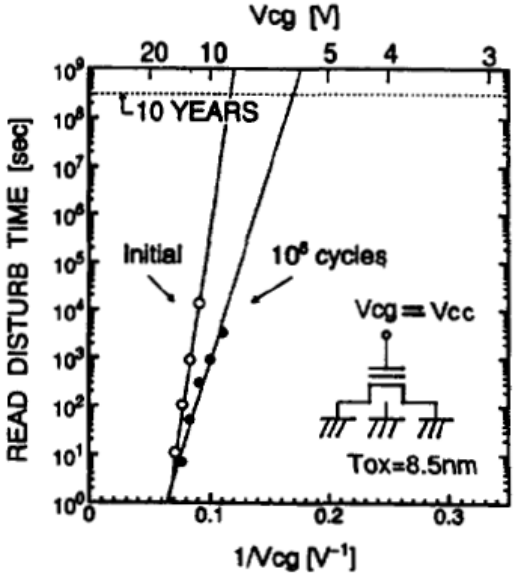

Fig.3.4.11 The read disturb characteristics of the SA-STI cell. The read disturb time is more than 10 years when a Vcc of 3.0V is used, even after 1 million W/E cycles .

3.4.6 Summary

A 0.67um^2 Self-Aligned Shallow Trench Isolation cell (SA-STI cell) for a 256 Mbit NAND Flash memory has been successfully developed by using a 0.35um technology. This technology is suitable to realize a low cost and high reliable flash memory, which may lead to the replacement of hard disk memories in the near future [3.4.5].

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3.5 Scaling Challenge of Self-Aligned STI cell (SA-STI cell)

Abstract ; The scaling limitations and challenges of Self-Aligned STI cell (SA-STI cell) over 2X~0X nm generations for NAND flash memories are described in this chapter. The scaling challenges are categorized to 1) narrow Read Window Margin (RWM) problem, 2) structural challenge, and 3) high field (5~10 MV/cm) problem. First, 1) the narrow RWM is investigated by extrapolating physical phenomena of FG-FG coupling interference, Electron Injection Spread (EIS), Back Pattern Dependence (BPD), and Random Telegraph Noise (RTN). The RWM is degraded not only by increasing programmed Vt distribution width, but also by increasing Vt of erase state mainly due to large FG-FG coupling interference. However, RWM is still positive in 1Z nm (10nm) generation with 60% reduction of FG-FG coupling by air-gap process. For 2) structural challenge, the Control Gate (CG) fabrication margin between Floating Gates (FGs) is becoming much severer beyond 1X nm generation. Very narrow 5nm FG width/space has to be controlled. For 3) high field problem, high field between CGs (word lines; WLs) is critical during program. By using WL air-gap, high field problem can be mitigated, and 1Y/1Z nm generations could be realized. Therefore, the SA-STI cell is expected to be able to scale down to 1Z nm (10nm) generation, with the air gap of 60% reduced FG-FG coupling interference and an accurate control of FG/CG formation process.

3.5.1 Introduction

The production volume of NAND Flash memory [3.5.1] is tremendously increasing with extensive applications, such as smart phone, tablet PC, and Solid-State Drive (SSD). The market size is expected to be over $25 Billion in 2012. In order to satisfy requirements of these applications, low cost and high reliable NAND flash memory has been intensively developed over 25 years. LOCOS isolation was used for 0.7um-0.3um generation [3.5.2]. However, LOCOS isolation had a critical limitation of isolation width of around 0.8um due to applied high voltage (~8V) between active areas [3.5.2]. Then Shallow Trench Isolation (STI) was applied to NAND Flash. As a suitable memory cell structure for NAND Flash, the Self-Aligned STI cell (SA-STI cell) had been developed [3.5.3]-[3.5.6] and implemented to NAND flash products [3.5.7]. This technology can reduce isolation width from 2*F @ LOCOS (F; Feature size) to F @ SA-STI, so cell size can be scaled down to ideal $4*F^2$ [3.5.3]. As the first generation of SA-STI cell, the SA-STI cell with Floating Gate (FG) wing was used to increase

coupling ratio and to decrease structure aspect ratio [3.5.4][3.5.5]. After that, from 90nm generation, the SA-STI cell with a single layer FG (SA-STI cell without FG wing) had started to use to avoid small tolerance of FG alignment, as the second generation of SA-STI cell [3.5.3]. Furthermore, the effective cell size can be reduced by Mu1ti-Level Cell (MLC, TLC, QLC). Therefore, small cell size of $4*F^2$ combined with Mu1ti-Level Cell can drastically reduce the bit cost.

The fabrication of the SA-STI cell is simple and uses only conventional techniques. The floating gate and STI patterning are carried out by the same mask, so the number of fabrication steps for the SA-STI process can be decreased with about 10% in comparison with that for a conventional LOCOS process. In addition, this technology has also demonstrated an excellent reliability, because the FG does not overlap the STI corner because FG over the tunnel oxide is patterned as the shape of the active area. The programming and erasing characteristics became much uniform and stable [3.5.3]-[3.5.5]. Therefore, the SA-STI cell has very high reliability and high performance [3.5.3]-[3.5.7].

The SA-STI cell structure and process have been used more than 10 years and 10 generations. Fig.3.5.1 shows a TEM cross section of recent mid-1X nm SA-STI memory cells [3.5.8]. However, for further scaling a SA-STI cell beyond mid-1X-nm generation, it is becoming hard to scale down due to facing the many physical limitations, such as FG-FG coupling interference [3.5.9], Random Telegraph Noise (RTN) [3.5.10]-[3.5.12], CG formations between FGs [3.5.13], WL high field problem, and reducing number of stored electrons [3.5.14], etc.

In this chapter 3.5, several scaling problems and limitations have been discussed over 2X~0X nm generations [3.5.34]. As a result, the SA-STI cell could be scaled down to 1Z nm (10nm) generation with an accurate control of FG/CG formation process and air gap process to manage high field problem.

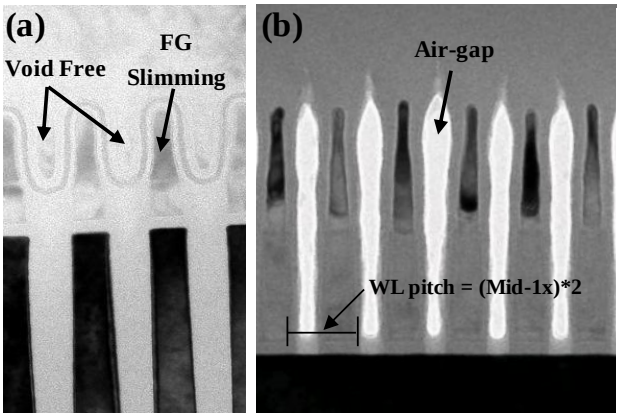


Fig. 4. Cross-section TEM View of the cell (a) along WL direction, (b) along BL direction. The CGs are well patterned with middle-1x nm half pitch.

Fig.3.5.1 TEM photograph of mid-1x nm SA-STI NAND flash cells [3.5.8].

3.5.2 Assumption of dimension scaling

Figure 3.5.2 shows a top view of conventional NAND cell strings. In order to investigate the scaling of the SA-STI cell, cell dimensions beyond 2X nm (26nm) generation are assumed, as shown in Table 1. Dimensions of 2X nm are given, 27nm for the Bit line (BL) half pitch and 26nm for the Word Line (WL) half pitch. Dimensions beyond 2Xnm are assumed to scale down by fixed scaling factor of x0.85 for BL half pitch and x0.8 for the WL half pitch. And also the channel width W and Inter-Poly Dielectric (IPD) thickness are assumed to scale down by the factors of x0.9 and x0.95, respectively.

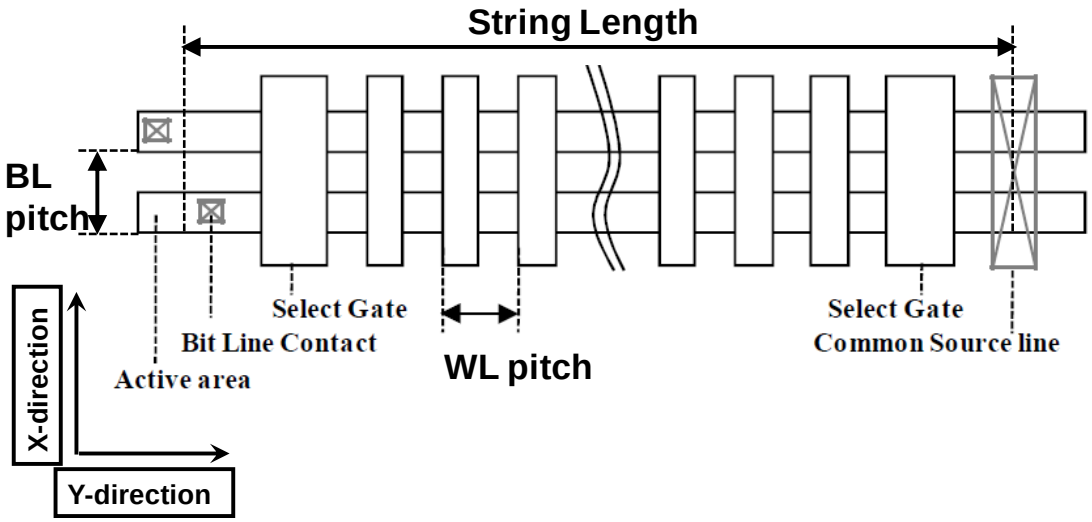


Fig.3.5.2. Top view of conventional NAND cell string. 64 cells are connected in series with two select gates. BL pitch and WL pitch are nearly equal to 2F (F; Feature size). Then unit cell size is close to ideal $4*F^2$.

Table 1 Assumption of cell dimensions and ONO (IPD) thickness, in generations of 2X~0X nm. Dimensions of 2X nm generation are given, as 27nm for BL half pitch and 26nm for WL half pitch. Dimensions of 2Y nm~ are assumed by scaling factors of x0.85 for BL half pitch (x-direction) and x0.8 for the Word Line (WL) half pitch (y-direction). And also, the scaling factors of channel width (W) and ONO thickness are assumed x0.9 and x0.95, respectively.

Generation	2X	2Y	1X	1Y	1Z	0X	Scaling factor
BL Half pitch (nm)	*27*	23.0	19.5	16.6	14.1	12.0	x0.85 assumption
WL Half pitch (nm), Gate length L	26	20.8	16.6	13.3	10.6	8.5	x0.8 assumption
Channel W (nm)	20	18	16.2	14.6	13.1	11.8	x0.9 assumption
ONO thickness (nm)	*12*	11.4	10.8	10.3	9.8	9.3	x0.95 assumption

3.5.3 Assumption for investigating Read Window Margin (RWM)

Figure 3.5.3 shows an image of read Vt window in MLC (2bit/cell) NAND cell. The "Vt window" is defined by a right-side edge of erase distribution and a left-side edge of L3 (highest programmed state) after completing all pages program operation in block (strings). Two programmed Vt distribution of L1/L2 have to be inside of the Vt window to be reliable read operation. Read Window Margin (RWM) is defined by RWM = (Vt window) - 2*(Programmed Vt distribution width), so that RWM means the separation margin of Vt distributions of each states.

As cell scaling, the RWM have been seriously degraded as cell scaling down from 0.7um to 2X nm generation, because several physical phenomena were getting worse. Therefore, for further scaling of NAND cell, it is very important to analyze and foresee the RWM in future scaled NAND cell. In order to investigate RWM, the scaling trend of physical phenomena of Electron Injection Spread (EIS) [3.5.15]-[3.5.17], FG-FG coupling interference [3.5.9], RTN [3.5.10]-[3.5.12], and Back Pattern Dependence (BPD) are assumed as following. And other assumptions of the page program sequence, parameter setting, etc, are also shown in following.

<u>Assumption of RWM calculation</u>;

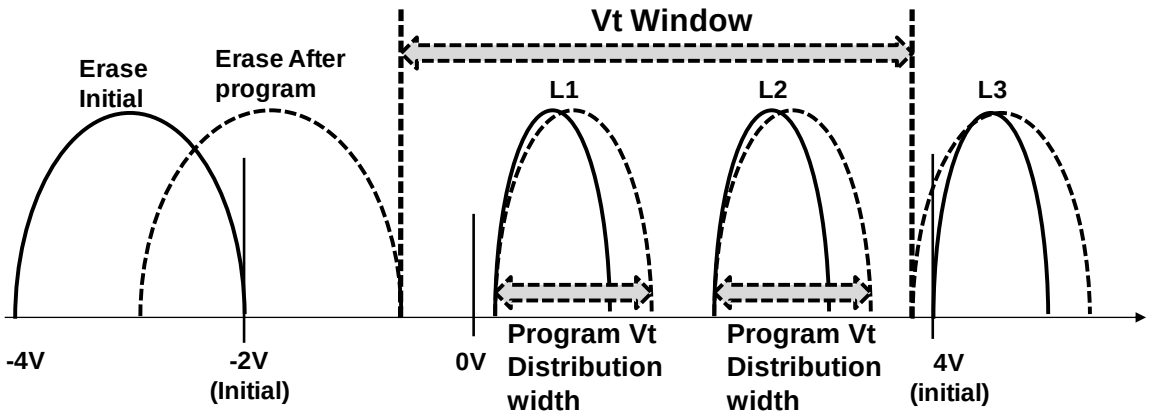
a) Vt distribution width (@ +/- 3sigma) is assumed to become wider by simple summation of values of Electron Injection Spread (EIS), FG-FG coupling interference, RTN, Back Pattern Dependence (BPD). Each value is given for 2Xnm generation, and is extrapolated for 2Y nm ~ 0X nm generations with the following formulas.
b) Program Electron Injection Spread (EIS) [3.5.15][3.5.16] is caused during program operation due to statistical spread in small number of injecting electrons during program pulse. The sigma of EIS is linear with sqrt(q*ISPP_Step/C_{IPD}) [3.5.15][3.5.16], and three sigma values are simply used for Vt distribution widening. Capacitance of interpoly dielectric, C_{IPD}, is scaled down from 2Xnm generation by x0.72 for each generation. ISPP_Step is program voltage step of ISPP (Increment Step Pulse Program) [3.5.18][3.5.19]. The measured standard deviations

(sigma) is 37.1mV for ISPP_step=300mV, as shown in Fig.3.5.4. A value of the sigma is assumed to be 50% larger due to FG depletion effects [3.5.17], etc. Then the sigma of 2X is assumed 55.6mV for ISPP_Step=300mV, and 78.7mV for ISPP_Step=600mV.

c) FG-FG coupling interference [3.5.9] is scaled from 2X nm generation to each generation by x(1/0.9) along WL, x(1/0.8) along BL, x(1/0.85) diagonal. And spread effect (additional Vt shift) is assumed 10% of FG-FG coupling value. FG-FG coupling values of 2X nm are assumed 94mV/V for two sides of x-direction (between BL-BL), 85mV/V for one side of y-direction (between WL-WL), and 25mV/V for two of xy-direction (diagonal), based on measurement results. Scaling factors of FG-FG coupling (x(1/0.9) along WL, x(1/0.8) along BL, x(1/0.85) diagonal) are the simple assumption by increasing FG-FG capacitance with decreasing FG-FG distance. This simple assumption would be optimistic because it is not including the effect of decreasing total FG capacitance, which is mainly due to less scaling of IPD and tunnel oxide thickness.
d) RTN is linear with 1/(W*sqrt(L)) [3.5.11]. The value of 2Xnm is assumed +/-107mV@ 3sigma, based on measurement results.
e) Back Pattern Dependence (BPD) is a Vt shift, which is caused by programming series-connected cells in the same string due to increasing series resistance in string. BPD is linear with L/W. The value of 2Xnm is assumed to 310mV, as shown in Fig.3.5.5.
f) Page program sequence is used the minimized FG-FG coupling program sequence [3.5.20][3.5.21], as shown in Fig.3.5.6. It means that, before MSB program, surrounding pages (LSB of WLn-1, WLn, WLn+1, and MSB of WLn-1) have already programmed. FG-FG coupling interference can be minimized for the programmed Vt distributions.
g) All Bit Line scheme (ABL) [3.5.22]. Vt shift value of x-direction FG-FG coupling interference is assumed that it is based on neighbor cell Vt shift of 3*sigma*SQRT(2)*(1/2) [sigma = (Vt distribution width (+/-3 sigma) of one program pulse)/6 = 3V/6 = 0.5V] [*(1/2) ; factor of random data pattern], because neighbor cells are programmed with target cell at same time.
h) Random data pattern.
i) Erase; initial Vt distribution; -3V +/-1V (Vt distribution width = 2V). The right side edge of Erase initial is -2V.
j) L1 verify level =0.5V, L2 verify level =2.25V, L3 verify level =4.0V, LSB verify level =0.8V, except for the case of Vt setting dependence in chapter 3.5.7.

k) ISPP step (Increment Step Pulse Program [3.5.18][3.5.19]) of LSB and MSB programming are 600mV and 300mV, respectively.

l) Data retention Vt shift is not including in this RWM investigation, because it is expected to manage by the multi-times read operations. And also, program disturb, read disturb and other effect are not included in this RWM investigation.



Read Window Margin (RWM) = (Vt Window) – 2*(Program Vt Distribution width)

Fig.3.5.3 Read Vt window of MLC NAND cell. Vt distributions of erase state and programmed L1, L2, L3 states are shifted up and become wider because of Electron Injection Spread (EIS), FG-FG coupling interference, RTN, and Back Pattern Dependence (BPD). Read Window Margin (RWM) is defined as RWM= (Vt window) – 2*(program Vt distribution width).

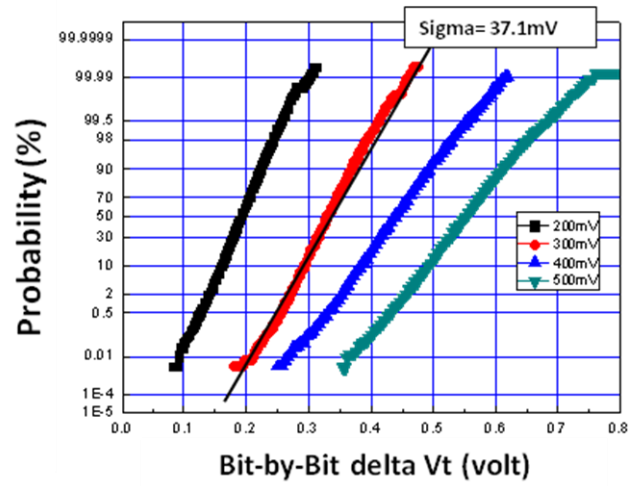


Fig.3.5.4 Electron Injection Spread (EIS) of 2X nm cell. In ISPP_step=300mV, the

standard deviations (sigma) is 37.1mV. With FG depletion effect [3.5.18], sigma is assumed to be larger of 50%. Then the sigma is assumed 55.6mV for 300mV ISPP_Step.

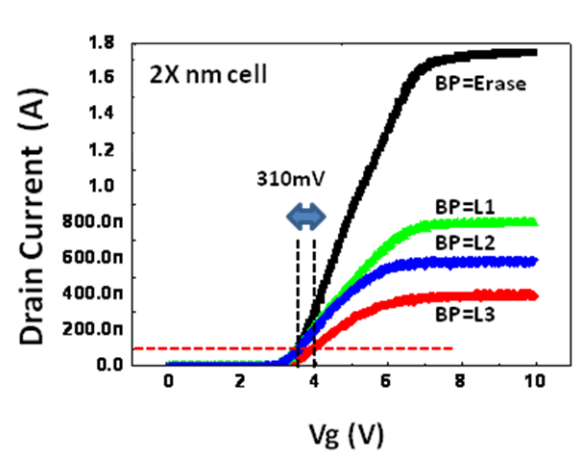


Fig.3.5.5 Back Pattern Dependence (BPD) of 64 cells string in 2X nm cell. Vt shift of BPD is assumed 310mV as worst case of BP=L3 (unselected cells are in L3).

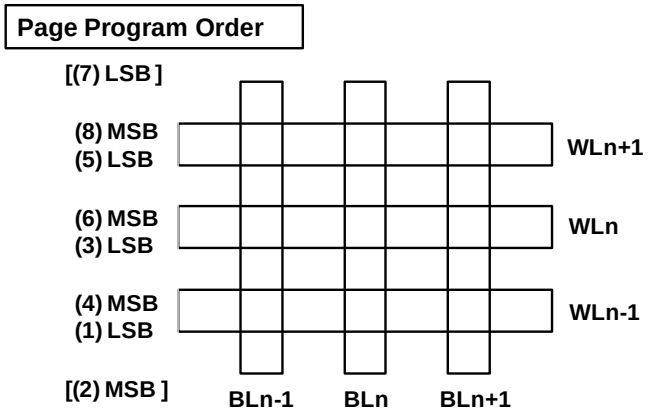


Fig.3.5.6 Page program sequence of the minimized FG-FG coupling interference. Before (6) MSB program of WLn, surrounding pages [(1)LSB of WLn-1, (3)LSB of WLn, (5) LSB of WLn+1, and (4) MSB of WLn-1] have already programmed. Then the FG-FG coupling interference can be minimized for the programmed Vt distributions.

3.5.4 Programmed Vt distribution width

In conventional program operation, a programmed Vt distribution width can be tight by using ISPP [3.5.18][3.5.19] and a bit-by-bit verify operations [3.5.23]. Initial

programmed Vt distribution width is determined by ISPP_step + EIS. And then it become wider by RTN, FG-FG coupling interference and BPD after all pages program in block (string).

The programmed Vt distribution width after all pages programmed in block have been calculated based on assumption of chapter 3.5.3, as shown in Fig.3.5.7. As memory cells are scaled down from 2X nm to 0X nm, the programmed Vt distribution width is increased from 1320mV to 2183mV. It is clear that major reasons to increase Vt distribution width are the FG-FG coupling and RTN.

In order to obtain appropriate Vt shift values of FG-FG coupling interference, the delta Vt of neighbor attack cell (subjects to target cell) [3.5.24] have been derived, as shown in Fig.3.5.8. Vt distributions of page programming steps are also described in Fig.3.5.8. For FG-FG coupling for the programmed states, delta Vt of attack cell is described as dVt_E_L1 or dVt_LSB_L2 + dVt_LSB_L3, as shown at 3) after MSB program in Fig.3.5.8. A dVt_E_L1 means delta Vt shift from erase state (@ 2) before MSB program) to L1 state. Larger value of dVt_E_L1 or dVt_LSB_L2+ dVt_LSB_L3 is used for calculation of FG-FG coupling Vt shift.

Vt shift value of x-direction FG-FG coupling interference is assumed that it is based on neighbor cell Vt shift of 3*sigma*SQRT(2)*(1/2) [standard deviation; sigma = (Vt distribution width (+/-3 sigma) of one program pulse)/6 = 3V/6 = 0.5V] [*(1/2) ; factor of random data pattern], as shown in section 3.5.3 g), because neighbor cells are programmed with target cell at same program sequence in All Bit Line scheme. We had assumed Vt shift as follows. Cells in programmed Vt distribution (3V width) are programmed to shift up by ISPP program. A certain cell (cellA) stops programming by passing verify at threshold voltage of Vt_CellA, and neighbor cells (cellB) has not passed verify yet at threshold voltage of Vt_cellB. The neighbor cells (cellB) are programmed by following ISPP steps, then it causes FG-FG coupling on cellA with Vt difference of (Vt_CellA-Vt_cellB). In this assumption, the distribution of Vt difference (Vt_CellA-Vt_cellB) is assumed to composition of Vt distribution (3V width), then sigma of Vt shift is SQRT($sigma^2$+$sigma^2$)=sigma*SQRT(2). And also, we assumed to be the same FG-FG coupling Vt shift between L1 and L2, by assuming to use preferable program operations, such as ABL parallel program method [3.5.31], BC state first program algorithm [3.5.32], and P3-pattern pre-pulse scheme [3.5.33], to reduce FG-FG coupling both L1/L2.

Erase Vt distribution at 2) Before MSB program in Fig.3.5.8 has already shifted up as dVt_Ei_E from Erase initial Vt distribution, by FG-FG coupling with surrounding cells of LSB program (both side of Y-direction/XY-direction/X-direction) and MSB

program (One side of Y-direction/XY-direction), as shown in Fig.3.5.6. As cell scaling, dVt_Ei_E becomes larger due to larger FG-FG coupling interference. Then dVt_E_L1 become smaller value as cell scaling. Therefore, y-direction FG-FG coupling interference for programmed state is relatively smaller than we expected, as shown in Fig.3.5.7.

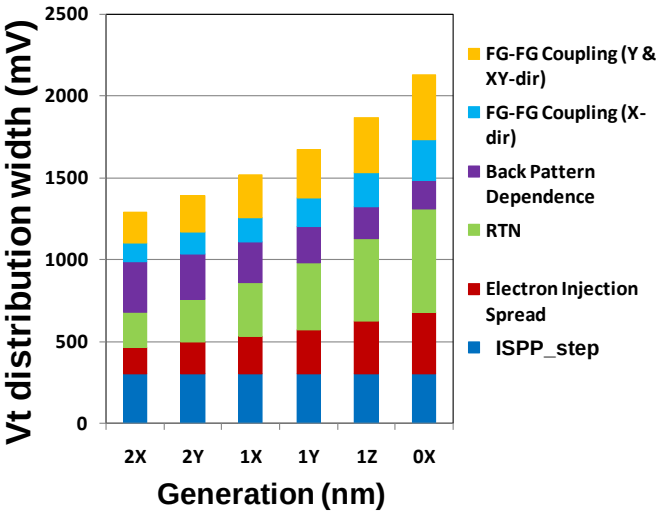


Fig.3.5.7 Calculated programmed Vt distribution width. Vt distribution width is increased as cell dimension scaling. Major impact factors to increase Vt distributions width are the FG-FG coupling and RTN.

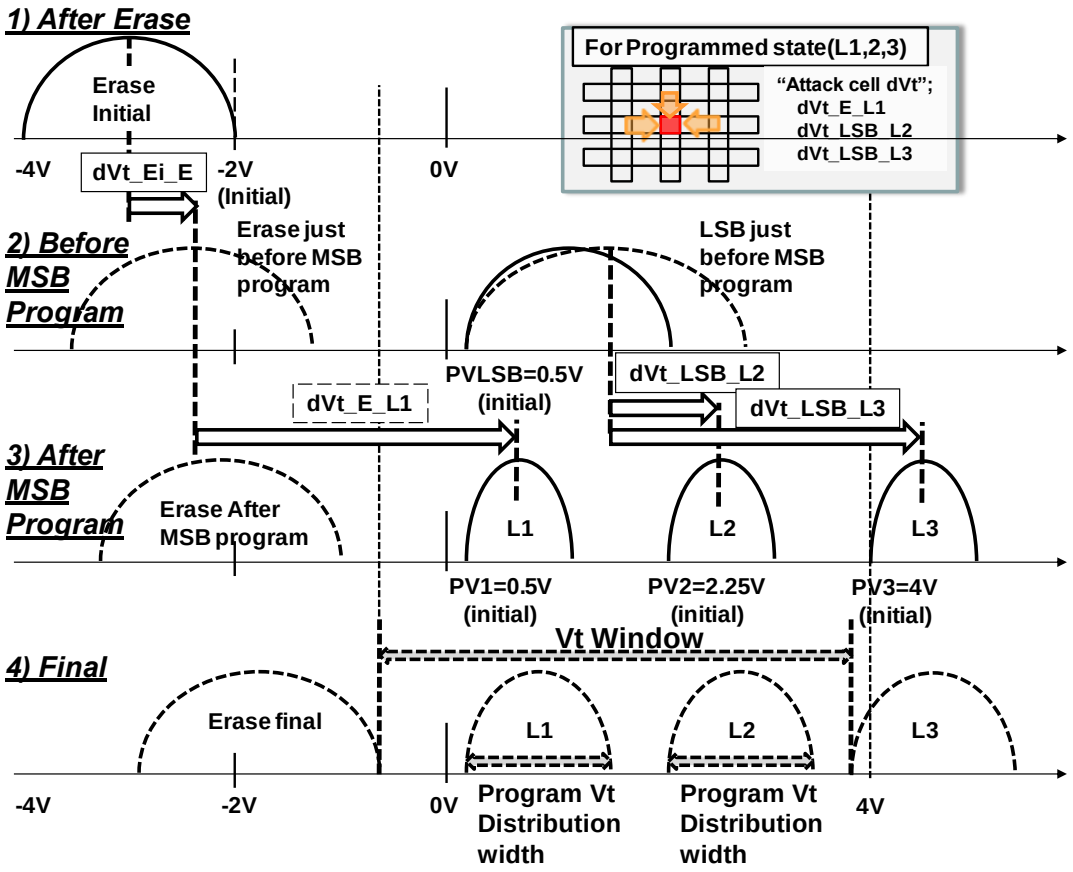


Fig.3.5.8 Vt distribution in page program steps. The attack cell delta Vt of dVt_E_L1 or dVt_LSB_L2 + dVt_LSB_L3 are subjected to the programmed target cell of y-direction neighbor cells, resulting wider Vt distribution width by FG-FG coupling interference. Then distribution width of the programmed cell becomes wider from 3)After MSB program to 4) Final.

3.5.5 Vt Window

Vt window is defined from the right-side edge of erase Vt distribution to the left-side edge of L3 Vt distribution, as shown in Fig.3.5.3. Figure 3.5.9 shows the calculation results of Vt window, the right-side edge of erase Vt distribution, and the left-side edge of L3 Vt distribution, in three cases of reducing FG-FG coupling of 0%, 30%, 60% by air gap [3.5.25]-[3.5.28] or low-k dielectric. The reducing FG-FG coupling is assumed both x-direction (STI air-gap [3.5.28]) and y-direction (WL air-gap [3.5.25]-[3.5.27]).

As shown in Fig.3.5.9, the Vt window become seriously narrower as cell scaling in case of conventional 0% FG-FG coupling reduction (see "Vt window 0%). This is

because the right-side edge of erase distribution is much increased as scaling. However, in case of -60% FG-FG coupling reduction, the right-side edge of erase distribution can be kept less than 0V even in 1Z nm generation. Then, Vt window can be kept more than 4000mV in 1Z nm generation.

In order to clarify the reason of increasing the right-side edge of erase, factors of increasing erase right-side edge are analyzed, as shown in Fig.3.5.10. The erase right edge is increased mainly by FG-FG coupling, especially by Y & XY direction FG-FG coupling. For erase state, the FG-FG coupling Vt shift is much larger than FG-FG coupling Vt shift of the programmed states. Figure 3.5.11 shows the reasons of large FG-FG coupling for Erase states. There are two reasons. One is large delta-Vt of attack cell, as shown in Fig.3.5.11 (a). This is because a dVt_Ei_L1, L2, L3 (attack cell delta Vt from erase initial state to each programming state L1, L2, L3) are much larger, in comparison with attack cell Vt shift for programmed state, such as dVt_E_L1 or dVt_LSB_L2 + dVt_LSB_L3, as shown in Fig.3.5.8. The other reason is that all of surrounding cells are subjected to cause FG-FG coupling Vt shift for erase state (Fig. 3.5.11(b)). Conversely, for the programmed cell, only part of surrounding cells (one side of y-direction [between WL-WL] and x-directions [between BL-BL]) have caused FG-FG coupling Vt shift, as shown in Fig.3.5.11 (b).

In order to obtain wider Vt window for 1Y and 1Z generations, it is important to reduce FG-FG coupling, specially FG-FG coupling of Y & XY direction. WL air-gap (or low-K) [3.5.25]-[3.5.27] and STI air-gap [3.5.28] have to be implemented as small FG-FG coupling as possible for future NAND cell.

Furthermore, the optimistic scaling factors of FG-FG coupling are used in this calculation, as described in section 3.5.3 c). Even if the optimistic values are used, the dominant factor of Vt window degradation is the FG-FG coupling. Therefore it is important to reduce FG-FG coupling for future scaled cells.

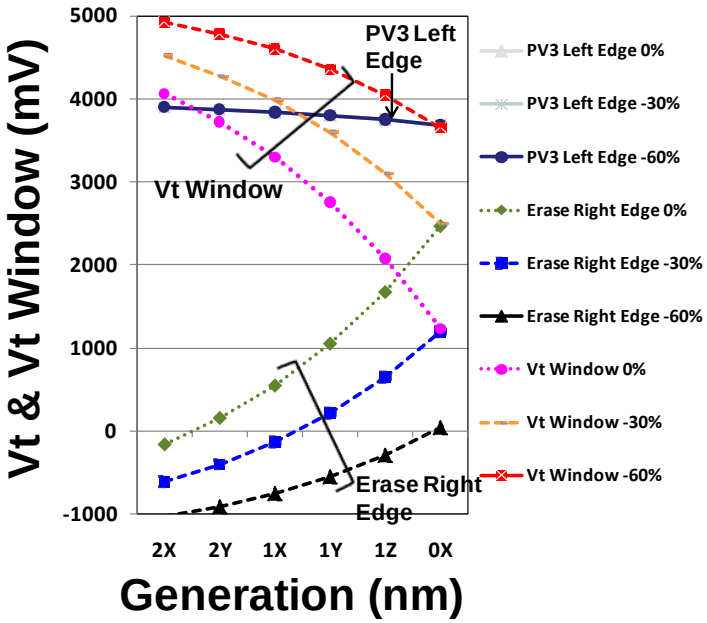


Fig.3.5.9 Calculated Vt window as cell scaling down. Vt window is decreased mainly by increasing Erase Right Edge (right-side edge of erase) . If FG-FG coupling interference can be reduced to -30% or -60%, the erase right edge can be improved much.

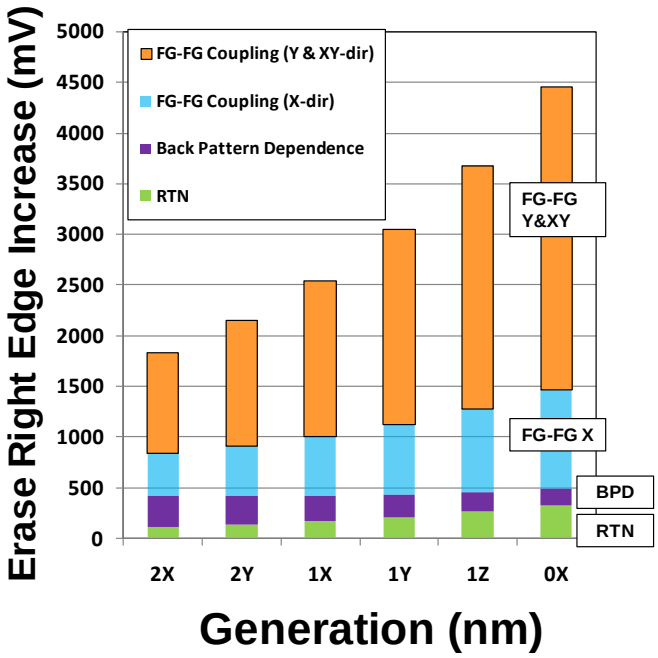


Fig.3.5.10 Increasing the right-side edge of Erase state, as scaling memory cells, in case of w/o reduction of FG-FG coupling. Erase right edge is increased mainly by

FG-FG coupling interference, especially by Y & XY- FG-FG coupling.

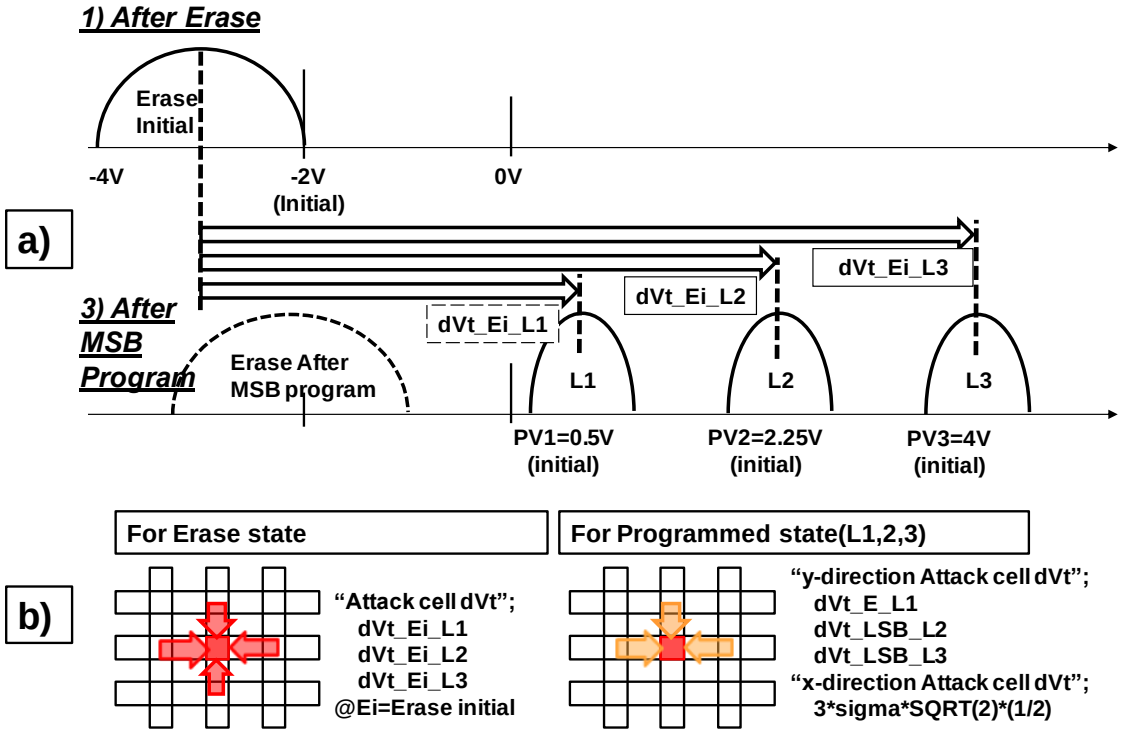


Fig.3.5.11 FG-FG coupling for Erase state. (a) The attack cell (neighbor of target cell) Vt shift of dVt_Ei_L1 or dVt_Ei_L2 or dVt_Ei_L3 are subjected to the Erased target cell. The Vt shift of erased state is larger than that of programmed state because Attack cell Vt shift for erased state is larger than that of programmed state (see Fig.3.5.9), and also (b) all of surrounding cells have subjected to erased cells, compared that all of surrounding cells have not subjected to programmed state.

3.5.6 Read Window Margin (RWM)

Figure 3.5.12 shows the scaling trend of RWM, which is calculated by the programmed Vt distribution width in Fig.3.5.7 and Vt window in Fig.3.5.9. RWMs are degraded as a cell scaling. In case of "No Air gap", 1X nm has marginal RWM, and 1Y nm generation has negative (-719mV) RWM. In case of "FG-FG coupling -30% air-gap", 1Y nm become marginal RWM, and 1Z nm generation has negative RWM. And also, in case of "FG-FG coupling -60% air-gap", 1Z nm generation has still positive RWM. This means that 30% FG-FG coupling reduction is needed for implement 1Y nm generation cell, and 50~60% reduction is needed for 1Z nm cell.

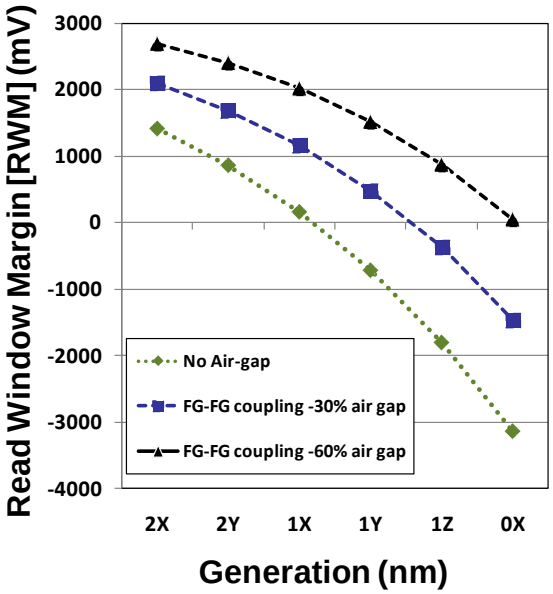


Fig.3.5.12 Calculated Read Window Margin (RWM), in no air-gap, 30% or 60% reduction of FG-FG coupling. RWM become less than 0V beyond 1X nm generation in case of no air-gap. However, by using air-gap with -60 % FG-FG coupling reduction, RWM can be kept positive even if 1Z generation is used.

3.5.7 RWM Vt setting dependence

In order to find out other solutions for wider RWM, Vt setting dependence has been investigated. Figure 3.5.13 shows RWM depended on Vt setting in case of 1Z nm with -30% FG-FG coupling reduction. In previous section, PV3 and Erase initial right edge are used fixed value of 4V and -2V, respectively. In this section, lower PV3 and lower Erase initial right edge are assumed, as shown in Fig.3.5.13.

RWM can be improved in case of decreasing Erase Initial right edge, even if programmed Vt distribution width are slightly increased. And RWM become positive in case of Erase Initial right edge=-4V. However, the decreasing Erase Vt setting would degrade reliability because of subjecting higher erase voltage stress. Then, in order to obtain wider RWM in 1Z nm generation, it should be combined the air-gap process of minimized FG-FG coupling with the decreasing Erase Vt setting.

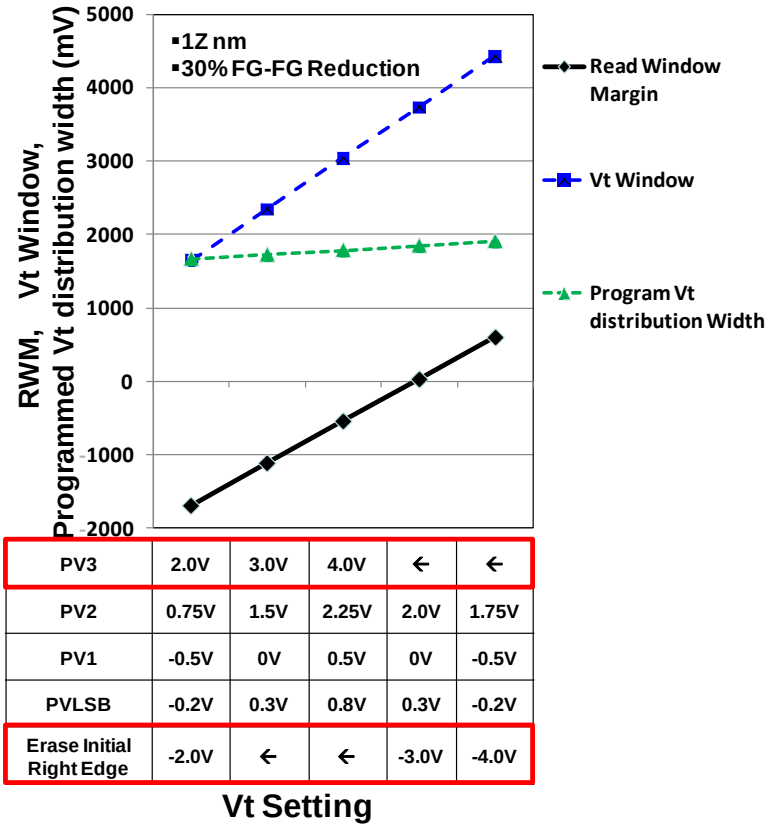


Fig.3.5.13 RWM and Vt window in 1Z nm generation in case of -30% FG-FG coupling. RWM increases by decreasing erase Vt setting.

3.5.8 Cell Structure Challenge

A structural challenge of the SA-STI cell is also investigated, based on assumption in Table 1. The critical structure of SA-STI cell is "CG formation margin", which is fabrication margin of CG between FGs [3.5.13]. Figure 3.5.14 shows an estimation of CG fabrication margin in the FG slimming structure beyond 2X nm generation. FG width and CG width are assumed to be equal in this estimation. As scaling down of the SA-STI cell, FG width and CG width are decreased to less than 10nm width @ 1X nm cell. The FG and CG width have to be controlled around 5nm in 1Y nm and 1Z nm generation, even ONO thickness is scaled down by the ratio of x0.95 for each generation. The depletion effects in FG [3.5.17] and CG during programming and erasing have to be also suppressed. Metal [3.5.29] or silicide material [3.5.14] will be applicable to FG and CG in future NAND cell.

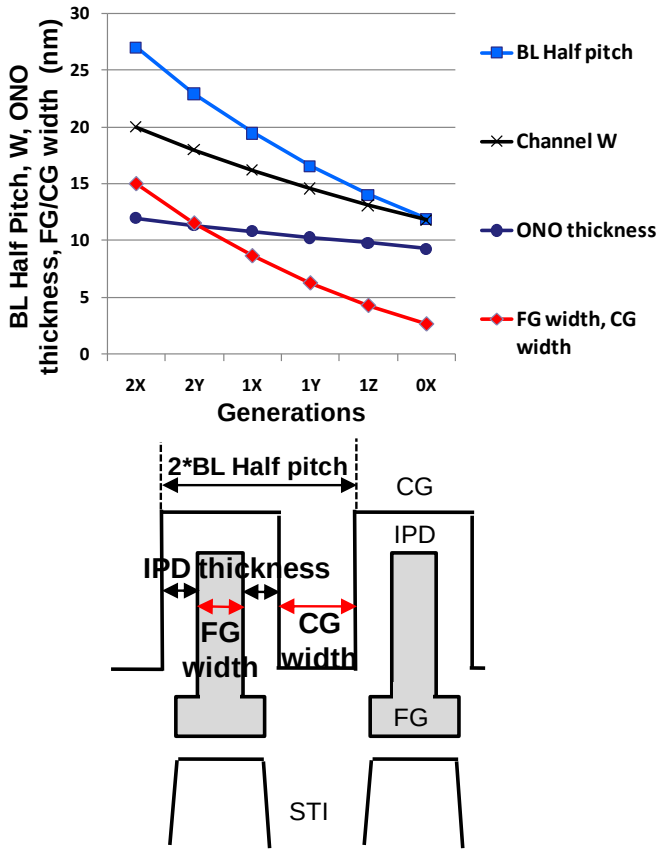


Fig.3.5.14 Estimated margin of CG fabrication between FGs. Very narrow CG and FG width of around 5 nm have to be controlled in 1Z nm generation.

3.5.9 High Field Limitation

A program and erase voltage of NAND Flash is high (~22V), and cannot be decreased drastically because a high electric field (10MV/cm~) of tunnel oxide is required for Fowler-Nordheim tunneling mechanism during program and erase.

The most serious high field problem in NAND cell is caused in between selected-WL and neighbor-WL during programming. In 2Xnm cell, the selected WL is in Vpgm (~22V) and the neighbor WL is in Vpass (7~10V), as shown Fig.3.5.15. There are three problems, 1) charge (electron) loss; charges in FG of neighbor cell is discharged to selected WL [3.5.30], 2) WL leakage or breakdown; high field between WLs (V_{PGM}-V_{PASS}_n+1/n-1 >10V) may cause leakage or breakdown, 3) program disturb; charge (electron) has injected from substrate to FG. It will be important for future generation to optimize V_{PASS}_n+1/n-1 to minimize failure rate generated by these three problems.

Figure 3.5.16 shows the estimated electric field as a function of Vpgm. Criteria

of maximum electric field between WLs, which is determined by 1) charge loss between FG and selected WL [3.5.30], can be increased from 6MV/cm [3.5.30] to 9.5MV/cm [3.5.8] by using air-gap. Even if air-gap is used, an available range of (Vpgm-Vpass) is reduced from 15V of 2Xnm cell to 10V of 1Z nm cell (Vpgm=23V/Vpass=8V to Vpgm=18V/Vpass=8V). However, if 1Z nm generation (word line half pitch; 10.6nm) is used, V_{PGM} =18V is available to program in case of neighbor V_{PASS}_n+1/n-1=8V. It means that enough high voltage of V_{PGM}=22V/V_{PASS}_n+1/n-1 =12V is available to program with decreasing V_{PASS}_n+2/n-2 to prevent 3) program disturb.

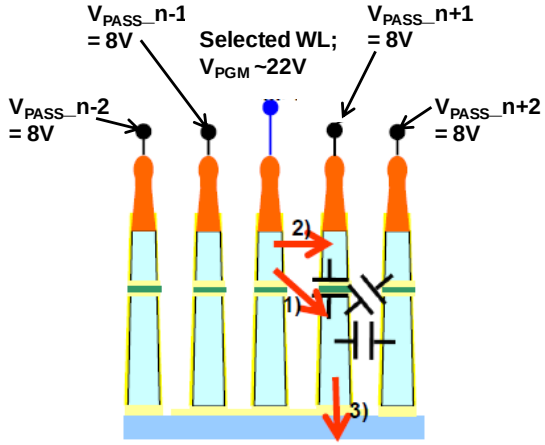


Fig.3.5.15 Word Line (WL) high field problem. 1) Charge loss from neighbor FG to selected WL (CG) [3.5.30], 2) leakage or breakdown between selected WL and neighbor WL, 3) Program Disturb in neighbor cell. Charges (electron) has injected from substrate to FG.

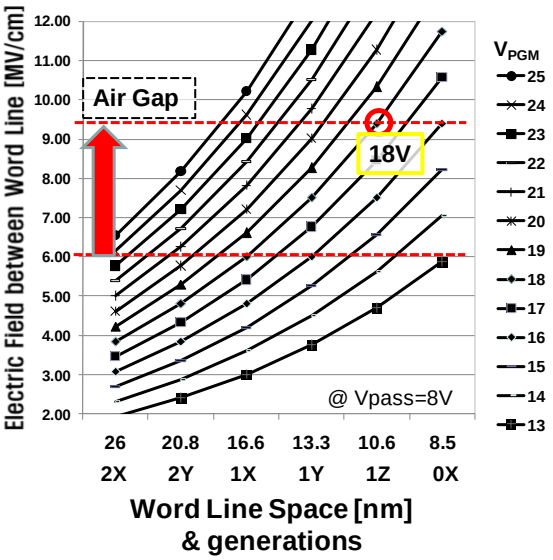


Fig.3.5.16 Estimated Electric field between word lines during programming. In 1Znm generation (word line space 10.6nm), high 18V can be applied due to using air-gap in word line space. [3.5.8]

3.5.10 Summary

A scaling challenge of the SA-STI cell has been investigated for NAND flash memories. Based on assuming the cell scaling dimension and physical parameter trend, we discussed Read Window Margin (RWM), structure challenge, and high field problem. As a result, it is clarified that WL and STI air-gap with 60% FG-FG coupling reduction, a tight control process of 5nm thick FG and CG, and WL air-gap to mitigate WL-WL high field problem are needed in order to realize 1Z nm (10nm) generation.

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3.6 Side-Wall Transfer Transistor Cell (SWATT cell)

Abstract ; A multi-level NAND Flash memory cell, using a new Side-WAll Transfer-Transistor (SWATT) structure, has been developed for a high performance and low bit cost Flash memory. With the SWATT cell, a relatively wide threshold voltage (Vth) distribution width of about 1.1V is sufficient for a 4-level memory cell in contrast to a narrow 0.6 V distribution width that is required for a conventional 4-level NAND cell. The key technology that allows this wide Vth distribution width is the Transfer Transistor which is located at the side wall of the Shallow Trench Isolation (STI) region and is connected in parallel with the floating gate transistor. During read, the Transfer Transistors of the unselected cells (connected in series with the selected cell) work as pass transistors. So, even if the Vth of the unselected floating gate transistor is higher than the control gate voltage, the unselected cell will be in the ON state. As a result, the Vth distribution of the floating gate transistor can be wider and the programming can be faster because the number of program/verify cycles can be reduced. Furthermore, the SWATT cell results in a very small cell size of $0.67um^2$ for a 0.35 um rule. Thus, the SWATT cell combines a small cell size with a multi-level scheme to realize a very low bit cost.

3.6.1 Introduction

It has been proposed that high-density Flash memories [3.6.1]–[3.6.8] will be applied as the mass storage of portable handy terminals, solid state cameras and PC cards, because it has many advantages such as a fast access time, low power dissipation and robustness. However, in order to access these markets, several requirements must be satisfied. The first and most important is a low bit cost. The second item is a high reliability, which is related to the program/erase endurance and data retention. The other items are high speed programming (<1usec/byte) and single 2.5–3.3 V power supply operation.

A NAND-structure Flash memory [3.6.1][3.6.2] had been proposed. This structure reduces the cell size without scaling the design rule by reducing the number of bit-line

contact. We have also developed operation methods for the NAND cell. A bi-polarity Fowler-Nordheim tunneling program/erase method [3.6.2][3.6.9][3.6.10] can be used to obtain a high reliability and high-speed programming. Moreover, a new bit-by-bit verify sequence [3.6.11] results in a tight distribution of the cell threshold voltage after programming. As a result, 3.3 V single power supply operation is possible. Because of the above mentioned reasons, the NAND Flash memory is the most promising candidate for mass storage applications. On the other hand, to reduce the cost per bit of Flash memory, multi-level memory cell technologies have been developed [3.6.12]–[3.6.16] as well as reduced memory cell sizes [3.6.17], [3.6.18]. The chip size can be reduced to about 60% by using a 4-level scheme. However, in a multi-level Flash memory, a narrow threshold voltage distribution of about 0.5 V is necessary for a 4-level memory cell. Due to this narrow threshold voltage distribution, the programming time of the multi-level cell is longer than that of a conventional 2-level cell, and also data retention failures will increase. To avoid these problems, it is important that the allowable threshold voltage distribution width is as wide as possible. In this chapter, a new Side-WAll Transfer-Transistor cell (SWATT cell) for multi-level NAND Flash memory [3.6.19][3.6.20] are described. Using this new cell technology, a wide Vt distribution of 1.1 V can be realized for a 4-level memory cell in comparison to a distribution of 0.6 V for the conventional cells. Therefore, in the SWATT cell, high speed programming and good data retention characteristics can be realized. Furthermore, the SWATT cell results in a very small cell size of 0.67um^2 for a 0.35um rule and a very simple fabrication process. Therefore, a very low bit cost can be achieved.

3.6.2 Concept of the SWATT cell

The schematic view and equivalent circuit of the SWATT cell are shown in Fig.3.6.1. One cell consists of both a floating gate transistor and a Transfer Transistor, which is located at the side wall of the Shallow Trench Isolation (STI) region. These two transistors are connected in parallel. Furthermore, 16 cells are connected in series between two select transistors, to form a NAND structure cell. The read conditions of a conventional NAND cell and a SWATT cell for the conventional 2-level scheme are shown in Fig.3.6.2. In a conventional cell, zero volt is applied to the gate of the selected memory cell, while 5.0 V is applied to the gates of the other cells in the NAND string. All the memory cells, except for the selected cell, serve as transfer gates. Therefore, for the conventional NAND cell, the threshold voltage of the in-series connected cells must be lower than the unselected control gate (CG) voltage of 4.5–5.5 V. Thus, the Vt

distribution of the cells in the programmed state must be narrow with a width of less than 3.0 V for 2-level operation, as shown in Fig.3.6.2 (a).

On the other hand, using the SWATT cell, the side-wall transfer transistor works as a pass transistor instead of a floating gate transistor, as shown in Fig.3.6.2 (b). So the threshold voltage of the floating gate transistor does not have to be lower than the unselected CG voltage of 4.5–5.5 V. Therefore, the Vt distribution of the floating gate transistor in the programmed state is allowed to be very wide with a width >3V for 2-level operation. As a result, the Vt distribution can be wider in comparison with the conventional NAND cell.

The threshold voltage distributions of the 2-level and 4-level scheme are compared in Fig.3.6.3. In a conventional NAND cell, the Vt distribution of the cells in the programmed states (“1”, “2”, and “3”) must be very narrow (0.6 V), because the in-series connected cells must work as pass transistors. However, in the SWATT cell, the Vt distribution of the floating gate transistor in the programmed “1” and “2” states is allowed to be very wide (1.1 V). The Vt distribution in the programmed “3” state is allowed to be even wider than 1.1 V.

This wide threshold voltage distribution result in a high programming speed [3.6.13] because of reducing the number of program/verify cycles [3.6.11] and good data retention characteristics.

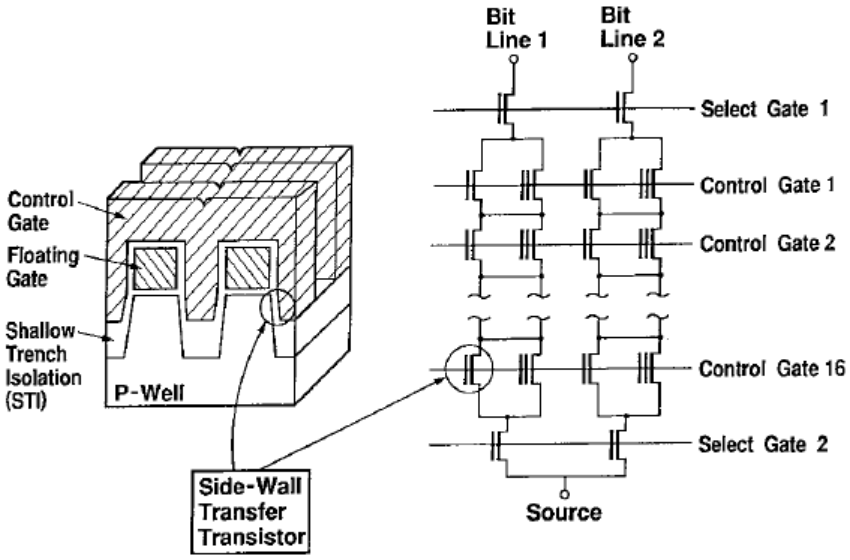

Fig.3.6.1. The schematic view and equivalent circuit of the Side-WAll Transfer Transistor cell (SWATT cell). A Transfer Transistor is located at the side wall of the Shallow Trench Isolation (STI) region and is connected in parallel with the floating gate transistor.

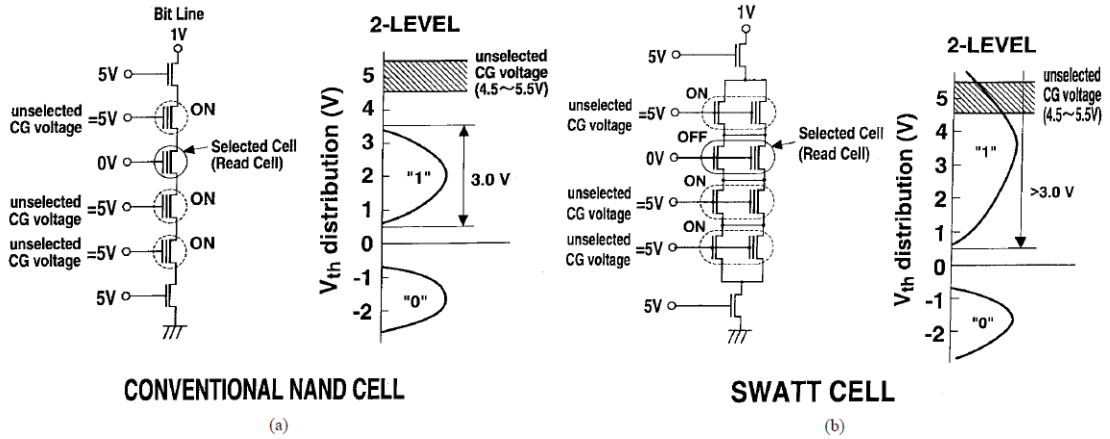

Fig.3.6.2. Read condition of (a) a conventional NAND cell and (b) the SWATT cell for a 2-level scheme. In the conventional NAND cell, the Vth distribution of the cells in programmed state must be narrow with a width of 3.0 V or less, because the unselected cells must work as pass transistors for a control gate voltage of 5 V. However, in the SWATT cell, the side-wall transfer transistor works as a pass transistor. Therefore, the Vth distribution of the floating gate transistor in the programmed state is allowed to be very wide with a width of >3.0 V for 2-level operation.

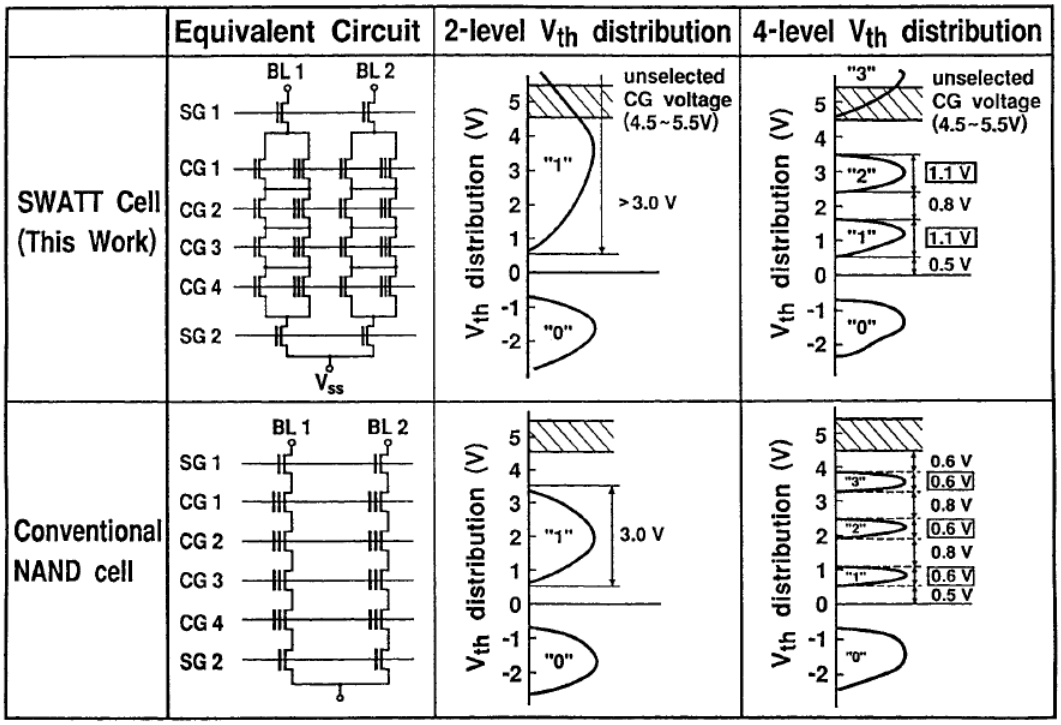

Fig.3.6.3. The cell threshold voltage distribution of the SWATT cell and the

conventional NAND cell for 2-level and 4-level operation. In the SWATT cell, a wide threshold distribution of 1.1 V is allowed for 4-level operation, in comparison with a 0.6V distribution that is required for the conventional NAND cell. The range of the unselected CG (control gate) voltage is limited because of read-disturb.

3.6.3 Fabrication Process

The top view of the SWATT cell is shown in Fig.3.6.4. This NAND structure cell has 16 memory transistors connected in series between two select transistors. The word line pitch is 0.7um. A very narrow bit-line pitch of 0.8um can be realized by using 0.4um width Shallow Trench Isolation (STI) technology. As a result, a small cell size of 0.67 um^2, including the select transistor and drain contact area, can be obtained under a 0.35um design rule. This cell size of $5.5*F^2$, where F is the minimum feature size, is very small in comparison with a conventional DRAM cell of $8*F^2$ and a NOR-type Flash cell of about $10*F^2$. The memory cell parameters are summarized in Table I.

The fabrication of the SWATT cell is simple and uses only conventional techniques. The process sequence of the SWATT cell is shown in Fig.3.6.5. First, a stacked layer of the gate oxide, the floating gate poly-silicon and the cap oxide is formed. Next, the trench isolation region is defined by patterning these three layers, followed by the trench etching, trench bottom Boron implantation and filling with LP-CVD SiO_2, as shown in Fig.3.6.5(a). Subsequently, the LP-CVD SiO_2 is etched back until the side-wall of the STI is exposed (Fig.3.6.5(b)). Boron (B+) ion implantation (60 KeV, 2E12/cm^2) is carried out for Vth adjustment of the side-wall transfer-transistor. After that, the interpoly dielectric (ONO) and Transfer-Transistor gate oxide are formed at the same time, as shown in Fig.3.6.5(c). Then, the control-gate poly-silicon is deposited, followed by the stacked gate patterning (Fig.3.6.5(d)). In this process, the thermal-oxide of the STI side-wall is about 2 times thicker as that on the polysilicon due to oxidation enhancement at the STI side walls. As a result, breakdown of the control gate does not occur even if a high voltage of about 20 V is applied to the control gate during the programming operation.

A cross-sectional TEM photograph is shown in Fig.3.6.6. Both the trench isolation and channel width (gate width) of the floating gate transistor are 0.4um. The vertical channel width of the side wall transfer transistor is about 0.2 um.

An accurate control of the threshold voltage of the side-wall transfer transistor is important for the SWATT cell. The range of the threshold voltage is determined as follows. The side wall transfer transistor must be in the ON state when the unselected

CG voltage (4.5–5.5 V) is applied to the control gate. So, the upper limit of the Vth of the side-wall transistor is 4.5 V. On the other hand, the side wall transfer transistor must be in the OFF state when the read voltage (about 3.9 V) between the “2” and “3” state for 4-level operation is applied to the control gate. Therefore, the threshold voltage of the side wall Transfer Transistor must be in the range from 3.9 V to 4.5 V for 4-level operation (from 0 V to 4.5 V for 2-level). The important statistical parameters of Vth of a side-wall transfer transistor are Boron concentration in the channel region and the side-wall gate oxide thickness. Boron concentration is well controlled by Boron implantation, as shown in Fig.3.6.5 (b). And also, the oxide thickness of the STI side wall is controlled within 10% variation. Therefore, the narrow range of the threshold voltage of the side-wall transfer transistor can be adjusted.

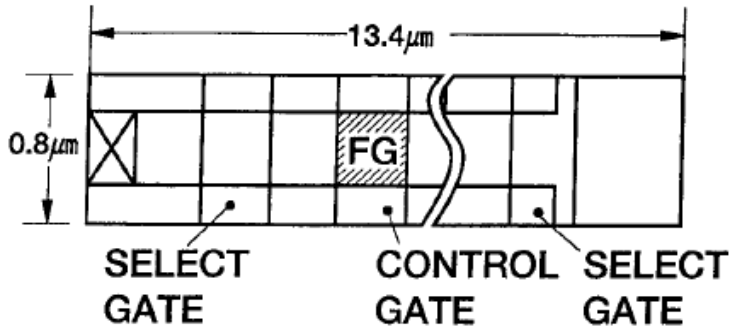

Fig.3.6.4. Top view of the SWATT cell. This NAND structure cell has 16 memory transistors arranged between two select transistors in series. The cell size of the SWATT cell is 0.67um^2 for a 0.35um design rule.

TABLE I MEMORY CELL PARAMETERS

Cell size	0.67 μm^2 (including select Tr etc.)
Gate Length	0.35 μm
Gate Width	0.4 μm
Trench Isolation Width	0.4 μm
Tunnel Oxide	8.5 nm
Interpoly Dielectric	ONO 16 nm (effective)
Side-Wall Dielectric (ONO)	40 nm (effective)

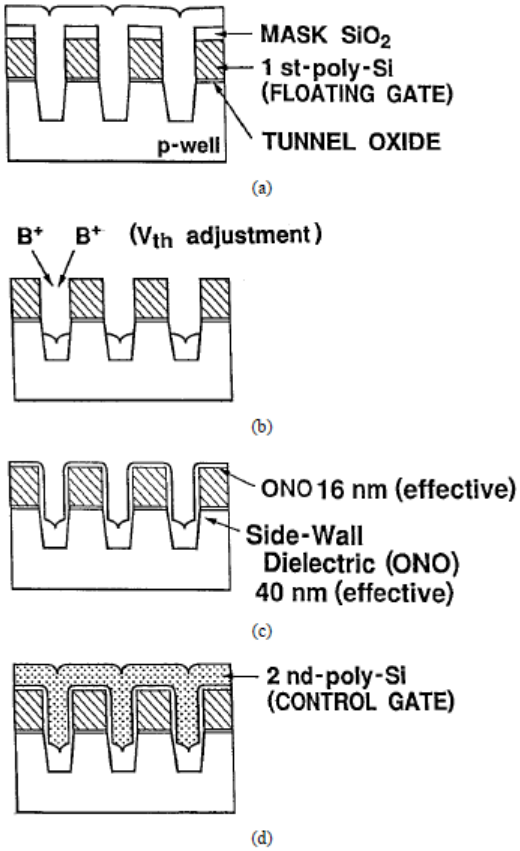

Fig.3.6.5. The process sequence of the SWATT process. (a) Trench etching, LP-CVD SiO_2 fill-in, (b) oxide etch-back and B+ implantation of the Vth adjustment of the side wall transfer transistor, (c) ONO formation, and (d) Control gate formation. The thermal-oxide of the STI side-wall is about 2 times thicker as that on the poly-silicon due to oxidation enhancement at the STI side walls.

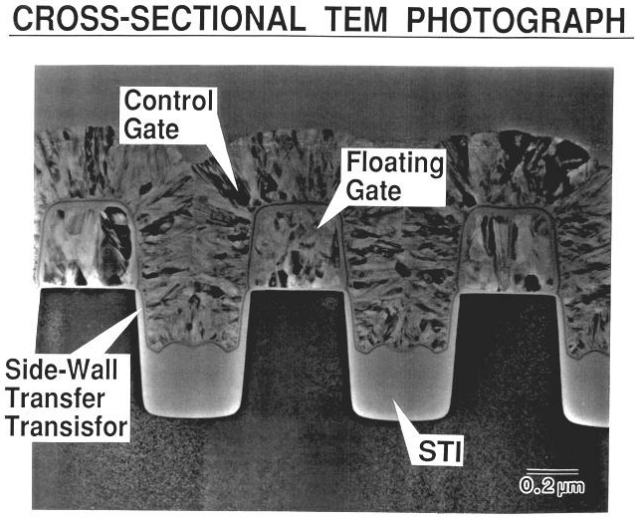

Fig.3.6.6. Cross-sectional TEM photograph of the SWATT cell along the word-line

(Control Gate) direction.

3.6.4 Results and Discussions

A. Isolation

For the NAND EEPROM, the high voltage isolation technology is important to reduce the bit-line pitch. The isolation between the bit-lines must satisfy two demands. One is a high punch-through or junction breakdown voltage of the bit line junction area (>10 V). The other is a high threshold voltage of the parasitic field transistor (>25 V) of the control gate (CG) in the memory cell.

Fig.3.6.7 shows the breakdown voltage of the bit-line junction, which is isolated by the Shallow Trench Isolation (STI). Junction breakdown occurs at about 19 V while no punch-through is observed. The breakdown voltage reduction to about 17 V by applying a negative p-well voltage (Vpwell=-2 V) also indicates that only junction breakdown occurs. The bitline junction breakdown voltage is higher than the required 10 V, which is high enough to realize a 0.4 um trench isolation.

Fig. 3.6.8 shows the threshold voltage of the parasitic field transistor in the SWATT cell. The 0.3 um thick STI field oxide results in a high threshold voltage (>30 V) of the parasitic field transistor between the neighboring bits. As a result, a very tight 0.8 um bit-line pitch can be realized by using STI.

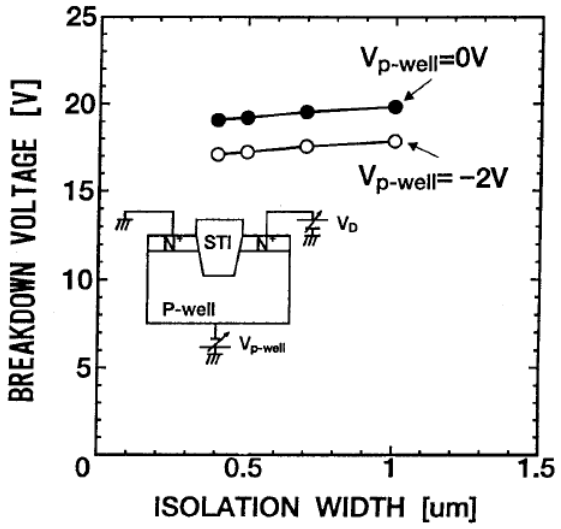

Fig.3.6.7. The breakdown voltage of the bit-line junction, which is isolated by Shallow Trench Isolation (STI). The bit-line junction breakdown voltage is higher than the required 10 V, which is high enough to realize a 0.4 um trench isolation.

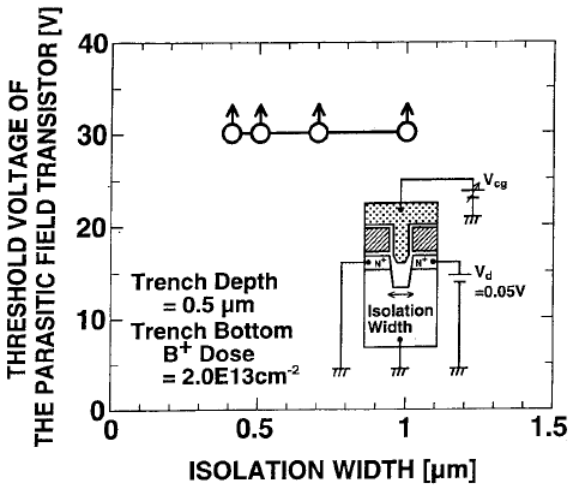

Fig.3.6.8. The threshold voltage of the parasitic field transistor in the SWATT cell, which is isolated by Shallow Trench Isolation (STI). The threshold voltage of the field transistor is higher than 30 V, which is high enough to realize a 0.4 um width trench isolation.

B. Cell Characteristics

The program and erase characteristics of the SWATT cell are shown in Fig.3.6.9 (a) and (b), respectively. During programming, a high voltage of about 20 V is applied to the control gate while the bit lines (source and drain) are grounded, electrons tunnel from the substrate to the floating gate over the whole channel area, resulting in a positive threshold voltage shift [3.6.2][3.6.9]. The threshold voltage saturates at about 4.2 V. This reason is explained as followed. In this memory cell (observed Vth=4.2 V), a floating gate transistor is programmed to high threshold voltage (Vth>4.2 V), so a floating gate transistor is in OFF state for measurement condition. On the other hand, the side wall transfer transistor is in the ON state for Vcg>4.2 V, because the Vth of the side-wall transfer transistor is about 4.2 V. Therefore, the Vth of side-wall transfer transistor is observed. Then, Vth saturates at about 4.2 V even after long programming time (>0.1 msec at 22 V).

During erasing, a high voltage of 20 V is applied to the p-well while the control gates are grounded. Electrons tunnel from the floating gate to the substrate, and the threshold voltage of the memory cells become negative. It can be seen that a fast programming (200 sec/512 byte) and erase operation (2 msec) can be accomplished.

Fig. 3.6.10 shows the sub-threshold characteristics of the SWATT cell at the erased “0” and programmed “1”, “2”, “3” states. In the programmed “3” state, the Vth of the floating gate transistor is higher than 4.5 V, so only the Id of the Side Wall Transfer

Transistor can be observed.

Fig.3.6.11 shows the coupling ratio of the SWATT cell as a function of the gate width (W). In general, as the isolation width between the memory cells is reduced, the coupling ratio is reduced due to the decreased floating gate wing area. However, in the SWATT cell, even if very tight 0.4um width isolation is used, a high coupling ratio of 0.65 can be obtained because the 0.3um high side wall (H) of the floating gate is used to increase the coupling ratio. Moreover, the coupling ratio increases as the gate width W is scaled down. This mean that the programming voltage and erasing voltage (Vpp) can be reduced as the memory cell is scaled down, which allows the design of more compact peripheral circuits such as row decoders and sense amplifiers. Furthermore, the variation of the coupling ratio of the SWATT cell can be very small because the side wall (H) of the floating gate is determined by the thickness of the floating gate poly-silicon. Therefore, a very tight Vt distribution of the SWATT cell can be expected.

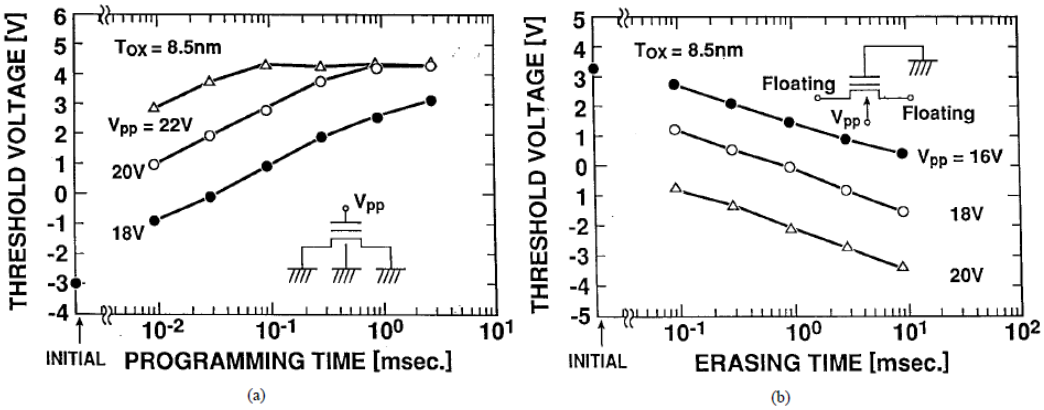

Fig.3.6.9. (a) The program and (b) erase characteristics of the SWATT cell. A short programming time of 200 usec and short erase time of 2 msec can be accomplished by Fowler-Nordheim tunneling over the channel area, applying a positive voltage of 21 V to the control gate during programming and 19 V to the p-well during erasing, respectively.

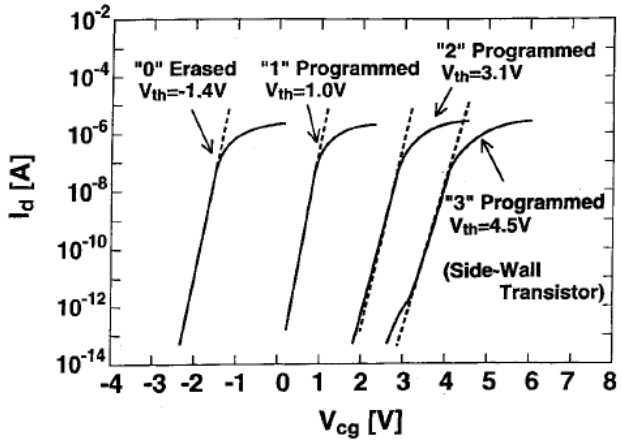

Fig.3.6.10. The subthreshold characteristics of the SWATT cell for the erased "0" and programmed "1", "2", "3" states. In the programmed "3" state, the Side Wall Transfer Transistor is in the ON state.

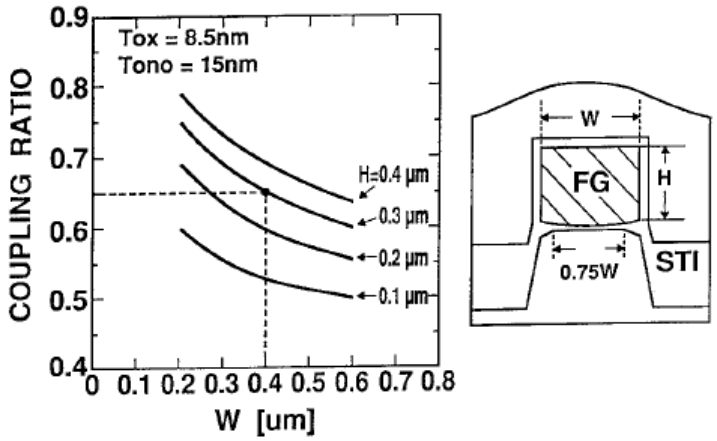

Fig.3.6.11. The coupling ratio of the SWATT cell as a function of the gate width (W). A high coupling ratio of 0.65 can be obtained because the 0.3 um high side-wall (H) of the floating gate is used to increase the coupling ratio.

C. Reliability

Fig.3.6.12 shows the program/erase endurance characteristics of a SWATT cell using the bi-polarity write/erase method [3.6.2][3.6.9]. This method guarantees a wide cell threshold window of as large as 3 V, even after one million write/erase cycles. These endurance characteristics of the SWATT cell are comparable with that of the conventional NAND cell [3.6.2] [3.6.10].

Read disturb occurs as a weak programming mode. When a certain positive voltage is applied to the control gate during a read cycle, a small Fowler-Nordheim tunneling

current flows from the substrate to the floating gate. Unfortunately, the tunnel oxide leakage currents, which are induced by the program and erase cycling stress, degrade the read disturb of the memory cell, as shown in Fig.3.6.13. However, even after one million write/erase cycles, the read disturb time is more than 10 years when a Vcg of 5.0 V is used.

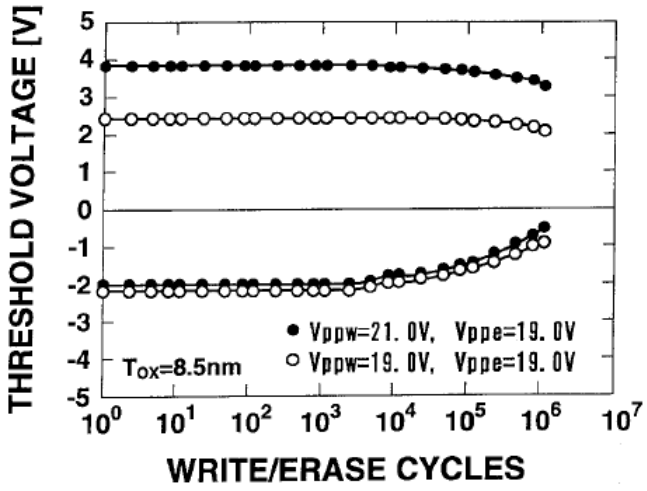

Fig.3.6.12. The program/erase endurance characteristics of the SWATT cell. Window narrowing has not been observed up to one million write/erase cycles.

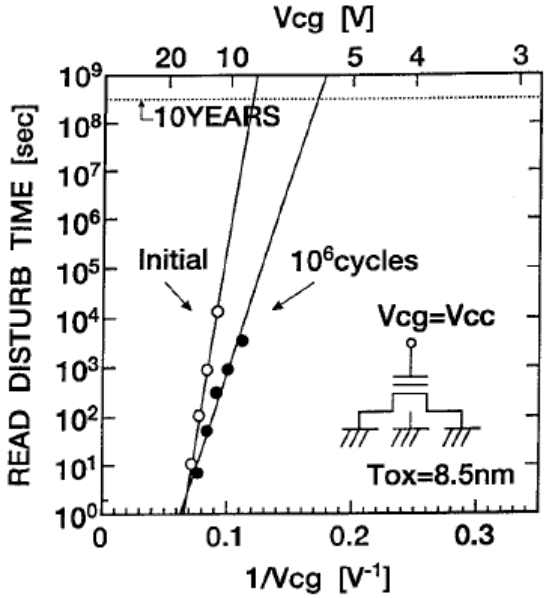

Fig.3.6.13. The read disturb characteristics of the SWATT cell. The read disturb time is more than 10 years when a Vcc of 5.0 V is used, even after 1 million program/erase cycles.

3.6.5 Summary

A Side-WAll Transfer-Transistor cell (SWATT cell) for multi-level NAND Flash memory has been successfully developed by using a 0.35 um technology. The SWATT cell has many advantages: (1) The side wall transfer-transistor structure allows a very wide threshold voltage distribution width of about 1.1 V for a 4-level memory cell, in comparison with a 0.6 V distribution that is necessary for conventional multi-level NAND Flash memory. This wide threshold distribution results in a high programming speed and good data retention characteristics. (2) The SWATT cell structure provides a very small $5.5*F^2$ cell size (F is feature size) that includes the select transistor and bit line contact area. In addition, (3) the SWATT cell structure can be realized with a very simple fabrication process. Thus, a very low bit cost can be realized by using the SWATT cell. Moreover, (4) a relative high coupling ratio of 0.65 can be obtained because the 0.3um high side wall of the floating gate is used to increase the coupling ratio. Furthermore, (5) the coupling ratio increases as the SWATT cell is scaled down. So, the programming and erasing voltage can be reduced as the SWATT cell is scaled down. Therefore, this technology is suitable to realize a low cost and high reliable Flash memory.

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3.7 Summary of Chapter 3.

Several NAND flash cell technologies have been intensively investigated.

First, the LOCOS isolation cell are successfully developed. A small NAND-structure cell of 1.13 μm^2 per bit has been achieved in 0.4 μm technology. The chip size of a 64 Mb NAND Flash using this cell is estimated to be 120 mm^2. In order to realize the small cell size, 0.8 μm field isolation is used with Field Through Implantation (FTI) technique. A negative bias of -0.5 V to the P-well of the memory cell is applied during programming. In addition, a bit-by-bit intelligent writing technology allows a 3.3 V data sensing scheme which can suppress read disturb to 1/1000 in comparison with the conventional 5 V scheme. As a result, it is expected that with this technology, 10^6 program and erase cycles can be achieved.

Second, the Self-Aligned STI cell (SA-STI cell) with FG wing has been developed. A novel high density $5*F^2$ (F; Feature size) NAND STI cell technology have been realized to obtain a low cost and high reliability NAND flash memories. The extremely small cell size of $0.31um^2$ has been achieved for the 0.25um design rule. To minimize the cell size, a floating gate is isolated with shallow trench isolation (STI) and a slit formation by a novel SiN spacer process, which has made it possible to realize a 0.55um-pitch isolation at a 0.25um design rule. Another structural feature to the cell and its small size is the borderless bit-line and source-line contacts which are self-aligned with the select-gate. The proposed NAND cell with the gate length of 0.2um and the isolation space of 0.25um shows a normal operation as a transistor without any punch-through. A tight distribution of the threshold voltages (2.0V) in 2Mbit memory cell array is achieved due to a good uniformity of the channel width in the self-aligned STI cells. And also, the peripheral low voltage CMOS transistors and high voltage transistors can be fabricated at the same time by using the self-aligned STI process. The advantages are (1) The number of process steps is reduced to 60% in comparison with a conventional process, and (2) high reliability of the gate oxide is realized even at high voltage transistors because a gate electrode does not overlap the trench corner. Therefore the SA-STI process integration combines a small cell size with a high reliability for a manufactuable 256Mbit and lGbit flash memory.

Third, an ultra high-density NAND-structured memory cell, using a new SA-STI cell without FG wing technology, has been developed for a high performance and low

bit cost 256Mbit Flash memory. The SA-STI technology results in an extremely small cell size of 0.67 um^2 per bit by using 0.35um design rule, 67% without dimension scaling. The key technologies to realize a small cell size are (1) 0.4um width Shallow Trench Isolation (STI) to isolate neighboring bits and (2) a floating gate that is self-aligned with the STI, eliminating the floating-gate wings. Even though the floating-gate wings are eliminated, a high coupling ratio of 0.65 can be obtained by using the side-walls of the floating gate to increase the coupling ratio. Using this self-aligned structure, a reliable tunnel oxide can be obtained because the floating gate does not overlap the trench corners, so enhanced tunneling at the trench corner is avoided. Therefore, the SA-STI cell combines a low bit cost with a high performance and a high reliability, such as the fast programming (0.2usec/byte), fast erasing (2msec), good program/erase endurance (>1 million cycles), and excellent read disturb characteristics (>10 years).

Next, the scaling limitations and challenges of SA-STI cell over 2X~0X nm generations are clarified for NAND flash memories. The scaling challenges are categorized to 1) narrow Read Window Margin (RWM) problem, 2) structural challenge, and 3) high field (5~10 MV/cm) problem. First, 1) the narrow RWM is investigated by extrapolating physical phenomena of FG-FG coupling interference, Electron Injection Spread (EIS), Back Pattern Dependence (BPD), and Random Telegraph Noise (RTN). The RWM is degraded not only by increasing programmed Vt distribution width, but also by increasing Vt of erase state mainly due to large FG-FG coupling interference. However, RWM is still positive in 1Z nm (10nm) generation with 60% reduction of FG-FG coupling by air-gap process. For 2) structural challenge, the Control Gate (CG) fabrication margin between Floating Gates (FGs) is becoming much severer beyond 1X nm generation. Very narrow 5nm FG width/space has to be controlled. For 3) high field problem, high field between CGs (word lines; WLs) is critical during program. By using WL air-gap, high field problem can be mitigated, and 1Y/1Z nm generations could be realized. Therefore, the SA-STI cell is expected to be able to scale down to 1Z nm (10nm) generation, with the air gap of 60% reduced FG-FG coupling interference and an accurate control of FG/CG formation process.

Finally, a multi-level NAND Flash memory cell, using a new Side-WAll Transfer-Transistor (SWATT) structure, has been developed for a high performance and low bit cost Flash memory. With the SWATT cell, a relatively wide threshold voltage (Vth) distribution of about 1.1V is sufficient for a 4-level memory cell in contrast to a narrow 0.6 V distribution that is required for a conventional 4-level NAND cell. The key technology that allows this wide Vth distribution width is the Transfer Transistor

which is located at the side wall of the Shallow Trench Isolation (STI) region and is connected in parallel with the floating gate transistor. During read, the Transfer Transistors of the unselected cells (connected in series with the selected cell) work as pass transistors. So, even if the Vth of the unselected floating gate transistor is higher than the control gate voltage, the unselected cell will be in the ON state. As a result, the Vth distribution of the floating gate transistor can be wider and the programming speed can be faster because the number of program/verify cycles can be reduced. Furthermore, the SWATT cell results in a very small cell size of $0.67um^2$ for a 0.35 um rule. Thus, the SWATT cell combines a small cell size with a multi-level scheme to realize a very low bit cost.

Chapter 4
Three-Dimensional NAND Flash Cell

4.1 Background of 3-Dimensional NAND cells

The demand of NAND Flash memory [4.1.1]-[4.1.3] is tremendously increasing with expanding applications, such as smart phone, tablet PC, and solid-state drive (SSD), because a bit cost is decreasing intensively by aggressive scaling of memory cell, as shown in Fig.4.1.1 [4.1.19]. However, beyond 20nm design rule, the scaling of planar (two-dimensional) NAND flash memory cell is facing several physical limitations, such as FG-FG coupling interference, random telegraph signal noise (RTN), etc., as described in chapter 3.5.

In order to scale down NAND Flash memory cell further, several three-dimensional (3D) NAND flash cells [4.1.4]-[4.1.6] have been proposed before 2006, as shown in Fig.4.1.2 [4.1.19]. However they could not decrease a bit cost effectively because of a complicate fabrication process, an increased process steps, and large unit cell size. In 2007, the BiCS cell (Bit Cost Scalable cell) had been proposed [4.1.7], as shown in Fig.4.1.2. The BiCS cell has a new process concept that poly-Si channel through-hole is fabricated after deposited stacked gate layers, as shown in Fig.4.1.3 and Fig.4.1.4. Due to this new process concept, fabrication process became simple and very low cost, and also it is expected that very small effective cell size could be achieved.

After introducing BiCS cell in 2007, several 3D NAND cells were proposed, such as an advanced BiCS [4.1.8][4.1.9], P-BiCS [4.1.10]-[4.1.12], VRAT [4.1.13], VG-NAND [4.1.14], TCAT [4.1.15], VG-TFT [4.1.16][4.1.17], as shown in Fig.4.1.2. As an example, TCAT cell is one of the similar concept of the BiCS cell, as shown in Fig.4.1.5 [4.1.15]. These 3D cells use SONOS(Silicon-Oxide-Nitride-Oxide-(poly-)Si) device structure with a charge trap nitride as a storage layer. However, it is well known that SONOS cell have serious inherent problems, such as slow erase speed, bad retention characteristics, and inevitable charge spreading issue through the charge trap nitride layer [4.1.18]. The stored charges in Si nitride move toward the neighbor cells, because the charge trap nitride layer is physically connected to neighbor cells. As a result,

SONOS cell would cause serious degradation of data-retention characteristics and poor Vt distribution of cell state.

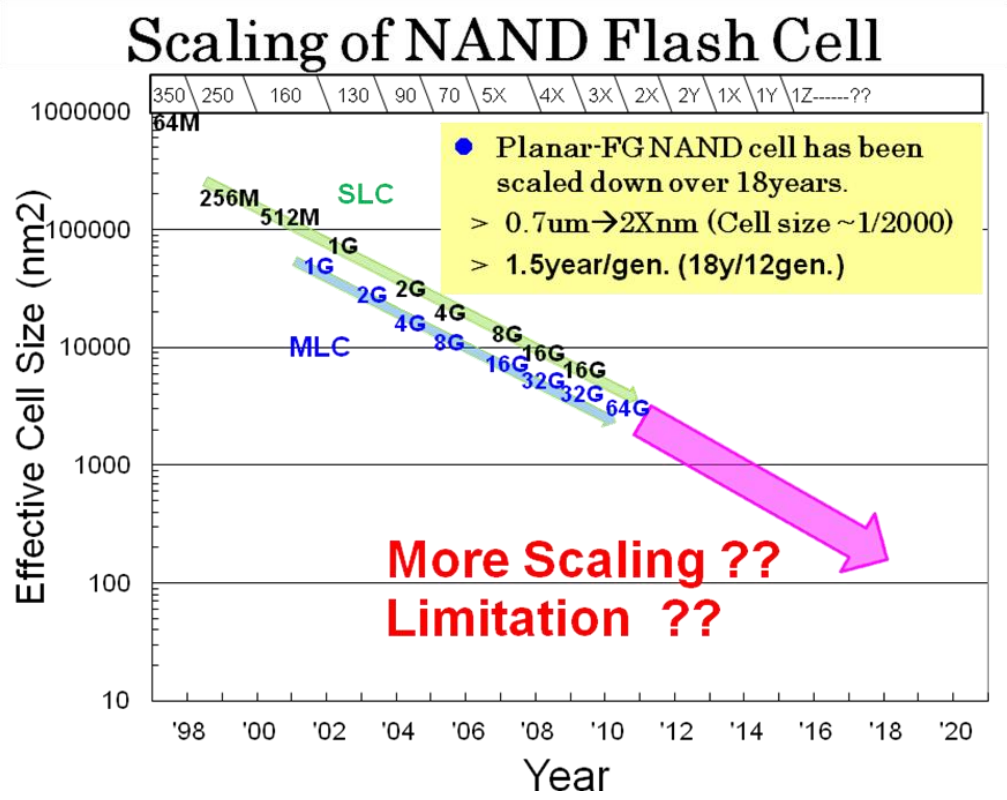

Fig.4.1.1 Scaling trend of NAND Flash memory cell [4.1.19].

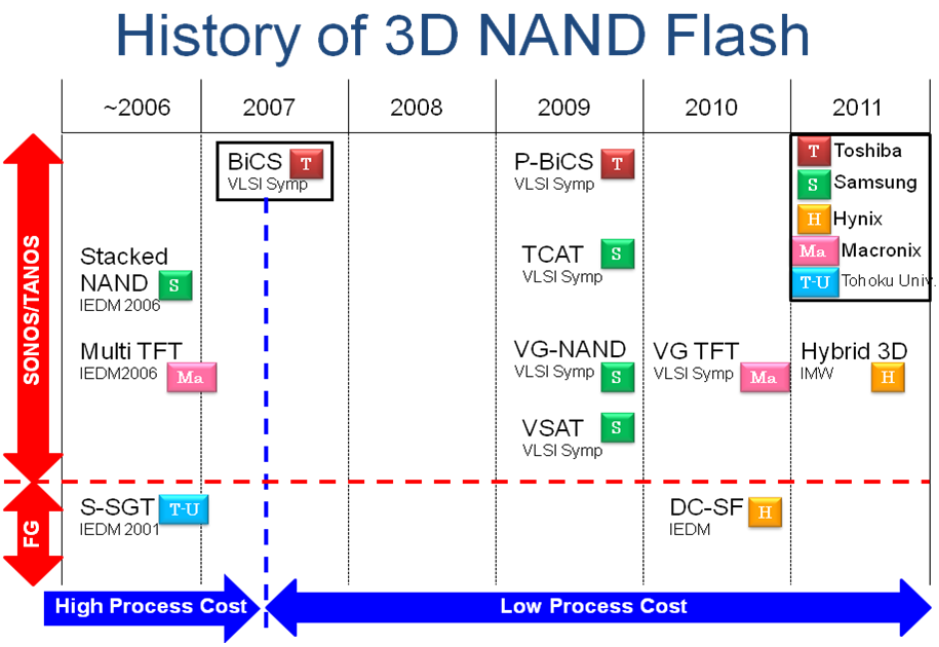

Fig.4.1.2 History of 3-dimensional NAND Flash [4.1.19].

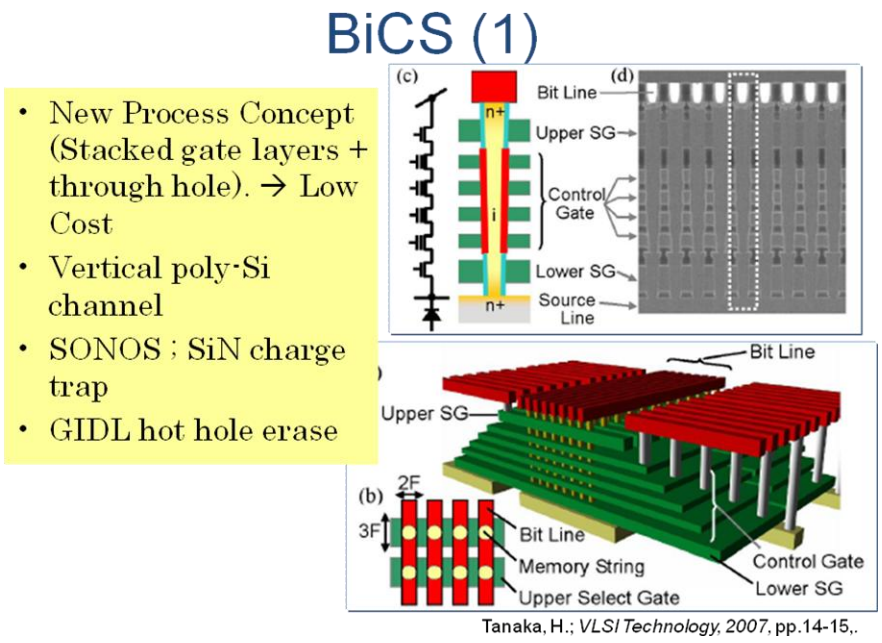

Fig.4.1.3 BiCS cell [4.1.7][4.1.19].

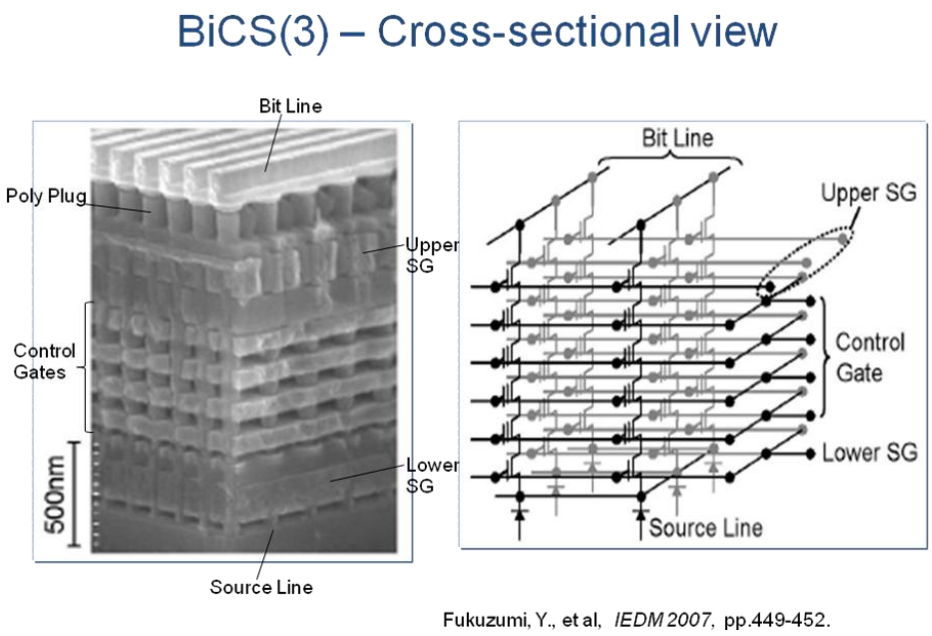

Fig.4.1.4 BiCS cell cross-sectional SEM photo and equivalent circuit [4.1.7][4.1.19].

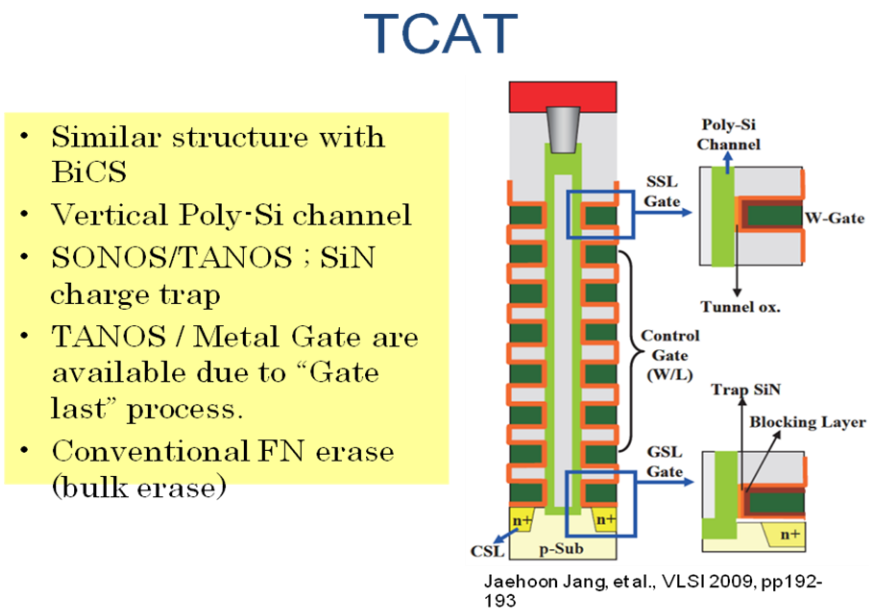

Fig.4.1.5 TCAT cell [4.1.15][4.1.19].

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4.2 Dual Control gate – Surrounding Floating gate Cell (DC-SF cell)

Abstract ; A novel three-dimensional (3D) Dual Control gate with Surrounding Floating gate (DC-SF) NAND flash cell has been successfully developed. The DC-SF cell consists of a surrounding floating gate with stacked dual control gates. With this structure, high coupling ratio, low voltage cell operation, and wide Program/Erase

window (9.2 V) can be obtained. Moreover, negligible FG-FG coupling interference (12 mV/V) is achieved due to the control-gate shield effect. As a result, DC-SF NAND flash cell can overcome the problems of SONOS-based 3D NAND flash. It is proposed that 3D DC-SF NAND flash cell is the most promising candidate for 1 Tb and beyond, with stacked multi bit FG cell (2 ~ 4 bits/cell).

4.2.1 Introduction

The market size of NAND Flash memory [4.2.1]-[4.2.3] is increasing with extensive applications, such as smart phone, tablet PC, and solid-state drive (SSD), because a bit cost is decreasing lower and lower. However, beyond 20-nm design rule, the scaling of NAND flash cell is becoming difficult due to the many physical limitations, such as FG-FG coupling interference, random telegraph noise (RTN), reducing number of stored electrons, etc. Thus, there has been tremendous attention on three-dimensional (3D) NAND flash memory [4.2.4]-[4.2.15]. Most of them use SONOS/TANOS device structure with a charge trap nitride as a storage layer. However, it is well known that these structures with a charge trap nitride layer have suffered from inherent problems, such as low erase speed, poor retention characteristics, and charge spreading issue [4.2.16] between cells along the charge trap nitride layer. The charge spreading problem is illustrated in Fig.4.2.1 (a). The stored charges in Si nitride move toward the neighbor cells through connected nitride, because the charge trap nitride layer is physically connected from top to bottom CGs in 3D SONOS/TANOS NAND Flash. As a result, this would cause degradation of data-retention characteristics and poor Vt distribution of cell state in 3D SONOS cell. As these problems are related to charge trap nitride, floating gate type 3D NAND flash is required to be used instead of charge trap nitride. However, applying conventional two-dimensional (2D) floating gate structure without schematic change is not suitable for 3D NAND flash because the lateral space occupation of floating gate is large.

Here, a dual control-gate with surrounding floating-gate (DC-SF) NAND flash cell for 3D NAND flash memory has been proposed [4.2.17]-[4.2.19]. This structure allows us to apply a floating gate to 3D NAND flash structure with minimal cell size of floating gate (FG) in lateral direction and high coupling ratio. The DC-SF cell and 3D SONOS cell [4.2.4]-[4.2.9] are compared in vertical schematic as shown in Fig.4.2.1. The surrounding FG in the DC-SF cell is completely isolated by IPD and tunnel oxide

as shown in Fig.4.2.1 (b). This implies that significant improvement of data retention is expected for the DC-SF cell due to no physical leakage path.

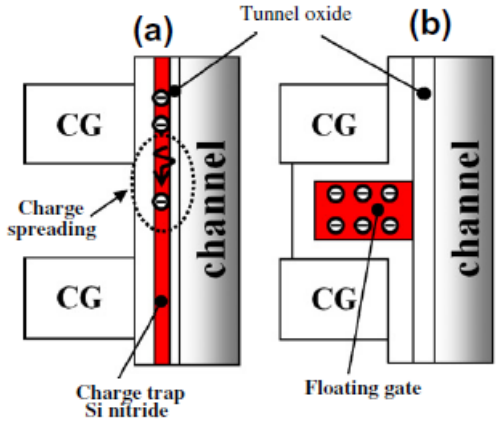


Fig.4.2.1. Comparison of 3D NAND flash cell structures. (a) SONOS cell (BiCS, etc). (b) DC-SF cell. In the case of SONOS cell, charge spreading problem is caused by connected charge trap Si nitride layer.

4.2.2 DC-SF NAND Flash cells

A. Concept

Figure 4.2.2 shows the cross-sectional schematic of the DC-SF NAND flash cell. A surrounding FG is located in between the two control gates (CGs), which is a new approach for 3D NAND flash memory. The detailed schematic of the cell structure is illustrated in right side of Fig.4.2.2. The surrounding FG is covered by inter poly dielectric (IPD) and tunnel oxide. Therefore, two CGs are vertically capacitive coupled with FG. The tunnel oxide is only formed in between the channel poly and FG, while IPD is added on the side wall of the CG, resulting in thicker dielectric layer formed between the channel poly and CG. This means that during program and erase, the charges can tunnel only through the tunnel oxide between the channel poly and FG without any tunneling between the channel poly and CGs.

There are several significant advantages of the DC-SF structure. The first advantage is that the floating gate, which is a proven and predictable technology in NAND flash memory, can be used as a charge storage node so that many issues related to charge trap (SONOS and TANOS) cell could be eliminated. The second is the significant improvement in the coupling ratio because a new concept of functionality is

implemented to 3D structure – one surrounding FG is controlled by two neighboring control gates. As a result, enlargement of surface area between FG and two CGs can be achieved. Therefore, it can be attributed to low bias cell operation for program and erase. The third is to shrink the unit cell size in the horizontal direction, because FG is not positioned between the CG and channel poly in a horizontal direction, but is positioned in between two CGs in a vertical direction, implying that it is suitable for fabrication of 3D NAND flash structure. The fourth is very small FG-FG coupling interference, because a CG positioned in two FGs plays a role of the electrical shield. Therefore, there is negligible capacitive coupled capacitance in between FGs. As a result, DC-SF allows wide program/erase (P/E) window and low bias cell operation for 3D NAND flash device. The equivalent circuit of DC-SF cell string is given in Fig.4.2.3. The single cell consists of one FG and two CGs.

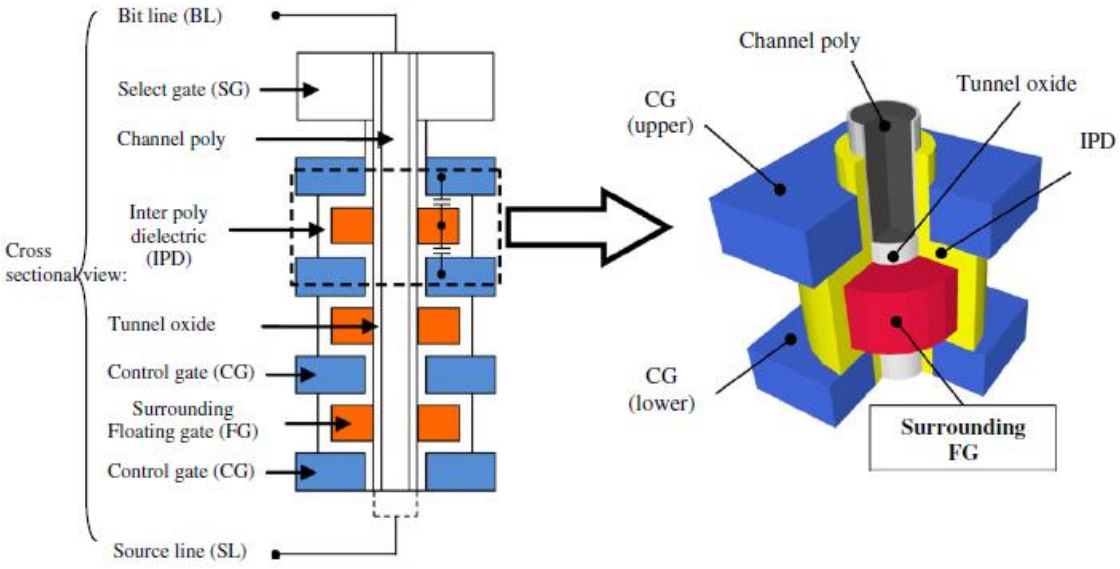


Fig.4.2.2. Cross-sectional schematic of the DC-SF NAND flash. ; Two control gate (CGs) are vertically capacitive coupled with floating gate (FG). Bird's view of the DC-SF NAND flash cell. ; Surrounding FG is capacitively coupled with both upper and lower CG.

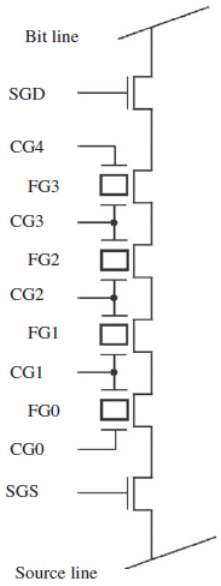


Fig.4.2.3. Equivalent circuit of the DC-SF NAND cell string.

B. Coupling Ratio

Figure 4.2.4 shows the top and cross-sectional view of the DC-SF cell. The capacitively coupled capacitance of the FG is estimated by two different formulas in the DC-SF structure. In the vertical direction of the FG, the coupled capacitance between the FG and two CGs (C_{IPD}) is determined by parallel plate capacitance, as shown in Equation (1).

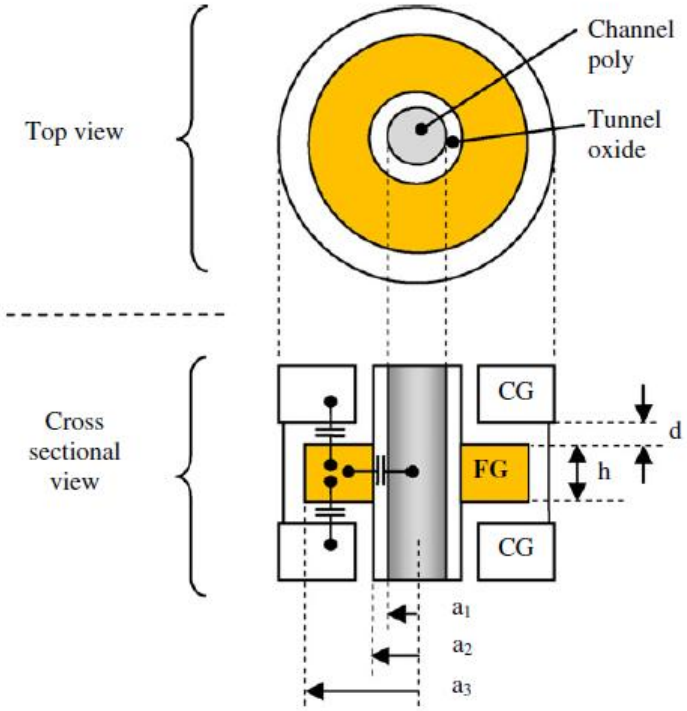
$$C_{IPD} = \frac{2\varepsilon_r \varepsilon_0 \pi (a_3^{\,2} - a_2^{\,2})}{d} \quad (1)$$

$$C_{Tox} = \frac{2\pi\varepsilon_r \varepsilon_0 h}{\ln(a_2 / a_1)} \quad (2)$$

On the other hand, the capacitively coupled capacitance of the FG with tunnel oxide (C_{Tox}) in the horizontal direction is extracted by coaxial cable capacitance as shown in Equation (2), because the FG is covered on the cylindrical channel poly. The calculation of coupling ratio is plotted as a function of the FG width, FG height and the radius of channel poly in case of T_{ox}=8nm and T_{IPD}=12nm thick, as shown in Fig.4.2.5. The high coupling ratio of 0.68 can be obtained, for example, in structure of a_1=20nm, a_2=28nm, a_3=68nm, h=40nm and d=12nm, that is (FG width)=(a_3-a_2)=40nm, (FG height)=h=40nm, (Radius of channel)=a_1=20nm.

The coupling ratio decreases with decreasing FG width (a_3-a_2), as shown in Fig.4.2.5(a), because the capacitor area of FG and CG decreases. On the contrary, the

coupling ratio increases as the FG height (Fig.4.2.5(b)) and radius of the channel (Fig.4.2.5(c)) poly decrease, implying that the cell size in the horizontal direction can be reduced by increasing the coupling ratio in this structure. This result indicates that high coupling ratio of about 0.7 can be maintained even though the cell size decreases, because the coupled capacitance of FG is compensated in both the directions. When compared with the conventional planar 2D NAND flash memory, which suffers from low coupling ratio as the cell size decreases, the DC-SF cell structure has an advantage of maintaining high coupling ratio even at the smaller cell size. With this structure, the coupling ratio of about 0.7 can be achieved.



a_1: radius of channel poly
a_2: radius of channel poly + tunnel oxide
a_3: radius of channel poly + tunnel oxide + FG
d: IPD thickness
h: FG poly Si height

Fig.4.2.4. Floating gate capacitance of the DC-SF cell.

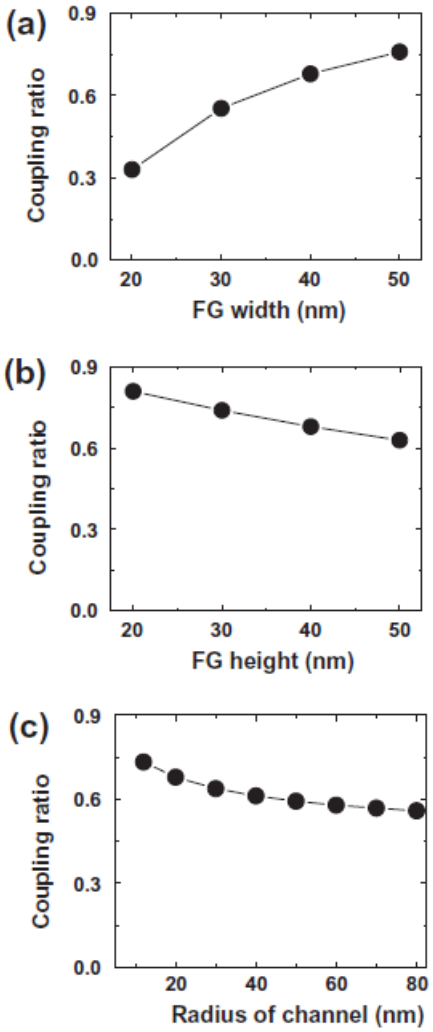


Fig.4.2.5. Coupling ratio of the DC-SF cell in case of T_{ox} = 8 nm and T_{IPD} = 12 nm. (a) Coupling ratio of the DC-SF as a function of FG width (a_3_a_2) (FG height: 40 nm and radius of channel poly: 20 nm). (b) Coupling ratio of the DC-SF as a function of FG height (h) (FG width: 40 nm and radius of channel poly: 20 nm). (c) Coupling ratio of DC-SF as a function of radius of channel poly (a_1) (FG height: 40 nm and FG width: 40 nm).

C. Device Fabrication

The process sequence of the DC-SF cell is shown in Fig.4.2.6. First, in-situ thermal CVD SiO_2 and poly Si are deposited in sequence to make multi-stacked layers. Thus, holes are formed by etch process through the entire SiO_2/poly-Si stacked layers (Fig.4.2.6(a)). To make a space for IPD and FG, oxide recess is carried out in the horizontal direction (Fig.4.2.6(b)). IPD deposition is followed (Fig.4.2.6(c)) and the

space is filled with FG poly-Si deposition overall inside the holes (Fig.4.2.6(d)). To define complete FGs in the hole, isotropic etch process of FG is performed. FGs of poly-Si are separated to each recess positions. Tunnel oxide is deposited (Fig.4.2.6(e)), and then the first channel poly-Si is deposited to cover tunnel oxide, then the first channel poly-Si and tunnel oxide at bottom of holes are removed by RIE. And then the second channel poly-Si is deposited to fill hole, as shown in Fig.4.2.6(f). The second channel poly-Si is electrically connected to substrate. The cross-sectional transmission electron microscopy (TEM) image of the DC-SF cell arrays is shown in Fig.4.2.7(a). It can be clearly seen that the surrounding FGs and CGs are well fabricated along the channel (Fig.4.2.7 (b)).

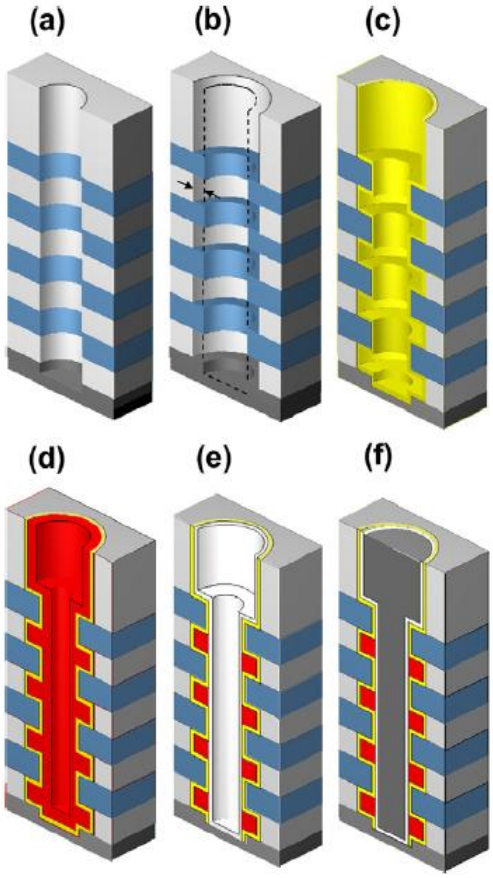


Fig.4.2.6. Process sequence of DC-SF NAND flash cell. (a) Oxide/poly deposition and hole formation by etch process. (b) Oxide recess is carried out to make a space for IPD and FG. (c) IPD deposition. (d) FG poly Si deposition. (e) Isotropic etch of FG and tunnel oxide deposition. (f) Channel poly deposition.

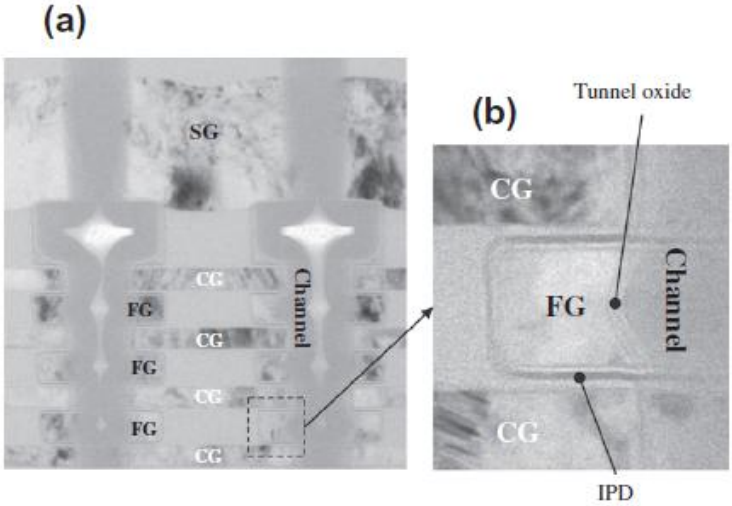


Fig.4.2.7. (a) TEM image of the DC-SF NAND cell string. FGs and CGs are stacked. (b) Detail TEM image of the cell, showing the FG and two CGs with tunnel oxide and IPD on the channel.

4.2.3 Results and Discussions

The operation conditions of the DC-SF cell are listed in Table 1. For the erase operation, an erase bias of -11 V is applied to all the CGs. Cell Vt decrease to negative. In program and read condition, FG2 between CG2 and CG3 is selected. The program bias (Vpgm ; 15V) is applied to both CG2 and CG3 simultaneously. Two different V_{pass} biases are used to prevent the program disturb. In the neighboring wordline of CG1 and CG4, lower Vpass bias of 2 V is applied. And the normal Vpass bias of 4V is applied to the other CGs during programming. The potentials of FG1 and FG3 are compensated by lower bias of 2V in order to prevent program disturb. For the read operation, zero bias is applied to both CG2 and CG3 with a read pass bias (Vread) of 4 V to the other CGs. As can be seen in Table 1, all the operation biases are significantly lower than those of conventional 3D NAND flash memory based on charge trap nitride. This is due to the well-designed cell structure of the DC-SF and high coupling ratio.

The I_d-V_g characteristics of the DC-SF NAND flash cell is plotted with different erase times in Fig.4.2.8. The figure shows that cell Vt decreases as the erase time increases, implying that the erase cell operates effectively. As a result, wide Program/Erase window of about 9.2 V is obtained.

Figure 4.2.9(a) shows the program characteristics. The cell Vt is plotted as a function of the program pulse width with various program biases. It shows that the DC-SF cell is well programmed even at a low program bias of 15 V. The coupling ratio of this cell is estimated to 0.71. Figure 4.2.9(b) shows the erase characteristics. The cell Vt is measured as a function of the erase pulse width with various erase biases. The DC-SF cell can be erased well at low erase bias of -11 V for 1 msec. These operation voltages are significantly lower than those of conventional 3D SONOS NAND flash memory structure and planar 2D NAND flash cell. This implies that cell operation in the DC-SF structure is considerably effective because of high coupling ratio.

The FG-FG coupling interference between a programmed cell and an adjacent cell was studied, as shown in Fig.4.2.10. The **Δ**Vt of the adjacent cell has been measured as a function of programmed cell Vt from 2.0 to 3.6 V. Very small capacitive coupling interference of 12mV/V is observed due to CG electric shield effect between FGs. And the FG-FG couplings of x-direction (along WL) and y-direction (along BL) for one-side are estimated to 1.1% and 0.7% of total FG capacitance, respectively, based on scaled cell size as shown in Fig.4.2.13(c). Then total FG-FG coupling of x- and y- directions is 3.6%. It is much smaller value in comparison with the conventional FG cell. With this small FG-FG interference result, it is expected that Vt distribution setting could be acceptable for multi-level cell (MLC) or triple-level cell (TLC) as shown in Fig.4.2.11.

Figure 4.2.12 shows the data-retention characteristics at two different temperatures (90 and 150 C). For the high-temperature condition, the program and erase charge-losses are 0.9V and 0.2V for 126 hours, respectively.

Table 1
Operation conditions for the DC-SF NAND cells. FG2 between CG2 and CG3 is selected in program and read.

Bias	Erase (V)	Program (V)	Read (V)
BL	0	0/Vcc	1
SGD	4.5	4.5	4.5
CG4	V_{erase}:−11	V_{pass2}:2	V_{read}:4
CG3	V_{erase}:−11	V_{pgm}:15	0
CG2	V_{erase}:−11	V_{pgm}:15	0
CG1	V_{erase}:−11	V_{pass2}:2	V_{read}:4
CG0	V_{erase}:−11	V_{pass1}:4	V_{read}:4
SGS	4.5	0	4.5
SL	0	Vcc	0

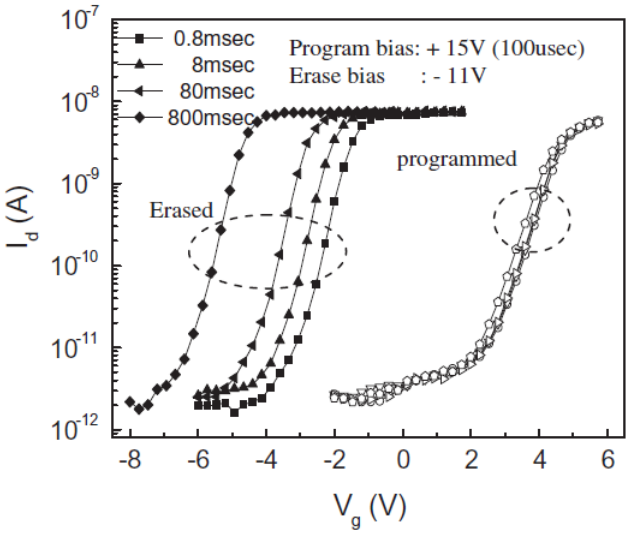
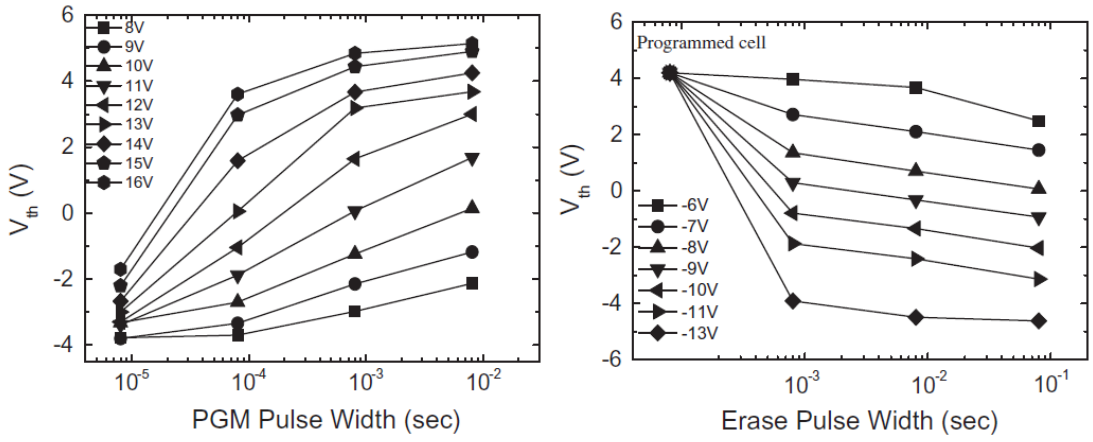


Fig.4.2.8. The Id–Vg characteristics of the DC-SF NAND flash cell. Vg is VCG2 (= VCG3) bias. Vread for unselected control gate are VCG0 = VCG1 = VCG4 = 4 V. And Bit line voltage is Vd = 1 V.



(a) (b)

Fig.4.2.9. The program and erase characteristics of the DC-SF NAND flash cells.

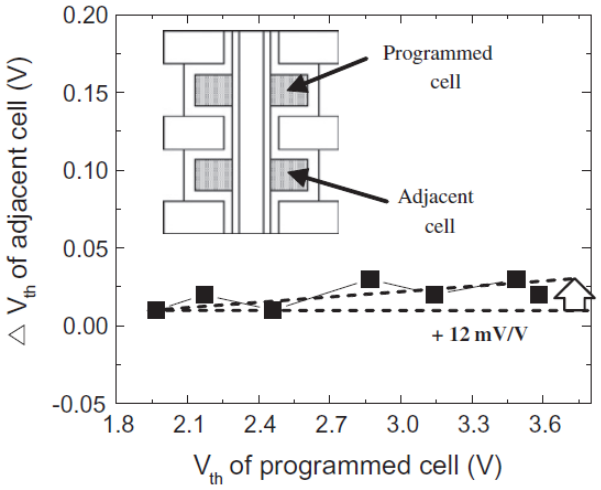


Fig.4.2.10. The interference characteristics between FG and FG (Vth difference of the adjacent FG vs. Vth of the programmed cell). Very small FG–FG coupling value of 12 mV/V is obtained.

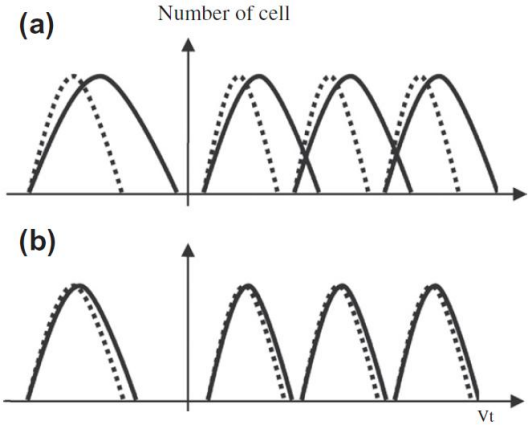


Fig. 4.2.11. Cell threshold voltage (Vt) setting comparison between: (a) conventional planar FG cell with large FG–FG coupling interference and (b) DC-SF cell with small FG–FG coupling interference. The DC-SF cell has a wider Vt setting margin due to negligible FG–FG coupling.

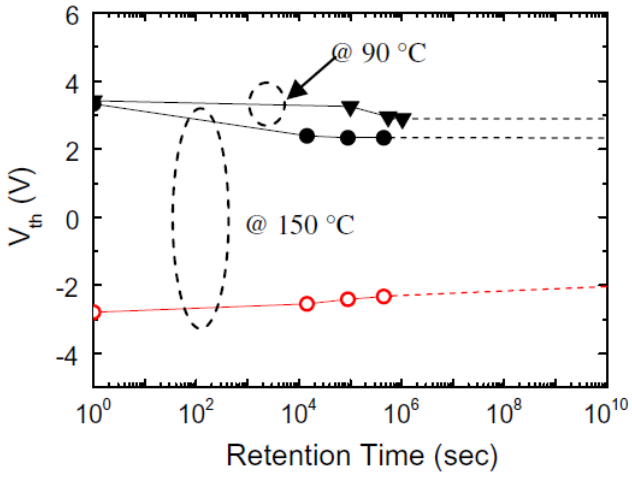


Fig.4.2.12. The data-retention characteristics of the DC-SF NAND flash cells. Amount of Vth shift is not significant, which suggests good retention characteristics.

4.2.4 Scaling Capability

In order to evaluate the scaling capability of the DC-SF cell, the effective cell size of the DC-SF structure and conventional 3D SONOS have been compared, as shown in Fig.4.2.13. The assumption of physical unit cell size is that *x*- and *y*-pitch of BiCS [4.2.4]-[4.2.9] / TCAT [4.2.12] are 100 and 160 nm, respectively. On the other hand, the *x*- and *y*-pitch of the DC-SF cell are 130 and 190 nm. The physical cell size of DC-SF cell is larger than that of BiCS/TCAT, because space margin between FG and slit edge (gate edge) is needed. The feature size here is assumed to be 40 nm for both DC-SF and BiCS/TCAT. And, in this design rule, the high coupling ratio of 0.60 can be still obtained in structure of a_1=15nm, a_2=23nm, a_3=50nm, h=30nm, and d=12nm, that is (FG width) =(a_3-a_2)=27nm, (FG height)=h=30nm, (Radius of channel)=a_1=15nm. Even if the physical cell size of the DC-SF cell is larger than that of conventional BiCS/TCAT, the effective cell size of the DC-SF can be comparable with BiCS/TCAT, because multi-bit cells (2 bits/cell, 3 bits/cell, and 4 bits/cell) are available due to wide cell Vt window and negligible FG-FG coupling interference. As a result, the DC-SF cell can realize 1 Tb NAND Flash device with 3 bits/cell +64 stacked.

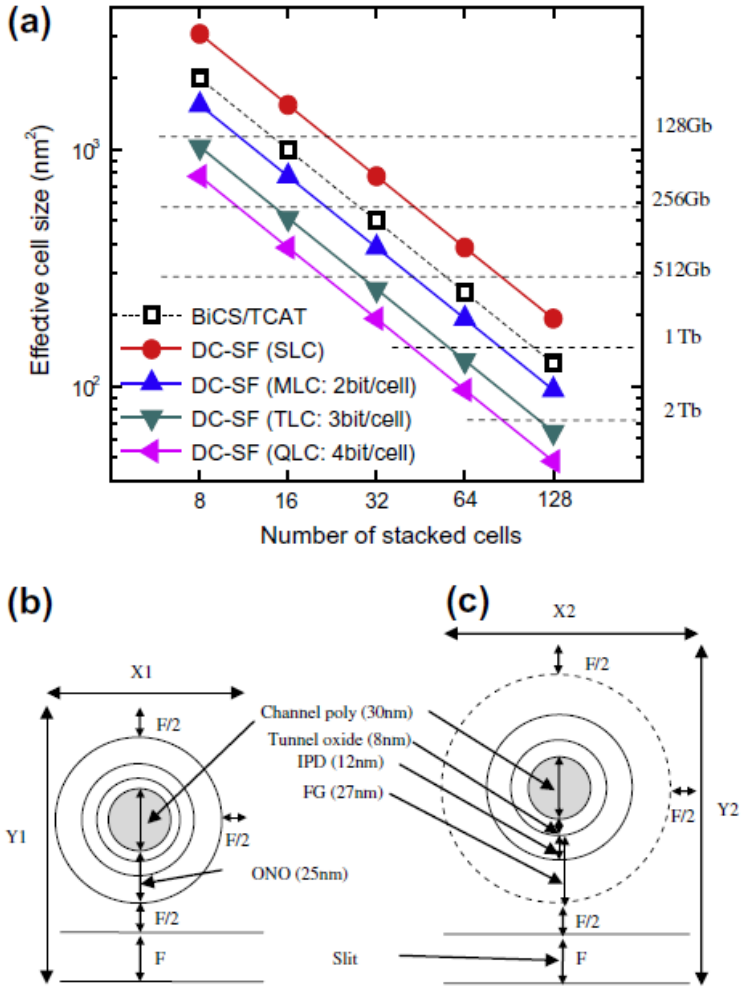


Fig.4.2.13. (a) Effective cell sizes for the DC-SF NAND flash cell. The DC-SF cell can be realized for 1 Tb with 3 bits/cell + 64 cells stacked, 2 Tb with 3 bits/cell + 128 cells stacked. (b) Assumption of cell size for BiCS (F = 40 nm, cell-to-cell distance: F/2, slit distance: F, X1 * Y1 = 100 * 160 nm2). (c) Assumption of cell size for DC-SF (F = 40 nm, cell-to-cell distance: F/2, slit distance: F, X2 * Y2 = 130 * 190 nm2).

4.2.5 Summary

The 3D DC-SF NAND flash memory cell has been successfully developed. Low voltage program/erase operation and wide Program/Erase window of 9.2 V are obtained. And also, it has been evaluated that the FG-FG capacitive coupling interference is drastically small (12mV/V), compared with conventional 2D FG flash cell (>100mV/V at 2Y nm generation). These results are sufficient to enable multi-bit cell operation of

MLC and TLC. Therefore, the 3D DC-SF NAND cell is a promising candidate for 1Tb and beyond NAND flash memories.

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SungKi Park, SungJoo Hong, “A novel three-dimensional dual control-gate with surrounding floating-gate (DC-SF) NAND flash cell Original Research Article”, *Solid-State Electronics, Volume 79, January 2013, Pages 166-171*

4.3 Advanced DC-SF cell

Abstract ; Advanced DC-SF (Dual Control gate with Surrounding Floating gate) cell process and operation schemes have been successfully developed for 3-dimensional NAND Flash memories. In order to improve performance and reliability of DC-SF cell, new Metal Control Gate Last (MCGL) process has been developed. The MCGL process can realize a low resistive tungsten (W) metal word-line, a low damage on tunnel oxide/IPD (Inter-Poly Dielectric), and a preferable FG shape. And also, new read and program operation schemes have been developed. In new read operation, the higher and lower $V_{pass-read}$ are alternately applied to unselected control gates (CGs) to compensate lowering FG potential to be a pass transistor. And in new program scheme, the optimized V_{pass} are applied to neighbor WL of selected WL to prevent program disturb and charge loss through IPD. Thus, by using MCGL process and new read/program schemes, high performance and high reliability of DC-SF cell can be realized for 3D NAND flash memories.

4.3.1 Introduction

Recently, several three-dimensional (3D) NAND flash cells have been proposed [4.3.3]-[4.3.8] to scale down NAND Flash memory cell [4.3.1][4.3.2] further. These 3D cells are using charge trap (CT) type flash cell, which stores charges in SiN layer, then they have several intrinsic disadvantages, such as slow erase speed, small data retention margin [4.3.9], and charge spreading issues [4.3.10]. In order to overcome the intrinsic disadvantages of CT type flash cell, Floating Gate (FG) type DC-SF 3D NAND flash memories was proposed [4.3.11][4.3.12], as shown in Fig.4.3.1. The DC-SF cell has several advantages, such as fast erase speed, wide Vt window, very small FG-FG coupling interference, etc. However, in the DC-SF cell process [4.3.11][4.3.12], there were still several critical problems, as shown in Fig.4.3.2(b), namely (1) High word line resistance of the poly gate, (2) damage on IPD ONO by the FG separation process, and (3) field confinement at FG edge during programming due to the horn shape FG. And also, read and program operations of the DC-SF cell had not been optimized yet, resulting in causing several disturb problems.

In this chapter, we propose a novel MCGL process and new read/program schemes for the DC-SF cell in order to overcome the above problems [4.3.15]. As a result, excellent performance and reliability of the DC-SF cell can be realized.

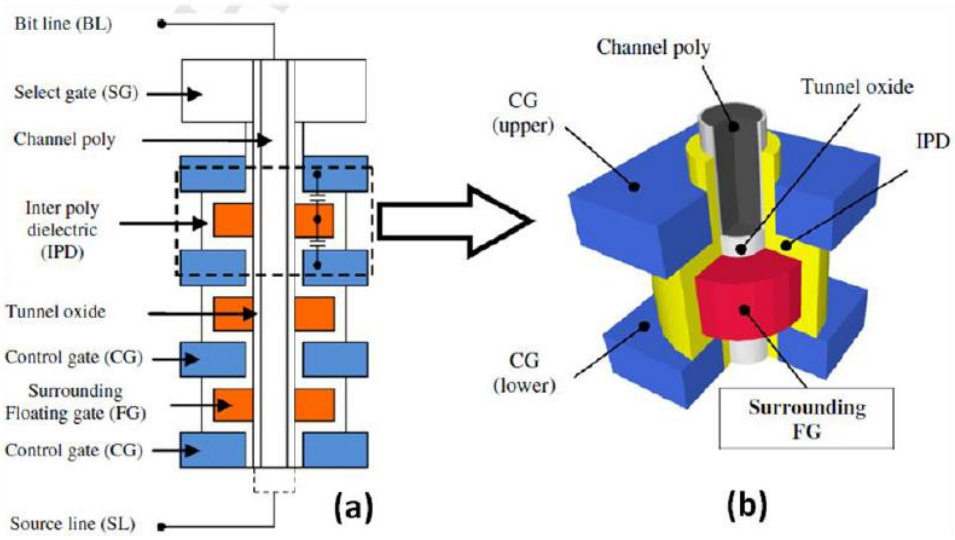

Fig.4.3.1. (a) Cross-sectional schematic and (b) Bird's view of the DC-SF NAND flash cell [4.3.11][4.3.12]. Two control gates (CGs) are vertically capacitive coupled with floating gate (FG). FG is surrounding channel poly-Si with tunnel oxide.

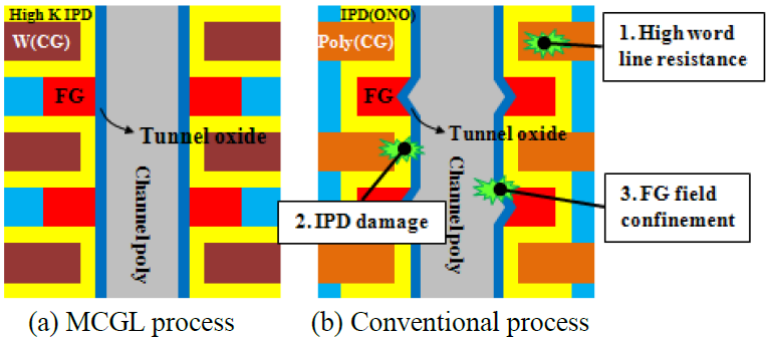

Fig.4.3.2 The DC-SF cell profile comparison, (a) MCGL process, and (b) Conventional process. In (b) conventional process, there are several problems, such as (1) High word line resistance, (2) IPD damage during FG separation process, and (3) FG Field confinement due to the horn shape FG. New MCGL process can solve all of these problems.

4.3.2 MCGL process

The new MCGL process sequence of the DC-SF cell is described in Fig. 4.3.3 [4.3.13]. First, the multiple silicon oxide/nitride layers are deposited on N+/p-Si substrate. Next, channel hole is patterned, and FGs are formed at oxide recess portion by isotropic poly etching (Fig.4.3.3(a)). Tunnel oxide is deposited, and channel contact

hole is formed by etching through N+ layers to connect substrate and channel poly-Si directly (Fig.4.3.3(b)). After channel poly-Si deposition, gates are patterned (Fig.4.3.3(c)). Then stacked silicon nitride has recessed (Fig.4.3.3(d)), and high-k IPD films are deposited on the FGs. After that, tungsten (W) film is deposited and separated to each stacked layers, as shown in Fig.4.3.3(e). Fig.4.3.4 shows the cross sectional TEM image of the DC-SF cell arrays, fabricated by the MCGL process.

In this MCGL process, 1) low word line resistance can be obtained by gate replacement process (SiN→W). And 2) IPD damage of FG separation process can be avoided due to IPD deposited after FG/channel-poly formation, in contrast with conventional process of ONO IPD before FG separation[4.3.11][4.3.12]. And also, 3) FG field confinement at FG edge during programming can be suppressed due to better FG shape by no IPD deposition before FG formation, as shown in Fig.4.3.4(b).

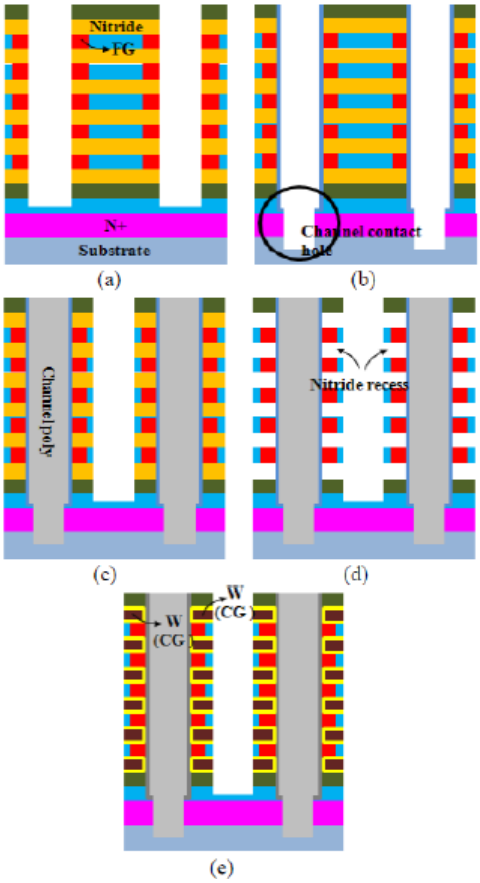

Fig.4.3.3 MCGL process sequence of the DC-SF NAND flash cell. (a) FG formation, (b) channel contact formation, (c) gate patterning, (d) nitride recess, (e) high-k IPD deposition and W (CG) formation.

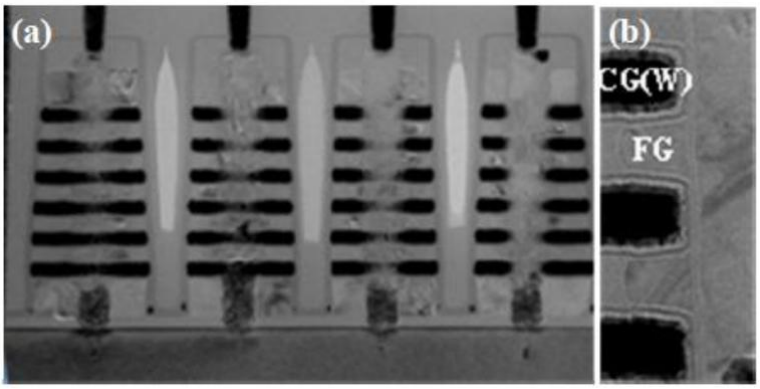

Fig.4.3.4 TEM image of (a) MCGL process DC-SF cell array and (b) the FG/CG shape. The cell structure is showing a preferable vertical FG shape.

4.3.3 New Read Scheme

Conventional read operation of the DC-SF NAND flash string is to apply the read voltage V_R to two neighbor CGs of the selected FG, while $V_{pass\text{-}read}$ is applied to unselected CGs [4.3.11][4.3.12]. In order to investigate read operation issues in conventional read, the FG1 stored charge dependence has been investigated in several read conditions by TCAD simulation [4.3.14], as shown in Fig.4.3.5.

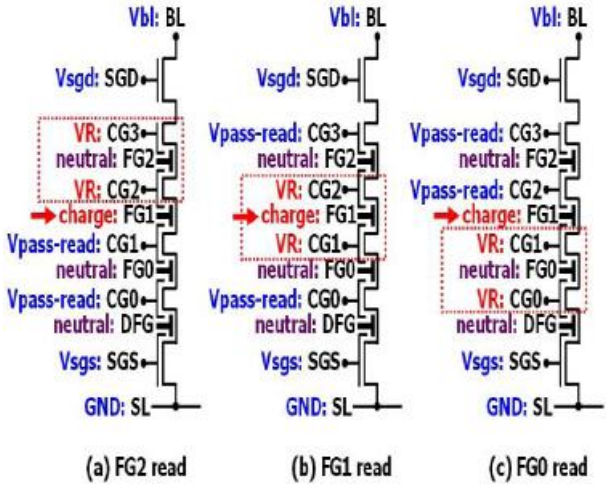

Fig.4.3.5 Conventional read operations, (a) FG2 read operation (CG2&3 VR), (b) FG1 read operation (CG1&2 VR), and (c) FG0 read operation (CG0&1 VR). Charges in FG1 is set to be various amount to derive the FG charge dependence.

Two unexpected characteristics are observed, as shown in Fig.4.3.6. One is that selected cell Vt (FG0 and FG2 read) have shifted up when neighbor FG1 charge is negatively increased. This is because a transconductance is degraded due to increasing channel resistance under FG1, which stored negative charges, as shown in Fig.4.3.7. The selected cell Vt (FG0 or FG2) cannot be read correctly when FG1 is negatively charged (>-5x10^{-15}C/um).

The other is that selected cell Vt (FG1 read) saturates when selected FG1 charge is positively increased (erase saturation phenomena). This is because CG Vt limits the selected cell Vt, as shown in Fig.4.3.8. Two neighbors CG1 and CG2 make the channel "off" directly, even when FG1 is positively charged.

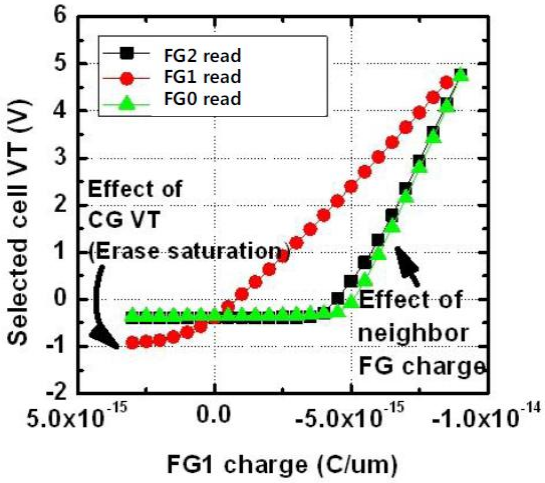

Fig.4.3.6 Simulated selected cell Vt of FG0, FG1, and FG2 read under various FG1 charges, as shown in Fig.5.

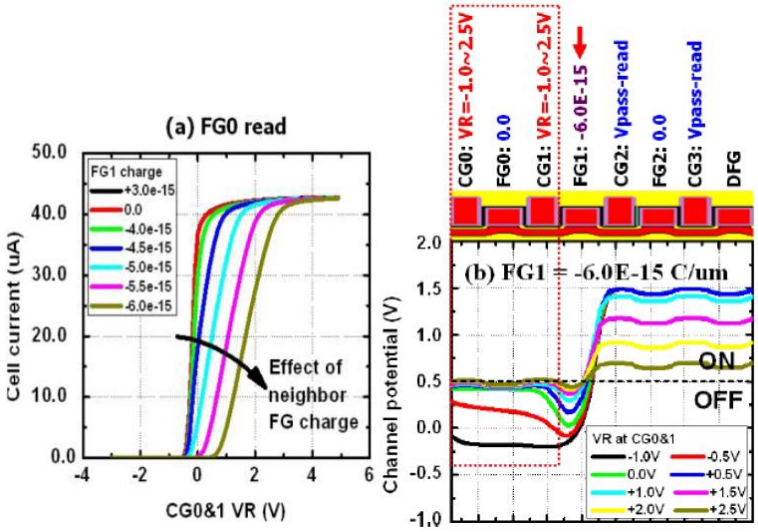

Fig.4.3.7 (a) Cell Id-Vg of FG0 read under various FG1 charge, (b)Channel potenatial at FG1=-6.0E-15 C/um. When FG1 has negative charge, the transconductance is degraded due to increasing channel resistance under FG1.

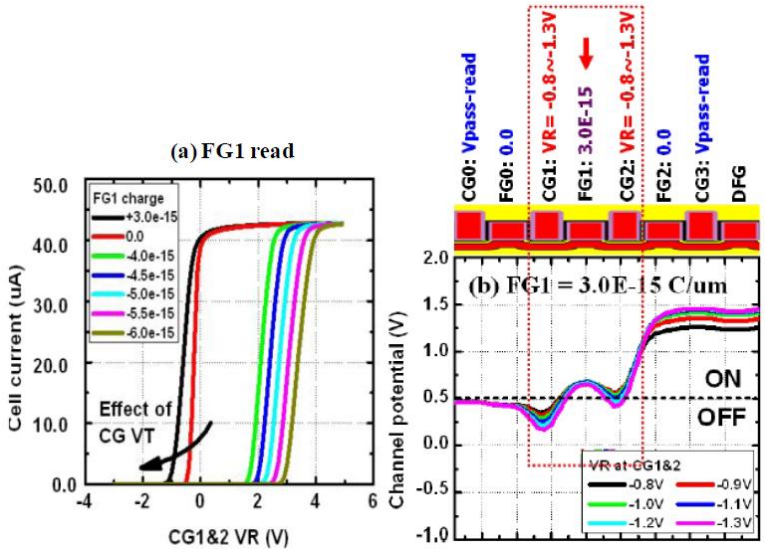

Fig.4.3.8 (a) Cell Id-Vg of FG1 read under various FG1 charge, (b)Channel potenatial at FG1=3.0E-15 C/um. The erase Vt saturation is caused by channel off state under CG1 and CG2.

In order to derive a proper read operation, a simple capacitor network model is used, as shown in Fig.4.3.9 [4.3.14].

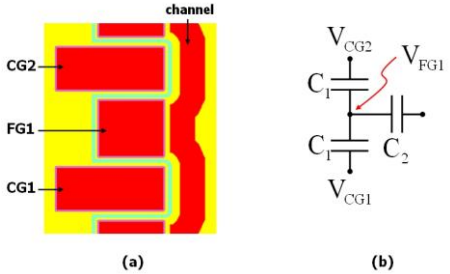

Fig.4.3.9 (a) Cross sectional view of DC-SF NAND unit cell. (b) Corresponding equivalent capacitor network.

Analytic expression of the FG1 potential is derived in (1). V_{FG1} is determined by the average bias of two neighbor CGs (V_{CG1} and V_{CG2}), stored charge (σ_{FG1}) in FG1 and the coupling ratio α as written in (2).

$$V_{FG1} = \alpha\left(\frac{V_{CG1}+V_{CG2}}{2} - V_{T,FG1}\right) \qquad (1)$$

$$\alpha = \frac{2C_1}{2C_1 + C_2} \qquad (2)$$

$$V_{T,FG1} = -\frac{\sigma_{FG1}}{2C_1} \qquad (3)$$

The FG1 potential V_{FG1} during FG0 read operation can be described as (4) by substituting V_{CG1} and V_{CG2} with V_R and $V_{pass\text{-}read,}$ respectively.

$$V_{FG1} = \alpha\left(\frac{V_R + V_{Pass\text{-}read}}{2} - V_{T,FG1}\right) \qquad (4)$$

Because V_R is pre-determined value for cell read operation, the potential decrease of the FG1 due to stored negative charge ($\Delta V_{T,FG1} = -\sigma_{FG1}/2C_1$) have to be compensated by increasing $V_{pass\text{-}read}$ to keep FG1 cell "ON" as pass transistor. Therefore, increasing $\Delta V_{pass\text{-}read}$ is determined quantitatively as written in (5). σ_{FG1_max} is the allowed maximum negative charge (allowed highest Vt).

$$\Delta V_{pass\text{-}read} = 2\,\Delta V_{T,FG1} = -\frac{\sigma_{FG1\text{-}max}}{C_1} \qquad (5)$$

The equation (5) had confirmed by $V_{pass\text{-}read}$ dependence in various FG1 charges (various $V_{T,FG1}$), as shown in Fig.4.3.10. V_{pass_read2} have to increase 4V to compensate a 2V Vt increase of neighbor FG1 cell. This is well corresponding to eq.(5).

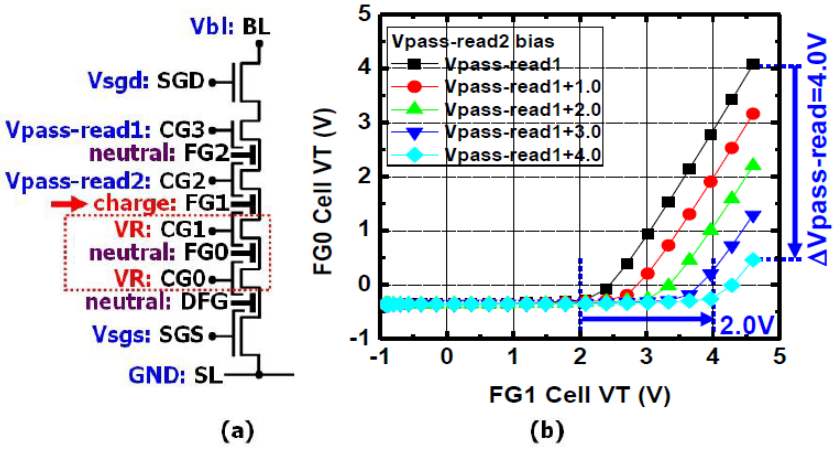

Fig.4.3.10 (a) FG0 read operation. (b) FG0 Cell Vt under several $V_{pass\text{-}read2}$ conditions. $V_{pass\text{-}read1}$ = 5.0V.

Most of NAND devices are currently adopting multi level cell (MLC) operation, which is using three read voltages (V_Rs) to identify each program levels, as shown in Fig.4.3.11. For each V_R for PV1,2,3 read, $V_{pass\text{-}read2}$ and $V_{pass\text{-}read1}$ (see Fig.4.3.10(a)) should be different voltages to compensate neighbor FG1 potential.

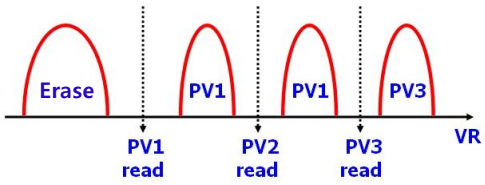

Fig.4.3.11 Multi level cell (MLC) read operation

$V_{pass\text{-}read2}$ compensates V_R change and σ_{FG1_max}, as described in eq. (6), which is derived as same as equation (5).

$$\Delta V_{pass\text{-}read2} = -\Delta V_R - \frac{\sigma_{FG\text{-}max}}{C_1} \qquad (6)$$

And also, in order to maintain that all unselected FG cells are "ON" even if cells are in high Vt (PV3) as worst case, $V_{pass\text{-}read1}$ has to be equal to V_R (eq. (7)). This is because $V_R+V_{pass\text{-}read2}$ for FG1 should be equal to $V_{pass\text{-}read2}+V_{pass\text{-}read1}$ for FG2 (see Fig.4.3.10 (a)).

$$V_{pass\text{-}read1} = V_R \qquad (7)$$

Fig.4.3.12 shows new read condition of MLC DC-SF NAND, which is from equation (6) and (7). $V_{pass\text{-}read2}$ has to be decreased as V_R is increased, conversely, $V_{pass\text{-}read1}$ has to be increased as V_R is increased. And in region of V_R =0~1V, $V_{pass\text{-}read1}$ is used fixed voltage of 1.0V, because CG voltage has to make channel "ON", as described in Fig.4.3.8. The new multi level read operation condition is summarized in Table 1.

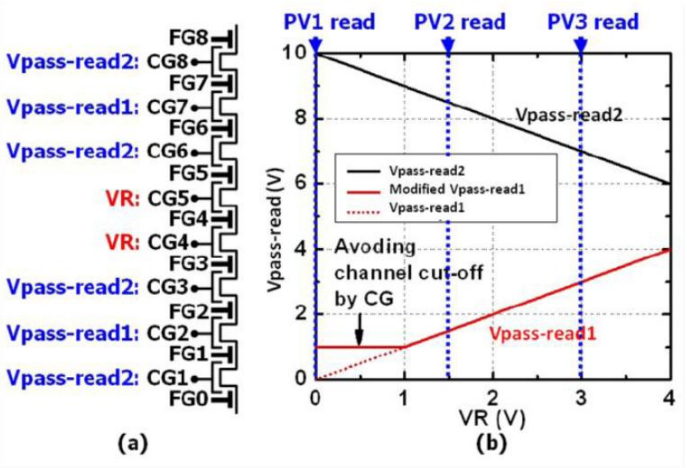

Fig.4.3.12 (a) New read operation of DC-SF NAND string. (b) Vpass_read1&2 dependence on V_R, as equation (6) and (7).

TABLE I. THE NEW READ SCHEME OF DC-SF NAND STRING

Electrode		PV1 read V_R =0.0V	PV2 read V_R =1.5V	PV3 read V_R = 3.0V
CG8	$V_{pass\text{-}read2}$	10.0 V	8.5 V	7.0 V
CG7	$V_{pass\text{-}read1}$	1.0 V	1.5 V	3.0 V
CG6	$V_{pass\text{-}read2}$	10.0 V	8.5 V	7.0 V
CG5	V_R	0.0 V	1.5V	3.0V
CG4				
CG3	$V_{pass\text{-}read2}$	10.0 V	8.5 V	7.0 V
CG2	$V_{pass\text{-}read1}$	1.0 V	1.5 V	3.0 V
CG1	$V_{pass\text{-}read2}$	10.0 V	8.5 V	7.0 V

4.3.4 New Programming Scheme

The programming scheme of DC-SF cell has to be optimized to avoid program disturb problems. Fig.4.3.13 describes program disturb modes (Inhibit modes) of DC-SF cell. There are two inhibit modes, mode (A) ; Electron injection mode, and mode (B) ; charge loss mode. The mode (A) is conventional program inhibit mode, which has a weak electron injection stress, caused by high field in tunnel oxide due to FG coupled with two CGs (ex. V_{pass_n+2} and V_{pgm_n+1}). The mode (A) becomes severe in case of the lower Vt (ex. Erase state) due to high field of tunnel oxide. On the other hand, the mode (B) is new charge loss mode as unique in the DC-SF cell. Electrons in FG are ejected to CG by high field in IPD. The mode (B) become severe in case of high cell Vt (ex. PV3 state, such as Vt=4V) and low V_{pass_n-2}. In order to minimize program disturb, V_{pass_n-2} and V_{pass_n+2} have to be optimized.

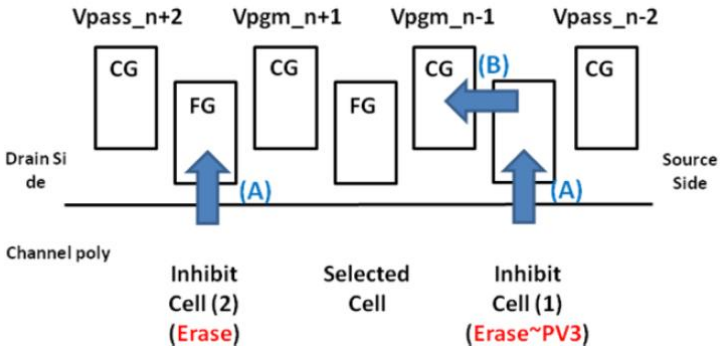

Fig.4.3.13 Two program inhibit modes of DC-SF cell. Mode (A) Electron Injection mode ; weak electron injection from substrate to FG due to high field on tunnel oxide. Mode (B) Charge Loss mode ; Electron emission from FG to CG due to high field on IPD.

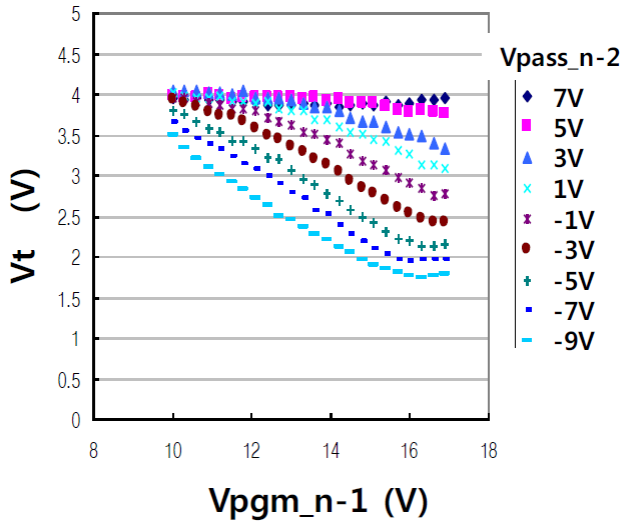

Fig.4.3.14. Measured charge loss of the mode (B) during programming of DC-SF cell. Charge Loss (Electron emission) from FG to CG is increased as increasing Vpgm_n-1 and decreasing Vpass_n-2.

Fig.4.3.14 shows the measurement results of the mode (B), which is accelerated by thin IPD (oxide equivalent 12nm thick). Vt is decreased as V_{pgm_n-1} is increased and as V_{pass_n-2} is decreased. From this data, maximum allowed electric field in IPD is estimated to 8.3 MV/cm from conditions of V_{pgm_n-1}=15V, V_{pass_n-2}=5V, and Vt= 4V.

Fig.4.3.15 shows the potential differences among FG/CG/substrate during programming (V_{pgm}=15V) in case of (a)Vt=-1V and (b)Vt=4V. The potential difference between FG and substrate (Vfg_sub) become large as V_{pass_n-2}, V_{pass_n+2} are increased. In

(a)Vt=-1V, Vfg_sub reaches to the mode (A) limitation (criteria) of 7V at V_{pass_n-2}, V_{pass_n+2} =1V. Then, in (a)Vt=-1V, V_{pass_n-2} and V_{pass_n+2} have to be less than 1V to keep Vfg_sub<7V. And in (b) Vt=4V, the potential difference between CG and FG (Vcg1_fg) reach to the mode (B) limitation of 12.5V at V_{pass_n-2}=-2V. The limitation is determined by the maximum allowed electric field of 8.3MV/cm in mode (B) in case of IPD thickness=15nm. Then, in (b)Vt=4V, V_{pass_n-2} have to be more than -2V to keep Vcg1_fg<12V. The mode (B) is located only in source side inhibit cell (1) (right-side cell) in Fig.4.3.13. Therefore, V_{pass_n-2} has to be the range of -2V to 1V, and V_{pass_n+2} have to be less than 1V, because drain side inhibit cell (2) is only in the case of low Vt (Erase state).

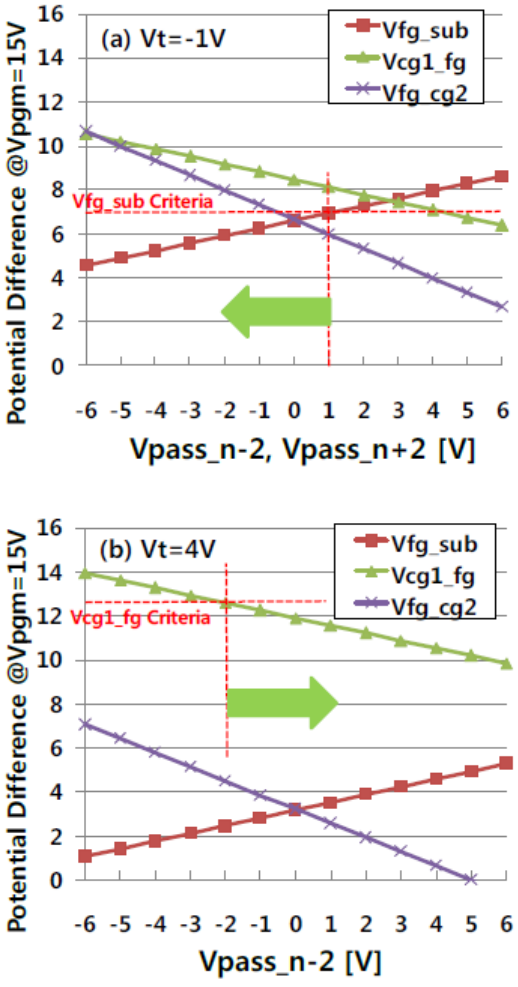

Fig.4.3.15. The potential difference among FG/CG/Substrate during programming in case of (a)Vt=-1V and (b)Vt=4V. In (a) Vt=-1V, maximum Vpass_n-2/Vpass_n+2 is determined to 1V by the criteria of mode (A). And, in (b) Vt=4V, minimum Vpass_n-2/Vpass_n+2 is determined to -2V by the criteria of mode (B).

Figure 4.3.16 shows one example of new ISPP program scheme for the DC-SF cell. V_{pgm}s (V_{pgm_n-1} and V_{pgm_n+1}) are incrementally stepped up (ISPP) of 0.4V step by reaching to 15V. And if more program pulses are needed, V_{pgm_n-1} has step up with 0.8V step and V_{pass_n-2} has step down by -0.8V step in order to prevent mode (A) at inhibit cell (1) in Fig.4.3.13. And V_{pgm_n+1} maintains 15V, then V_{pass_n+2} can be kept positive voltage of 0.5~1.0V to transfer bit-line voltage (0V) for programming cells.

The coupling ratio of DC-SF cell is sensitive with the channel diameters [4.3.12], which are normally large at top-side cells and small at bottom-side cells. Then, the programming voltage and inhibit voltage would need to be optimized as matching with coupling ratio for each cell layers.

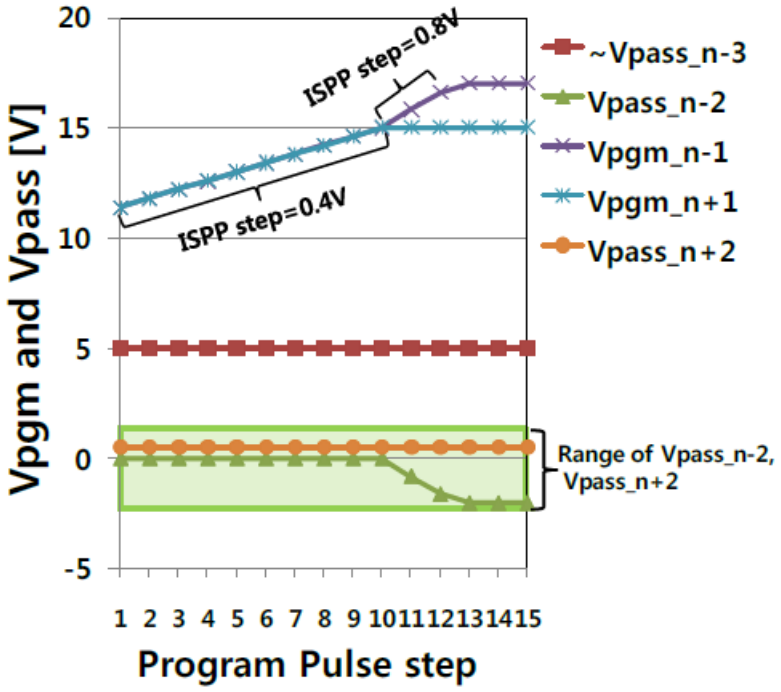

Fig.4.3.16 The proposed program scheme of the DC-SF cell.

Fig.4.3.17 shows the program disturbance of neighbor cell. Almost no Vt shift is observed in neighbor cell because optimized V_{pass} for neighbor cell is used during programming.

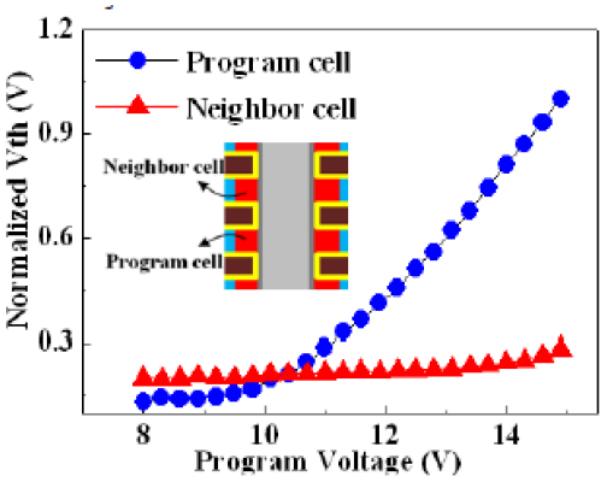

Fig.4.3.17 Program disturbance of neighbor cell. Low Vpass_n-2=1V is used.

4.3.5 Reliability

Program/erase cycling characteristics are shown in Fig.4.3.18. Vth shift after cycling is small, less than 1.3V even after 1k cycles. Data retention characteristic is also evaluated. PV3 Vth shift of 60mV after 250°C 120 min is small, which is comparable with conventional planar FG NAND flash characteristics. Therefore, we have not observed any serious process damages on tunnel oxide and IPD of DC-SF cell by optimizing MCGL process.

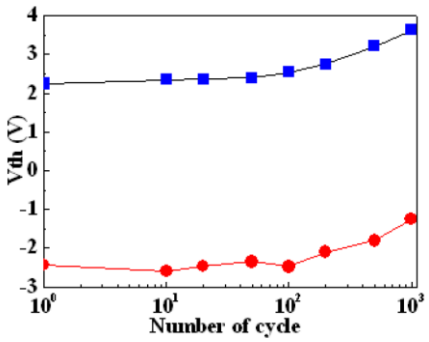

Fig.4.3.18. Program/erase endurance characteristics of DC-SF cell.

4.3.6 Summary

An advanced DC-SF cell technology has been successfully developed for 3D NAND flash memory. Low resistance word line, low damage on tunnel/IPD, and preferable FG shape can be realized by new Metal Control Gate Last process (MCGL

process). And new read and program operation schemes are proposed to prevent disturb problems. As a result, high performance and high reliability can be achieved. Therefore, the DC-SF cell with new MCGL process integration scheme becomes a promising candidate for MLC/TLC 3DNAND Flash memories.

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4.4 Summary of chapter 4

This chapter describes novel three-dimensional (3D) Dual Control gate with

Surrounding Floating gate (DC-SF) NAND Flash memory cell.

In chapter 4.2, 3D DC-SF NAND flash cell had been proposed. The DC-SF cell consists of a surrounding floating gate with stacked dual control gates. With this structure, high coupling ratio, low voltage cell operation, and wide Program/Erase window (9.2 V) can be obtained. Moreover, negligible FG-FG coupling interference (12 mV/V) is achieved due to the control-gate shield effect. As a result, the DC-SF NAND flash cell can overcome the problems of SONOS-based 3D NAND flash.

In chapter 4.3, an advanced DC-SF (Dual Control gate with Surrounding Floating gate) cell process and operation schemes had been discussed. In order to improve performance and reliability of DC-SF cell, new Metal Control Gate Last (MCGL) process has been developed. The MCGL process can realize a low resistive tungsten (W) metal word-line, a low damage on tunnel oxide/IPD (Inter-Poly Dielectric), and a preferable FG shape. And also, new read and program operation schemes have been developed. In new read operation, the higher and lower $V_{pass-read}$ are alternately applied to unselected control gates (CGs) to compensate lowering FG potential to be a pass transistor. And in new program scheme, the optimized V_{pass} are applied to neighbor WL of selected WL to prevent program disturb and charge loss through IPD. Thus, by using MCGL process and new read/program schemes, high performance and high reliability of DC-SF cell can be realized for 3D NAND flash memories.

In addition, future prospects of 3D NAND cell are discussed. In order to prospect scaling transition from 2D cell to 3D cell, the effective memory cell size of several 3D NAND cell are calculated based on assumptions of Fig.4.4.1 and Fig.4.4.2 [4.4.1]. In SONOS or TANOS 3D cell, thickness of gate dielectric ONO (tono) is assumed fixed value of 20nm thick. And taper of channel hole of BiCS/TCAT/DC-SF or channel poly of VG-NAND are defined as size different of top and bottom is fixed value of 10nm (D). Minimum width (minW) of hole size of BiCS/TCAT/DC-SF or minimum channel poly-Si space are 20nm. Size of X- and Y-direction of each cells are shown in Fig.4.4.2. Based on this assumption, effective cell size of each types of cells are calculated. Figure 4.4.3 shows scaling trend of effective memory cell size of 3D NAND memory cells. It can be seen that 3D NAND memory cell cannot be effectively scaled down as feature size is scaled down, in comparison with P-FG MLC (Planar FG MLC cell). It means that increasing number of stacked cell is the only way to reduce effective memory cell size in 3D cells.

Figure 4.4.4 shows transition scenario from 2D planar FG NAND cell to 3D NAND cell. The effective cell size of 1Y nm 2D cell is nearly equal to that of 16 stacked 3D

NAND of BiCS or TCAT or DC-SF cell. This means that transition from 2D cell to 3D cell is possible from 1Ynm generation 2D NAND cell if more than 16 stacked cells can be fabricated.

Figure 4.4.5 shows the scaling scenario of NAND flash memory by 2020. 3D NAND cell can be realized extremely small cell size with more than 32 stacked cells. 2 Tera bit NAND Flash can be expected with 128 stacked cell on 2020.

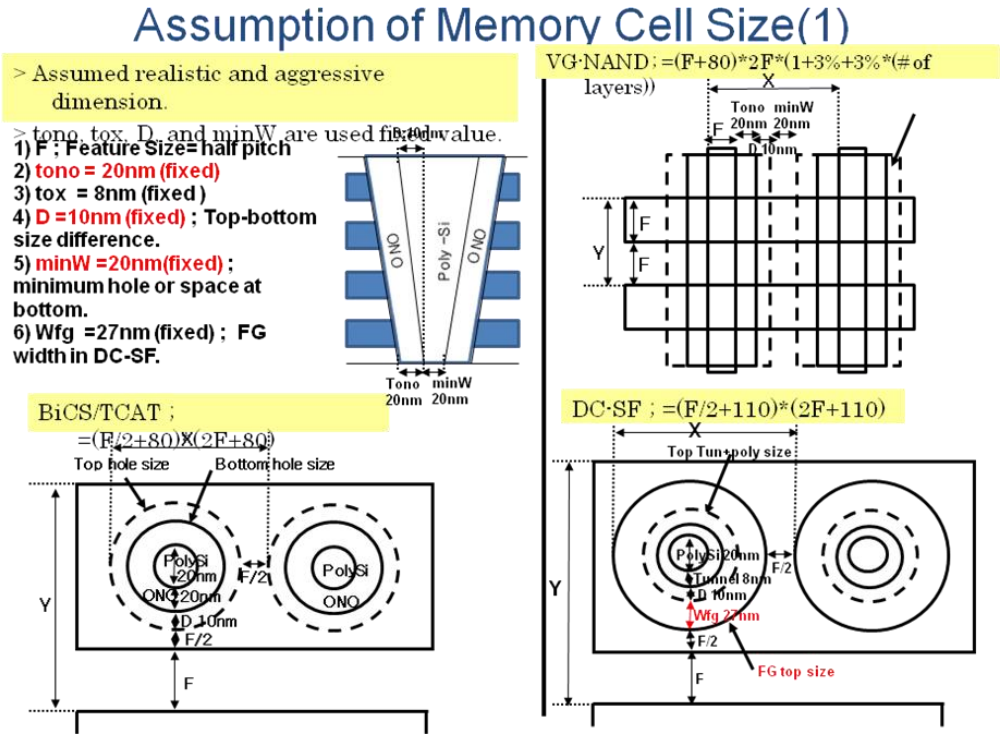

Fig.4.4.1 Assumption of 3D NAND Flash memory cell size calculation (1).

Assumption of Memory Cell Size (2)

	Planar-FG	P-BiCS/TCAT	VG-NAND	DC-SF
Cell Size	1.25*X*Y (=5F2)	X*Y	X*Y*(1+3%+3%*(# of stacked layer))	X*Y
X [BL pith]	2F	F/2+2*tono+2*D+minW	F+2*tono+2*D+minW	F/2+2*tox+2*D+minW+2*Wfg
Y [WL pitch]	2F	2F+2*tono+2*D+minW	2F	2F+2*tox+2*D+minW+2*Wfg
Physical Cell Size [nm2] @F=40nm	8000	16000	9600	24700
Effective Cell Size @F=40nm,16stacked	-------	1000	906	1544 (SLC), 772(MLC)

- 3D memory cell size is strongly limited by tono, D, and minW, which are independent on Feature size, F.

1) F ; Feature Size= half pitch
2) tono = 20nm (fixed)
3) tox = 8nm (fixed)
4) D =10nm (fixed) ; Top-bottom size difference.
5) minW =20nm(fixed) ; minimum hole or space at bottom.
6) Wfg =27nm (fixed) ; FG width in DC-SF.

Fig.4.4.2 Assumption of 3D NAND Flash memory cell size calculation (2).

Scalability of 3D Memory Cell

- BiCS/TCAT/DC-SF cannot be scaled down efficiently with feature size (F) scaling.
- Scalability ;
  Planar-FG
  >> VG-NAND
  > BiCS/TCAT = DC-SF
- 40nm Feature size (ArFi limitation) would be reasonable to use 3D cell, not to increase process cost.

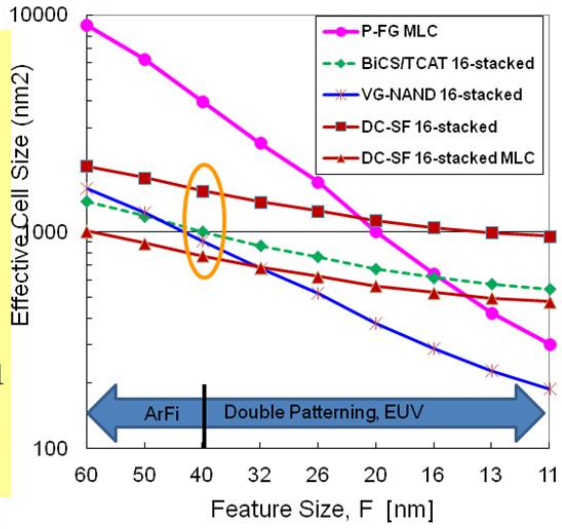

Fig.4.4.3 Scalability of 3D NAND Flash memory cell.

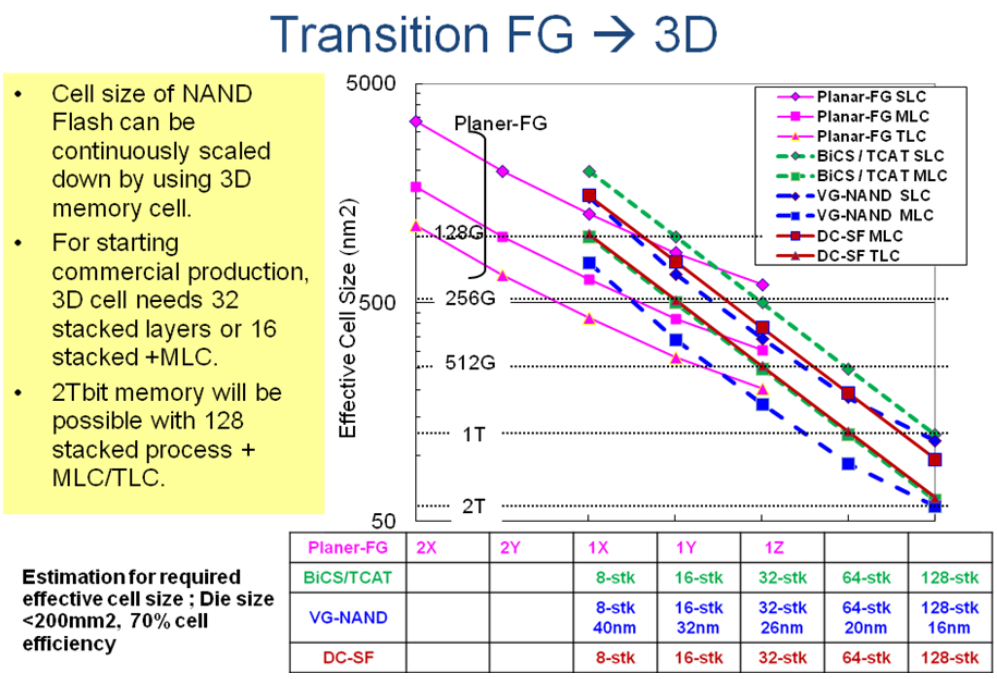

Fig.4.4.4 Transition scenario from planar FG cell to 3D cell.

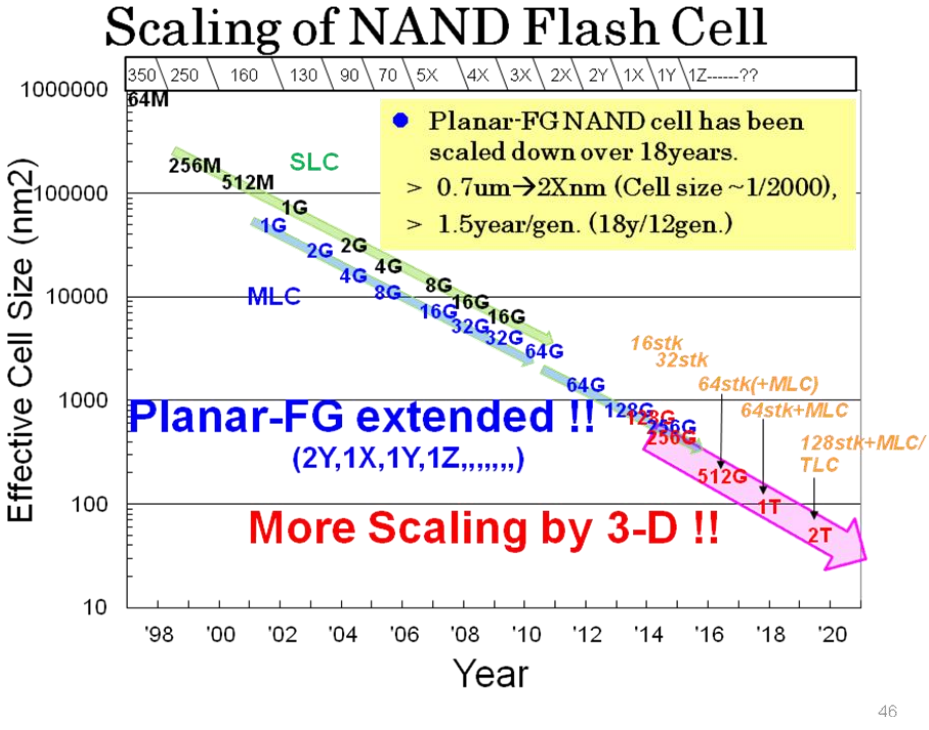

Fig.4.4.5 Scaling trend and future prospect of NAND Flash cell.

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Chapter 5
Reliability of NAND Flash Memory

5.1 Background of Flash Reliability

Reliability of NAND flash memory [5.1.1] is most interesting than that of other semiconductor devices. This is because a very high electric field (>10MV/cm) is applied to tunnel oxide during program and erase operations, in comparison with a low field (<5MV/cm) in other device. Program and erase of NAND flash performs by electron injection and emission to/from Floating Gate (FG). There are several methods of electron injection and emission. For electron injection, there are two methods. One is Channel Hot Electron (CHE) injection. The voltages (5~12V) are applied to drain and Control Gate (CG), as drain current flows. A part of electrons of drain current in channel become hot, and are injected to FG over energy barrier of gate oxide. The CHE can operate the electron injection by relatively low applied voltage (~12V), however large channel electron current is needed to make a required hot electron injection. Then program efficiency (injected electron / drain electron current) is quite low (~10^{-6}). It is difficult to implement parallel programming (page programming). The other electron injection method is Fowler-Nordheim tunneling (FN-t) injection. High voltage (~23V) is applied to CG to inject electrons from channel to FG. The applied voltage is needed to be high (~23V), however program efficiency is high (~1). Therefore, it is possible to program many cells at same time (parallel program or page programming).

For electron emission, there are mainly two methods. One is FN-t emission at source or drain gate overlap area. High voltage (~20V) is applied to source or drain to eject electrons from FG. During FN-t emission at source or drain, large source (or drain) leakage current is caused by band-to-band tunneling (BB-t) mechanism. By BB-t, electron-hole pairs are generated in substrate. A part of holes are accelerated by high field at source (or drain), and are injected to tunnel oxide. Then some holes are trapped in tunnel oxide. These hole traps have degraded Program/Erase cycling and data retention, as described in chapter 5.2. The other electron emission method is FN-t

emission entire channel region (entire tunnel oxide). The BB-t does not occur due to no voltage difference between source (or drain) and substrate.

The possible program and erase methods of flash memory are summarized in Table 5.1.1. Reliability performances are compared between these program and erase methods in chapter 5.2 [5.1.6]-[5.1.7] and 5.3[5.1.5].

Table 5.1.1 Program and erase method of NOR and NAND Flash.

	Electron Injection	Electron Emission
NOR Flash	CHE	FN-t @ S
NOR Flash [5.1.5]	CHE	Uniform FN-t
NAND Flash [5.1.1]	CHE	---
NAND Flash [5.1.2][5.1.3][5.1.8]	Uniform FN-t	FN-t @ D
NAND Flash [5.1.4]-[5.1.8]	Uniform FN-t	Uniform FN-t

CHE; Channel Hot Electron,

FN-t @ S ; FN-t at source,

FN-t @ D ; FN-t at drain,

Uniform FN-t ; FN-t entire channel (tunnel oxide)

It had been reported that high field FN-t during program and erase causes oxide degradation in tunnel oxide. Fig.5.1.1 shows one of the degradation mechanisms [5.1.9] of FN-t. Hot electron injection from cathode (FG) to anode (substrate) makes electron-hole pairs at anode. And a part of hot holes has injected to tunnel oxide and trapped inside tunnel oxide. Electron trap has also occurred in tunnel oxide during FN-t stress. These hole and electron traps have caused oxide degradation in tunnel oxide, and have directly impacts on program/erase cycling endurance characteristics, such as program/erase window narrowing, as described in chapter 5.2 and 5.3.

Data retention is also degraded by electron and hole traps in tunnel oxide, as shown in Fig.5.1.2. Detrapping trapped charges in tunnel oxide is a major roots cause of Vt shift during data retention test, as described in chapter 5.2. And trapped holes would make a stress induced leakage current (SILC) for tunnel oxide, because potential barrier may locally decrease by hole traps. SILC make a tail bits in Vt distribution, as shown in Fig. 5.1.2.

Figure 5.1.3 shows read disturb phenomena. Read disturb failure is mainly caused in erase state after program/erase cycling stress. The stress induced leakage current (SILC), which is generated by program/erase cycling stress, is major root cause, as described in chapter 5.3.

In NAND Flash program and erase operation, a high voltage is applied to CG or substrate. This high program and erase voltage cannot be effectively scaled down as feature size of memory cell is scaled. Therefore, high field stress problem has been caused in memory cells. One of problem is “the negative Vt shift” during programming, as described in chapter 5.4 [5.1.11].

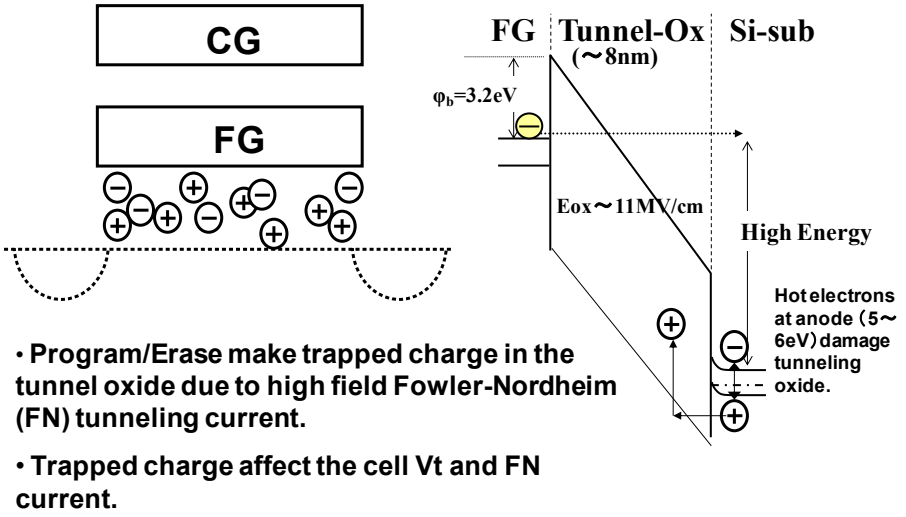

Fig.5.1.1 Reliability degradation by Fowler-Nordheim tunneling stress[5.1.9]

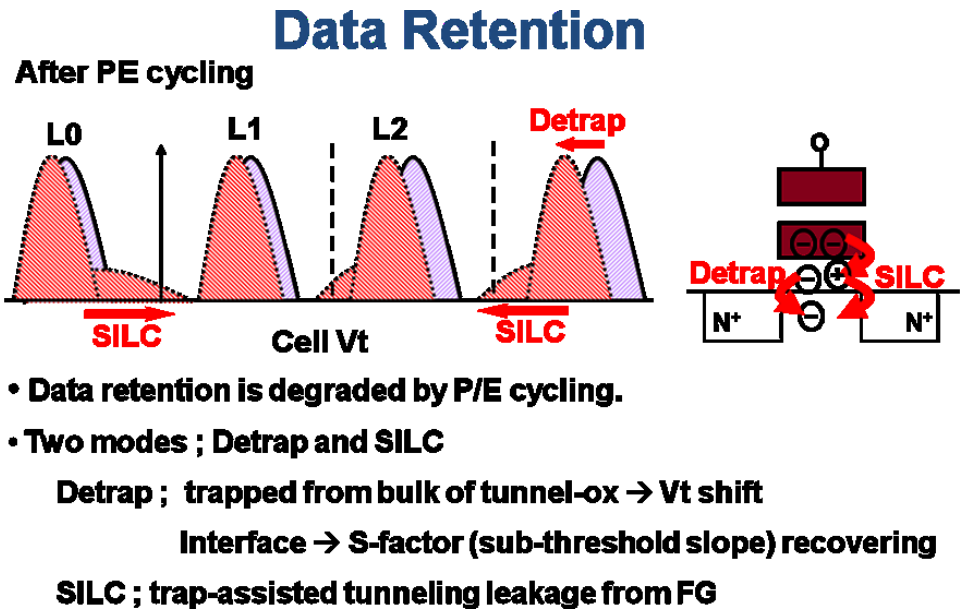

Fig.5.1.2 Data Retention phenomena

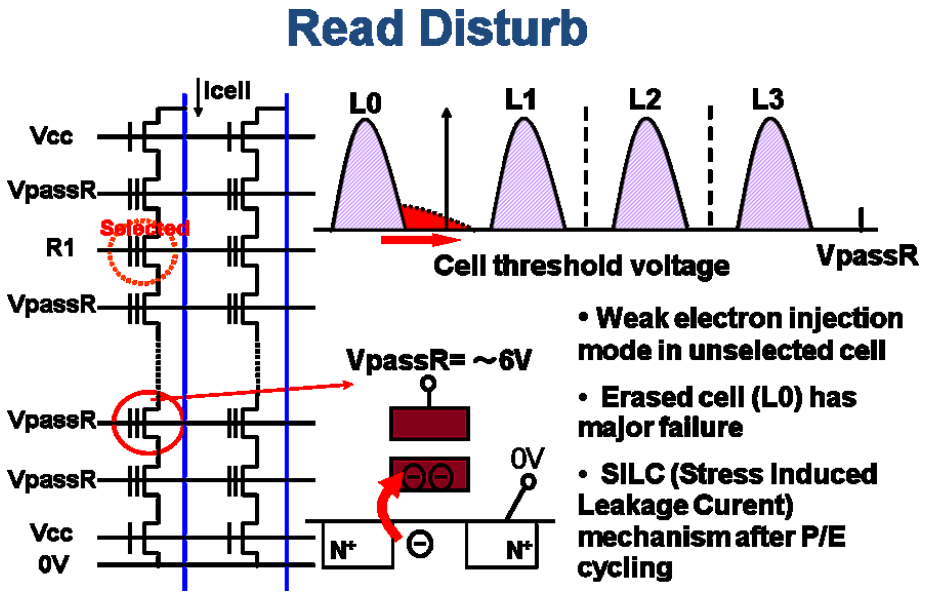

Fig.5.1.3 Read Disturb

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5.2 Program/Erase cycling and Data Retention

Abstract ; The data retention characteristics of a Flash memory cell have been drastically improved by applying a bi-polarity write and erase technology which uses uniform Fowler-Nordheim tunneling over the whole channel area both during write

(program) and erase. It is clarified experimentally that the detrapping of electrons from the gate oxide to the substrate results in an extended retention time of erase state. A bi-polarity write and erase technology also guarantees a wide cell threshold voltage window even after 1 million write/erase cycles. This technology results in a highly reliable flash memory with an extended data retention time.

5.2.1 Introduction

The write/erase endurance and the data retention are key characteristics of floating gate memories such as EEPROMs and Flash EEPROMs (Electrically Erasable and Programmable Read Only Memories) [5.2.1]-[5.2.13]. An essential requirement for the memory cell is sufficient data retention even after a large number of write/erase cycles. However, the data retention is degraded by the high field stress in the thin oxide during the write and erase operations.

In order to improve the reliability of the Flash memory cell, the degradation mechanisms of the memory cell have been studied [5.2.14]-[5.2.19]. The degradation behavior of the memory cell is related to the charge-trapping process in the thin oxide during both the write and erase operations [5.2.14]-[5.2.19], which are performed by the tunneling of electrons through the thin gate oxide. The generation of traps in the thin gate oxide strongly depends on the write and erase condition that is used [5.2.14], [5.2.16]-[5.2.19].

Therefore, the write/erase endurance and the data retention characteristics of the Flash memory cell have been studied and the results are presented in this chapter [5.2.23]. In chapter 5.2.2, the devices and the experimental technology used in this study will be presented and compared. In chapter 5.2.3, the write/erase endurance characteristics are discussed. In chapter 5.2.4, the data retention characteristics of two different write and erase technologies are compared. Furthermore, the scaling limit of the tunnel oxide thickness is discussed with respect to the data retention. Finally, the conclusions of this study are given in chapter 5.2.5.

5.2.2 Devices and Experiments

The Flash memory cell in this work is a conventional n-channel floating gate transistor with a tunnel oxide over the entire channel region, as shown in Fig. 5.2.1. The key process features are shown in Table 1. The thin gate oxide of 5.6-12.1nm is thermally grown at 800C. The effective oxide thickness of the oxide-nitride-oxide

(ONO) inter-poly dielectric is 25 nm [5.2.20].

The endurance and data retention characteristics of the Flash memory cell programmed by two different write and erase technologies are compared [5.2.16], [5.2.18]. One is a uniform write and uniform erase technology (Fig.5.2.1), using uniform Fowler-Nordheim tunneling over the whole channel area both during the write and erase operation. The other is a uniform write and non-uniform erase technology (Fig. 5.2.2), using uniform tunneling over the whole channel area during the write operation (Fig.5.2.2(a)) and local non-uniform tunneling at the drain during the erase operation (Fig.5.2.2(b)). A uniform write and non-uniform erase technology can also be applied to NOR-type cells, such as the DINOR cell [5.2.10] and the Hi-CR cell [5.2.12]. However, a uniform write and uniform erase technology can only be applied to NAND-type cells because it is not possible to apply a selective write operation in a NOR-type cell.

The programming voltages (Vpp) are determined by the voltage when the threshold voltage reaches a value of 2.5V after a write operation after ten cycles, and -3.0 V after an erase operation after ten cycles, as shown in Table 2. The programming time is fixed at 1 msec. This method of Vpp determination is suitable for the comparison of these two technologies, because an initial window widening during the first 10 write/erase cycles occurs in the uniform write and non-uniform erase technology, as will be shown in the next section. The threshold voltage of the Flash memory cell is measured with a drain voltage of 1 V. The charge trapping in the tunnel oxide can be studied by measuring test devices in which the floating gates are connected with the control gates. The accelerated data retention tests were done at a temperature of 150-300C after different numbers of write/ erase cycles from 10 to 1 million had been applied to the devices.

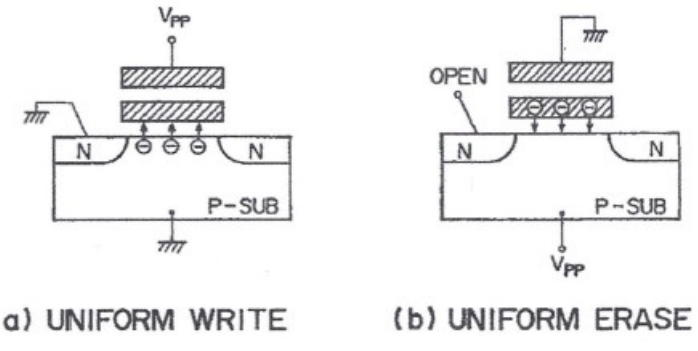
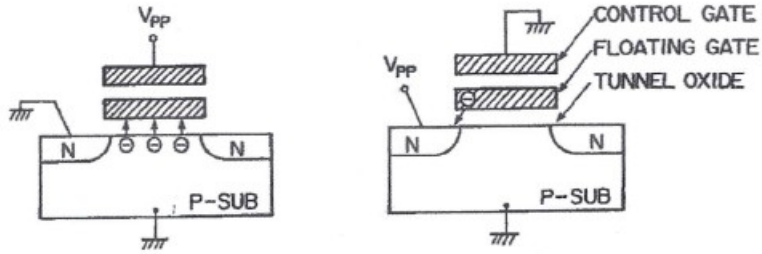


Fig.5.2.1 Operation of the uniform write and uniform erase technology. (a) uniform write; A positive high voltage is applied to control gate with the drain and substrate grounded. Electrons are injected to the floating gate over the whole channel area. (b) uniform erase; A positive high voltage is applied to the substrate with the control gate

grounded. Electrons in the floating gate are emitted uniformly over the whole channel area.



(a) UNIFORM WRITE (b) NON-UNIFORM ERASE

Fig.5.2.2 Operation of the uniform write and non-uniform erase technology. (a) uniform write; A positive high voltage is applied to the control gate with drain and substrate grounded. (b) non-uniform erase ; A positive high voltage is applied to the drain with the control gate grounded.

Table 1 Device fabrication.

GATE OXIDE	
THICKNESS	5.6-12.1 nm
INTERPOLY	
INSULATOR(ONO) THICKNESS	25 nm
GATE LENGTH	1.0 um

Table 2 Write/erase voltage (V_{pp}). t_p=1 msec.

	uniform write and uniform erase technology		uniform write and non-uniform erase technology	
	WRITE	ERASE	WRITE	ERASE
5.6nm	15.0	17.7	14.7	17.9
7.5nm	17.0	19.8	15.7	18.5
9.7nm	19.4	22.5	15.8	21.0
12.1nm	22.0	25.0	17.0	23.8

5.2.3 Write and Erase Endurance

The write/erase endurance characteristics of the two different technologies are shown in Fig.5.2.3. The uniform write and uniform erase technology guarantees a wide cell threshold voltage window of as large as 4 V, even after 1 million write and erase cycles (Fig.5.2.3 (a)). However, the threshold window obtained by the uniform write and non-uniform erase technology begins to close rapidly after around 100 write and erase cycles, and fails after 100K write and erase cycles (Fig.5.2.3 (b)).

In the case of the uniform write and non-uniform erase technology, holes are generated near the drain of the memory cell by band-to-band tunneling due to the presence of a high voltage over drain junction during the erase. A small part of these holes is injected into the thin gate oxide after being accelerated in the depletion region. The injection of hot holes results in hole trapping in gate oxide near the drain. As a result, field enhancement occurs resulting in an initial threshold window widening, which is observed in the first 10 write/ erase cycles. During the first cycle, the threshold window is small (about 1.5V), because field enhancement has not yet occurred. After a few cycles, holes are trapped locally in gate oxide near the drain, and the Fowler-Nordheim tunneling during both the non-uniform erase and the uniform write could be confined to a small region near the drain. Therefore, the electron trapping in the gate oxide near the drain area is enhanced, subsequently, these trapped electrons impede the tunneling of electrons between the floating gate and the substrate. As a result, window narrowing rapidly occurs.

On the other hand, in the uniform write and uniform erase technology, the write and erase operation is performed without hot-hole generation by band-to-band tunneling mechanism, therefore, the initial window widening does not occur.

In the uniform write and uniform erase technology, the threshold voltage of the erased cell is dependent on the number of write/erase cycles. However, the threshold of the written cell is not dependent on the number of write/erase cycles. This can be explained as follows. The oxide traps and interface traps are generated uniformly over the entire channel area because the Fowler-Nordheim tunneling of electrons is performed uniformly during both the write and erase operations. The uniformly trapped oxide charges over the channel area affect not only the electron tunneling current through the oxide, but also the flat-band voltage. The threshold voltage of the erased cell decreases slightly up to 1K cycles (Fig.5.2.3(a)) due to the trapping of holes generated in the oxide during the Fowler-Nordheim tunneling. The trapped holes result in an increased tunnel current as well as an decrease of the flat-band voltage. After about 1K cycles, the threshold voltage of the erased cell increases due to electron trapping. On the other hand, the threshold voltage of the written cell remains almost constant up to 1 million cycles in spite of the negative charge trapping in the oxide. The trapped oxide charge reduces the electric field during a write operation resulting in less charge stored in the floating gate and therefore a lower threshold voltage. However, this lower threshold voltage is compensated by an increased flat-band voltage due to the trapped negative charge [5.2.16].

The influence of the trapped oxide charges on the flat-band voltage is confirmed by measuring the flat-band voltage shift during simulated write and erase stress cycles of the test devices in which the floating gates are connected with the control gates, as shown in Fig.5.2.4. Using the uniform write and uniform erase technology, the threshold voltage shift is negative at the beginning but becomes positive with an increasing number of stress cycles, because hole trapping mainly occurs up to the first 1K cycles while electron trapping becomes dominant after l K cycles.

Figure 5.2.5 shows the dependence of the endurance characteristics on the tunnel oxide thickness. In the case of the uniform write and uniform erase technology, the window narrowing of the thicker tunnel oxides is larger than that of the thinner oxides. The window widening around one thousand write and erase cycles is also larger in thicker tunnel oxides, as compared with the thinner oxides. The increased hole trapping is caused by an increased hole generation in thicker oxides. Consequently, since holes are involved in the generation of traps, the electron trapping will also be enhanced for thicker oxides. In the case of the uniform write and non-uniform erase technology, the window widening and narrowing is almost independent of the oxide thickness over the 7.5-12.1 nm thickness range. However, for a 5.6 nm oxide thickness, the window narrowing is strongly reduced for both write/erase technologies. However, the

breakdown of the 5.6 nm oxide occurs very early, before 1 million cycles, in the uniform write and non-uniform erase case.

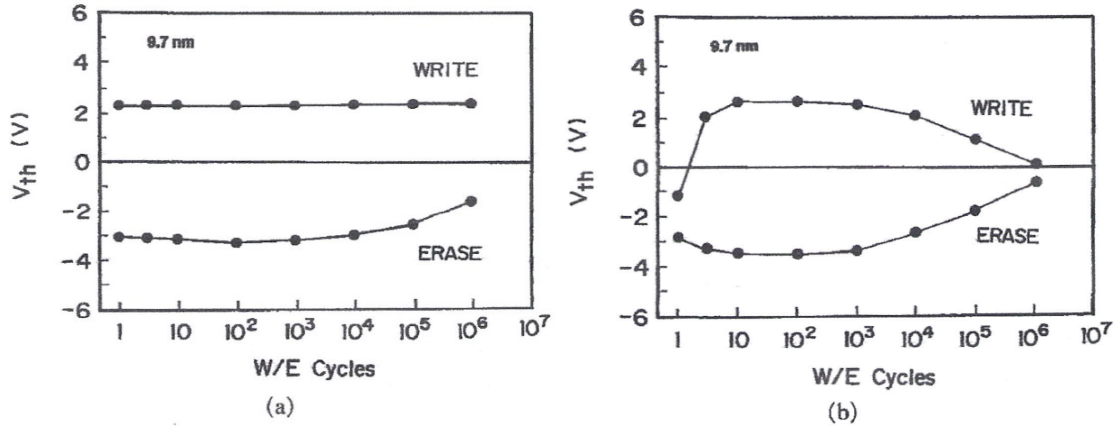


Fig.5.2.3 Write/Erase Endurance characteristics, (a) uniform write and uniform erase technology, using uniform injection and uniform emission over the whole channel area. (b) uniform write and non-uniform erase technology, using uniform injection over the whole channel area and local non-uniform emission at the drain, respectively.

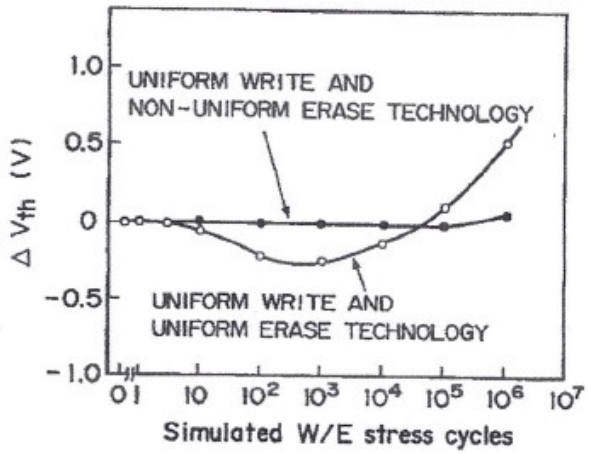


Fig.5.2.4 Threshold voltage shift of the test device in which the floating gate is connected with the control gate, during simulated write and erase stress. Simulated write/erase stress condition: In the case of uniform write and uniform erase technology, high voltage pulses of 12.0V, 0.1 msec and 13.5V, 0.1 msec are applied to the gate and substrate, respectively. In the case of the uniform write and non-uniform erase technology, high voltage pulse of 10.4V, 0.1 msec and 13.0V, 0.1 msec are applied to the gate and drain, respectively. In the uniform write and uniform erase technology, trapped oxide charges are directly affecting the threshold voltage. However, in uniform write and non-uniform erase technology, trapped oxide charges are not

directly affecting the threshold voltage.

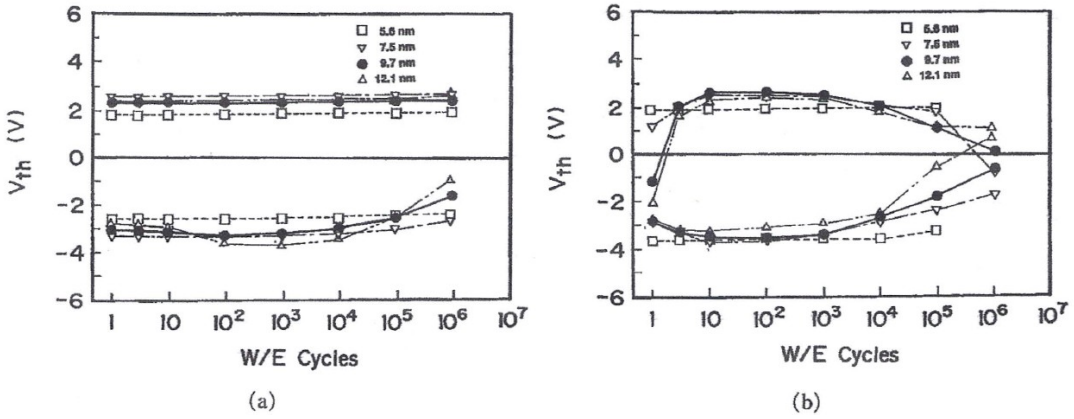


Fig.5.2.5 Dependence of the write/erase endurance characteristics on the tunnel oxide thickness. (a) uniform write and uniform erase technology. (b) uniform write and non-uniform erase technology.

5.2.4 Data Retention Characteristics

A. Write and Erase Method Dependence

The data retention characteristics were measured in the memory cells which are programmed by the two write/erase technologies at 300°C bake temperature after different numbers of write/erase cycles from 10 to 1 million (Fig.5.2.6). In the case of the uniform write and non-uniform erase technology, the stored positive charge gradually decays as the baking time increases, so the threshold window decreases (Fig.5.2.6(b)). However, in the case of the uniform write and uniform erase technology, the stored positive charge effectively increases up to a 100-minute baking time due to the detrapping of electrons from the gate oxide to the substrate during the retention bake (Fig.5.2.6(a) and Fig.5.2.7) . This increase of the effectively stored positive charge up to the 100-minute retention bake becomes larger with an increasing number of cycles because the amount of trapped negative charge in the thin oxide increases. The effect of detrapping electrons is equivalent to the effect of trapping holes in the gate oxide. As a result, the detrapping of the electrons suppresses the data loss of the positively charged cell because the stored positive charge is effectively increasing at the beginning of the bake. This effect extends the data retention time of the memory cells programmed by the uniform write and uniform erase technology. Figure 5.2.8 shows the data retention time after write and erase cycling. The data retention time can be extended by using the uniform write and uniform erase technology, especially beyond 100K write and erase

cycles.

Figure 5.2.9 shows the data retention characteristics after various W/E (write/erase) cycles of both a written and an erased cell for the uniform write and uniform erase technology. A threshold voltage (Vth) shift in a written cell can be observed after a 20 min bake in a cell subjected to a large number of write/erase cycles. This is also due to the detrapping of electrons from the tunnel oxide, which will be further discussed in the next section.

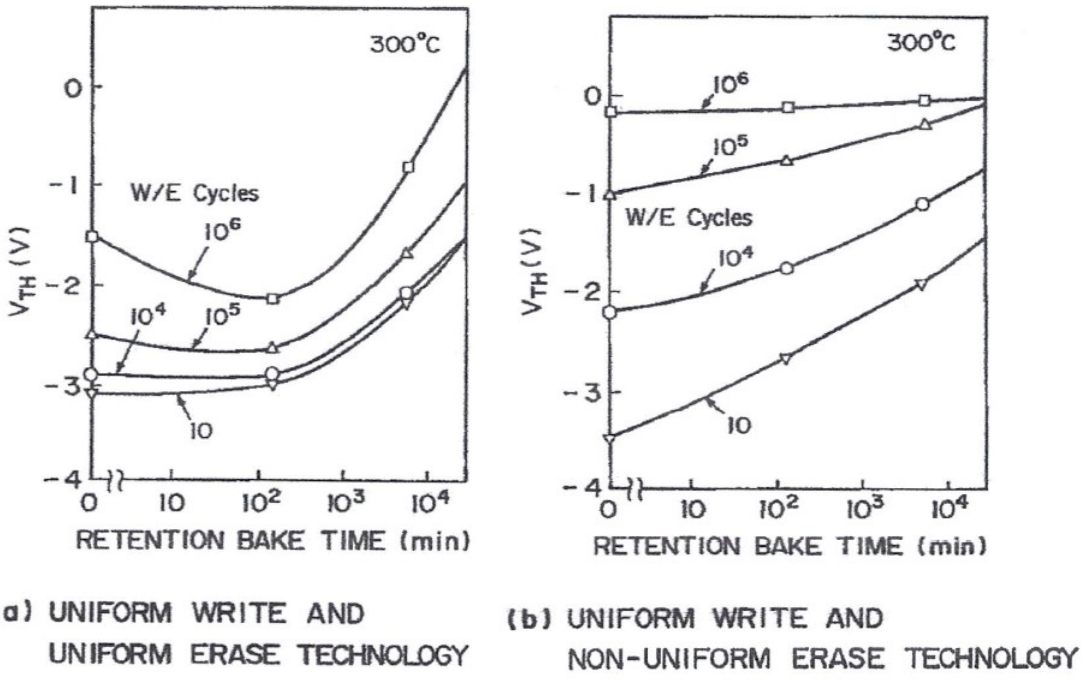


Fig.5.2.6 Data retention characteristics of the erased cell, which stores positive charges in the floating gate，as a function of retention bake time at 300°C in (a) uniform write and uniform erase technology and (b) uniform write and non-uniform erase technology, subjected to 10, 10K, 100K, 1 million Write and Erase cycles (W/*E* cycles).

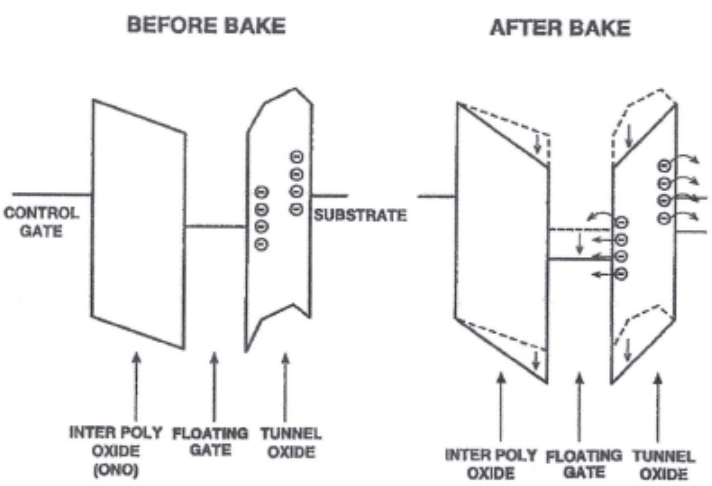


Fig.5.2.7 Band diagram before and after baking. The effect of detrapping electrons from the gate oxide to the substrate is equivalent to the effect of trapping holes in the gate oxide.

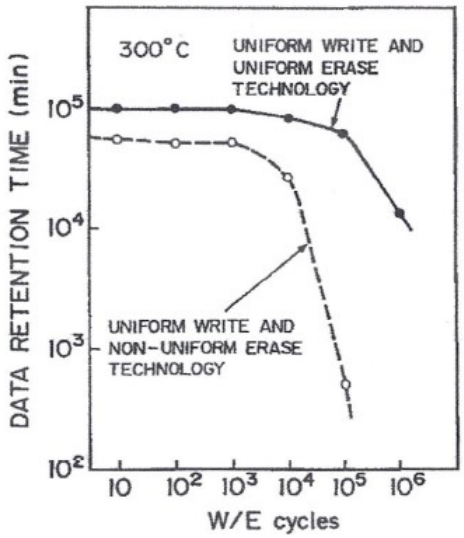


Fig.5.2.8 Data retention time of the erased memory cell after write and erase cycling. The data retention time is defined by the time that the threshold voltage reaches -0.5 V during the retention bake at 300°C.

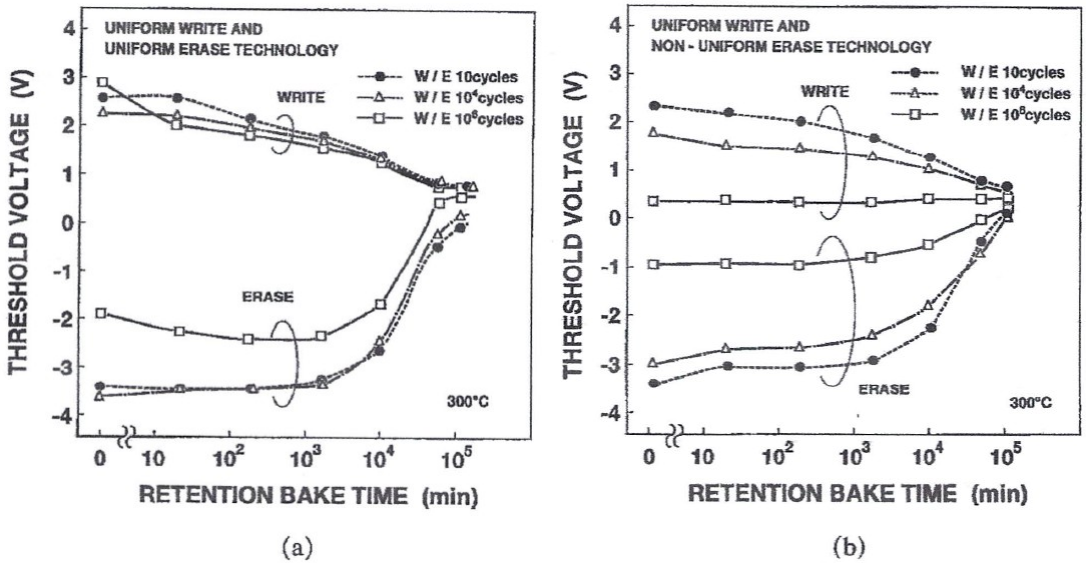


Fig.5.2.9 Data retention characteristics after different write/erase cyc1e. (a) uniform write and uniform erase technology, (b) uniform write and non-uniform erase technology.

B. Temperature Dependence

In order to estimate the data retention life time of the memory cell under the operation temperature (<85°C) in case of the uniform write and uniform erase technology, the data retention characteristics at different temperatures (150-300C) have been measured, as shown in Fig.5.2.10. The memory cells with a 9.7 nm tunnel oxide are subjected to 1 million write/erase cycles. For the written cell, the Vth monotonically shifts negative toward the neutral Vth (0.7 V), as baking time increases. The negative *Vth* shift (Fig.5.2.11 (a)) after 20 min baking increases with the number of write/erase cycles. This is because both the charge loss from the floating gate and the electron detrapping from the tunnel oxide to the substrate are enhanced at high temperatures. For practical applications of the NAND EEPROM, the negative Vth shift of the written cell at 100C is estimated to be less than 0.2V. So the minimum Vth of the written cell should be determined with a margin of 0.2V.

For the erased cell, the phenomenon of the effective increase of the stored positive charge can be observed at all test temperatures from 150-300C. However, the threshold shift depends on the temperature. For a bake of 300°C, the threshold voltage shifts negative until 200 min, after that, the Vth shifts positive toward the neutral Vth (0.7 V). However, for 150-250C baking, the initial Vth-shift is positive (about 0.3 V) after 20 min baking, after that the Vth shift is negative for 1000 min and becomes positive again with Vth shifting towards the neutral Vth. The first positive Vth shift after about 20 min

baking can be explained by the charge loss from the floating gate due to the high-field-stress induced leakage current in the tunnel oxide [5.2.19][5.2.21][5.2.22]. The negative shift of the Vth can be explained by the effect of electron detrapping from the tunnel oxide to the substrate, as shown in chapter 5.2.4 A.

Because of the lower detrapping rate of electrons at lower temperatures, the time at which the minimum Vth is reached during the bake is longer at lower temperature, for example, 1000 min at 250C and 10,000 at 200C. Therefore, at the operation temperature (<100°C), the maximum negative *Vth* shift will occur after more than 1,000,000 min.

Figure 5.2.12 shows the estimation of the data retention time using the temperature dependence of the data retention of the memory cell for different numbers of write/erase cycles. Due to the write/erase cycling, the data retention time is shortened. However, ten years data retention time for an operation temperature of less than 100C can be guaranteed even after 1 million cycles in the case of the uniform write and uniform erase technology.

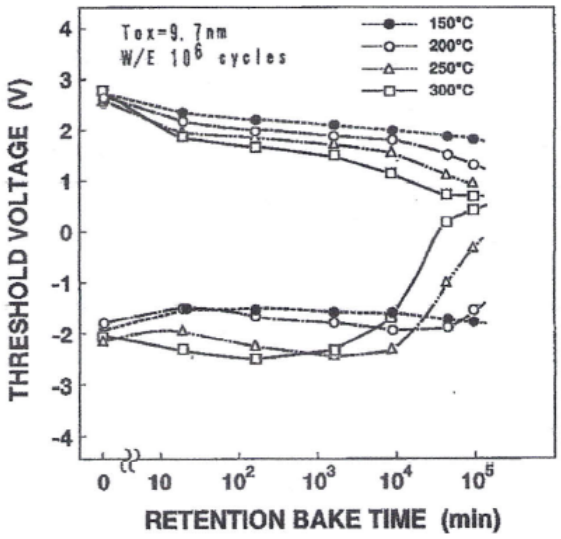


Fig.5.2.10 Dependence of the data retention characteristics on the baking temperature in the uniform write and uniform erase technology.

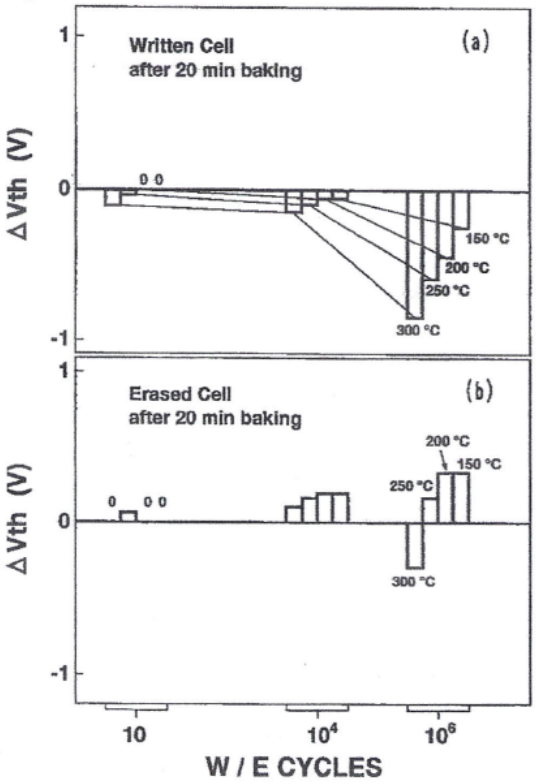


Fig.5.2.11 Threshold voltage shift after a 20 min bake at 150-300C. (a) written ce11, (b) erased cell.

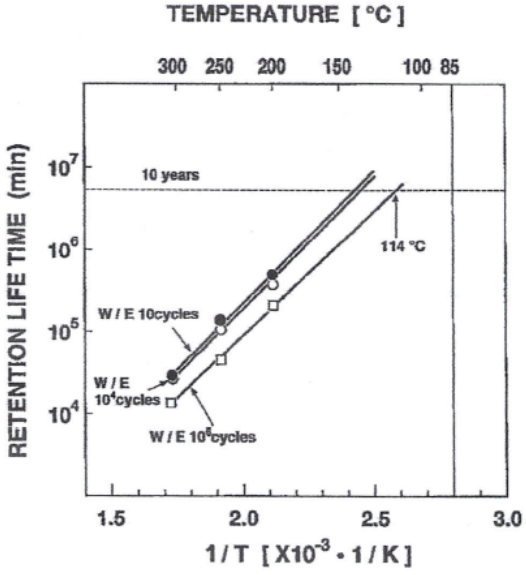


Fig.5.2.12 Estimation of the data retention time at the operation temperature.

C. Tunnel Oxide Thickness Dependence

In order to clarify the scaling limit of the tunnel oxide thickness with respect to the data retention, the data retention characteristics of cells with various tunnel oxide thicknesses have been measured, as shown in Fig.5.2.13. The negative Vth shift of a written cell after a 20 min bake decreases with decreasing oxide thickness, as shown in Fig.5.2.14(a), because the amount of electrons that can detrap is smaller. For an erased cell, the negative Vth shift can be observed in cells having a 7.5-12.1 nm tunnel oxide, however, the negative Vth shift is not observed for cells with a tunnel oxide of 5.6 nm. The Vth shift is positive for those cells. This is because the stress leakage current increases as the tunnel oxide becomes thinner, so in the 5.6 nm tunnel oxide case, the charge loss from the floating gate is larger than the influence of the detrapping of electrons.

Figure 5.2.15 shows the dependence of the data retention time on both the tunnel oxide thickness and the number of write/erase cycles. For the thinner tunnel oxides, the data retention time is shortened in case of 10-10K write/erase cycles, however, in the case of 1 million cycles, the data retention time is extended because of the reduced window narrowing due to the reduced electron detrapping. Therefore, the scaling of the tunnel oxide is not limited by the degradation of the data retention due to the thinning of the tunnel oxide up to a thickness of 5.6 nm.

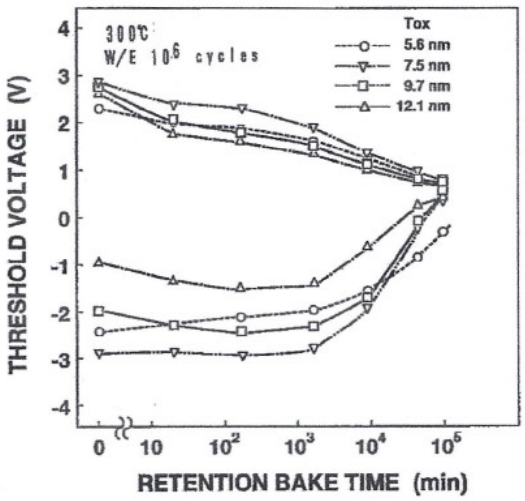


Fig.5.2.13 Dependence of the data retention characteristics on the tunnel oxide thickness in the uniform write and uniform erase technology

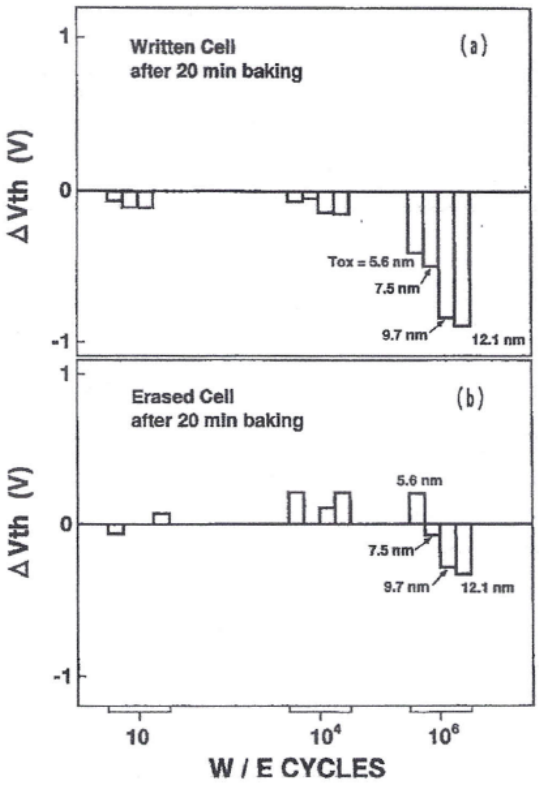


Fig.5.2.14 Threshold voltage shift after a 20 min bake at 300C. The memory cell has a 5.6-12.1nm tunnel oxide. (a) written cell, (b) erased cell.

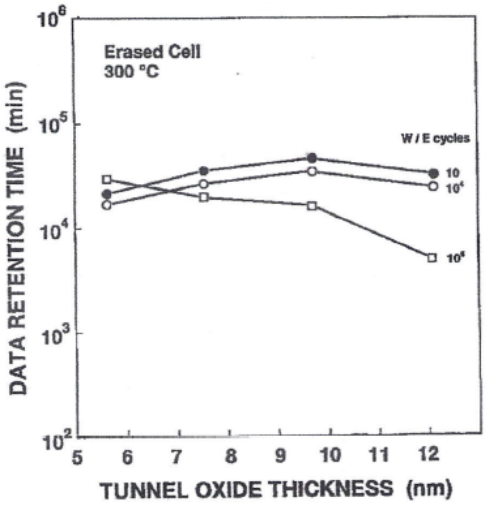


Fig.5.2.15 Data retention time at 300C depending on the tunnel oxide thickness and the number of write/erase cycles.

5.2.5 Summary

A highly reliable EEPROM has been successfully developed by using a uniform write and uniform erase technology. This technology is performed by uniform injection and uniform emission of electrons over the whole channel area of a Flash memory cell both during write and erase. The wide cell threshold voltage window, even after 1 million write and erase cycles, and the stored positive charge which is effectively increased in an erased cell during the retention bake, drastically improve the data retention time. This technology can be applied to the NAND-type cell, however it cannot be applied to the NOR-type cell because it is not possible to apply a selective write operation. Therefore, the NAND-type cell has an advantage for reliability, as compared with the NOR-type cell.

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5.3 Read Disturb

Abstract ; Read disturb and data retention characteristics have been described in two different write/erase methods on flash memories. It is clarified experimentally that Flash memory cell, which is written and erased by bi-polarity uniform Fowler-Nordheim tunneling (FN-t), has ten times as long retention time as the conventional one, which is written by channel-hot-electron(CHE) injection and erased by uni-polarity FN-t. This difference of data retentivity between these two Write/Erase(W/E) technology is due to decreasing the Stress Induced Leakage Current (SILC) in thin tunnel oxide by bi-polarity FN-t stress. And also, this improvement in data retention is more remarkable, according as the tunnel oxide thickness decreases. Therefore, a bi-polarity FN-t W/E technology, which enables a Flash memory cell to scale down its oxide thickness, promisingly becomes the key technology to realize highly reliable Flash and NAND Flash memories.

5.3.1 Introduction

A high density Flash memory [5.3.1]-[5.3.3] is expected to be a promising device for next-generation non-volatile memory market. However, it has been reported that the thin oxide leakage currents, which are induced by the write and erase cycling stress, degrade the data retention of memory cell [5.3.4]. These oxide leakage currents increase with decreasing the thin oxide thickness, and make it difficult to scale down the gate oxide thickness of the memory cell [5.3.5].

In this chapter, a reliable bi-polarity write/erase technology is proposed. The thin gate oxide leakage current is greatly reduced by this technology, as compared with conventional technology. So, data retention time can be extended even after a large number of write and erase cycles [5.3.8].

5.3.2 Stress Induced Leakage Current (SILC)

The stress induced leakage currents (SILC) which are subjected to three types of simulated W/E stressing are compared. Figure 5.3.1 shows the stressing waveform for simulated W/E stress. Table 1 shows stress conditions which are corresponding to write/erase conditions in flash memory cells. A high voltage is applied to gate or substrate and source/drain(S/D). The SILCs are induced by the electron injection and emission between the gate and substrate, as shown in Fig.5.3.2. It is newly observed that

the SILC induced by (a) bi-polarity dynamic stressing is about one order smaller than that induced by both (b) the electron emitted stress and (c) the electron injected stress. This result shows that the origin of the SILC can be removed by reverse FN-t stress and it would be the directional defect or strain or trapped holes in the SiO_2. This improvement of the SILC results in extension of read disturb and data retention time in Flash memory cell.

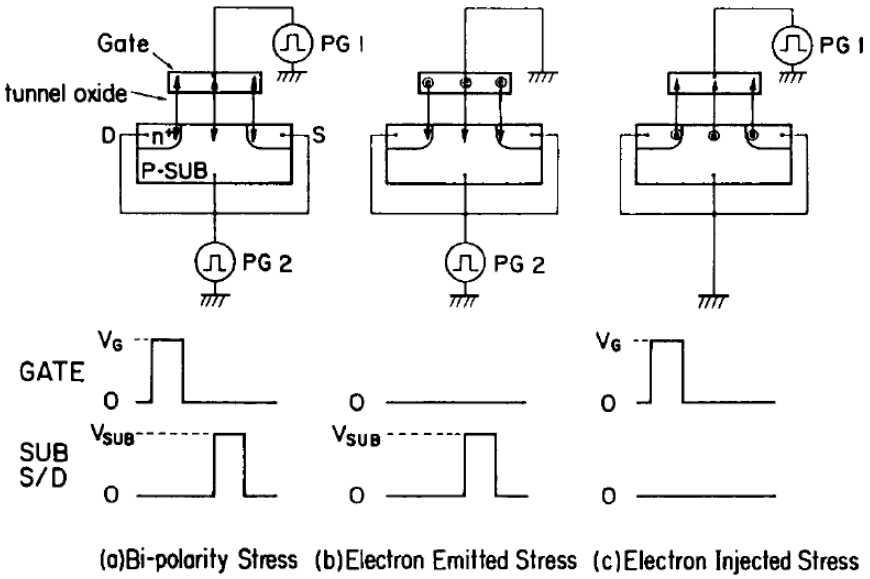


Fig.5.3.1 Set-up and stressing waveform for (a)Bi-polarity stress, (b) Electron emitted stress and (c) Electron injected stress. Stress conditions are shown in Table 1.

Table 1. Stress conditions: high voltage pulses are applied to the gate and substrate. Stress voltage Vg and Vsub are determined by the voltage that the opposite tunneling currents are approximately the same.

Tox	GATE	SUB S/D
5.6nm	6.79V 0.2msec	8.0V 0.2msec
7.5nm	7.91V 0.2msec	9.15V 0.2msec

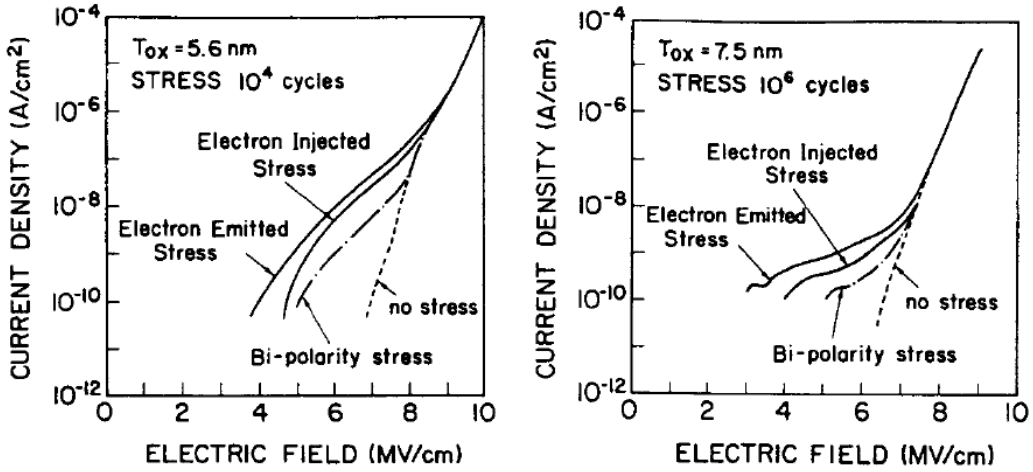


Fig.5.3.2 Stress Induced Leakage currents (SILC) of tunnel oxide at low voltages for 5.6 and 7.5 nm oxide after Bi-polarity stress, Electron emitted stress, and Electron injected stress. In the case of Bi-polarity stress, oxide leakage current is small as compared with the others.

5.3.3 Read Disturb

Read Disturb characteristics of the Flash memory cell programmed by two W/E technologies are compared. One is a bi-polarity FN-t W/E technology, performed by uniform injection and uniform emission over the whole channel area of Flash memory cell (Fig.5.3.3). The other is a conventional channel-hot-electron (CHE) write and FN-t erase technology, performed by CHE injection at drain and uniform emission over the whole channel area (Fig.5.3.3). In erasing, a high voltage is applied to the substrate [5.3.6] as well as source/drain in order to prevent from causing the degradation of the thin gate oxide due to band-to-band tunneling stress [5.3.7]. Table 2 shows device parameter of flash memory cell which are used in this experiments.

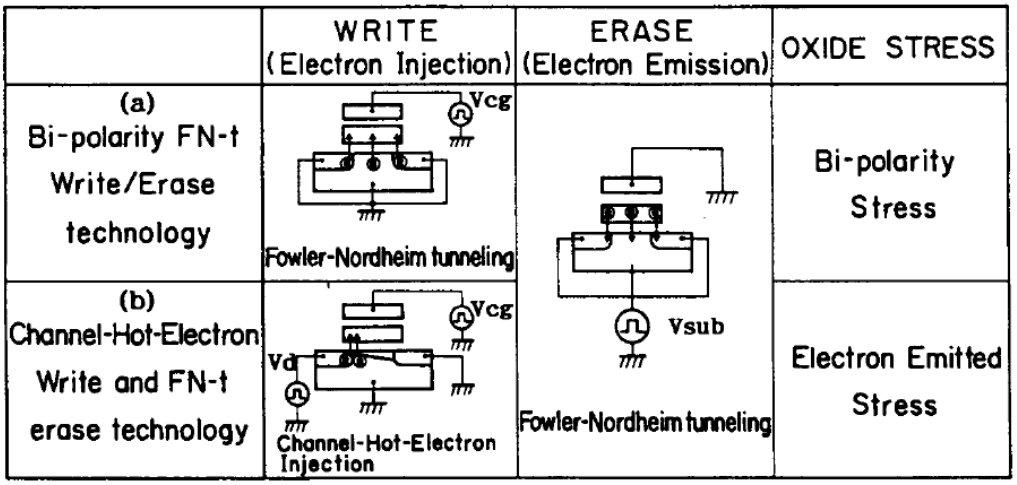
Figure 5.3.4 shows the Write/Erase endurance characteristics of two W/E technologies. The closure of the cell threshold window has not been found up to 100,000 write/erase cycles in both two technologies.

Read Disturb characteristics are measured at applied various gate voltage conditions, which are accelerated electric field test. In the case of a CHE write and FN-t erase technology, the stored positive charges rapidly decay as stress time (retention time) increases, so the threshold window decreases (Fig.5.3.5). However, in the case of a bipolarity FN-t W/E technology, data loss of the stored positive charges is greatly improved. So, data retention time of a bi-polarity FN-t W/E technology is extended about ten times as long as that of conventional technology. This phenomenon can be

explained that the SILC is reduced by bi-polarity FN tunneling stress.

Figure 5.3.6 shows data retention time under read disturb condition after write and erase cycling as a function of the tunnel oxide thickness. The improvement in data retention is more effective with decreasing the oxide thickness. So, in bi-polarity FN-t W/E technology, the thin gate oxide thickness can be reduced with scaling down the Flash memory cell. Then, it gives advantages of low voltage program and erase operations.

Initial data loss is measured at 300 C, as shown in Fig.5.3.7. It is confirmed that initial data loss of bi-polarity FN-t W/E technology is smaller than that of CHE write and FN-t erase technology due to reduction of stress induced oxide leakage current.



Flg.5.3.3 Comparison between (a)bi-polarity FN tunneling write/erase technology, corresponding to bi-polarity stress of tunnel oxide and (b)channel hot electron(CHE) write and FN tunneling erase technology, corresponding to electron emitted stress of tunnel oxide, because of no leakage current induced by CHE injection.

TABLE 2

Device Fabrication

GATE OXIDE THICKNESS	5-10 nm
INTERPOLY INSULATOR(ONO) THICKNESS	25 nm
GATE LENGTH	0.8 um

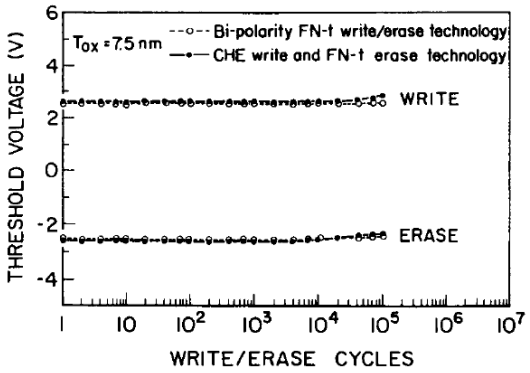


Fig.5.3.4 Endurance characteristics of Flash memory cell with 7.5 nm tunnel oxide. In bi-polarity FN tunneling W/E technology, write: Vcg=18V, 1msec, erase: Vsub=20V, lmsec. In conventional technology, write: Vcg=7V, Vd=8.5V, 1 msec. erase: Vsub=20V, 1 msec.

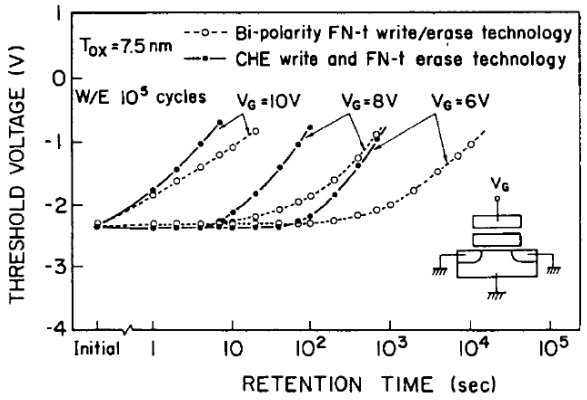


Fig.5.3.5 Read Disturb characteristics at the applied various gate voltage stress. Flash memory cell having 7.5 nm thick oxide are subjected to 100,000 write/erase cycles. In bi-polarity FN tunneling W/E technology, data loss of stored positive charge is improved as compared with conventional technology, it is corresponding to results of oxide leakage currents.

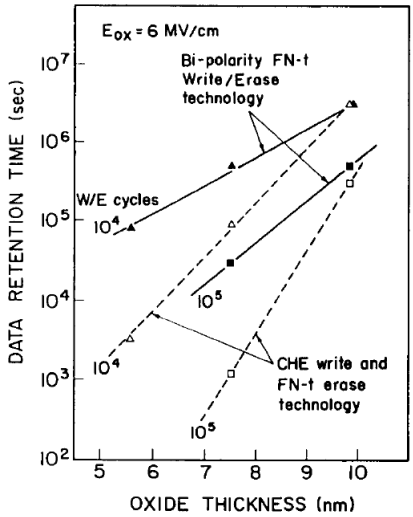


Fig.5.3.6 Data retention time of the Flash memory cell after write and erase cycling as a function of tunnel oxide thickness. Data retention time is defined by the time that Vth reaches -1.0V during the applied gate voltage stress (accelerated read disturb condition). In bi-polarity FN tunneling write/erase technology, the tunnel oxide thickness can be reduced with scaling down the Flash memory cell.

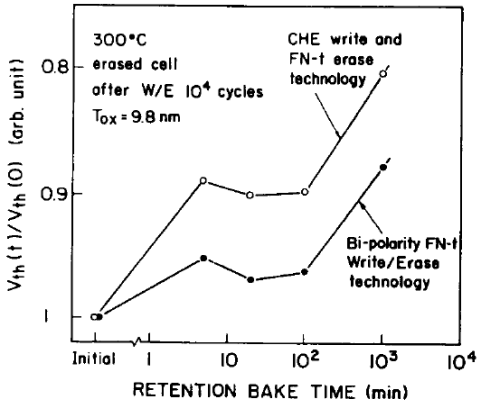


Fig.5.3.7 Initial data loss of the erased cell which stores positive charges in floating gate as a function of retention bake time at 300C in a bi-polarity FN tunneling write/erase technology and CHE write and F-N tunneling erase technology, subjected to 10,000 Write and Erase cycles.

5.3.4 Summary

A highly reliable Flash memory cell has been successfully developed by using a bi-polarity FN tunneling W/E technology. Data retention time can be extended by using this technology, because the Stress Induced Leakage Current (SILC), which is induced

by write/erase cycling stress, can be drastically reduced by bi-polarity FN-t operation. This improvement is more remarkable in the case of thinner tunnel oxide. Therefore, the tunnel oxide thickness can be reduced with scaling down the Flash memory cell. It is the key technology to realize high density flash and NAND flash memories.

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5.4 Negative Vt shift phenomena

Abstract ; A novel program inhibit phenomena of "negative" cell-Vt shift has been investigated for the first time in 2X~3X nm Self-Aligned STI NAND flash memory cells. The negative Vt shift is caused in an inhibit cell when along-WL adjacent cell is programming. The magnitude of the negative shift becomes larger in case of higher program voltage (V_{PGM}), lower Field oxide Height (FH), slower program speed of the adjacent cell, and high Vt of victim cell. The experimental results suggest that the

mechanism of negative Vt shift is attributed to hot holes that are generated by FN electrons injection from channel/junction to the control gate (CG). This phenomenon will become worse with cell size scaling since hot hole generation is increased by increasing electron injection due to narrower floating gate (FG) space. Therefore, this negative Vt shift phenomenon is one of the new scaling limiter of NAND flash memory cell, that needs to be managed for 2bits and 3bits/cell in 2X nm and beyond NAND Flash memory.

5.4.1 Introduction

The Self-Aligned Shallow Trench Isolation cell (SA-STI cell) [5.4.1][5.4.2] has been used for NAND Flash memory products for a long time from 0.2um generation [5.4.3] to present mid-1X nm generation [5.4.4]. The structure of the SA-STI cell along Word Line (WL) is shown in Fig.5.4.1. A floating gate (FG) is self-aligned patterned with STI to avoid overlap of FG on STI edge corner. In the SA-STI cell, the side wall of FG is used for increasing a capacitance between FG and CG, to increase a coupling ratio. Then the Field oxide Height (FH), which is the distance between channel Si and top of STI field oxide, has to be decreased as small as possible to increase a coupling ratio, as shown in Fig.5.4.1(a). The decreasing FH can also obtain small FG-FG coupling interference [5.4.6] along WL direction. However, in small FH, high voltage (~20V) is applied directly between substrate (channel) and CG during program and erase. This high electric field is a concern that could have an impact on reliability and performance of NAND flash memory.

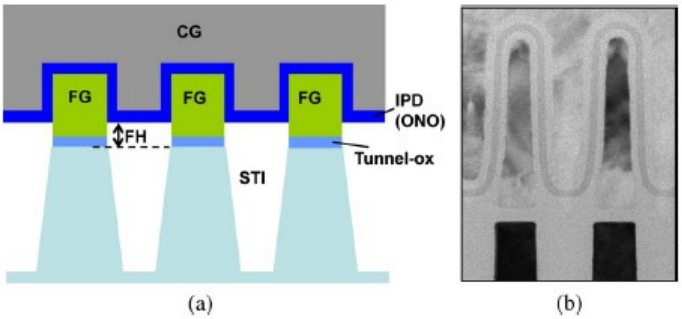

Fig.5.4.1 (a) The Self-Aligned Shallow Trench Isolation cell (SA-STI cell) structure along word line (WL), and b) TEM micrograph of 26nm SA-STI cell [5.4.5]. A Field oxide Height (FH) is the distance between channel Si and the top of STI field oxide.

This chapter describes newly observed “negative” Vt shift phenomena in program inhibit conditions of 2X-3Xnm SA-STI NAND Flash cell [5.4.7][5.4.19]. The negative Vt shift occurs in small FH case, thus it is one of high field effect during programming. The negative Vt shift phenomena make the Vt read window margin worse for MLC/TLC due to widening Vt distribution width. Therefore, the negative shift phenomena could become a new potential obstacle of scaling NAND Flash cells in the scaled 2X~ nm NAND Flash.

5.4.2 Experimental

A 2X and 3X nm rule SA-STI cells with various FH were used for this experiment. The range of FH small/middle/large in experiments are 10~20nm. And thickness of IPD (ONO) is around 12nm. The cross-sectional TEM micrograph of 26nm SA-STI cell [5.4.5] is shown in Fig.1(b).

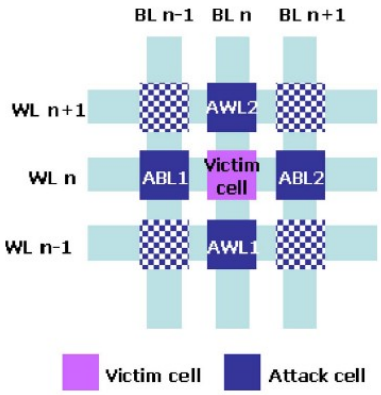

Fig.5.4.2 The cell arrangement for program-inhibited test. Attack cells of ABL1&2 are the adjacent cells along WL direction, and Attack cells of AWL1&2 are adjacent cells along BL direction.

Fig.5.4.2 shows the cell arrangement for program-inhibited test. Attack cells of ABL1&2 are adjacent cells along WL direction, and Attack cells of AWL1&2 are adjacent cells along BL direction. The Vt of inhibit victim cells are monitored before and after programming the attack cells.

For an analysis of current flow in SA-STI structure in program condition in chapter 5.4.6, a cell-structured capacitor is used. Terminals of CG, FG, Source/drain junction, and substrate are independently connected to monitor the current.

5.4.3 Negative Vt shift

Fig.5.4.3 shows the victim cell Vt shift during programming the attack cell. In case of Attack AWL2, the Vt of the victim cell monotonously increases with Attack AWL2 cell Vt increased due to conventional FG-FG coupling interference [5.4.6]. However, In case of ABL1&2, the Vt of the victim cell initially increases and then decreases as the Attack ABL1&2 are programmed. Vt shift caused by programming neighbor cell should be positive if it is caused by conventional FG-FG coupling interference. However Vt shift is showing negative direction as Attack cell Vt increases over Vt>7. We call this phenomenon as "negative Vt shift". This negative Vt shift has been observed for the first time.

Fig.5.4.4 shows the dependence of the negative Vt shift on FH. The negative Vt shift has a strong FH dependence. The negative Vt shift is larger when FH is small. In region of Attack cell Vt<6, the slope of (victim cell Vt) / (Attack cell Vt) is showing the conventional FG-FG coupling interference. In case of FH low, the slope is smaller than the case of FH middle and large. That means FH low case has small FG-FG coupling interference due to CG shield effect between FGs.

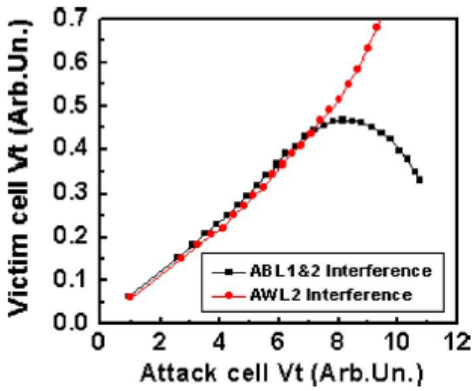

Fig.5.4.3 Victim cell Vt shift versus attack cell programmed Vt. Negative Vt shift phenomena is observed in case of Attack ABL1 and ABL2. Victim cell Vt is corresponding to L1 for MLC.

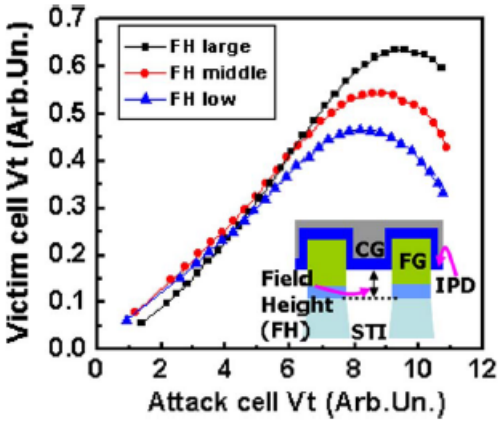

Fig.5.4.4 Field Height (FH) dependence of "negative" Vt shift. Small FH has the larger "negative" shift. Victim cell Vt is corresponding to L1 for MLC.

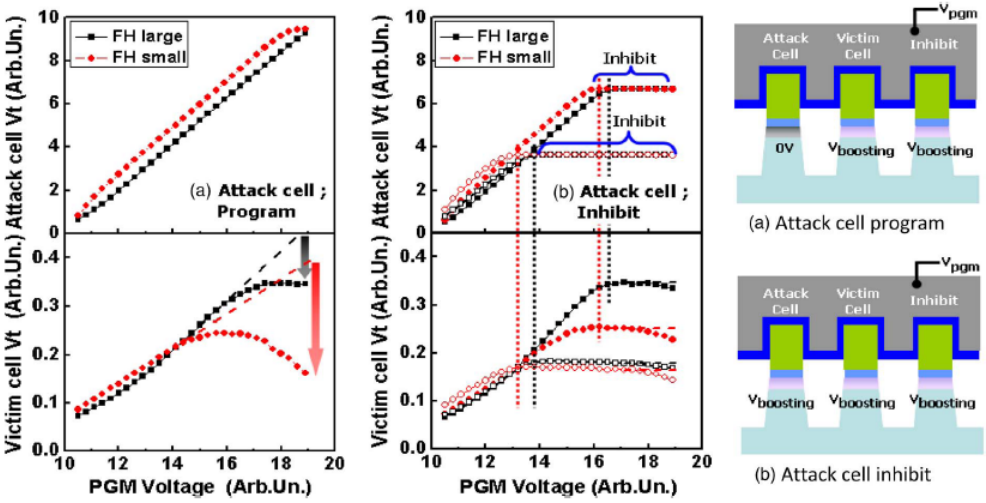

Fig.5.4.5 Victim cell Vt shift in (a) Attack cell; Program and (b) Attack cell; Inhibit. In case of (a) Attack cell program, large negative shift of Victim cell is observed, however in case of (b) Attack cell; inhibit, negative Vt shift is much smaller. Difference of bias conditions between (a) and (b) is a channel voltage of 0V for program or Vboost (~8V) for inhibit. Victim cell Vt is corresponding to L1 for MLC.

Fig.5.4.5 shows the victim cell Vt dependence on (a) Attack cell; Program and (b) Attack cell; Inhibit condition, which are illustrated in right side of Fig.5.4.5. In (a) Attack cell; program, Attack cell Vt is monotonously increased. Victim cell Vt initially increases and then decreases as Attack cell Vt increases. These Vt movement is the same as that in Fig.5.4.3 and Fig.5.4.4. However, in the case of (b) Attack cell; inhibit, attack cell Vt initially increases, and when the attack cell Vt has reached to around 4 or 7, Attack cell Vt stops increasing by changing channel voltage from 0V to

$V_{boosting}$ (inhibit mode) during program pulse. This operation is corresponding to the program verify operation [5.4.10] in product, such that, when Vt has reached to certain Vt, programming is stopped by changing to inhibit mode during next program pulse (channel voltage changes from 0V to $V_{boosting}$). For victim cell Vt in (b) Attack cell inhibit, a negative shift is much smaller than case (a) Attack cell ; program, when Attack cells are in inhibit mode, even high program voltage (Vpgm) is applied. Because the same high Vpgm pulses are applied in both cases of (a) and (b), the difference of bias condition between (a)Attack cell; Program and (b) Attack cell: Inhibit is only the channel voltage in Attack cell, which are 0V for Program or $V_{boosting}$ for inhibit, as shown in right side of Fig.5.4.5. Thus, the channel voltage of 0V in Attack cell make a negative Vt shift in inhibit victim cell, especially in case of small FH.

$V_{boosting}$ (~8V) is generated by Vpass for unselected WL with capacitive coupling between unselected WL and the cell channel where is isolated by select transistor in NAND string in the self boosting program inhibit scheme [5.4.8][5.4.9].

5.4.4 Program speed dependence

The program speed dependence of attack cell is measured in actual page program sequence of MLC NAND product with Incremental Step Pulse Program (ISPP) [5.4.8] and bit-by-bit verify operation [5.4.10]. Fig.5.4.6 shows the victim cell delta Vt versus attack cell program speed for 16Kbits (2KByte) page. The horizontal axis shows the Vt distribution of a page after applying one program-voltage pulse (Vpgm), which means that the left side cells have slower programming speed, and the right side cells have faster programming speed. In case of (a) Attack cell ABL1=L1 & ABL2 =L1 (programming to L1 (lower Vt) ; Erase →L1), victim cell delta Vt is larger in slow attack cell and the smaller in fast attack cell, due to conventional FG-FG interference. The slower attack cells have the larger victim cell delta Vt, because attack cell Vt change during program (Erase → L1) is larger in slow attack cell, as shown in an illustration of upper of Fig.5.4.6 (a).

In order to make sure the larger Vt change in slow attack cell, the bit-by-bit Vt distribution after program and erase are measured. Figure 5.4.7 shows the bit-by-bit correspondence of program and erase Vt distributions after one program pulse and one erase pulse. We can see that the program cells in left side of programmed Vt distribution are also in left side of erased Vt distribution, and similarly that the program cells in right side of programmed Vt distribution are also in right side of erased Vt distribution. Therefore, it is confirmed that the slow program cells are in left side of

erased Vt distribution, as shown in an illustration of upper of Fig.5.4.6 (a).

On the other hand, in case of (b) Attack cell ABL1=L3 and ABL2=L3 (programming to L3 (higher Vt) ; LSB →L3) in Fig.5.4.6(b), the victim cell delta Vt is smaller in slow attack cell and larger in fast attack cell, even if Vt shift by a conventional FG-FG coupling should be the same between slow and fast cells due to the same attack cell Vt change during program (LSB → L3), as shown in an illustration of upper of Fig.5.4.6(b). This means the negative Vt shift is much larger (-0.2~-0.4V) in case of slow attack cell, compared with fast attack cell.

The reason is supposed that in slow attack cell, the larger number and higher voltage (Vpgm) of program pulses are subjected in condition of channel voltage=0V (see Fig.5.4.5 (a) attack cell program). Then negative shift become larger in slow attack cell. Conversely, in fast attack cell, the larger number and higher voltage of program pulse are shortly subjected in condition of channel voltage=0V, because fast attack cell become inhibit-mode (channel voltage=$V_{boosting}$) earlier than slow attack cell.

Furthermore, this new negative Vt shift results in wider placement Vt distribution. In case of (a) Attack cell ABL1=L1 & ABL2 =L1, victim cell delta Vt distribution width is 0.36V, however in case of (b) Attack cell ABL1=L3 & ABL2=L3, victim cell delta Vt distribution width is 0.48V. These Vt distribution width have an impact on read window margin of MLC/TLC NAND flash product.

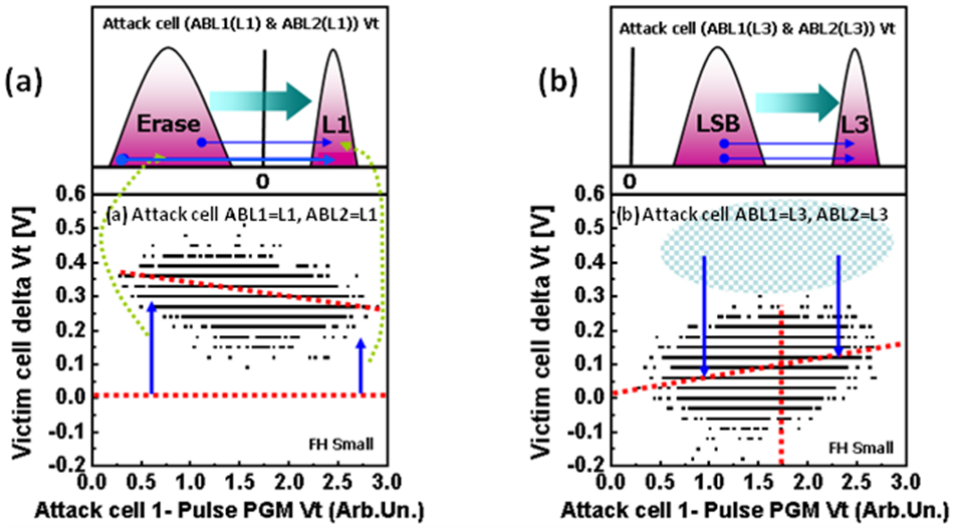

Fig.5.4.6 Victim cell delta Vt distribution of 16Kbits cell versus Attack cell program speed (Attack cell Vt distribution of a page after applying one program-voltage pulse). In case of (a) Attack cell ABL1=L1 & ABL2 =L1, Victim cell delta Vt shows dependence of conventional FG-FG coupling interference. However in case of (b)

Attack cell ABL1=L3 & ABL2=L3, Victim cell delta Vt shows the larger negative Vt shift for slow attack cell. Victim cell Vt is corresponding to L3 for MLC.

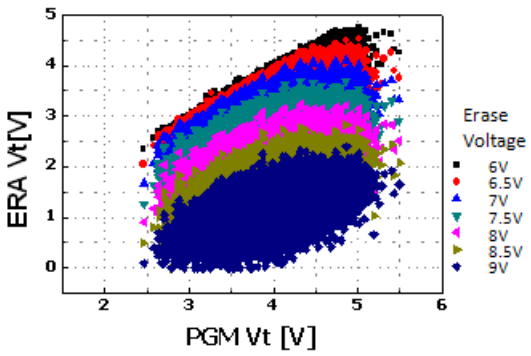

Fig.5.4.7 The bit-by-bit correspondence of program and erase Vt after one program pulse and one erase pulse. Several erase voltages are used (6V~9V). The erased Vt has a parallel shift as erase voltage increases. Then it is supposed that erased Vt distribution in more negative Vt has the same correspondence, so that it is confirmed that the slow program cells are in left side of erased Vt distribution.

5.4.5 Victim cell Vt dependence

Fig.5.4.8 shows the dependence on program state of victim cell, (a) L1, (b) L2, and (c) L3. The victim cell delta Vt of L3 is smaller than that of L1 and L2, especially in case of Attack cell ABL1=L3 & ABL2=L3. It means the negative Vt shift is larger in victim cell L3. This is considered that the FG of L3 is negatively charged, then it could gather more positive charge during attack cell programming.

Summarizing the results of the negative Vt shifts phenomena (chapter 5.4.3~5.4.5), the negative Vt shift are enhanced in case of 1) neighbor cell along WL (ABL1,2) in programming (channel voltage =0V), 2) small FH, 3) higher V_{PGM}, 4) attack cell ; L3, 5) attack cell; slow programming, and 6) victim cell; higher Vt (L3).

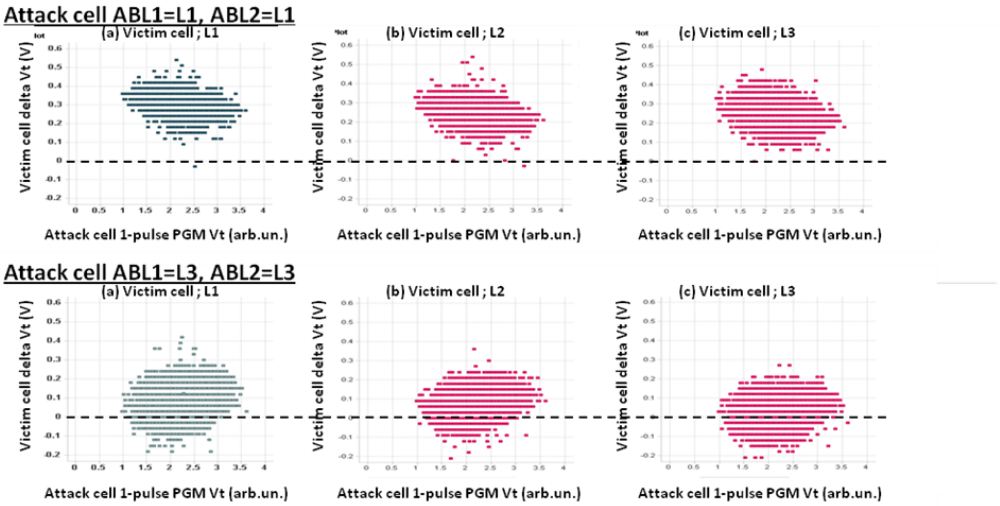

Fig.5.4.8 The dependence of victim cell delta Vt on program states (L1, L2, L3), in Attack cell ABL1=L1 & ABL2 =L1 and Attack cell ABL1=L3 & ABL2 =L3. Victim cell delta Vt of (c) L3 has the larger negative shift than that of (a)L1 and (b)L2.

5.4.6 Carrier Separation in programming conditions

In order to clarify mechanism of negative Vt shift, a cell-structured test capacitor is measured by using a carrier separation technique [5.4.11]-[5.4.15], as shown in Fig.5.4.9. A cell-structured test capacitor has a stripe patterned active area/ STI and flat CG pattern, with source and drain. A measurement condition of Fig.5.4.9 is that a control gate voltage (V_{CG}) sweeps while keeping V_{FG}=constant (8V) and V_{well}=$V_{juction}$=0V. The image of electron flow is illustrated in Fig.5.4.10. Measured current of I_{CG}, I_{FG}, and $I_{junction}$ in Fig.5.4.9 can be expressed by using electron flow as shown in Fig.5.4.10.

$$I_{CG} = - I_{CG\_Juction} - I_{CG\_FG} \quad \text{---(1)}$$

$$I_{FG} = - I_{FG\_Junction} + I_{CG\_FG} \quad \text{---(2)}$$

$$I_{junction} = I_{CG\_Junction} + I_{FG\_Junction} \quad \text{---(3)}$$

$$I_{FG\_Junction} = \text{Constant.}$$

It is observed that the hole current (I_{well}) is increased as V_{CG} increased in high V_{CG}>18 region. In region of V_{CG}>18, $I_{CG\_Junction}$ and I_{CG_FG} are increased as V_{CG} increased, while $I_{FG\_Junction}$ are basically constant because of constant V_{FG}. At V_{CG}>18 in Fig.5.4.9, $I_{junction}$ of small FH is larger than $I_{junction}$ of middle FH, and also I_{well} of small FH is larger than I_{well} of middle FH. From these observations of $I_{Junction}$ and I_{well}

in Fig.5.4.9, I_{well} (hole current) is considered to be generated by $I_{CG\_Junction}$, not by I_{CG_FG}, as shown in Fig.5.4.10. $I_{CG\_Junction}$ is the electron flow of FN injection from channel/junction to CG. $I_{CG\_Junction}$ may generate I_{well} (hole current) based on anode hole injection model [5.4.11]-[5.4.18].

For I_{FG}, I_{FG} is almost constant at $V_{CG}<20$ because $I_{FG\_Junction}$ = Constant while I_{CG_FG} is small due to small V_{CG}-V_{FG}. As increased V_{CG} to $V_{CG}>20$, I_{FG} polarity is changed, because I_{CG_FG} is increased by increasing (V_{CG}-V_{FG}) and become dominant current of I_{FG}.

Fig.5.4.11 shows a current flow in constant V_{CG}. Even if a voltage between channel/junction and CG is constant, I_{CG} is increased as V_{FG} is increased. This means that I_{CG}, which is mainly a direct electron injection from channel/junction to CG, is strongly enhanced by V_{FG}, even if constant V_{CG} is applied. As a scaling down of memory cell size, a FG-FG space becomes narrow. Then I_{CG} will increase because V_{FG} could enhance I_{CG} intensively. It suggests that negative Vt shift phenomena may be enhanced as scaling down of memory cell.

The ratio of (substrate hole current) / (gate electron current) [=$I_{well}/I_{junction}$] in Fig.5.4.11 is the range of 10^{-3} over V_{FG}=3~5. The substrate hole current (I_{well}) is mainly generated by FN current through tunnel oxide ($I_{FG\_Junction}$). The value is the same range as previous reported value [5.4.11]-[5.4.13], [5.4.15], [5.4.18] for the same oxide thickness and electric field. However, in Fig.5.4.9, the ratio of (substrate hole current)/(gate electron current) [=I_{well}/I_{CG}], in which the substrate hole current (I_{well}) is mainly generated by FN current from channel to CG, is the range of 10^{-4}. It is one or two order smaller value than previous reported value of 10^{-3}~ 10^{-2} [5.4.11]. The reason of smaller substrate hole current is not clear, however it would be that the large number of the generated holes does not flow to substrate due to cell structure, which is different from flat capacitor in previous report [5.4.11]. It suggests that the generated holes could flow to any directions, including the direction of FG.

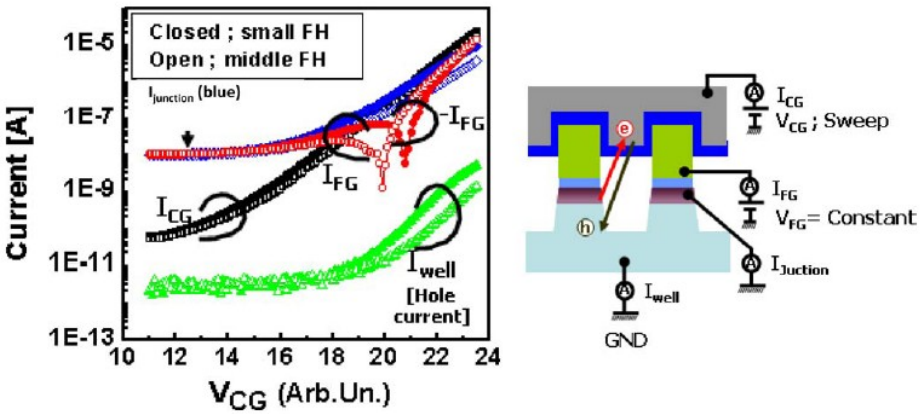

Fig.5.4.9 Current analysis of cell structured capacitor by carrier separation technique. Hole currents (I_{Well}) are observed, and are increased as V_{CG} is increased. A large hole current is generated due to large $I_{junction}$ in case of small FH.

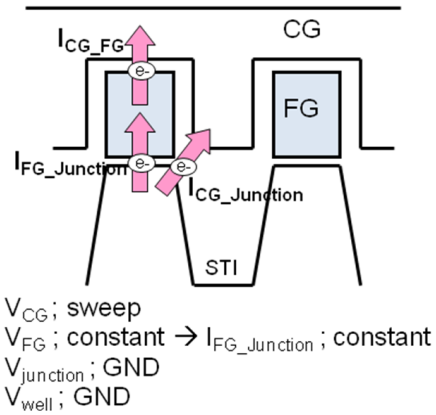

Fig.5.4.10 Electron flow in condition of Fig. 5.4.9. $I_{junction}$ (in Fig.5.4.9) = $I_{CG\_Junction}$ + $I_{FG\_Junction}$. Hole current (I_{well}) at region of V_{CG}>18 (Fig.5.4.9) is generated by $I_{CG\_Junction}$.

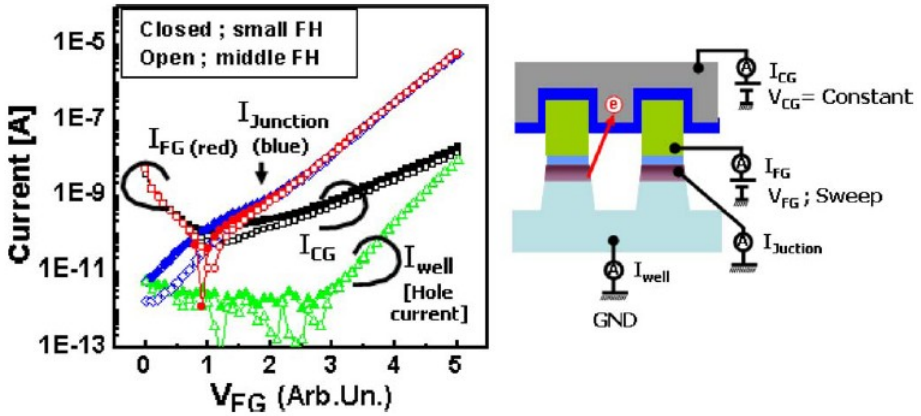

Fig.5.4.11 Current analysis of cell structured capacitance. Even if V_{CG} is constant, I_{CG} (direct electron injection from channel/junction to CG) is increased as V_{FG} is increased.

This means I_{CG} is enhanced by FG potential.

5.4.7 Model

From the results of current flow in cell structured capacitor, the mechanism of negative Vt shift is considered as illustrated in Fig.5.4.12. During programming, electrons are injected from channel/junction (0V) to CG (V_{PGM}) directly. Electron injection generates hot holes by impact ionization, and hot holes are injected to IPD on STI. Parts of hot holes are injected into to the FG of victim cell through the field-oxide dielectric or IPD. Consequently, the Vt of victim cell has shifted negatively.

This phenomenon would be accelerated with memory cell scaling since I_{CG} increases due to narrow FG-FG space field effect. Then the negative Vt shift phenomena will be worse in future scaled memory cells. Then the negative Vt shift will be one of new scaling limitation factor to manage Vt read window margin of 2bit and 3 bit/cell in 2X nm and beyond NAND Flash memory cell.

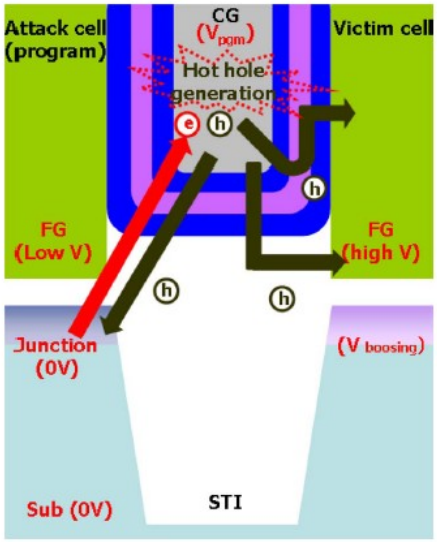

Fig.5.4.12 Suggested mechanism of negative Vt shift in victim cell. Electron injection from channel/Junction (0V) to CG (V_{PGM}) could generate hot hole at CG, and parts of hot holes are injected to FG of victim cell through field dielectric and IPD. This hot hole injection causes “negative Vt Shift.”

5.4.8 Summary

Negative Vt shift phenomenon in a program inhibit cell has been presented. The

magnitude of the negative Vt shift become large in small FH, higher program voltage, slower program speed of attack cell, and higher Vt (L3) of victim cell. This mechanism has been explained by hot hole generation by FN electron injection from channel/junction to CG, and then hot holes are injected from CG to FG of inhibit cell. The negative Vt shift phenomenon will be a new obstacle that needs to be managed for 2 and 3bit/cell in 2Xnm and beyond NAND flash memories.

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5.5 Summary of Chapter 5

In chapter 5, phenomena of flash reliability have been described.

In chapter 5.2, program/erase cycling degradation and data retention characteristics were described. The data retention characteristics of Flash memory cell have been

drastically improved by applying a bi-polarity write and erase technology which uses uniform Fowler-Nordheim tunneling over the whole channel area both during write and erase. It is clarified experimentally that the detrapping of electrons from the gate oxide to the substrate results in an extended retention time of erase state. A bi-polarity write and erase technology also guarantees a wide cell threshold voltage window even after 1 million write/erase cycles. This technology results in a highly reliable Flash memory with an extended data retention time.

In chapter 5.3, read disturb and data retention characteristics were described. It is clarified experimentally that Flash memory cell written and erased by Fowler-Nordheim tunneling (FN-t) has ten times as long retention time as the conventional one, which is written by channel-hot-electron(CHE) inject ion and erased by FN-t. This difference of data retentivity between these two Write/Erase(W/E) technology is due to decreasing the Stress Induced Leakage Current (SILC) of thin gate oxide by bi-polarity FN-t stress. And also, this improvement in data retention is more remarkable, according as the gate oxide thickness decreases. Therefore, a bi-polarity FN-t W/E technology, which enables a Flash memory cell to scale down its oxide thickness, promisingly becomes the key technology to realize reliable Flash memory.

In chapter 5.4, a novel program inhibit phenomena of “negative” cell-Vt shift has been investigated for the first time in 2X~3X nm Self-Aligned STI NAND flash memory cells. The negative Vt shift is caused in an inhibit cell when along-WL adjacent cell is programming. The magnitude of the negative shift becomes larger in case of higher program voltage (V_{PGM}), lower Field oxide Height (FH), slower program speed of the adjacent cell, and high Vt of victim cell. The experimental results suggest that the mechanism of negative Vt shift is attributed to hot holes that are generated by FN electrons injection from channel/junction to the control gate (CG). This phenomenon will become worse with cell size scaling since hot hole generation is increased by increasing electron injection due to narrower floating gate (FG) space. Therefore, this negative Vt shift phenomenon is one of the new scaling limiter of NAND flash memory cell, that needs to be managed for 2bits and 3bits/cell in 2X nm and beyond NAND Flash memory.

Flash memory reliability and physical phenomena are summarized in Fig.5.5.1 [5.5.1]. It is clarified that traps in tunnel oxide, detrapping, SILC(Stress Induced Leakage Current) are the major roots cause of degradation of flash memory reliability.

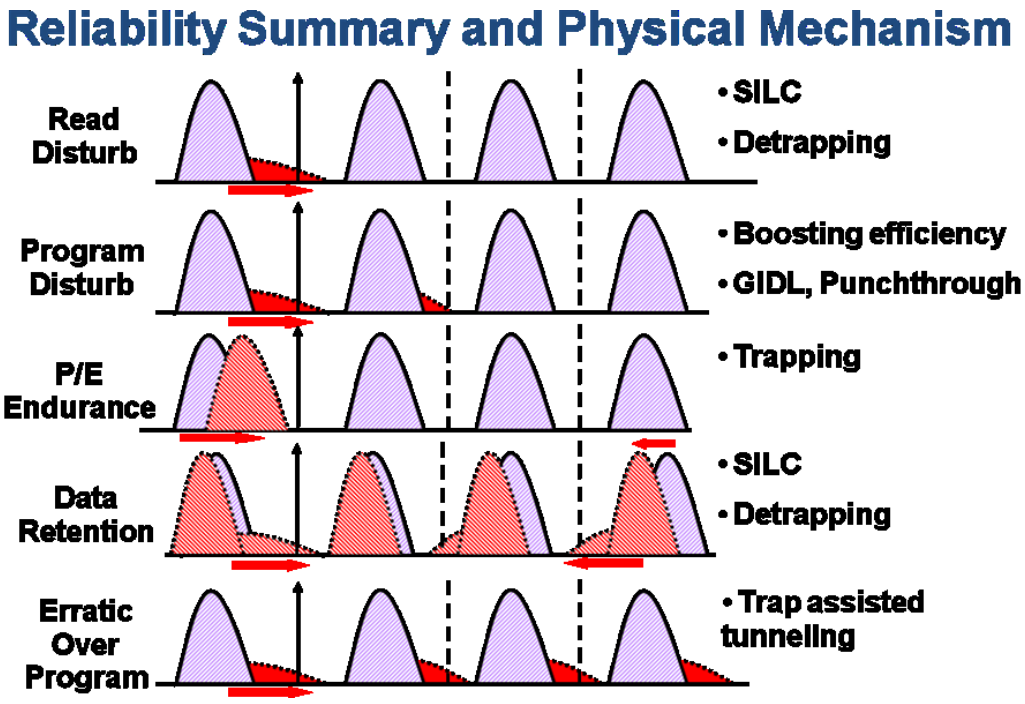

Fig.5.5.1 Reliability Summary and Physical mechanism

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Chapter 6
Conclusions

6.1 Discussion and contribution

This chapter describes the history and trend of NAND flash memory cell technology, corresponding to the contribution of this thesis.

The development of NAND Flash had started on 1987 in R&D center, Toshiba Corp [6.1]. There were two major targets to achieve, "low bit cost" and "high reliability". In order to achieve low bit cost, memory cell size has to be as small as possible. In general, ideal "physical" memory cell size is $4*F^2$ (F; Feature size), which is defined by 2*F pitch for both x- and y-directions. The first NAND flash cells of 1um rule [6.2][6.3] was $8*F^2$ cell size by using wide x-direction pitch of 4um (4*F) because LOCOS isolation width was 3um wide due to limitation of high voltage operation. The LOCOS isolation width had limited by the punch-through of bit-line junction and threshold voltage of parasitic field LOCOS transistor, because a high voltage of ~22V was applied to junction and control gate during programming.

In order to reduce the LOCOS isolation width, new FTI (Field-Through-Implantation) process had been developed [6.4] (**Chapter 3.2**). Very narrow LOCOS isolation width of 0.8um (2*F in 0.4um feature size) could be realized. Memory cell size could be scaled down to $6*F^2$ by using 3*F bit-line pitch in 0.4um rule.

For scaling down memory cell size further, the Self-Aligned Shallow Trench Isolation cell (the SA-STI cell) had been proposed [6.5] (**Chapter 3.3, 3.4**). The isolation width could be scaled down to F by using STI, then BL pitch can be reduced to 2*F in comparison with that of LOCOS cell of 3*F bit-line pitch. Therefore, the cell size of NAND Flash memory could be drastically shrunk to 66% (from $6F^2$ to ideal $4F^2$; F: Feature size). The SA-STI cell process was applied to NAND Flash product with structure of the SA-STI with FG wing [6.6] (**Chapter 3.3**), because the aspect ratio of stacked gate can be reduced by FG wing structure. The SA-STI cell with FG wing had been used from 0.25um generation to 0.12um (or 50 nm) generation. After that, the

SA-STI cell without FG wing had been used from 90nm (or 50nm) generation [6.5] (**Chapter 3.4**). The SA-STI cell has an excellent scalability. The cell size could decrease straightforward as feature-size decreased from 0.25um [6.6] to current 1Xnm [6.7] (Fig. 3.1.2 in chapter 3.1). Therefore, the SA-STI cell structure and process have been used more than 10 years and 10 generations due to simple process and structure. Moreover, The SA-STI cell has other advantage of an excellent reliability. The tunnel oxide has no degradation at STI edge corner because of no sharp STI edge corner by fabricating floating gate with STI patterning.

The cell size of NAND flash became ideal $4*F^2$ by the SA-STI cell. The feature size (F) is normally determined by capability of lithography tool. At present, most advanced lithography tool is ArF immersion (ArFi) stepper. Minimum feature size is 38~40nm. Then scaling of feature size (F) had limited by 38-40nm. In order to accelerate to scale down NAND flash memory cell size further, the double patterning process [6.22] had started to use from 3Xnm generation. The side-wall spacer is used as a patterning mask in conventional double patterning process. Thanks to double patterning, feature size could be scaled down from 38~40nm to 19~20nm. Furthermore, quadruple (x4) patterning has been used beyond 20nm [6.7]. Feature size (F) can be scaled down to 10nm by using ArFi.

The memory cell size of SA-STI cell could be extensibly scaled down by using double and quad patterning. However, the SA-STI cell has been facing serious physical limitations, such as FG-FG coupling interference, electron injection spread, RTN, etc. The scaling challenge and limitations were quantitatively analyzed and then clarified the solutions to overcome scaling limitation[6.8] (**Chapter 3.5**). It was concluded that 1Y-1Znm (13-10nm) SA-STI cell could be realized by using 60% air-gap process.

MLC (Multi-Level-Cell) is other important technology to reduce "effective" memory cell size without F scaling. In MLC (2bits/cell), Vt distribution width has to be tightly controlled to be lower than Vpass_read voltage to prevent read failure. The new SWATT cell had been proposed [6.9] (**Chapter 3.6**). Due to the SWATT cell, Vt distribution width can be wider, for example, from 0.8V to 1.1V, because of function of transfer transistor at side-wall of STI.

Recently, 3-Dimentional (3D) NAND Flash cell was proposed [6.10] in order to decrease memory cell size furthermore. The 3D cells have vertically stacked structure by new concept of stacked gate layers. Then effective cell size can be reduced without scaling feature size of F. However, the conventional 3D NAND cells were using the charge trap cell, which is called "SONOS" (or "TANOS") cell. SONOS cell has two serious problems of slow erase (erase Vt saturation) and poor data retention. Then, the

2D SONOS cell could not be started production in several years ago. In addition, in 3D SONOS cell, data retention has degraded by the charge spreading in SiN, because charge trap layer SiN are connected between upper and lower cells.

The novel FG (Floating Gate) 3D NAND cell has proposed [6.11] (**Chapter 4.2**), which are called the DC-SF cell (Dual Control gate – Surrounding Floating gate cell). Due to replacing a charge trap cell to a FG cell, the problem related with 3D SONOS could be perfectly solved. The DC-SF cell has a unique structure of FG coupled with two upper and lower control gates. Therefore, the operation of DC-SF cell is unique. The new read and program schemes have been investigated and proposed [6.12] (**Chapter 4.3**).

The other requirement for NAND Flash is "high reliability". At a term of starting NAND flash development, the program/erase schemes were intensively discussed internal development team in order to select proper scheme. It was not clear how program/erase scheme had an impact on reliability. Then, the reliability of NAND Flash cell had analyzed on several Program/Erase (P/E) schemes. Figure 6.1.1 shows three P/E schemes of NAND Flash, "CHE (Channel Hot-Electron) program scheme" [6.1], "Non-uniform P/E scheme" [6.13][6.14], and "Uniform P/E scheme" [6.15][6.16][6.17]. In order to decide proper P/E scheme, performances and reliabilities were evaluated.

The P/E cycling endurance and data retention characteristics are evaluated and analyzed in the two P/E scheme [6.15][6.18] (**Chapter 5.2**). It had been clarified that the uniform P/E scheme, which is used in NAND Flash, was appropriate reliability in comparison with other schemes [6.15][6.18][6.19]. And also, the read disturb characteristics had been analyzed in the cells which were subjected to P/E cycling endurance stress [6.17][6.19] (**Chapter 5.3**). It had been clarified that the uniform P/E scheme had the better read disturb characteristics because SILC (Stress Induced Leakage Current) could be suppressed by bi-polarity FN (Fowler-Nodheim) program scheme. As a result, the uniform P/E scheme was decided for NAND flash operation.

The uniform P/E scheme had another important advantage. Unlike a NOR Flash, no huge hot-electron injection current is required for programming, but uniform P/E scheme has realized very low power consumption for program even when the number of memory cells to be programmed is increased. Therefore the NAND flash memory can be easily programmed in large pages (512bytes~32Kbytes cells) so that the programming speed per byte can be quite fast (~100Mbyte/s). Due to high reliability and fast programming, the uniform program/erase scheme became de-facto standard technology. All of NAND suppliers (Toshiba/SanDisk, Samsung, Micron/Intel, SK

Hynix) have used the uniform P/E scheme for all NAND flash products over 20 years.

In a 2X~3X nm Self-Aligned STI NAND flash memory cells, a new program inhibit phenomena of "negative" cell-Vt shift has been observed for the first time [6.20] (**Chapter 5.4**). The negative Vt shift is caused in an inhibit cell when along-WL adjacent cell is programming. The experimental results suggest that the mechanism of negative Vt shift is attributed to hot holes that are generated by FN electrons injection from channel/junction to the control gate (CG). This negative Vt shift phenomenon is one of the new scaling limiter of NAND flash memory cell, that needs to be managed for 2bits and 3bits/cell in 2X nm and beyond NAND Flash memory.

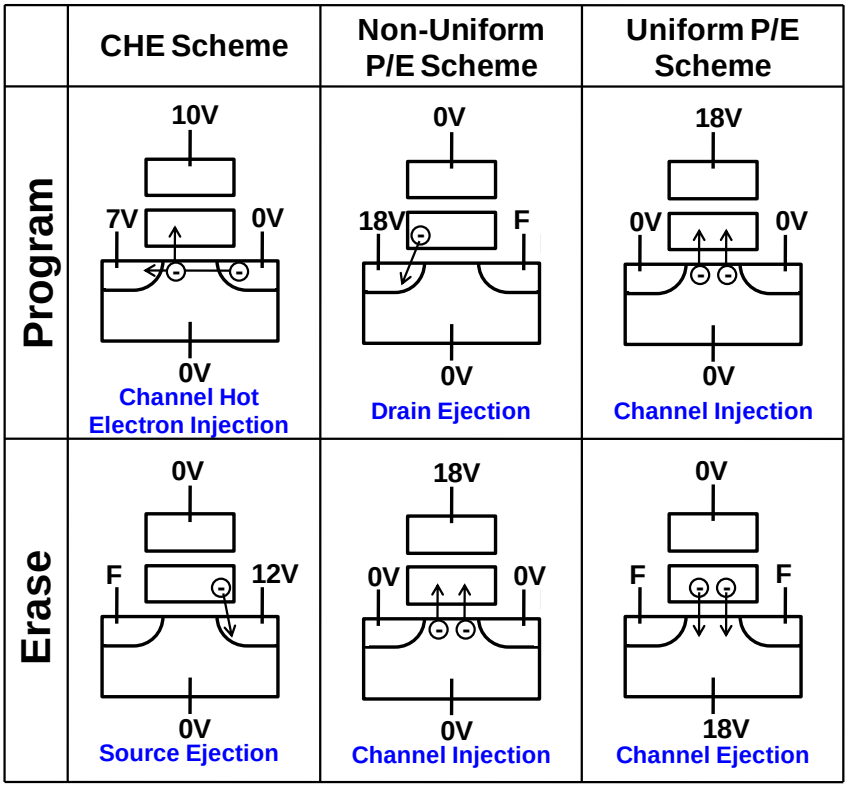

Fig. 6.1.1 Program and Erase scheme of NAND Flash. Uniform P/E scheme has been used as standard in all NAND Flash product for more than 20 years.

6.2 Conclusion

Memory cell technologies of NAND flash have been discussed. Several NAND flash memory cell have been proposed and intensively investigated to achieve low bit cost, small memory cell size, high performance, and high reliability.

In this chapter, the achievement of this research are summarized. The following are

investigated in this research.

1) The LOCOS isolation NAND cell is developed. A small memory cell size of 1.13 μm^2 per bit has been achieved in 0.4 μm technology. In order to realize the small cell size, narrow 0.8 μm LOCOS field isolation is realized with Field Through Implantation (FTI) technique. A negative bias of -0.5 V to the P-well of the memory cell is applied during programming to improve field isolation. In addition, a bit-by-bit intelligent writing technology allows a 3.3 V data sensing scheme which can suppress read disturb to 1/1000 in comparison with the conventional 5 V scheme. As a result, 10^6 write and erase cycles can be achieved and that the tunnel oxide can be scaled down from 10 nm to 8 nm.
2) The Self-Aligned STI cell with FG wing has been developed. The extremely small cell size of $0.31um^2$ has been achieved for the 0.25um design rule. To minimize the cell size, a floating gate is isolated with shallow trench isolation (STI) and a slit formation by a novel SiN spacer process, which has made it possible to realize a 0.55um-pitch isolation at a 0.25um design rule. A tight Vt distribution width (2.0V) in 2Mbit memory cell array is achieved due to a good uniformity of the channel width in the self-aligned STI cells. And also, the peripheral low voltage CMOS transistors and high voltage transistors can be fabricated at the same time by using the self-aligned STI process. As a result, (1) The number of process steps is reduced to 60% in comparison with a conventional process, and (2) high reliability of the gate oxide is realized even at high voltage transistors because a gate electrode does not overlap the trench corner. Therefore this SA-STI process integration combines a small cell size (a low cost) with a high reliability for a manufactuable 256Mbit and lGbit flash memory.
3) The Self-Aligned STI cell (SA-STI cell) without FG wing has been developed. The SA-STI technology results in a small cell size of 0.67 um^2 per bit by using 0.35um design rule, 67% without dimension scaling. The key technologies to realize a small cell size are (1) 0.4um width Shallow Trench Isolation (STI) to isolate neighboring bits and (2) a floating gate that is self-aligned with the STI, eliminating the floating-gate wings. Even though the floating-gate wings are eliminated, a high coupling ratio of 0.65 can be obtained by using the side-walls of the floating gate to increase the coupling ratio. Therefore, the SA-STI cell can achieve a high performance and a high reliability, such as the fast programming (0.2usec/byte), fast erasing (2msec), and good program/erase endurance (>1 million cycles).
4) The scaling limitations and challenges of SA-STI cell are investigated over 2X~0X

nm generations for NAND flash memories. The scaling challenges are categorized to 1) narrow Read Window Margin (RWM) problem, 2) structural challenge, and 3) high field (5~10 MV/cm) problem. First, 1) the narrow RWM is investigated by extrapolating physical phenomena of FG-FG coupling interference, Electron Injection Spread (EIS), Back Pattern Dependence (BPD), and Random Telegraph Noise (RTN). The RWM is degraded not only by increasing programmed Vt distribution width, but also by increasing Vt of erase state mainly due to large FG-FG coupling interference. However, RWM is still positive in 1Z nm (10nm) generation with 60% reduction of FG-FG coupling by air-gap process. For 2) structural challenge, the Control Gate (CG) fabrication margin between Floating Gates (FGs) is becoming much severer beyond 1X nm generation. Very narrow 5nm FG width/space has to be controlled. For 3) high field problem, high field between CGs (word lines; WLs) is critical during program. By using WL air-gap, high field problem can be mitigated, and 1Y/1Z nm generations could be realized. Therefore, the SA-STI cell is expected to be able to scale down to 1Z nm (10nm) generation, with the air gap of 60% reduced FG-FG coupling interference and an accurate control of FG/CG formation process.

5) A new Side-WAll Transfer-Transistor (SWATT) cell has been developed for a high performance and reliable multi-level cell (MLC) NAND Flash memory. With the SWATT cell, a relatively wide threshold voltage (Vth) distribution width of 1.1V is sufficient for a 4-level memory cell in contrast to a narrow 0.6 V distribution. The key technology that allows this wide Vth distribution width is the Transfer Transistor which is located at the side wall of STI region and is connected in parallel with the floating gate transistor. During read, the Transfer Transistors of the unselected cells work as pass transistors. So, even if the Vth of the unselected floating gate transistor is higher than the control gate voltage, the unselected cell is in the ON state. As a result, the Vth distribution of the floating gate transistor can be wider and the programming can be faster because the number of program/verify cycles can be reduced.

6) Three-dimensional (3D) Dual Control gate with Surrounding Floating gate (DC-SF) NAND flash cell has been proposed. The DC-SF cell consists of a surrounding floating gate with stacked dual control gates. With this structure, high coupling ratio, low voltage cell operation, and wide Program/Erase window (9.2 V) can be obtained. Moreover, negligible FG-FG coupling interference (12 mV/V) is achieved due to the control-gate shield effect. As a result, the DC-SF NAND flash cell can overcome the problems of conventional SONOS-based 3D NAND flash.

7) An advanced DC-SF (Dual Control gate with Surrounding Floating gate) cell process and operation schemes have been developed. In order to improve performance and reliability of DC-SF cell, new Metal Control Gate Last (MCGL) process has been developed. The MCGL process can realize a low resistive tungsten (W) metal word-line, a low damage on tunnel oxide/IPD (Inter-Poly Dielectric), and a preferable FG shape. And also, new read and program operation schemes have been developed. In new read operation, the higher and lower $V_{pass-read}$ are alternately applied to unselected control gates (CGs) to compensate lowering FG potential to be a pass transistor. And in new program scheme, the optimized V_{pass} are applied to neighbor WL of selected WL to prevent program disturb and charge loss through IPD. Thus, by using MCGL process and new read/program schemes, high performance and high reliability of DC-SF cell can be realized for 3D NAND flash memories.

8) Program/erase cycling degradation and data retention characteristics of NAND Flash were investigated. The data retention characteristics have been drastically improved by applying a bi-polarity write (program) and erase scheme (uniform P/E scheme) which uses uniform Fowler-Nordheim tunneling over the whole channel area both during write and erase. It is clarified experimentally that the detrapping of electrons from the gate oxide to the substrate results in an extended retention time of erase state. A bi-polarity write and erase scheme also guarantees a wide cell threshold voltage window even after 1 million write/erase cycles.

9) Read disturb and data retention characteristics of NAND flash were investigated. It is clarified experimentally that Flash memory cell written and erased by Fowler-Nordheim(FN) tunneling has ten times as long retention time as the conventional one, which is written by channel-hot-electron(CHE) inject ion and erased by FN tunneling. This difference of data retentivity between these two Write/Erase(W/E) technology is due to decreasing the thin gate oxide leakage current by bi-polarity FN tunneling stress. And also, this improvement in data retention is more remarkable, according as the gate oxide thickness decreases.

10) Novel negative Vt shift phenomena in inhibit cell during programming had been analyzed for the first time in 2X~3X nm Self-Aligned STI NAND flash memory cells. The negative Vt shift is caused in an inhibit cell when along-WL adjacent cell is programming. The magnitude of the negative shift becomes larger in case of higher program voltage (V_{PGM}), lower Field oxide Height (FH), slower program speed of the adjacent cell, and high Vt of victim cell. The experimental results suggest that the mechanism of negative Vt shift is attributed to hot holes that are

generated by FN electrons injection from channel/junction to the control gate (CG). This phenomenon will become worse with cell size scaling since hot hole generation is increased by increasing electron injection due to narrower floating gate (FG) space. Therefore, this negative Vt shift phenomenon is one of the new scaling limiter of NAND flash memory cell.

6.3 Perspective

This chapter describes the prospective technologies of NAND flash memory. Figure 6.3.1 shows the scaling trend and the future scenario of NAND flash memory [6.24]. The 2-dimensional SA-STI (2D planar FG) cell has been scaled down to 1Xnm cell. However, it is facing critical scaling limitations in 1Y-1Z nm generations [6.8], as shown in chapter 3.5. A severe FG-FG coupling interference is major root cause of critical scaling limitation to degrade RWM (Read Window Margin). The 1Y-1Z nm SA-STI cell could be realized with reliability management of system solution, such as signal processing. However, process cost of 1Y-1Z nm cell would be much increased due to applying quadruple patterning process for several layers in both x- and y-direction of cells.

On the other hand, 3D NAND cell has been intensively developed. 3D NAND cell can be realized extremely small cell size with more than 32 stacked cells. If 128 stacked cells can be realized, 2-Tera bits NAND Flash memory product will be provided around on 2020. Critical challenges of 3D NAND cell is the extremely high aspect ratio process. The difficulty of high aspect ratio process can be solved by the multi-stacked technology, which is divided stacked layers, for example, 128 stacked cells are fabricated by 4 times of 32 stacked. If multi-stacked technology can be realized, the effective cell size scaling scenario would be much accelerated, as 50% shrinkage of effective cell size for each generation in contrast to 64~70% shrinkage in 2D planar FG cell (Fig.6.3.1). And also, multi-stacked 3D cell does not have so many development items between generation and generation in contrast to many new development items for 2D planar FG cell. Therefore, bit cost of 3D NAND flash will be accelerated to reduce with increasing bit density for future, as shown in Fig.6.3.1.

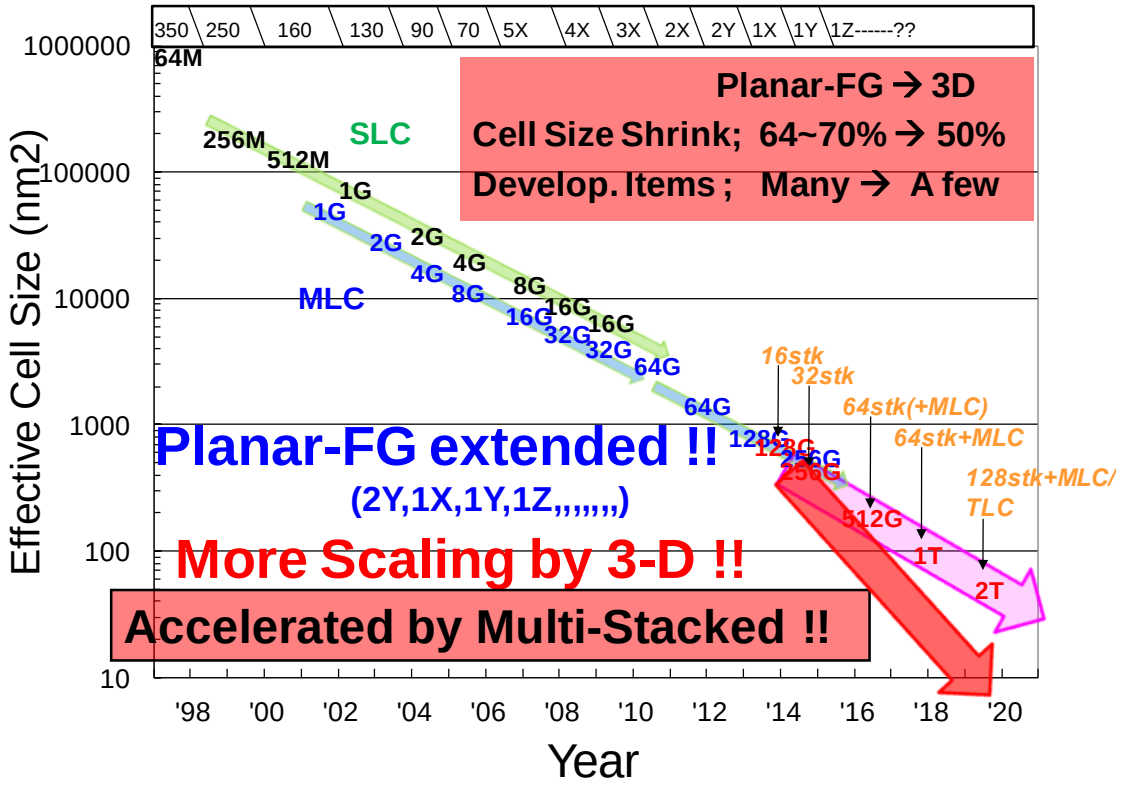

Fig.6.3.1 Scaling trend of NAND Flash memory cell.

The reliability of NAND flash is also important for future applications. However, as the memory cell scaling, the reliability has been degraded by many physical limitations (Chapter 3.5). The important reliability aspects of program/erase cycling and data retention are trade-off relationship, as shown in Fig.6.3.2 [6.23]. Future target of P/E cycling and data retention will be compromised as <1K P/E cycling and <1 year data retention even with system solutions.

Performance and reliability are also trade-off relationship [6.23]. If high speed programming is required, the reliability (such as P/E cycling) will be degraded because the higher electrical field is applied to tunnel oxide in memory cell during program. On the other hand, some application would require higher guarantee of reliability, such as >10K P/E cycling, >3 years retention. Performance should be compromised due to applying bunch of system solutions. Therefore, target reliability of NAND Flash memory would be much subdivided to each applications, such as memory cards, consumer application (smartphone, tablet-PC, etc), high end applications (enterprise server SSD), etc.

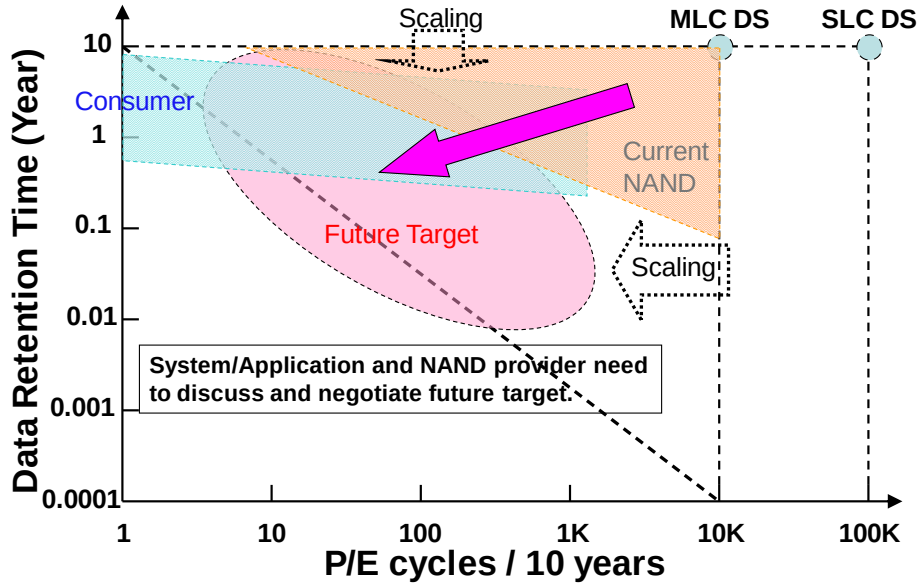

Fig.6.3.2 Prospect of Data retention versus Program/Erase cycling. Due to encountering physical limitation, reliability in future scaling device will be worse than current device. System management would be essential.

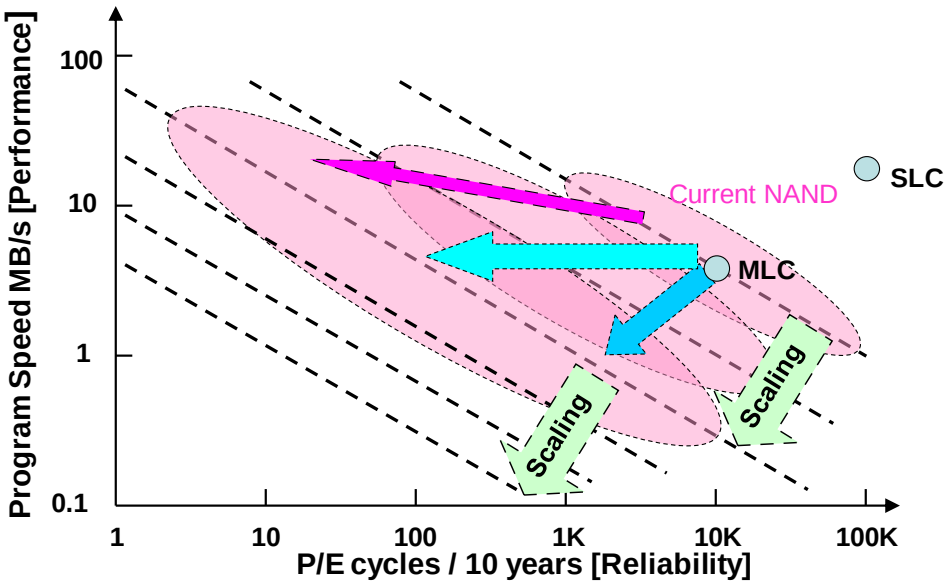

Fig.6.3.3 Prospect of Performance versus Reliability. Performance and reliability are "trade-off". As device scaling, both performance and reliability will be degraded naturally. By efforts of increasing page size, performance could be kept or be improved.

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United States Patents （米国登録特許）

	Patent #	Inventors		Patent Date
1	8,369,147	***Aritome; Seiichi***	Non-volatile multilevel memory cell programming	5-Feb-13
2	8,350,309	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**8-Jan-13**
3	8,339,858	***Aritome; Seiichi***	Selecting programming voltages in response to at least a data latch in communication with a sense amplifier	**25-Dec-12**
4	8,338,879	***Aritome; Seiichi***	Transistor constructions and processing methods	**25-Dec-12**
5	8,325,520	***Aritome; Seiichi***	Reducing effects of program disturb in a memory device	**4-Dec-12**
6	8,305,810	***Aritome; Seiichi***	Multiple select gates with non-volatile memory cells	**6-Nov-12**
7	8,264,879	***Aritome; Seiichi***	Sensing memory cells	**11-Sep-12**
8	8,259,494	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**4-Sep-12**
9	8,248,849	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**21-Aug-12**
10	8,238,167	***Aritome; Seiichi***	Memory voltage cycle adjustment	**7-Aug-12**
11	8,238,155	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Zhudong, **TW**)	Multilevel memory cell operation	**7-Aug-12**
12	8,228,742	***Aritome; Seiichi***	Memory read methods, apparatus, and systems	**24-Jul-12**
13	8,223,549	***Aritome; Seiichi*** (Boise, ID), **Liu; Haitao** (Meridian, ID), **Li; Di** (Boise, ID)	NAND flash memory programming	**17-Jul-12**
14	8,208,278	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Boise, ID)	Couplings within memory devices	**26-Jun-12**
15	8,199,572	***Aritome; Seiichi***	Non-volatile memory with both single and multiple level cells	**12-Jun-12**
16	8,193,590	***Aritome; Seiichi***	Interconnecting bit lines in memory devices for multiplexing	**5-Jun-12**
17	8,164,950	**Torsi; Alessandro** (Avezzano, **IT**), **Musilli; Carlo** (Avezzano, **IT**), ***Aritome; Seiichi*** (Zhudong Town, **TW**)	Reduction of punch-through disturb during programming of a memory device	**24-Apr-12**
18	8,163,610	***Aritome; Seiichi***	Fabrication of finned memory arrays	**24-Apr-12**
19	8,159,879	***Aritome; Seiichi***	Reducing effects of program disturb in a memory device	**17-Apr-12**
20	8,154,926	***Aritome; Seiichi***	Memory cell programming	**10-Apr-12**
21	8,144,519	***Aritome; Seiichi***	Programming a flash memory device	**27-Mar-12**
22	8,129,781	**Prall; Kirk D** (Boise, ID), **Moradi; Behnam** (Boise, ID), ***Aritome; Seiichi*** (Boise, ID), **Li; Di** (Boise, ID), **Larsen; Chris** (Manassas, VA)	Method of forming memory devices by performing halogen ion implantation and diffusion processes	**6-Mar-12**
23	8,120,954	***Aritome; Seiichi***	Method, apparatus, and system for erasing memory	**21-Feb-12**
24	8,116,137	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Zhudong, **TW**)	Memory cell operation	**14-Feb-12**
25	8,116,135	***Aritome; Seiichi***	Non-volatile memory cell read failure reduction	**14-Feb-12**
26	8,102,707	***Aritome; Seiichi***	Non-volatile multilevel memory cells	**24-Jan-12**
27	8,084,802	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**27-Dec-11**
28	8,072,814	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Hsinchu, **TW**)	NAND with back biased operation	**6-Dec-11**
29	8,069,382	***Aritome; Seiichi***	Memory cell programming	**29-Nov-11**
30	8,059,474	***Aritome; Seiichi*** (Boise, ID), **Torsi; Alessandro** (Avezzano, **IT**), **Musilli; Carlo** (Avezzano, **IT**)	Reducing read failure in a memory device	**15-Nov-11**
31	8,050,096	***Aritome; Seiichi***	Programming method to reduce gate coupling interference for non-volatile memory	**1-Nov-11**
32	8,050,090	***Aritome; Seiichi*** (Boise, ID), **Antosh; Jeffrey C.** (Nampa, ID), **Frianeza; Roderick C.** (Boise, ID)	Memory page boosting method, device and system	**1-Nov-11**
33	8,030,211	***Aritome; Seiichi***	Methods for forming bit line contacts and bit lines during the formation of a semiconductor device	**4-Oct-11**
34	8,023,329	***Aritome; Seiichi*** (Boise, ID), **Marquart; Todd** (Boise, ID)	Reducing effects of program disturb in a memory device	**20-Sep-11**
35	8,018,778	***Aritome; Seiichi***	Memory read methods, apparatus, and systems	**13-Sep-11**
36	8,004,031	***Aritome; Seiichi***	Memory device transistors	**23-Aug-11**
37	8,000,136	***Aritome; Seiichi***	Non-volatile memory with both single and multiple level cells	**16-Aug-11**
38	7,995,391	***Aritome; Seiichi***	Multiple select gates with non-volatile memory cells	**9-Aug-11**
39	7,989,288	***Aritome; Seiichi***	Transistor constructions and processing methods	**2-Aug-11**
40	7,983,090	***Aritome; Seiichi***	Memory voltage cycle adjustment	**19-Jul-11**

41	7,977,190	***Aritome; Seiichi***	Memory devices having reduced interference between floating gates and methods of fabricating such devices	**12-Jul-11**
42	7,968,951	***Aritome; Seiichi***	Interconnecting bit lines in memory devices for multiplexing	**28-Jun-11**
43	7,968,930	***Aritome; Seiichi***	Finned memory cells	**28-Jun-11**
44	7,961,517	***Aritome; Seiichi***	Program and read trim setting	**14-Jun-11**
45	7,952,927	***Aritome; Seiichi***	Adjusting program and erase voltages in a memory device	**31-May-11**
46	7,952,922	***Aritome; Seiichi***	Method for programming a non-volatile memory device to reduce floating-gate-to-floating-gate coupling effect	**31-May-11**
47	7,924,619	***Aritome; Seiichi***	Programming method to reduce word line to word line breakdown for NAND flash	**12-Apr-11**
48	7,916,543	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Zhudong, **TW**)	Memory cell operation	**29-Mar-11**
49	7,898,863	***Aritome; Seiichi***	Method, apparatus, and system for improved read operation in memory	**1-Mar-11**
50	7,898,861	***Aritome; Seiichi***	Reducing effects of program disturb in a memory device	**1-Mar-11**
51	7,898,856	***Aritome; Seiichi***	Memory cell heights	**1-Mar-11**
52	7,893,477	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**22-Feb-11**
53	7,889,561	***Aritome; Seiichi*** (Boise, ID), **Goda; Akira** (Boise, ID)	Read operation for NAND memory	**15-Feb-11**
54	7,888,728	**Yaegashi; Toshitake** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile semiconductor memory device and its manufacturing method	**15-Feb-11**
55	7,864,575	***Aritome; Seiichi***	Non-volatile multilevel memory cell programming	**4-Jan-11**
56	7,859,922	***Aritome; Seiichi***	Programming a flash memory device	**28-Dec-10**
57	7,853,841	***Aritome; Seiichi***	Memory cell programming	**14-Dec-10**
58	7,843,735	***Aritome; Seiichi***	Sensing memory cells	**30-Nov-10**
59	7,835,194	***Aritome; Seiichi***	Erase operation in a flash memory device	**16-Nov-10**
60	7,826,274	***Aritome; Seiichi***	Non-volatile memory cell read failure reduction	**2-Nov-10**
61	7,826,265	***Aritome; Seiichi***	Memory device with variable trim setting	**2-Nov-10**
62	7,824,994	**Prall; Kirk** (Boise, ID), **Moradi; Behnam** (Haymarket, VA), ***Aritome; Seiichi*** (Boise, ID), **Li; Di** (Boise, ID), **Larsen; Chris** (Manassas, VA)	Method of forming memory devices by performing halogen ion implantation and diffusion processes	**2-Nov-10**
63	7,800,947	***Aritome; Seiichi***	Multiple select gates with non-volatile memory cells	**21-Sep-10**
64	7,795,664	***Aritome; Seiichi***	Finned memory cells	**14-Sep-10**
65	7,787,277	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**31-Aug-10**
66	7,773,418	***Aritome; Seiichi***	Non-volatile memory with both single and multiple level cells	**10-Aug-10**
67	7,768,839	***Aritome; Seiichi***	Memory read methods, apparatus, and systems	**3-Aug-10**
68	7,768,838	***Aritome; Seiichi***	Operating memory cells	**3-Aug-10**
69	7,763,933	***Aritome; Seiichi***	Transistor constructions and processing methods	**27-Jul-10**
70	7,755,940	***Aritome; Seiichi***	Method, apparatus, and system for erasing memory	**13-Jul-10**
71	7,751,236	***Aritome; Seiichi***	MEM suspended gate non-volatile memory	**6-Jul-10**
72	7,749,836	***Aritome; Seiichi***	Nonvolatile semiconductor memory and manufacturing method thereof	**6-Jul-10**
73	7,742,335	***Aritome; Seiichi***	Non-volatile multilevel memory cells	**22-Jun-10**
74	7,738,291	***Aritome; Seiichi*** (Boise, ID), **Antosh; Jeffrey C.** (Nampa, ID), **Frianeza; Roderick C.** (Boise, ID)	Memory page boosting method, device and system	**15-Jun-10**
75	7,733,705	**Torsi; Alessandro** (Avezzano, **IT**), **Musilli; Carlo** (Avezzano, **IT**), ***Aritome; Seiichi*** (Hsinchu County, **TW**)	Reduction of punch-through disturb during programming of a memory device	**8-Jun-10**
76	7,729,171	***Aritome; Seiichi***	Multiple select gate architecture with select gates of different lengths	**1-Jun-10**
77	7,724,577	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Hsinchu, **TW**)	NAND with back biased operation	**25-May-10**
78	7,715,239	***Aritome; Seiichi***	Memory voltage cycle adjustment	**11-May-10**
79	7,715,234	***Aritome; Seiichi*** (Boise, ID), **Marquart; Todd** (Boise, ID)	Reducing effects of program disturb in a memory device	**11-May-10**
80	7,701,765	***Aritome; Seiichi***	Non-volatile multilevel memory cell programming	**20-Apr-10**
81	7,697,335	***Aritome; Seiichi***	Multiple select gate architecture	**13-Apr-10**
82	7,684,243	***Aritome; Seiichi*** (Boise, ID), **Torsi; Alessandro** (Avezzano, **IT**), **Musilli; Carlo** (Avezzano, **IT**)	Reducing read failure in a memory device	**23-Mar-10**
83	7,675,778	***Aritome; Seiichi***	Memory devices having reduced word line current and method of operating and manufacturing the same	**9-Mar-10**
84	7,675,772	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Zhudong, **TW**)	Multilevel memory cell operation	**9-Mar-10**
85	7,668,012	***Aritome; Seiichi***	Memory cell programming	**23-Feb-10**
86	7,663,930	***Aritome; Seiichi***	Programming a non-volatile memory device	**16-Feb-10**
87	7,660,158	***Aritome; Seiichi***	Programming method to reduce gate coupling interference for non-volatile memory	**9-Feb-10**
88	7,638,878	***Aritome; Seiichi***	Devices and systems including the bit lines and bit line contacts	**29-Dec-09**

89	7,633,786	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Boise, ID)	Couplings within memory devices and methods	**15-Dec-09**
90	7,630,256	***Aritome; Seiichi***	Erase operation in a flash drive memory	**8-Dec-09**
91	7,626,866	***Aritome; Seiichi*** (Boise, ID), **Liu; Haitao** (Meridian, ID), **Li; Di** (Boise, ID)	NAND flash memory programming	**1-Dec-09**
92	7,619,918	***Aritome; Seiichi***	Apparatus, method, and system for flash memory	**17-Nov-09**
93	7,609,557	***Aritome; Seiichi***	Non-volatile memory cell read failure reduction	**27-Oct-09**
94	7,609,549	***Aritome; Seiichi***	Non-volatile multilevel memory cell programming	**27-Oct-09**
95	7,606,075	***Aritome; Seiichi*** (Boise, ID), **Goda; Akira** (Boise, ID)	Read operation for NAND memory	**20-Oct-09**
96	7,598,165	***Aritome; Seiichi***	Methods for forming a multiplexer of a memory device	**6-Oct-09**
97	7,580,287	***Aritome; Seiichi***	Program and read trim setting	**25-Aug-09**
98	7,573,752	***Aritome; Seiichi***	NAND flash memory cell programming	**11-Aug-09**
99	7,561,469	***Aritome; Seiichi***	Programming method to reduce word line to word line breakdown for NAND flash	**14-Jul-09**
100	7,560,335	***Aritome; Seiichi***	Memory device transistors	**14-Jul-09**
101	7,551,466	***Aritome; Seiichi***	Bit line coupling	**23-Jun-09**
102	7,539,066	***Aritome; Seiichi***	Method, apparatus, and system for improved erase operation in flash memory	**26-May-09**
103	7,539,052	***Aritome; Seiichi***	Non-volatile multilevel memory cell programming	**26-May-09**
104	7,534,681	***Aritome; Seiichi***	Memory device fabrication	**19-May-09**
105	7,525,841	***Aritome; Seiichi***	Programming method for NAND flash	**28-Apr-09**
106	7,515,481	***Aritome; Seiichi***	Memory block erasing in a flash memory device	**7-Apr-09**
107	7,511,994	***Aritome; Seiichi***	MEM suspended gate non-volatile memory	**31-Mar-09**
108	7,499,330	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Boise, ID), **Marquart; Todd** (Boise, ID)	Programming method for NAND EEPROM	**3-Mar-09**
109	7,495,966	***Aritome; Seiichi***	Memory voltage cycle adjustment	**24-Feb-09**
110	7,485,528	**Prall; Kirk** (Boise, ID), **Moradi; Behnam** (Haymarket, VA), ***Aritome; Seiichi*** (Boise, ID), **Li; Di** (Boise, ID), **Larsen; Chris** (Manassas, VA)	Method of forming memory devices by performing halogen ion implantation and diffusion processes	**3-Feb-09**
111	7,483,311	***Aritome; Seiichi***	Erase operation in a flash memory device	**27-Jan-09**
112	7,474,560	***Aritome; Seiichi***	Non-volatile memory with both single and multiple level cells	**6-Jan-09**
113	7,471,565	***Aritome; Seiichi***	Reducing effects of program disturb in a memory device	**30-Dec-08**
114	7,463,520	***Aritome; Seiichi***	Memory device with variable trim settings	**9-Dec-08**
115	7,452,766	***Aritome; Seiichi***	Finned memory cells and the fabrication thereof	**18-Nov-08**
116	7,450,425	***Aritome; Seiichi***	Non-volatile memory cell read failure reduction	**11-Nov-08**
117	7,440,321	***Aritome; Seiichi***	Multiple select gate architecture with select gates of different lengths	**21-Oct-08**
118	7,439,167	***Aritome; Seiichi***	Nonvolatile semiconductor memory and manufacturing method thereof	**21-Oct-08**
119	7,433,231	***Aritome; Seiichi***	Multiple select gates with non-volatile memory cells	**7-Oct-08**
120	7,425,739	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**16-Sep-08**
121	7,414,895	***Aritome; Seiichi***	NAND flash memory cell programming	**19-Aug-08**
122	7,414,284	***Aritome; Seiichi***	Nonvolatile semiconductor memory and manufacturing method thereof	**19-Aug-08**
123	7,411,832	***Aritome; Seiichi***	Programming a non-volatile memory device	**12-Aug-08**
124	7,408,810	***Aritome; Seiichi*** (Boise, ID), **Marquart; Todd** (Boise, ID)	Minimizing effects of program disturb in a memory device	**5-Aug-08**
125	7,403,425	***Aritome; Seiichi***	Programming a flash memory device	**22-Jul-08**
126	7,400,532	***Aritome; Seiichi***	Programming method to reduce gate coupling interference for non-volatile memory	**15-Jul-08**
127	7,394,693	***Aritome; Seiichi***	Multiple select gate architecture	**1-Jul-08**
128	7,391,654	***Aritome; Seiichi***	Memory block erasing in a flash memory device	**24-Jun-08**
129	7,372,742	***Aritome; Seiichi***	Memory block erasing in a flash memory device	**13-May-08**
130	7,364,951	**Goda; Akira** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Hazama; Hiroaki** (Hachioji, **JP**), **Iizuka; Hirohisa** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Moriyama; Wakako** (Yokohama, **JP**)	Nonvolatile semiconductor memory device and method for manufacturing the same	**29-Apr-08**
131	7,359,228	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**15-Apr-08**
132	7,336,541	***Aritome; Seiichi***	NAND flash memory cell programming	**26-Feb-08**

133	7,332,762	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**19-Feb-08**
134	7,292,476	**Goda; Akira** (Boise, ID), ***Aritome; Seiichi*** (Boise, ID), **Marquart; Todd** (Boise, ID)	Programming method for NAND EEPROM	**6-Nov-07**
135	7,263,006	***Aritome; Seiichi***	Memory block erasing in a flash memory device	**28-Aug-07**
136	7,259,991	***Aritome; Seiichi***	Operation of multiple select gate architecture	**21-Aug-07**
137	7,212,447	***Aritome; Seiichi***	NAND flash memory cell programming	**1-May-07**
138	7,192,831	***Aritome; Seiichi***	Nonvolatile semiconductor memory and manufacturing method thereof	**20-Mar-07**
139	7,151,685	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**19-Dec-06**
140	7,139,201	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**21-Nov-06**
141	7,095,085	**Goda; Akira** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Hazama; Hiroaki** (Hachioji, **JP**), **Iizuka; Hirohisa** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Moriyama; Wakako** (Yokohama, **JP**)	Nonvolatile semiconductor memory device and method for manufacturing the same	**22-Aug-06**
142	7,005,345	**Yaegashi; Toshitake** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile semiconductor memory device and its manufacturing method	**28-Feb-06**
143	7,002,845	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**21-Feb-06**
144	6,974,979	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**13-Dec-05**
145	6,967,892	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**22-Nov-05**
146	6,891,246	***Aritome; Seiichi***	Nonvolatile semiconductor memory and manufacturing method thereof	**10-May-05**
147	6,836,444	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**28-Dec-04**
148	6,828,627	**Goda; Akira** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Arai; Norihisa** (Omiya, **JP**), **Koido; Naoki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Maruyama; Tohru** (Yokohama, **JP**), **Hazama; Hiroaki** (Hachioji, **JP**), **Iizuka; Hirohisa** (Centreville, VA)	Semiconductor device	**7-Dec-04**

149	6,828,624	**Goda; Akira** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Hazama; Hiroaki** (Hachioji, **JP**), **Iizuka; Hirohisa** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Moriyama; Wakako** (Yokohama, **JP**)	Nonvolatile semiconductor memory device covered with insulating film which is hard for an oxidizing agent to pass therethrough	**7-Dec-04**
150	6,781,895	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**24-Aug-04**
151	6,747,311	**Goda; Akira** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Hazama; Hiroaki** (Hachioji, **JP**), **Iizuka; Hirohisa** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Moriyama; Wakako** (Yokohama, **JP**)	Nonvolatile semiconductor memory device and method for manufacturing the same	**8-Jun-04**
152	6,703,669	**Goda; Akira** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Arai; Norihisa** (Omiya, **JP**), **Koido; Naoki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Maruyama; Tohru** (Yokohama, **JP**), **Hazama; Hiroaki** (Hachioji, **JP**), **Iizuka; Hirohisa** (Centreville, VA)	Semiconductor device having serially connected memory cell transistors provided between two current terminals	**9-Mar-04**
153	6,703,658	**Yaegashi; Toshitake** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile semiconductor memory device and its manufacturing method	**9-Mar-04**
154	6,680,230	**Arai; Norihisa** (Saitama, **JP**), **Arai; Fumitaka** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Shimizu; Akira** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**)	Semiconductor device and method of fabricating the same	**20-Jan-04**
155	6,611,447	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**26-Aug-03**
156	6,611,010	**Goda; Akira** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor device	**26-Aug-03**
157	6,586,805	**Yaegashi; Toshitake** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile semiconductor memory device	**1-Jul-03**
158	6,512,253	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**28-Jan-03**
159	6,495,896	**Yaegashi; Toshitake** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**)	Semiconductor integrated circuit device with high and low voltage wells	**17-Dec-02**
160	6,472,701	**Yaegashi; Toshitake** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile semiconductor memory device and its manufacturing method	**29-Oct-02**
161	6,462,373	**Shimizu; Kazuhiro** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), **Koido; Naoki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Tsunoda; Hiroaki** (Yokkaichi, **JP**), **Iguchi; Tadashi** (Yokkaichi, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Terasaka; Kunihiro** (Yokkaichi, **JP**), **Iizuka; Hirohisa** (Centreville, VA)	Nonvolatile semiconductor memory device having tapered portion on side wall of charge accumulation layer	**8-Oct-02**
162	6,424,588	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**23-Jul-02**
163	6,413,809	**Nakamura; Takuya** (Kanagawa-Ken, **JP**), **Koido; Naoki** (Yokohama, **JP**), **Iizuka; Hirohisa** (Yokohama, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Arai; Fumitaka** (Isogo-Ku, **JP**)	Method of manufacturing a non-volatile memory having an element isolation insulation film embedded in the trench	**2-Jul-02**

164	6,396,086	**Takeuchi; Yuji** (Kawasaki, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Umemura; Masashi** (Yokkaichi, **JP**), **Murahama; Yuuichiro** (Yokkaichi, **JP**), **Araki; Hitoshi** (Yokkaichi, **JP**), **Yahata; Masamitsu** (Yokohama, **JP**), **Ikeda; Osamu** (Yokohama, **JP**)	Semiconductor device and semiconductor integrated circuit having a conductive film on element region	**28-May-02**
165	6,353,242	**Watanabe; Hiroshi** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Yaegashi; Toshitake** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**)	Nonvolatile semiconductor memory	**5-Mar-02**
166	6,342,715	**Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Watanabe; Toshiharu** (Yokohama, **JP**), **Narita; Kazuhito** (Kawasaki, **JP**)	Nonvolatile semiconductor memory device	**29-Jan-02**
167	6,340,611	**Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Watanabe; Toshiharu** (Yokohama, **JP**), **Narita; Kazuhito** (Kawasaki, **JP**)	Nonvolatile semiconductor memory device	**22-Jan-02**
168	6,310,374	**Satoh; Shinji** (Fujisawa, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device having extracting electrode	**30-Oct-01**
169	6,292,390	**Sakui; Koji** (Tokyo, **JP**), **Hasegawa; Takehiro** (Yokohama, **JP**), **Watanabe; Shigeyoshi** (Yokohama, **JP**), **Masuoka; Fujio** (Yokohama, **JP**), **Fuse; Tsuneaki** (Tokyo, **JP**), **Seshita; Toshiki** (Kawasaki, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Nitayama; Akihiro** (Kawasaki, **JP**), **Horiguchi; Fumio** (Tokyo, **JP**)	Semiconductor device	**18-Sep-01**
170	6,265,739	**Yaegashi; Toshitake** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile semiconductor memory device and its manufacturing method	**24-Jul-01**
171	6,258,665	**Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Narita; Kazuhito** (Kawasaki, **JP**)	Non-volatile semiconductor memory device and method for manufacturing the same	**10-Jul-01**
172	6,240,012	**Nakamura; Hiroshi** (Kawasaki, **JP**), **Takeuchi; Ken** (Tokyo, **JP**), **Oodaira; Hideko** (Kuroishi, **JP**), **Imamiya; Kenichi** (Kawasaki, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device capable of realizing a chip with high operation reliability and high yield	**29-May-01**
173	6,232,822	**Sakui; Koji** (Tokyo, **JP**), **Hasegawa; Takehiro** (Yokohama, **JP**), **Watanabe; Shigeyoshi** (Yokohama, **JP**), **Masuoka; Fujio** (Yokohama, **JP**), **Fuse; Tsuneaki** (Tokyo, **JP**), **Seshita; Toshiki** (Kawasaki, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Nitayama; Akihiro** (Kawasaki, **JP**), **Horiguchi; Fumio** (Tokyo, **JP**)	Semiconductor device including a bipolar transistor biased to produce a negative base current by the impact ionization mechanism	**15-May-01**
174	6,222,225	**Nakamura; Takuya** (Kanagawa-Ken, **JP**), **Koido; Naoki** (Yokohama, **JP**), **Iizuka; Hirohisa** (Yokohama, **JP**), **Narita; Kazuhito** (Yokkaichi, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Arai; Fumitaka** (Isogo-Ku, **JP**)	Semiconductor device and manufacturing method thereof	**24-Apr-01**
175	6,191,975	**Shimizu; Kazuhiro** (Yokohama, **JP**), **Satoh; Shinji** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Non-volatile NAND type semiconductor memory device with stacked gate memory cells and a stacked gate select transistor	**20-Feb-01**
176	6,188,611	**Endoh; Tetsuo** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Shuto; Susumu** (Ichikawa, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Hemink; Gertjan** (Kawasaki, **JP**), **Tanzawa; Toru** (Ebina, **JP**)	Non-volatile semiconductor memory device	**13-Feb-01**
177	6,172,911	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device with an improved verify voltage generator	**9-Jan-01**
178	6,160,297	**Shimizu; Kazuhiro** (Yokohama, **JP**), **Watanabe; Hiroshi** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Watanabe; Toshiharu** (Yokohama, **JP**)	Semiconductor memory device having a first source line arranged between a memory cell string and bit lines in the direction crossing the bit lines and a second source line arranged in parallel to the bit lines	**12-Dec-00**
179	6,157,056	**Takeuchi; Yuji** (Kawasaki, **JP**), **Watanabe; Toshiharu** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Watanabe; Hiroshi** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**)	Semiconductor memory device having a plurality of memory cell transistors arranged to constitute memory cell arrays	**5-Dec-00**

180	6,115,287	**Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device using SOI	**5-Sep-00**
181	6,080,624	**Kamiya; Eiji** (Kawasaki, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory and method for manufacturing the same	**27-Jun-00**
182	6,061,280	***Aritome; Seiichi*** (Yokohama, **JP**)	Data protection system for nonvolatile semiconductor memory device	**9-May-00**
183	6,060,740	**Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Narita; Kauhito** (Kawasaki, **JP**)	Non-volatile semiconductor memory device and method for manufacturing the same	**9-May-00**
184	6,057,580	**Watanabe; Hiroshi** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device having shallow trench isolation structure	**2-May-00**
185	6,049,482	***Aritome; Seiichi*** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**)	Non-volatile semiconductor memory device	**11-Apr-00**
186	6,046,940	**Takeuchi; Ken** (Tokyo, **JP**), **Sakui; Koji** (Tokyo, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device	**4-Apr-00**
187	6,023,423	***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device	**8-Feb-00**
188	6,014,330	**Endoh; Tetsuo** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Shuto; Susumu** (Ichikawa, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Hemink; Gertjan** (Kawasaki, **JP**), **Tanzawa; Toru** (Ebina, **JP**)	Non-volatile semiconductor memory device	**11-Jan-00**
189	5,978,265	**Kirisawa; Ryouhei** (Yokohama, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Nakayama; Ryozo** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Masuoka; Fujio** (Yokohama, **JP**)	Non-volatile semiconductor memory device with nand type memory cell arrays	**2-Nov-99**
190	5,949,101	***Aritome; Seiichi*** (Yokohama, **JP**)	Semiconductor memory device comprising multi-level logic value of the threshold voltage	**7-Sep-99**
191	5,946,231	**Endoh; Tetsuo** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Shuto; Susumu** (Ichikawa, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Hemink; Gertjan** (Kawasaki, **JP**), **Tanzawa; Toru** (Ebina, **JP**)	Non-volatile semiconductor memory device	**31-Aug-99**
192	5,946,230	**Shimizu; Kazuhiro** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**), **Satoh; Shinji** (Fujisawa, **JP**)	Nonvolatile semiconductor memory device having the reliability of gate insulating film of memory cells enhanced and method for manufacturing the same	**31-Aug-99**
193	5,940,321	**Takeuchi; Ken** (Tokyo, **JP**), **Sakui; Koji** (Tokyo, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device	**17-Aug-99**
194	5,909,399	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**1-Jun-99**
195	5,889,304	**Watanabe; Hiroshi** (Yokohama, **JP**), **Shimizu; Kazuhiro** (Yokohama, **JP**), **Takeuchi; Yuji** (Kawasaki, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device	**30-Mar-99**
196	5,818,791	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Oa-Ku, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**6-Oct-98**
197	5,793,696	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**11-Aug-98**

198	5,774,397	**Endoh; Tetsuo** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Shuto; Susumu** (Ichikawa, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Hemink; Gertjan** (Kawasaki, **JP**), **Tanzawa; Toru** (Ebina, **JP**)	Non-volatile semiconductor memory device and method of programming a non-volatile memory cell to a predetermined state	**30-Jun-98**
199	5,766,996	**Hayakawa; Toshiyuki** (Kanagawa-ken, **JP**), ***Aritome; Seiichi*** (Kanagawa-ken, **JP**)	Method of manufacturing a semiconductor device	**16-Jun-98**
200	5,724,300	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**3-Mar-98**
201	5,698,879	***Aritome; Seiichi*** (Yokohama, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Takeuchi; Ken** (Tokyo, **JP**)	Nonvolatile semiconductor memory device	**16-Dec-97**
202	5,680,347	**Takeuchi; Ken** (Tokyo, **JP**), **Sakui; Koji** (Tokyo, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), ***Aritome; Seiichi*** (Yokohama, **JP**)	Nonvolatile semiconductor memory device	**21-Oct-97**
203	5,615,165	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Ota-Ku, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**25-Mar-97**
204	5,602,789	**Endoh; Tetsuo** (Sendai, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Ohuchi; Kazunori** (Yokohama, **JP**), **Kirisawa; Ryouhei** (Kitakami, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Tokyo, **JP**)	Electrically erasable and programmable non-volatile and multi-level memory systemn with write-verify controller	**11-Feb-97**
205	5,568,421	***Aritome; Seiichi*** (Kawasaki, **JP**)	Semiconductor memory device on which selective transistors are connected to a plurality of respective memory cell units	**22-Oct-96**
206	5,555,204	**Endoh; Tetsuo** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Shuto; Susumu** (Ichikawa, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Hemink; Gertjan** (Kawasaki, **JP**), **Tanzawa; Toru** (Ebina, **JP**)	Non-volatile semiconductor memory device	**10-Sep-96**
207	5,546,351	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Yokohama, **JP**), **Shirota; Riichiro** (Fujisawa, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Kawasaki, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo-To, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**13-Aug-96**
208	5,528,547	***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**)	Electrically erasable programmable read-only memory with electric field decreasing controller	**18-Jun-96**
209	5,469,444	**Endoh; Tetsuo** (Yokohama, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Ohuchi; Kazunori** (Yokohama, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Tokyo, **JP**)	Electrically erasable and programmable non-volatile memory system with write-verify controller using two reference levels	**21-Nov-95**
210	5,402,373	***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**)	Electrically erasable programmable read-only memory with electric field decreasing controller	**28-Mar-95**
211	5,397,723	**Shirota; Riichiro** (Kawasaki, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Nakayama; Ryozo** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), **Endoh; Tetsuro** (Yokohama, **JP**), **Watanabe; Shigeyoshi** (Yokohama, **JP**)	Process for forming arrayed field effect transistors highly integrated on substrate	**14-Mar-95**

212	5,386,422	**Endoh; Tetsuo** (Yokohama, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Ohuchi; Kazunori** (Yokohama, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Tokyo, **JP**)	Electrically erasable and programmable non-volatile memory system with write-verify controller using two reference levels	**31-Jan-95**
213	5,361,227	**Tanaka; Tomoharu** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Kato; Hideo** (Kawasaki, **JP**), **Nakai; Hiroto** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Tokyo, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Nakamura; Hiroshi** (Yokohama, **JP**), **Odaira; Hideko** (Machida, **JP**), **Okamoto; Yutaka** (Kawasaki, **JP**), **Asano; Masamichi** (Tokyo, **JP**), **Tokushige; Kaoru** (Yokohama, **JP**)	Non-volatile semiconductor memory device and memory system using the same	**1-Nov-94**
214	5,321,699	**Endoh; Tetsuo** (Yokohama, **JP**), **Shirota; Riichiro** (Kwasaki, **JP**), **Ohuchi; Kazunori** (Yokohama, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), **Tanaka; Yoshiyuki** (Tokyo, **JP**)	Electrically erasable and programmable non-volatile memory system with write-verify controller using two reference levels	**14-Jun-94**
215	5,293,337	***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Momodomi; Masaki** (Yokohama, **JP**)	Electrically erasable programmable read-only memory with electric field decreasing controller	**8-Mar-94**
216	5,179,427	**Nakayama; Ryozo** (Yokohama, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**), **Itoh; Yasuo** (Kawasaki, **JP**), **Kirisawa; Ryouhei** (Yokohama, **JP**), **Odaira; Hideko** (Tokyo, **JP**), **Momodomi; Masaki** (Yokohama, **JP**), **Iwata; Yoshihisa** (Yokohama, **JP**), **Tanaka; Tomoharu** (Yokohama, **JP**), ***Aritome; Seiichi*** (Kawasaki, **JP**), **Endoh; Tetsuo** (Yokohama, **JP**), **Masuoka; Fujio** (Yokohama, **JP**)	Non-volatile semiconductor memory device with voltage stabilizing electrode	**12-Jan-93**
217	5,172,198	***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**)	MOS type semiconductor device	**15-Dec-92**
218	5,031,011	***Aritome; Seiichi*** (Kawasaki, **JP**), **Shirota; Riichiro** (Kawasaki, **JP**)	MOS type semiconductor device	**9-Jul-91**

Japan Patents　（日本登録特許）

項番	公報番号	発明の名称	発明者	備考
1	特許4634973	半導体記憶装置	中村 寛、有留 誠一、今宮 賢一、大平 秀子、竹内 健、清水 和裕、成田 一仁	【登録日】平成22年11月26日（2010. 11. 26）
2	特許4599375	不揮発性半導体メモリ	渡部 浩、八重樫 利武、有留 誠一、清水 和裕、竹内 祐司	【登録日】平成22年10月1日（2010. 10. 1）
3	特許4550686	不揮発性半導体記憶装置	中村 寛、大平 秀子、今宮 賢一、竹内 健、有留 誠一	【登録日】平成22年7月16日（2010. 7. 16）
4	特許4439142	不揮発性半導体メモリの製造方法	有留 誠一	【登録日】平成22年1月15日（2010. 1. 15）
5	特許4284311	半導体記憶装置の製造方法	丸山 徹、ヘミンク・ゲルトヤン、渡部 浩、有留 誠一	【登録日】平成21年3月27日（2009. 3. 27）
6	特許4237344	半導体装置及びその製造方法	中村 卓矢、小井土 直樹、飯塚 裕久、成田 一仁、有留 誠一、荒井 史隆	【登録日】平成20年12月26日（2008. 12. 26）
7	特許4130494	不揮発性半導体メモリ	渡部 浩、八重樫 利武、有留 誠一、清水 和裕、竹内 祐司	【登録日】平成20年5月30日（2008. 5. 30）
8	特許3967409	半導体集積回路装置	有留 誠一	【登録日】平成19年6月8日（2007. 6. 8）
9	特許3959165	不揮発性半導体記憶装置	清水 和裕、有留 誠一	【登録日】平成19年5月18日（2007. 5. 18）
10	特許3940758	不揮発性半導体記憶装置	清水 和裕、有留 誠一	【登録日】平成19年4月6日（2007. 4. 6）
11	特許3914170	半導体記憶装置	有留 誠一	【登録日】平成19年2月9日（2007. 2. 9）
12	特許3906190	フラッシュメモリシステムおよびエラー訂正方法	田 中 智 晴、百 冨 正 樹、加 藤 秀 雄、中 井 弘 人、田 中 義 幸、白 田 理一郎、有 留 誠 一、伊 藤 寧 夫、岩 田 佳 久、中 村 寛、大 平 秀 子、岡 本 豊、浅 野 正 通、徳 重 芳	【登録日】平成19年1月19日（2007. 1. 19）
13	特許3905984	不揮発性半導体記憶装置	中村 寛、大平 秀子、今宮 賢一、竹内 健、有留 誠一	【登録日】平成19年1月19日（2007. 1. 19）
14	特許3895855	不揮発性半導体記憶装置	有留 誠一、清水 和裕	【登録日】平成18年12月22日（2006. 12. 22）
15	特許3895816	不揮発性半導体記憶装置とその制御方法、メモリカード、及び記憶システム	有留 誠一	【登録日】平成18年12月22日（2006. 12. 22）
16	特許3883534	不揮発性半導体記憶装置	田 中 智 晴、百 冨 正 樹、加 藤 秀 雄、中 井 弘 人、田 中 義 幸、白 田 理一郎、有 留 誠 一、伊 藤 寧 夫、岩 田 佳 久、中 村 寛、大 平 秀 子、岡 本 豊、浅 野 正 通、徳 重 芳	【登録日】平成18年11月24日（2006. 11. 24）
17	特許3878374	不揮発性半導体記憶装置	清水 和裕、白田 理一郎、有留 誠一、小井土 直樹、飯塚 裕久、角田 弘昭、井口 直、成田 一仁、寺坂 国博	【登録日】平成18年11月10日（2006. 11. 10）
18	特許3866586	半導体記憶装置	遠藤 哲郎、首藤 晋、有留 誠一	【登録日】平成18年10月13日（2006. 10. 13）
19	特許3853981	半導体記憶装置の製造方法	中村 寛、有留 誠一、今宮 賢一、大平 秀子、竹内 健、清水 和裕、成田 一仁	【登録日】平成18年9月15日（2006. 9. 15）
20	特許3764177	半導体記憶装置およびその製造方法	丸山 徹、ヘミンク・ゲルトヤン、渡部 浩、有留 誠一	【登録日】平成18年1月27日（2006. 1. 27）
21	特許3749891	記憶システム	田 中 智 晴、百 冨 正 樹、加 藤 秀 雄、中 井 弘 人、田 中 義 幸、白 田 理一郎、有 留 誠 一、伊 藤 寧 夫、岩 田 佳 久、中 村 寛、大 平 秀 子、岡 本 豊、浅 野 正 通、徳 重 芳	【登録日】平成17年12月9日（2005. 12. 9）
22	特許3725708	半導体装置	竹内 祐司、有留 誠一、白田 理一郎、村濱 優一郎、荒木 仁、梅村 政司、矢羽田 正光、池田 修	【登録日】平成17年9月30日（2005. 9. 30）
23	特許3710880	不揮発性半導体記憶装置	渡部 浩、清水 和裕、竹内 祐司、有留 誠一	【登録日】平成17年8月19日（2005. 8. 19）
24	特許3641103	不揮発性半導体メモリ装置の製造方法	神谷 栄二、有留 誠一	【登録日】平成17年1月28日（2005. 1. 28）
25	特許3602691	不揮発性半導体記憶装置およびその製造方法	清水 和裕、有留 誠一	【登録日】平成16年10月1日（2004. 10. 1）
26	特許3600393	半導体装置及びその製造方法	清水 和裕、渡部 浩、竹内 祐司、有留 誠一、渡辺 寿治	【登録日】平成16年9月24日（2004. 9. 24）
27	特許3586072	不揮発性半導体記憶装置	八重樫 利武、清水 和裕、有留 誠一	【登録日】平成16年8月13日（2004. 8. 13）
28	特許3585938	半導体装置	百瀬 寿代、有留 誠一、岩井 洋、森本 豊太、小野 瑞城	【登録日】平成16年8月13日（2004. 8. 13）
29	特許3583583	半導体装置及びその製造方法	渡部 浩、清水 和裕、有留 誠一、竹内 祐司	【登録日】平成16年8月6日（2004. 8. 6）
30	特許3540640	不揮発性半導体記憶装置	清水 和裕、佐藤 信司、有留 誠一	【登録日】平成16年4月2日（2004. 4. 2）
31	特許3532659	不揮発性半導体記憶装置	竹内 健、田中 智晴、有留 誠一、作井 康司	【登録日】平成16年3月12日（2004. 3. 12）
32	特許3519583	不揮発性半導体記憶装置およびその製造方法	清水 和裕、佐藤 信司、有留 誠一	【登録日】平成16年2月6日（2004. 2. 6）
33	特許3512976	不揮発性半導体記憶装置およびその製造方法	清水 和裕、成田 一仁、有留 誠一	【登録日】平成16年1月16日（2004. 1. 16）
34	特許3501405	不揮発性半導体装置の製造方法	杉前 紀久子、遠藤 哲郎、有留 誠一、白田 理一郎	【登録日】平成15年12月12日（2003. 12. 12）

35	特許3495337	メモリベリファイ回路	田中智晴、百冨正樹、加藤秀雄、中井弘人、田中義幸、白田理一郎、有留誠一、伊藤寧夫、岩田佳久、中村寛、大平秀子、岡本豊、浅野正通、徳重芳	【登録日】平成15年11月21日(2003. 11. 21)
36	特許3474857	メモリセルのメモリ状態変更方法および不揮発性半導体メモリ装置	田中智晴、百冨正樹、加藤秀雄、中井弘人、田中義幸、白田理一郎、有留誠一、伊藤寧夫、岩田佳久、中村寛、大平秀子、岡本豊、浅野正通、徳重芳	【登録日】平成15年9月19日(2003. 9. 19)
37	特許3474856	不揮発性半導体記憶装置	田中智晴、百冨正樹、加藤秀雄、中井弘人、田中義幸、白田理一郎、有留誠一、伊藤寧夫、岩田佳久、中村寛、大平秀子、岡本豊、浅野正通、徳重芳	【登録日】平成15年9月19日(2003. 9. 19)
38	特許3469362	半導体記憶装置	有留誠一	【登録日】平成15年9月5日(2003. 9. 5)
39	特許3450438	半導体装置	有留誠一、田中智晴	【登録日】平成15年7月11日(2003. 7. 11)
40	特許3441140	半導体記憶装置	遠藤哲郎、首藤晋、有留誠一	【登録日】平成15年6月20日(2003. 6. 20)
41	特許3410747	不揮発性半導体記憶装置	飯塚裕久、遠藤哲郎、有留誠一	【登録日】平成15年3月20日(2003. 3. 20)
42	特許3405567	不揮発性半導体記憶装置	有留誠一、渡部浩、遠藤哲郎、白田理一郎	【登録日】平成15年3月7日(2003. 3. 7)
43	特許3400130	不揮発性半導体記憶装置	佐藤信司、有留誠一、清水和裕	【登録日】平成15年2月21日(2003. 2. 21)
44	特許3400129	不揮発性半導体記憶装置	遠藤哲郎、有留誠一	【登録日】平成15年2月21日(2003. 2. 21)
45	特許3383429	不揮発性半導体記憶装置およびデータ書き込み方法	有留誠一、ヘミンク・ゲルトヤン、遠藤哲郎、田中智晴、白田理一郎	【登録日】平成14年12月20日(2002. 12. 20)
46	特許3383428	半導体記憶装置	首藤晋、ヘミンク・ゲルトヤン、遠藤哲郎、田中智晴、有留誠一、作井康司	【登録日】平成14年12月20日(2002. 12. 20)
47	特許3383427	不揮発性半導体装置	渡部浩、有留誠一、中村寛、田中智晴、遠藤哲郎、白田理一郎	【登録日】平成14年12月20日(2002. 12. 20)
48	特許3383404	半導体装置の製造方法	首藤晋、有留誠一、ヘミンク・ゲルトヤン、丸山徹、渡部浩	【登録日】平成14年12月20日(2002. 12. 20)
49	特許3382151	メモリシステムおよび記憶システム	田中智晴、百冨正樹、加藤秀雄、中井弘人、田中義幸、白田理一郎、有留誠一、伊藤寧夫、岩田佳久、中村寛、大平秀子、岡本豊、浅野正通、徳重芳	【登録日】平成14年12月20日(2002. 12. 20)
50	特許3382024	不揮発性半導体記憶装置及びその製造方法	ヘミンク・ゲルトヤン、有留誠一	【登録日】平成14年12月20日(2002. 12. 20)
51	特許3378386	半導体記憶装置	丸山徹、中村寛、田中智晴、有留誠一、遠藤哲郎	【登録日】平成14年12月6日(2002. 12. 6)
52	特許3362970	不揮発性半導体記憶装置及びその製造方法	山口哲哉、丸山徹、有留誠一	【登録日】平成14年10月25日(2002. 10. 25)
53	特許3354418	半導体記憶装置	竹内祐司、清水和裕、渡部浩、有留誠一、渡辺寿治	【登録日】平成14年9月27日(2002. 9. 27)
54	特許3308727	半導体装置の製造方法	首藤晋、遠藤哲郎、有留誠一	【登録日】平成14年5月17日(2002. 5. 17)
55	特許3238576	不揮発性半導体記憶装置	有留誠一、田中智晴、竹内健	【登録日】平成13年10月5日(2001. 10. 5)
56	特許3228996	不揮発性半導体記憶装置	有留誠一、遠藤哲郎、白田理一郎、田中智晴	【登録日】平成13年9月7日(2001. 9. 7)
57	特許3226589	不揮発性半導体記憶装置の製造方法	有留誠一、遠藤哲郎、白田理一郎	【登録日】平成13年8月31日(2001. 8. 31)
58	特許3210373	不揮発性半導体記憶装置	白田理一郎、桐沢亮平、中山良三、有留誠一、遠藤哲郎	【登録日】平成13年7月13日(2001. 7. 13)
59	特許3207354	不揮発性半導体記憶装置	田中智晴、百冨正樹、加藤秀雄、中井弘人、田中義幸、白田理一郎、有留誠一、伊藤寧夫、岩田佳久、中村寛、大平秀子、岡本豊、浅野正通、徳重芳	【登録日】平成13年7月6日(2001. 7. 6)
60	特許3192861	不揮発性半導体記憶装置	有留誠一	【登録日】平成13年5月25日(2001. 5. 25)
61	特許3152756	不揮発性半導体記憶装置	有留誠一、遠藤哲郎、田中智晴、白田理一郎	【登録日】平成13年1月26日(2001. 1. 26)
62	特許3152720	不揮発性半導体記憶装置	遠藤哲郎、白田理一郎、大内和則、田中義幸、桐澤亮平、有留誠一、田中智晴、百冨正樹	【登録日】平成13年1月26日(2001. 1. 26)
63	特許3104978	不揮発性半導体記憶装置の制御方法	有留誠一、白田理一郎、桐澤亮平	【登録日】平成12年9月1日(2000. 9. 1)
64	特許3099887	不揮発性半導体記憶装置	有留誠一、白田理一郎、百冨正樹、岩田佳久、桐澤亮平	【登録日】平成12年8月18日(2000. 8. 18)
65	特許3029297	半導体記憶装置	有留誠一、桐沢亮平、中山良三、遠藤哲郎、白田理一郎、井上千佳	【登録日】平成12年2月4日(2000. 2. 4)
66	特許2957586	不揮発性メモリセルの製造方法	大平秀子、中山良三、白田理一郎、桐澤亮平、遠藤哲郎、有留誠一、舛岡富士雄	【登録日】平成11年(1999)7月23日
67	特許2944104	不揮発性半導体記憶装置	中山良三、白田理一郎、伊藤寧夫、桐澤亮平、大平秀子、百冨正樹、岩田佳久、田中智晴、有留誠一、遠藤哲郎、舛岡富士雄	【登録日】平成11年(1999)6月25日
68	特許2904498	不揮発性半導体メモリ装置およびその製造方法	有留誠一、桐沢亮平、白田理一郎	【登録日】平成11年(1999)3月26日

69	特許2885412	不揮発性半導体メモリ装置	有留 誠一、桐沢 亮平、白田 理一郎、中山 良三、百冨 正樹、伊藤 寧夫、岩田 佳久、遠藤 哲郎、田中 智晴、舛岡 富士雄	【登録日】平成11年（1999）2月12日
70	特許2877463	不揮発性半導体記憶装置	有留 誠一	【登録日】平成11年（1999）1月22日
71	特許2818202	不揮発性半導体記憶装置	桐澤 亮平、白田 理一郎、有留 誠一、舛岡 富士雄、	【登録日】平成10年（1998）8月21日
72	特許2818190	不揮発性半導体記憶装置およびその製造方法	井上 聡、桐澤 亮平、中山 良三、白田 理一郎、有留 誠一、百冨 正樹、岩田 佳久、舛岡 富士雄	【登録日】平成10年（1998）8月21日
73	特許2809802	不揮発性半導体記憶装置	有留 誠一、白田 理一郎、舛岡 富士雄	【登録日】平成10年（1998）7月31日
74	特許2772020	MOS型半導体装置	有留 誠一、白田 理一郎	【登録日】平成10年（1998）4月17日
75	特許2718716	不揮発性半導体メモリ装置およびそのデータ書替え方法	桐澤 亮平、白田 理一郎、中山 良三、有留 誠一、舛岡 富士雄、百冨 正樹、伊藤 寧夫	【登録日】平成9年（1997）11月14日
76	特許2647321	不揮発性半導体記憶装置及びこれを用いた記憶システム	田中智晴、百冨正樹、加藤秀雄、中井弘人、田中義幸、白田理一郎、有留誠一、伊藤寧夫、岩田佳久、中村寛、大平秀子、岡本豊、浅野正通、徳重芳	【登録日】平成9年（1997）5月9日