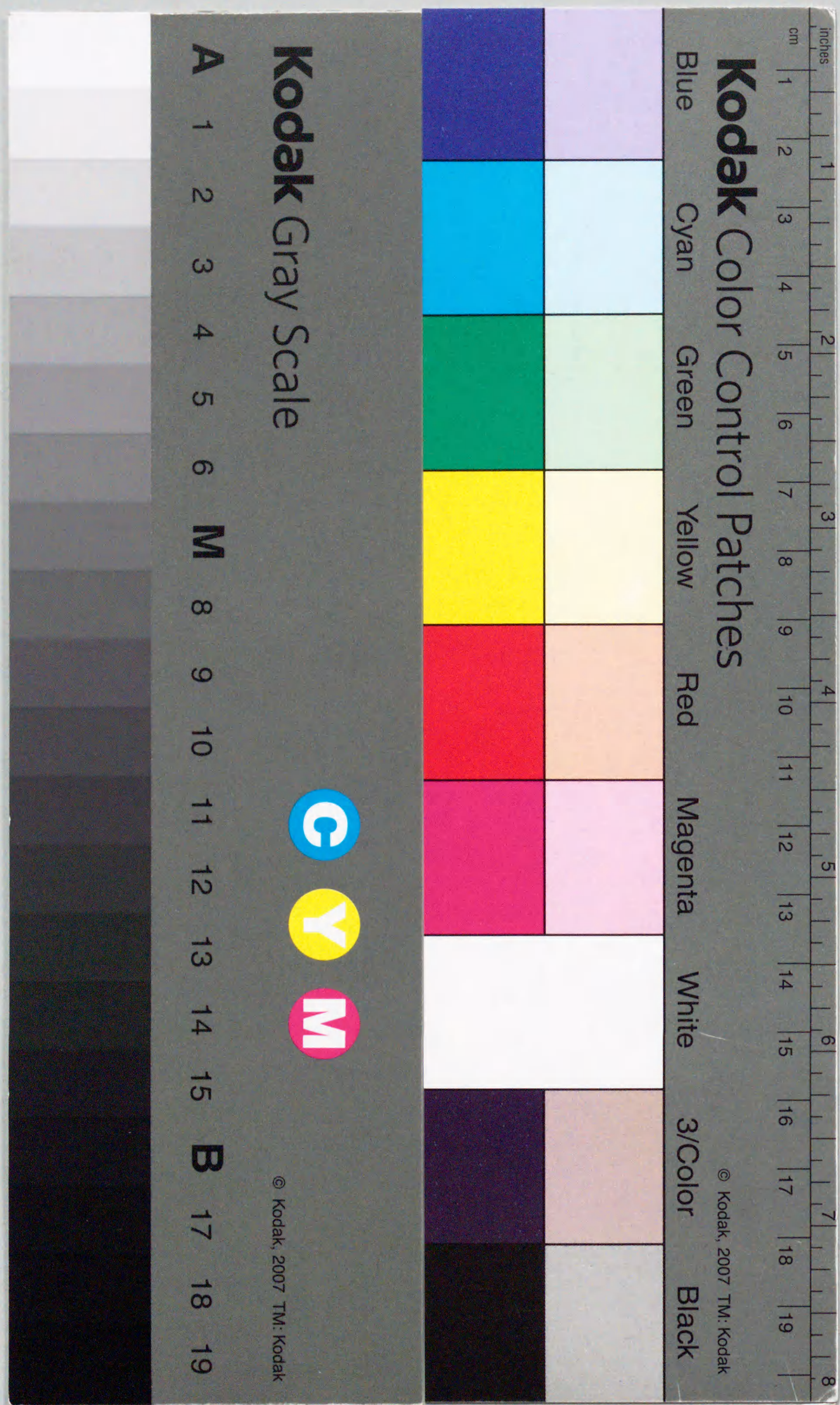

Investigation of thin-film polycrystalline silicon for solar cells by a new solid phase crystallization method

February 1994

Takao MATSUYAMA

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Acknowledgement

1. Introduction

1.1 History of solar cells

In 1954, the first solar cell using crystalline silicon (c-Si) was developed by Chapin, Fuller, and Pearson of Bell Telephone Laboratories,[1] and a conversion efficiency of 6% was soon obtained. In 1958, the U. S. Vanguard space satellite used c-Si solar cells to power its radio. The cells worked so well that solar cells were soon recognized as an effective power source for space operations. As for terrestrial applications of solar cells, numerous products have been over the last 30 years for commercial use. This is because photovoltaic conversion of solar energy into electricity provides an abundant, clean, and relatively homogeneously distributed source of energy compared with oil resources. Solar cells themselves require no fuel, and therefore, there is no pollution from exhaust gases. In addition, as solar cells do not have moving parts, they are silent in operation, and their lifetime is long.

c-Si and polycrystalline silicon (poly-Si) solar cells are the most popular cells at present, but, their cost is so high that they cannot compete with conventional energy sources such as thermal-power generation. The main reason for the expensiveness of c-Si and poly-Si solar cells is their fabrication process. A high temperature is required in the processes of crystal growth and junction formation. The necessity of slicing and polishing also causes loss of materials. In addition, because a semiconductor layer serves as the substrate, thickness of c-Si and poly-Si used in solar cells is as thick as 300μm, which also increases the cost. Therefore, expensive c-Si and poly-Si solar cells have been utilized in restricted applications, such as satellites, lighthouses, and so on.

Amorphous silicon (a-Si) films are also good candidates for a solar cell material. Since Spear and LeComber succeeded in the valency control of hydrogenated a-Si deposited by a glow discharge method with silane (SiH_4) in 1975,[2] a-Si films have been gathering much attention as a low-cost solar cell material. Their fabrication temperature is low, the amount of material required is small due to their high optical absorption coefficient, and they can utilized low-cost substrates. The conversion efficiency of a-Si solar cells has increased gradually, and presently reaching 12 % for a single junction a-Si solar cell with a size of 10 cm x 10 cm,[3] 10.05 % for a tandem type a-Si/a-Si solar cell with a size of

30 cm x 40 cm[4] and 13.7 % for a three-stack type a-Si/a-Si/amorphous silicon germanium (a-SiGe) solar cell with a size of 0.25 cm^2 .[5] But a-Si films show a light-induced degradation,[6] which becomes a large problem for a-Si solar cells in outdoor use. There are many reports on the origin of this light-induced degradation,[7-10] but it has not yet been resolved.

Recently, thin-film poly-Si has gathered considerable attention as a solar cell material which does not exhibit the light-induced degradation of a-Si and offers high photosensitivity in the long wavelength region of more than 800 nm, where a-Si films have no photosensitivity. There is also a report on a solar cell with a high theoretical conversion efficiency of 29 %, in spite of a thickness of only 10 μm.[11] But it presents a problem from the viewpoint of mechanical strength when slicing thick poly-Si and c-Si to a thickness of less than 100 μm. So, it is necessary to prepare thin-film poly-Si or c-Si on substrates in order to fabricate solar cells with high conversion efficiency and low cost. To lower the cost of solar cells, substrates such as glass, stainless steel, and so on, should be used.

1.2 Conventional fabrication method of thin-film polycrystalline silicon for solar cells

A number of methods are used to fabricate thin-film poly-Si on substrates for solar cells, such as chemical vapour deposition (CVD)[12, 13] and dipping.[14] In the CVD method, gases such as chlorosilane (SiH_nCl_{4-n} (n:0, 1, 2)) and monosilane (SiH_4) are used as a source gas and the film is deposited onto substrates by the thermal decomposition of the source gas in a reaction chamber, as shown in Figure 1.2-1. The substrates are set onto a susceptor heated by a R.F. coil and the typical substrate temperature is about 1100 °C. The deposition rate of the films is on the order of 1 μm/min. at this temperature. It is difficult to apply the films deposited on substrates to good active layers in solar cells, because of their very small grain. In general, the films after deposition are treated by thermal annealing again to increase their grain size. Figure 1.2-2 shows the principal of the dipping method. In this method, a substrate such as graphite is introduced into liquid silicon, and poly-Si films are fabricated by pulling up the graphite at a speed of a few cm/min. The thickness of the poly-Si is 100 μm.

Concerning junction formation, homojunctions and heterojunctions have been investigated. The fabrication methods for homojunctions use the diffusion[15] of phosphorus (P) and boron (B), and the ion implantation[16] of P ions (P^+) and B ions (B^-) into poly-Si. Heterojunctions are fabricated by depositing a-Si[17] or microcrystalline silicon (μc-Si)[18] onto poly-Si.

Conventional fabrication methods require a high-temperature process of more than 1000 °C. So the materials that can be used as the substrate are limited. Cheap substrates, such as glass and stainless steel, can not be used because the melting points of these substrates are lower than 1000 °C. Therefore, conventional fabrication methods do not suit the preparation of thin-film poly-Si for low-cost solar cells.

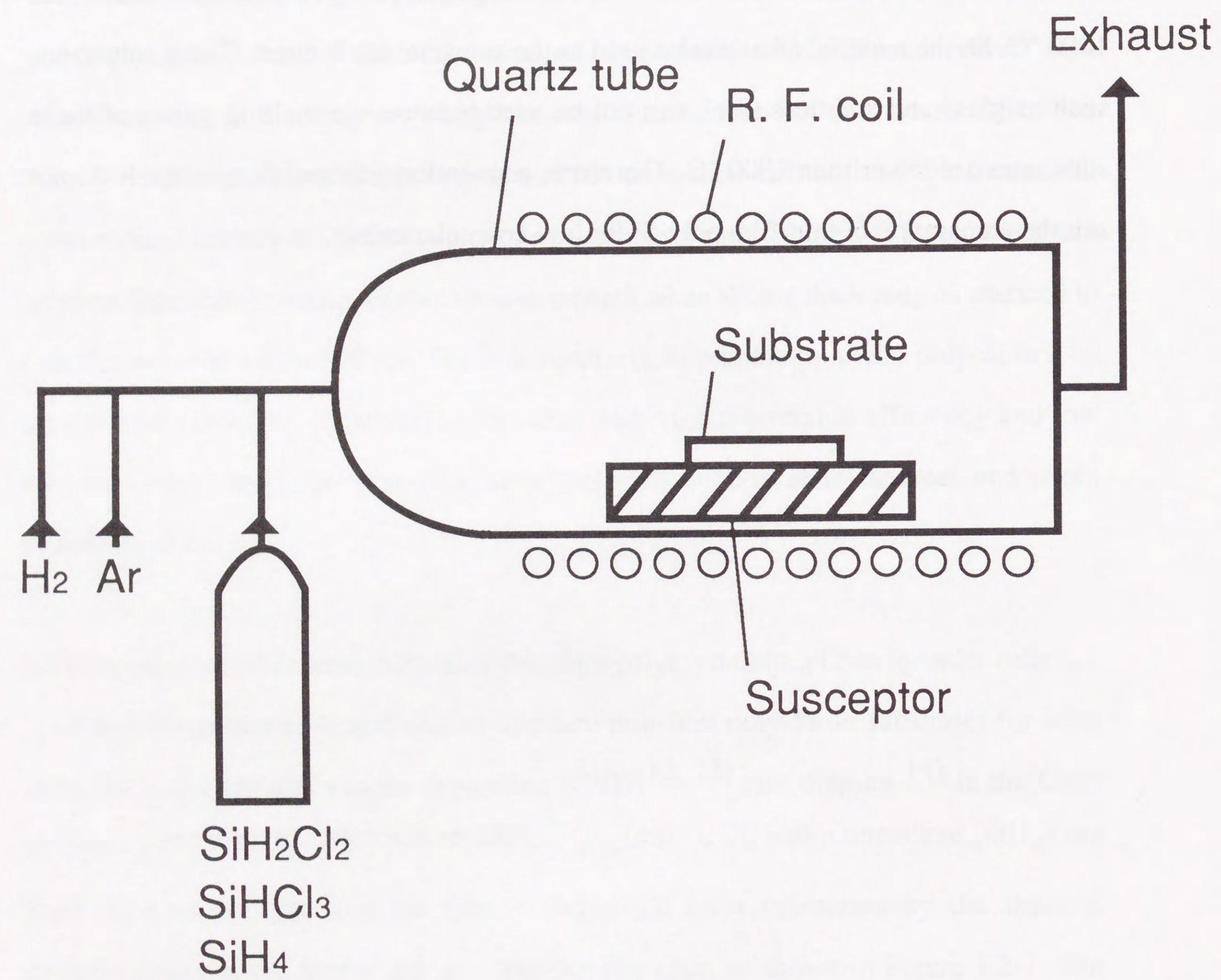


Fig. 1.2-1 A conventional CVD apparatus for the preparation of thin-film poly-Si.

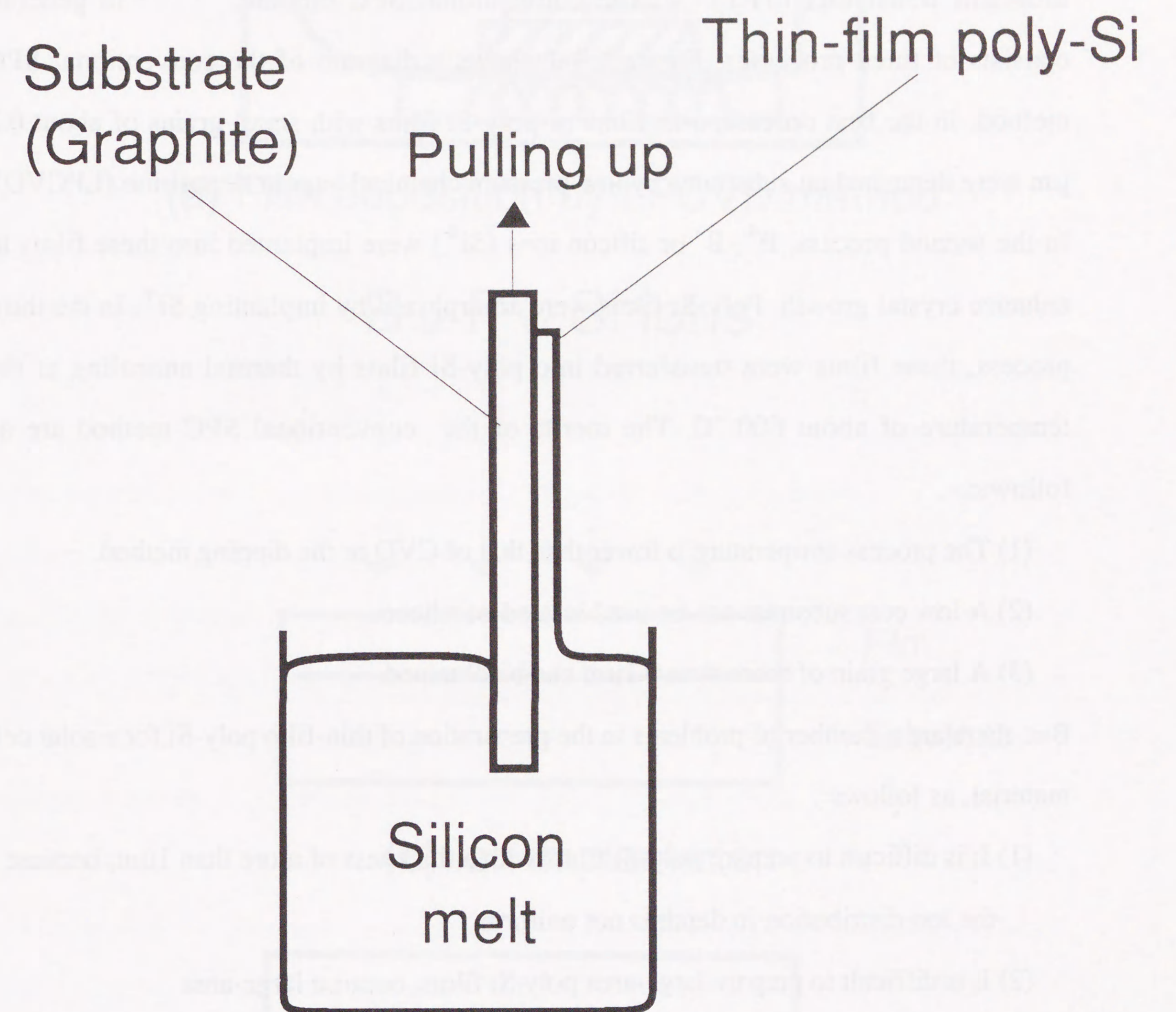


Fig. 1.2-2 The principal of dipping method.

1.3 Solid phase crystallization method

One of the methods for fabricating thin-film poly-Si at the low temperature of about 600°C is the solid phase crystallization (SPC) method. Thin-film poly-Si prepared by the conventional SPC method has a thickness of less than 0.5 µm and has been applied to thin-film transistors (TFT).[19] The conventional SPC method,[20, 21] in general, consists of three processes. Figure 1.3-1 shows a diagram of the conventional SPC method. In the first process, a-Si films or poly-Si films with small grains of about 0.2 µm were deposited on substrates by low pressure chemical vapour deposition (LPCVD). In the second process, P^+, B^- or silicon ions (Si^+) were implanted into these films to enhance crystal growth. Poly-Si films were amorphized by implanting Si^+. In the third process, these films were transferred into poly-Si films by thermal annealing at the temperature of about 600 °C. The merits of the conventional SPC method are as follows:.

(1) The process temperature is lower than that of CVD or the dipping method.

(2) A low cost substrate can be used instead of silicon.

(3) A large grain of more than 0.1µm can be obtained.

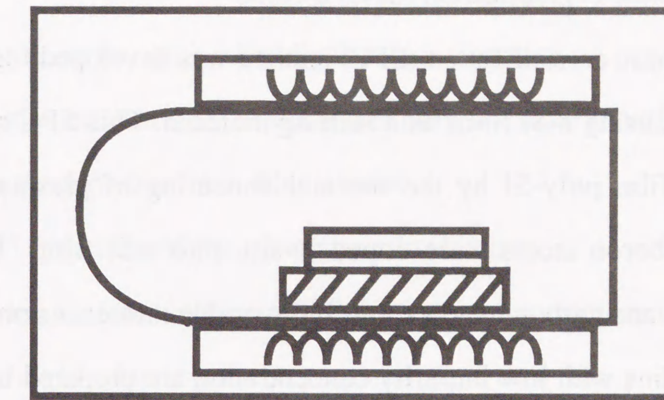
But, there are a number of problems in the preparation of thin-film poly-Si for a solar cell material, as follows:.

(1) It is difficult to prepare poly-Si films with a thickness of more than 1µm, because the ion distribution in depth is not uniform.

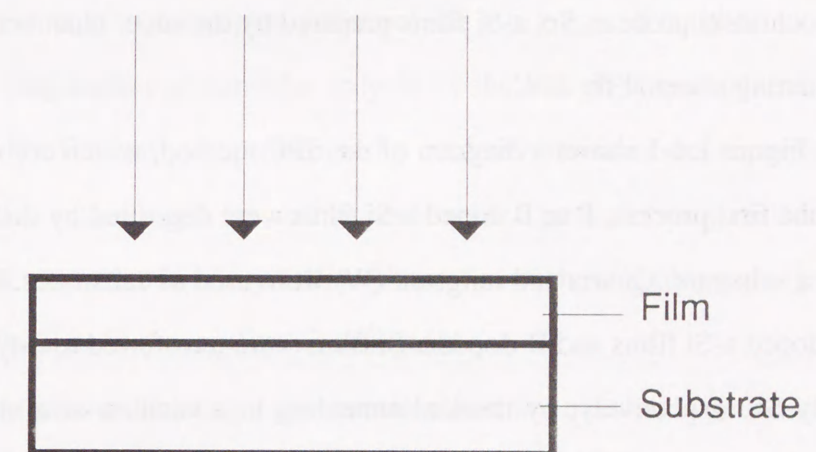
(2) It is difficult to prepare large-area poly-Si films, because large-area implantation is not so easy.

(3) The process is complicated.

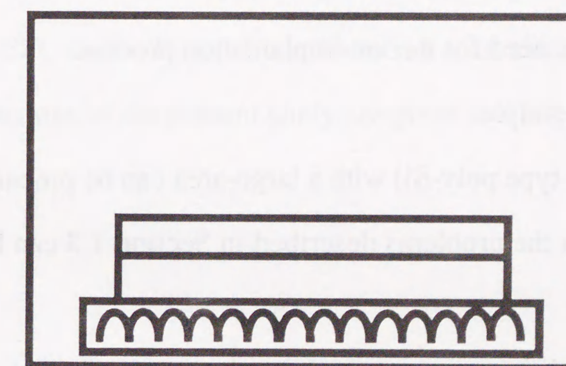
There are no reports on solar cells using poly-Si films prepared by the conventional SPC method. So, to resolve these problems and to apply poly-Si films prepared by the SPC method to solar cells, a new SPC method must be developed, while maintaining the merits of the low-temperature process.



(a) Film deposition by LPCVD method



(b) Ion implantation



(c) Thermal annealing

Fig. 1.3-1 Diagram of the conventional SPC method.

1.4 A new solid phase crystallization (SPC) method

A new solid phase crystallization (SPC) method was developed for the preparation of thin-film poly-Si, using a-Si films as a starting material. This SPC method is a way of fabricating thin-film poly-Si by the thermal annealing of plasma-CVD a-Si films. Phosphorus and boron atoms were doped in-situ into a-Si films. Impurities such as oxygen, nitrogen, and carbon have various unfavorable influences on the crystallization of silicon. a-Si films with low impurity concentration are prepared by a super chamber method.[22)] The impurity concentrations of oxygen, nitrogen and carbon are $2x10^{18}$ cm^{-3}, $1x10^{17}$ cm^{-3} and $2x10^{18}$ cm^{-3}, respectively, in the a-Si films fabricated using the super chamber. This oxygen concentration is almost the same as that in c-Si made by the Czochralski process. So, a-Si films prepared by the super chamber method were used as a starting material for SPC.

Figure 1.4-1 shows a diagram of the SPC method, which consists of two processes. In the first process, P or B doped a-Si films were deposited by the plasma-CVD method on a substrate. Quartz and tungsten (W) were used as substrates. In the second process, P-doped a-Si films and B-doped a-Si films were transferred to n-type poly-Si and p-type poly-Si, respectively, by thermal annealing in a vacuum or a nitrogen atmosphere at various temperatures. The typical annealing temperature is 600 °C. This SPC method has three main features:

(1) Impurities (phosphorus or boron atoms) are doped in-situ into a-Si as a starting material, without the need for the ion implantation process.

(2) The process is very simple.

(3) n-type poly-Si (or p-type poly-Si) with a large-area can be prepared.

So, it is recognized that the problems described in Section 1.3 can be resolved by a new SPC method.

The following conditions are required for the preparation of thin-film poly-Si on substrates instead of silicon:

(1) There must be no chemical reaction between the substrate materials and the silicon at the process temperature, and the silicon atoms must adhere to the substrates.

(2) The coefficient of thermal expansion of the substrate materials must fit that of the silicon.

(3) A flat surface must be obtained easily for the substrates.

(4) The composition elements of the substrates must not have an unfavorable influence on the growth of thin-film silicon.

(5) The electrical resistivity of the substrates must be low.

Table 1.4-1 shows the materials which fulfill the required conditions of (1) - (5). A new SPC method is a way of adapting to the preparation of thin-film poly-Si on substrates other than silicon, because the quartz and W substrates used in the new SPC method satisfy these conditions. Quartz and W can also be changed to glass and W-coated stainless-steel, respectively.

The purpose of this work is to develop thin-film poly-Si as a solar cell material.

In Chapter 2, the preparation of thin-film poly-Si by the new SPC method and the improvement of the thin-film poly-Si properties by nucleation control are reported. I propose three innovative technologies for nucleation control: a partial doping method, a textured substrate, and a seed made of crystalline phase. For each technology, the grain size and Hall mobility of thin-film poly-Si are investigated.

Chapter 3 describes solar cells using a new junction formation technology and solar cells applying this new junction formation technology to thin-film poly-Si prepared by the new SPC method. The junction fabrication method, in which the process temperature was below 200 °C, was developed for solar cells using a-Si and c-Si. Thin-film poly-Si prepared by the new SPC method was also analyzed in solar cells.

Finally, the conclusions of the present study are given in Chapter 4.

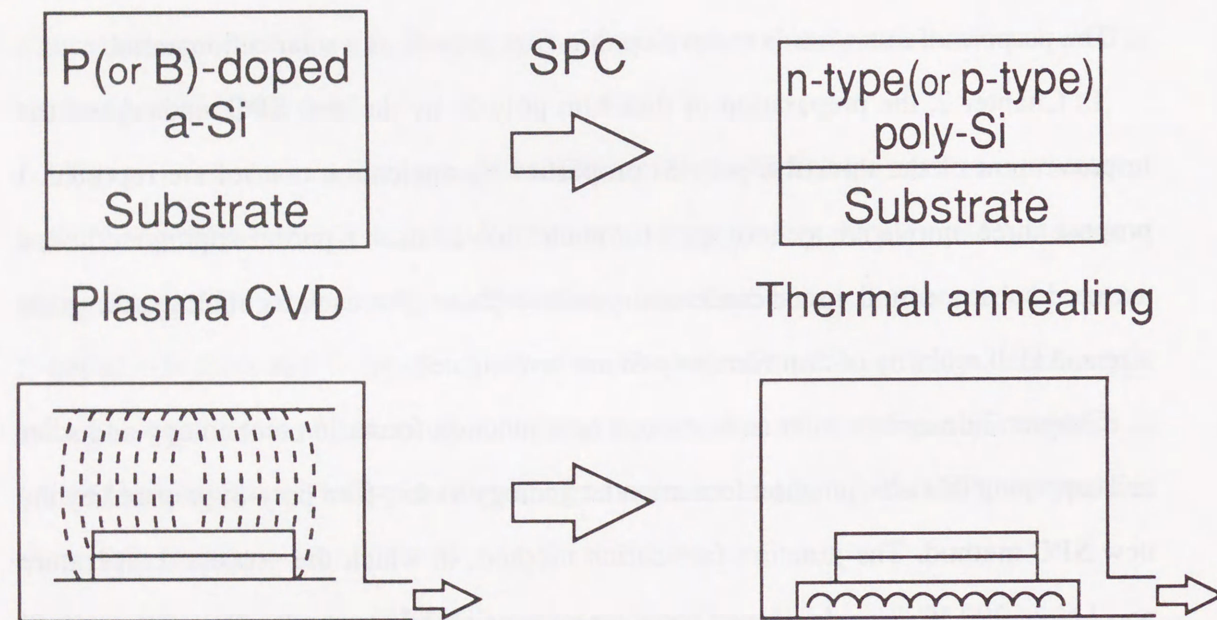


Fig. 1.4-1 Diagram of the SPC method consisting of two processes.

Table 1.4-1 The properties of various substrates

Materials	Coefficient of thermal expansion	Other properties
Si	2.6 (×10^{-6}°C)	Melting point: 1417°C
Ta	6.6	Melting point: 3007°C
Mo	3.7 - 5.3	Melting point: 2608°C
W	6.0	Melting point: 3380°C
C(Graphite)	2.0 - 2.4	Pore ratio : 1 - 3%
SiO_2 (Quartz)	0.4	----------
Al_2O_3	7.8	Heat-resistance temperature : 1750°C

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2 Theoretical background

2.1 Introduction

In order to investigate polycrystalline silicon (poly-Si), it is necessary to study kinetics of growth and carrier transport.

As for growth process, many phase transformations occur by nucleation and growth. In classical theory, it is proposed that clusters of atoms in the configuration of the transformation product arise in the original material. Initially, the clusters are small and consequently unstable because of their high surface-to-volume ratio. Eventually, however, some clusters grow to a size beyond which they are stable, i.e., they become nuclei. At constant temperature, a constant rate of production of nuclei will be established. In section 2.2, transient time, nucleation rate, and growth rate, which have much influence on grain size of poly-Si, are discussed.

The electrical properties of poly-Si films have been interpreted in terms of two distinct models: the segregation theory, [1, 2] according to which impurity atoms tend to segregate at the grain boundary where they are electrically inactive, and the grain boundary trapping theory[3, 4] assuming the presence of a large amount of trapping states at the grain boundary able to capture, and therefore immobilize, free carriers. These charged states at the grain boundary create potential barriers, which oppose the passage of carriers from a grain to the neighboring ones.

The basic limitation of the segregation model is that it does not explain the temperature dependence of the film resistivity. On the other hand, a theory combining the grain-boundary trapping model with a thermionic-emission mechanism through the barriers can explain most of electrical properties of poly-Si film. So, in section 2.3, this theory is described.

The p-n junctions are of supreme importance both in the modern electronic applications and in the understanding of other semiconductor devices. The p-n junction theory serves as the foundation of the physics of semiconductor devices. The basic theory of current-voltage characteristics of p-n junction was established by Shockley.[5] This theory was then extended by Sah et al.[6] and by Moll.[7] So, section 2.4 mentions the theory which is basis of device physics.

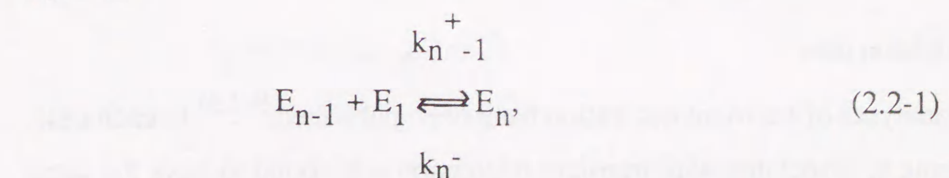
2.2 Solid phase crystallization

Crystalline silicon growth in solid phase consists of two processes such as nucleation and growth. It is necessary to study the theory of nucleation and growth. According to classical theory, microcrystallites (containing only a few atoms) will nucleate frequently. Because of a large surface-to-volume ratio, these tend to shrink. From thermodynamic considerations, however, a few will become large enough that further growth is energetically favorable. Growth in the microcrystalline regime occurs by the same basic mechanism as growth in the macrocrystalline regime: The rate at which each atom at an amorphous-crystalline interface makes a transition between the amorphous state and the crystalline state is a function of the energy levels of the two states. Growth is energetically favorable when the free energy of the system is lowered by the transition of an interface atom from the amorphous to the crystalline state.

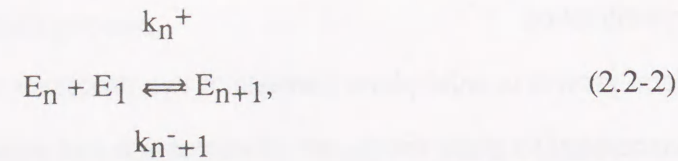
The free energy of formation of a cluster of size n consists of two components: the Gibbs-free-energy difference between crystalline and amorphous phases (proportional to volume, or n) and the energy required to maintain the amorphous-crystalline interface (proportional to surface area or $n^{2/3}$). The Gibbs-free-energy difference between the amorphous and crystalline phases is denoted as g and is in units of eV/atom. It is taken to be positive. That is, the energy of each atom in the cluster is lower than the energy of an atom in the amorphous phase by g.

At small cluster sizes, the interfacial energy outweighs the energy difference due to the phase change−the net free energy of formation ΔG_n is positive. The maximum free energy of formation, denoted $\Delta G_n{}^*$, occurs at the critical cluster size n^* and enters into the temperature dependence of the steady-state nucleation rate r_n as mentioned the later.

The forward reaction rate is the rate that a cluster grows from n to n+1 atoms, and the reverse reaction rate is the rate that a cluster shrinks from n+1 to n atoms as following equations:



$$E_{n-1} + E_1 \underset{k_n^-}{\overset{k_{n-1}^+}{\rightleftharpoons}} E_n, \qquad (2.2\text{-}1)$$



where E_n represents a cluster of n molecules and E_1 a single molecule. k_n^+ is the rate of addition of molecules to a cluster E_n, and k_n^- is the rate of loss of molecules from E_n. These rates are found by defining an unbiased atomic jump frequency υ at the amorphous-crystalline interface. Furthermore, since υ is probably closely related to the jump rate in the amorphous phase, it can be characterized by the activation energy of self-diffusion in amorphous silicon E_d:

$$\upsilon \propto \exp(-E_d/kT), \qquad (2.2\text{-}3)$$

where k is Boltzmann's constant, T is absolute temperature. Since all reaction rates are proportional to υ, E_d is the activation energies for transient time τ_0, steady-state nucleation rate r_n, and growth velocity v_g.

The reaction rates are also proportional to the number of atoms at the cluster surface and may be written in the following form:

$$k_{n-n+1} \propto n^{2/3}\exp(-E_d/kT) \times \exp[(\Delta G_{n+1}-\Delta G_n)/2kT],$$

$$k_{n+1-n} \propto n^{2/3}\exp(-E_d/kT) \times \exp[(\Delta G_n-\Delta G_{n+1})/2kT]. \qquad (2.2\text{-}4)$$

A complete analysis of the reaction rates [Eq.(2.2-4)] and ΔG_n (described above) provides values for transient time, nucleation rate, and growth velocity within the scope of classical theory. The respective activation energies, as shown below, are related to ΔG_n^*, g, and E_d. The transient time is the effective time to reach a steady-state nucleation rate from the initial conditions (no clusters). At steady state the number of clusters N_n of each cluster size n is time independent, and the net forward reaction rate ($N_n k_{n-n+1} - N_{n+1}k_{n+1-n}$) is equal to the steady-state nucleation rate r_n for all n. Growth velocity is obtained from the net forward reaction rate for a large cluster.

(1) Transient nucleation time

A number of analyses of transient nucleation have been published.[9-13] In each case, a characteristic time τ_t associated with transient nucleation was found to have the same

temperature dependence. By assuming that the free energy of formation is a weak function of temperature, the form is

$$\tau_t \propto T/k_n^*, \qquad (2.2\text{-}5)$$

where k_n^* is the forward (or reverse) reaction rate at the critical cluster size. From Eq.(2.2-4),

$$k_n^* \propto n^{2/3}\exp(-E_d/kT). \qquad (2.2\text{-}6)$$

Kashchiev's theoretical results,[13] which are in good agreement with experiment, indicate that τ_0 is proportional to τ_t:

$$\tau_0 \propto T\exp(E_d/kT). \qquad (2.2\text{-}7)$$

(2) Nucleation rate

The theoretical temperature dependence of the steady-state nucleation rate r_n[14] is

$$r_n \propto \upsilon \cdot \exp(-\Delta G_n^*/kT). \qquad (2.2\text{-}8)$$

Since the unbiased atomic jump frequency υ is proportional to $1/\tau_0$, using Eq.(2.2-7), one obtaines

$$r_n \propto (1/T)\cdot\exp[-(E_d+\Delta G_n^*)/kT]. \qquad (2.2\text{-}9)$$

(3) Growth rate

The growth rate can be found from the net forward reaction rate for a large cluster. Addition of one atom to a large cluster will not significantly change the surface energy. The change in free energy, then, is -g. From Eq.(2.2-4), by assuming g>>2kT,

$$dn/dt = k_{n-n+1} - k_{n+1-n}$$

$$\propto n^{2/3}\exp(-E_d/kT) \times [\exp(g/2kT)-\exp(-g/2kT)]$$

$$\propto n^{2/3}\exp[-(E_d-g/2)/kT]. \qquad (2.2\text{-}10)$$

Because n is proportional to the radius cubed (r^3), Eq.(2.2-10) is easily solved for v_g (=dr/dt):

$$v_g \propto \exp[-(E_d-g/2)/kT]. \qquad (2.2\text{-}11)$$

2.3 Transport of polycrystalline silicon films

A polycrystalline material is composed of small crystallites joined together by grain boundaries. Inside of each crystallite, the atoms are arranged in a periodic manner so that it can be considered as a small single crystal. The grain boundary is a complex structure, usually consisting of a few atomic layers of disordered atoms. It is important to consider the effects of the grain boundary on the electrical properties for discussing the transport of polycrystalline semiconductors. Seto considered that carrier trapping at the grain boundary governed the electrical transport properties of polycrystalline films.[15] In a real polycrystalline material, the crystallites have a distribution of sizes and irregular shapes. In order to simplify the model, following assumptions were used:

(1) Poly-Si is composed of identical crystallites having a grain size of L cm.

(2) Only one type of impurity atom presents, and the impurity atoms are totally ionized and uniformly distributed with a concentration of N cm^{-3}.

(3) The grain boundary is of negligible thickness compared to L and contains N_t cm^{-2} of traps located at energy E_t with respect to the intrinsic Fermi level.

Using these assumptions, an abrupt depletion approximation is used to calculate the energy band diagram in the crystallites. In Figure 2.3-1, all the mobile carriers in a region of (L/2-l) cm from the grain boundary are trapped by the trapping states, resulting in a depletion region. Using the above approximation, Poisson's equation becomes

$$d^2V/dx^2 = qN/\varepsilon, \qquad l < x < L/2, \qquad (2.3\text{-}1)$$

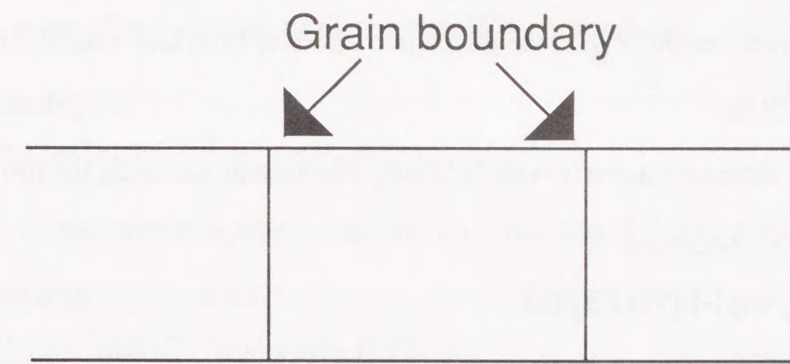
where ε is the dielectric permittivity of poly-Si. Integrating Eq.(2.3-1) twice and applying the boundary conditions that V(x) is continuous and dV/dx is zero at x=l gives

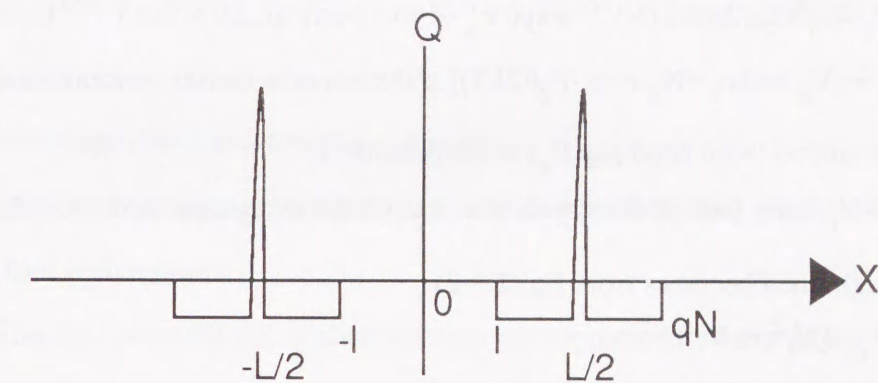
$$V(x)=(qN/2\varepsilon)(x-l)^2+V_{v0}, \qquad l < x < L/2, \qquad (2.3\text{-}2)$$

where V_{v0} is the potential of the valence band edge at the center of the crystallite. In this calculation, the intrinsic Fermi level is taken to be at zero energy and energy is positive towards the valence band. There exist two possible conditions depending on the doping concentration: (a) $LN<N_t$, and (b) $LN>N_t$.

Under $LN<N_t$ condition, the crystallite is completely depleted of carriers and the traps are partially filled, so that l=0 and Eq.(2.3-2) becomes

$$V(x)=(qN/2\varepsilon)x^2+V_{v0}, \qquad x \le L/2. \qquad (2.3\text{-}3)$$





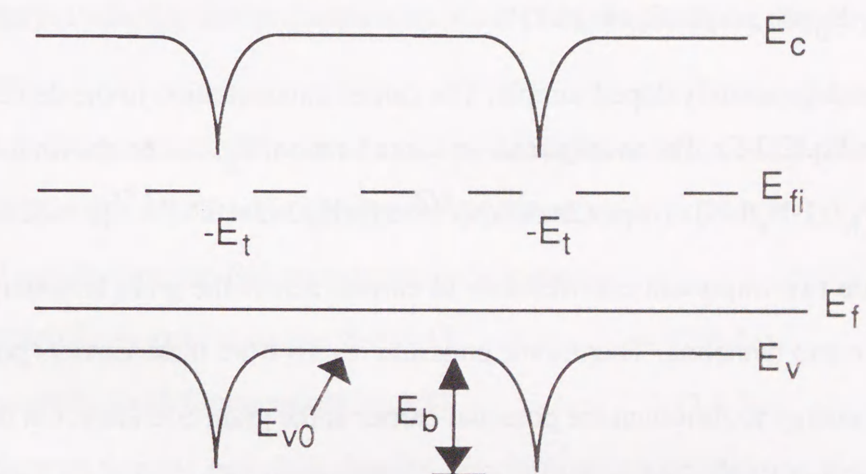


Fig. 2.3-1 (a) Model for the crystal structure of poly-Si films. (b) The charge distribution within the crystallite and at the grain boundary. (c) The energy band structure for poly-Si crystallites.

The potential barrier height, V_B, is the difference between V(0) and V(L/2), i.e.,

$$V_B=qL^2N/8\varepsilon \qquad (2.3\text{-}4)$$

showing that V_B increases linearly with N. Using Boltzmann statistics, the mobile carrier concentration, p(x), becomes

$$p(x)=N_V \exp\{-[qV(x)-E_f]/kT\}, \qquad (2.3\text{-}5)$$

where N_V is the density of states and E_f is the Fermi level. The average carrier concentration, P_a, is obtained by integrating Eq.(2.3-5) from -L/2 to L/2 and dividing by the grain size. The result is

$$P_a=(n_i/Lq)(2\pi\varepsilon kT/N)^{1/2}\cdot\exp[(E_B+E_f)/kT]\cdot\mathrm{erf}[(qL/2)(N/2\varepsilon kT)^{1/2}], \qquad (2.3\text{-}6)$$

where $E_B=qV_B$ and $n_i=N_V \exp[-E_g/(2kT)]$ is the intrinsic carrier concentration of single-crystalline silicon (with band gap E_g) at temperature T.

If $LN>N_t$, only part of the crystallite is depleted of carriers and l>0. The potential barrier height then becomes from Eq.(2.3-2)

$$V_B=qN_t^2/8\varepsilon N. \qquad (2.3\text{-}7)$$

The average carrier concentration, P_a, is obtained by averaging over the crystallite. In the undepleted region, the carrier concentration, P_b, is the same as that of a doped single-crystalline silicon,

$$P_b=N_V \exp[-(E_{v0}-E_f)/kT] \qquad (2.3\text{-}8)$$

for a nondegenerately doped sample. The carrier concentration in the depletion region is given in Eq.(2.3-5). The average carrier concentration, P_a, can be shown to be

$$P_a=P_b\{(1-N_t/LN)+1/(qL)(2\pi\varepsilon kT/N)^{1/2}\cdot\mathrm{erf}[qN_t/2\cdot(2\varepsilon kTN)^{-1/2}]\}. \qquad (2.3\text{-}9)$$

There are two important contributions to current across the grain boundary: thermionic emission and tunneling. Thermionic emission results from those carriers possessing high enough energy to surmount the potential barrier at the grain boundary. On the other hand, the tunneling current arises from carriers with energy less than the barrier height. The barrier height decreases to a small value for a doped poly-Si, therefore, the tunneling current should be neglected. The thermionic emission current density, J_{th}, for an applied voltage, V_a, across a grain boundary is

$$J_{th}=qP_a(kT/2m^*\pi)^{1/2}\cdot\exp(-qV_B/kT)[\exp(qV_a/kT)-1], \qquad (2.3\text{-}10)$$

where m^* is the effective mass of the carrier. If V_a is small, $qV_a \ll kT$, Eq.(2.3-10) can be expanded to give

$$J_{th}=q^2P_a(2m^*\pi kT)^{-1/2}\cdot\exp(-qV_B/kT)V_a, \qquad (2.3\text{-}11)$$

which is a linear current-voltage relationship. From Eq.(2.3-11), the conductivity of a poly-Si film with a grain size L cm is

$$\sigma=Lq^2P_a(2m^*\pi kT)^{-1/2}\cdot\exp(-qV_B/kT). \qquad (2.3\text{-}12)$$

Inserting Eqs. (2.3-6) and (2.3-9) into Eq.(2.3-12), following relationships are obtained.

$$\sigma\propto\exp[-(E_g-E_f)/kT], \quad \text{if } NL < N_t, \qquad (2.3\text{-}13)$$

$$\sigma\propto T^{-1/2}\exp[-E_g/kT], \quad \text{if } NL > N_t. \qquad (2.3\text{-}14)$$

2.4 Current-voltage characteristics of p-n junction

The ideal current-voltage characteristics in dark are derived on the basis of the following four assumptions:

(1) The built-in potential and applied voltages are supported by a dipole layer with abrupt boundaries, and outside the boundaries the semiconductor is assumed to be neutral.

(2) Throughout the depletion layer, the Boltzmann relations are valid.

(3) The injected minority carrier densities are small compared with the majority-carrier densities.

(4) The facts that no generation current exists in the depletion layer, and the electron and hole currents are constant through the depletion layer.

At thermal equilibrium, the Boltzmann relation is given by

$$n_e=n_i\exp[(E_F-E_i)/kT]\equiv n_i\exp[q(\Psi-\phi)/kT] \qquad (2.4\text{-}1a)$$

$$p_h=n_i\exp[(E_i-E_F)/kT]\equiv n_i\exp[q(\phi-\psi)/kT] \qquad (2.4\text{-}1b)$$

where n_e is electron density, p_h is hole density, n_i is intrinsic carrier density, E_F is Fermi level, E_i is intrinsic Fermi level, and ψ and ϕ are the potentials corresponding to the intrinsic level and the Fermi level, respectively (or $\psi\equiv-E_i/q$, $\phi\equiv-E_F/q$). When a voltage is applied, the minority carrier densities on both sides of a junction are changed, and the p_hn_e product is no longer given by n_i^2. The imrefs is defined as follows:

$$n_e\equiv n_i\exp[q(\Psi-\phi n)/kT] \qquad (2.4\text{-}2a)$$

$$p_h \equiv n_i \exp[q(\phi p-\psi)/kT] \qquad (2.4\text{-}2b)$$

where ϕn and ϕp are the imrefs or quasi-Fermi levels for electrons and holes, respectively. From Eqs.(2.4-2a) and (2.4-2b), ϕn and ϕp are obtained to be

$$\phi n \equiv \psi - kT/q \cdot \ln(n_e/n_i) \qquad (2.4\text{-}3a)$$

$$\phi p \equiv \psi + kT/q \cdot \ln(p_h/n_i) \qquad (2.4\text{-}3b)$$

the $p_h n_e$ product becomes

$$p_h n_e = n_i^2 \exp[q(\phi p-\phi n)/kT] \qquad (2.4\text{-}4)$$

For a forward bias, $(\phi p-\phi n)>0$, and $p_h n_e > n_i^2$: on the other hand, for a reversed bias, $(\phi p-\phi n)<0$, and $p_h n_e < n_i^2$.

Since the electron density n_e varies in the junction from the n side to the p side by many orders of magnitude, whereas the electron current J_n is almost constant, it follows that ϕn must also be almost constant over the depletion layer. The electrostatic potential difference across the junction is given by

$$V_s = \phi p - \phi n. \qquad (2.4\text{-}5)$$

Eqs.(2.4-4) and (2.4-5) can be combined to give the electron density at the boundary of the depletion-layer region on the p side $(x=-x_p)$

$$n_p = n_i^2/p_p \exp(qV_s/kT) = n_{p0} \exp(qV_s/kT) \qquad (2.4\text{-}6)$$

where n_{p0} is the equilibrium electron density on the p side. Similarly,

$$p_n = p_{n0} \exp(qV_s/kT) \qquad (2.4\text{-}7)$$

at $x=x_n$ for the n type boundary.Eqs.(2.4-6) and (2.4-7) serve as the most important boundary equations for ideal current-voltage equation.

From the continuity equations, following equations are obtained for the steady-state:

$$-(n_n-n_{n0})/\tau_n + \mu_n E \cdot (\partial n_n/\partial x) + \mu_n n_n \cdot (\partial E/\partial x) + D_n \cdot (\partial^2 n_n/\partial x^2) = 0, \quad (2.4\text{-}8a)$$

$$-(p_n-p_{n0})/\tau_p + \mu_p E \cdot (\partial p_n/\partial x) + \mu_p p_n \cdot (\partial E/\partial x) + D_p \cdot (\partial^2 p_n/\partial x^2) = 0. \quad (2.4\text{-}8b)$$

We can eliminate the term in $\partial E/\partial x$ from the above equations with the condition that $(p_n-p_{n0})/\tau_p$ equals $(n_n-n_{n0})/\tau_n$. This gives

$$-(p_n-p_{no})/\tau_p + \mu_a E \cdot (p_n \cdot \partial n_n/\partial x - n_n \cdot \partial p_n/\partial x)/(p_n-n_n)$$
$$+ D_a \cdot (p_n \cdot \partial^2 n_n/\partial x^2 + n_n \cdot \partial^2 p_n/\partial x^2)/(p_n+n_n) = 0 \quad (2.4\text{-}9)$$

where

$$D_a \equiv D_n D_p (p_n+n_n)/(p_n D_p + n_n D_n) \equiv \text{ambipolar diffusion coeff.} \quad (2.4\text{-}10)$$

$$\mu_a \equiv \mu_n \mu_p (p_n-n_n)/(p_n \mu_p + n_n \mu_n) \equiv \text{ambipolar mobility.} \quad (2.4\text{-}11)$$

It can be shown that from the assumption (3) (e.g., $p_n << n_n \approx n_{n0}$ in the n-type semiconductor) Eq.(2.4-9) reduces to

$$-(p_n-p_{n0})/\tau_p - \mu_p E \cdot \partial p_n/\partial x + D_p \cdot \partial^2 p_n/\partial x^2 = 0 \qquad (2.4\text{-}12)$$

In the neutral region where there is no electric field, Eq.(2.4-12) further reduces to

$$\partial^2 p_n/\partial x^2 - (p_n-p_{n0})/\tau_p D_p = 0. \qquad (2.4\text{-}13)$$

The solution of Eq.(2.4-13) with the boundary condition Eq.(2.4-7) and $p_n(x=\infty)=p_{n0}$, gives

$$p_n - p_{n0} = p_{n0}(e^{qV/kT}-1)e^{-(x-x_n)/L_p} \qquad (2.4\text{-}14)$$

where

$$L_p \equiv (D_p \tau_p)^{1/2}. \qquad (2.4\text{-}15)$$

And at $x=x_n$

$$J_p = -qD_p \cdot \partial p_n/\partial x_{\,x_n} = qD_p p_{n0}/L_p (e^{qV/kT}-1). \qquad (2.4\text{-}16)$$

Similarly following equation is obtained for the p side

$$J_n = qD_n \cdot \partial n_p/\partial x_{\,-x_p} = qD_n n_{p0}/L_n (e^{qV/kT}-1). \qquad (2.4\text{-}17)$$

The total current is given by the sum of Eqs.(2.4-16) and (2.4-17):

$$J = J_p + J_n = J_s (e^{qV/kT}-1), \qquad (2.4\text{-}18)$$

$$J_s \equiv qD_p p_{n0}/L_p + qD_n n_{p0}/L_n. \qquad (2.4\text{-}19)$$

The rate of generation of electron-j=hole pairs can be obtained with the condition $p<n_i$ and $n<n_i$:

$$U = -[\sigma_p \sigma_n \upsilon_{th} N_t / [\sigma_n \exp\{(E_t-E_i)/kT\} + \sigma_p \exp\{(E_i-E_t)/kT\}]] n_i \equiv -n_i/\tau_e \quad (2.4\text{-}20)$$

where σ_p is the hole capture cross section, σ_n is the electron capture cross section, υ_{th} is the carrier thermal velocity, N_t is the trap density, E_i is the intrinsic Fermi level, E_t is the trap energy level, and τ_e is the effective lifetime.

Using Eq.(2.4-20), the total forward current considering the generation-recombination process can be obtained (for $p_{n0} >> n_{p0}$/ and $V>kT/q$):

$$J_F = q(D_p/\tau_p)^{1/2}(n_i^2/N_D)\exp(qV/kT) + (qW/2)\sigma \upsilon_{th} N_t n_i \exp(qV/2kT), \quad (2.4\text{-}21)$$

where W is the depletion width. The experimental results in general can be represented by the following empirical form

$$J_F \propto \exp(qV/nkT) \qquad (2.4\text{-}22)$$

where the factor n=2 when the recombination current dominates, as shown in Figure 2.4-1 curve (a), and n=1 when the diffusion current dominates, as shown in Fig. 2.4-1 curve (b). When both currents are comparable, n has a value between 1 and 2.

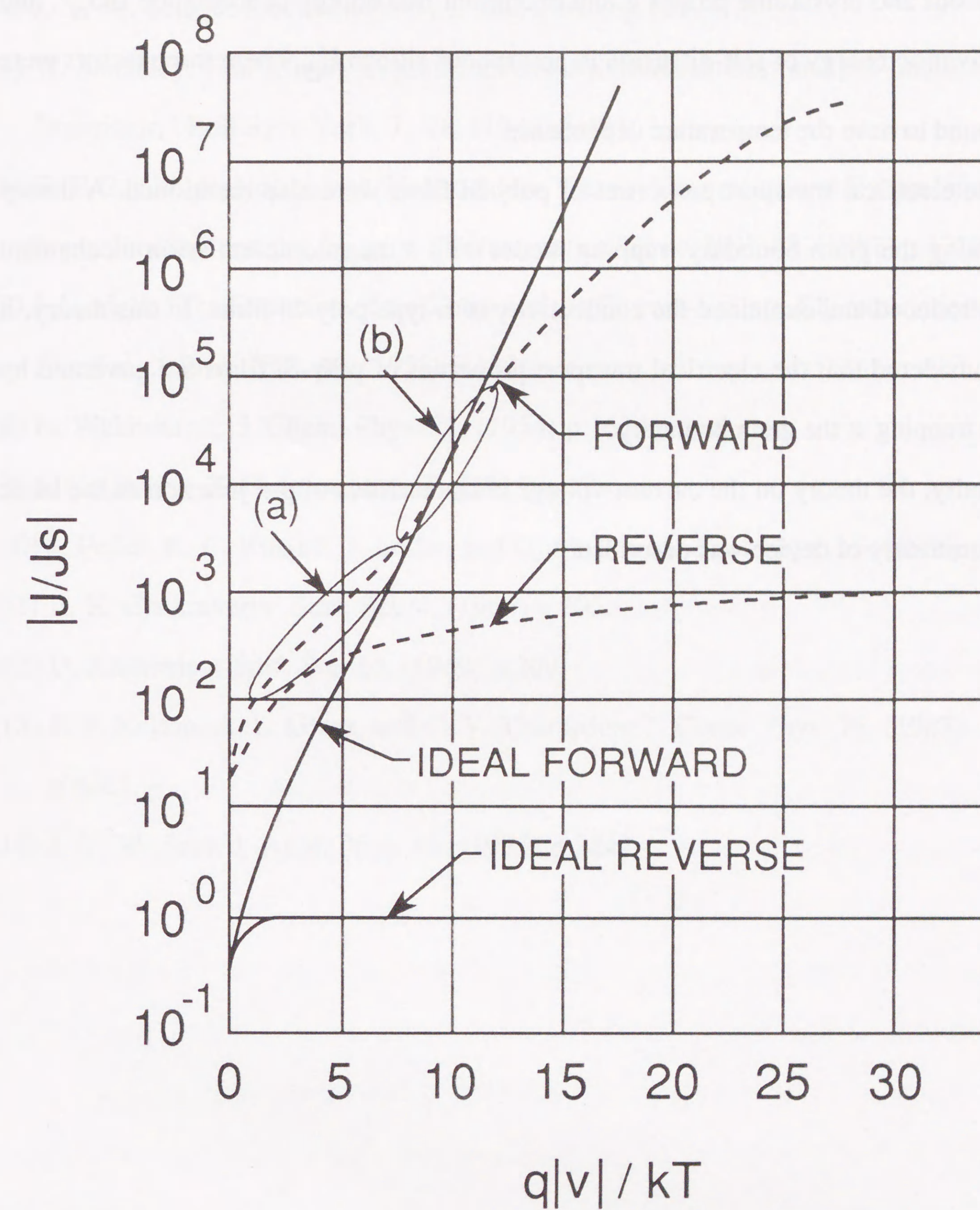


Fig. 2.4-1 Current-voltage characteristics of a practional Si deode
(a) generation-recombination current region
(b) diffusion current region

2.5 Summary

The crystallized theory of poly-Si from a-Si was described. The transient time, nucleation rate, and growth velocity, which were very important factor for the crystallization, were explained using the Gibbs-free-energy difference between the amorphous and crystalline phases g, the maximum free energy of formation ΔG_n^*, and the activation energy of self-diffusion in amorphous silicon E_d. These three factors were also found to have the temperature dependence.

The electrical transport properties of poly-Si films were also mentioned. A theory combining the grain boundary trapping model with a thermionic-emission mechanism was introduced and explained the conductivity of n-type poly-Si films. In this theory, it was considered that the electrical transport properties of poly-Si films are governed by carrier trapping at the grain boundary.

Finally, the theory on the current-voltage characteristics of p-n junction as the basic transport theory of device was described.

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3 Development of thin-film polycrystalline silicon by a new SPC method

3.1 Introduction

For the development of solar cells with a much higher conversion efficiency, it is necessary to develop materials with high photosensitivity in the long-wavelength region where amorphous silicon (a-Si) films have no photosensitivity as shown in Figure 3.1-1. Thin-film poly-Si is a hopeful material for this purpose, and it was fabricated by a new SPC method.

It is important for enlargement of grain size in thin-film poly-Si to control the density of nuclei generated in the initial stage of the SPC process. In order to find a way to control nucleation, the effects of phosphorus and boron atoms as dopants for silicon during solid-phase crystallization were investigated. For nucleation control, the position and density of nuclei generated in the initial stage of SPC are tried to be restrained. The development of a way for controlling the position of nuclei generation led to the SPC method called by partial doping method. This partial doping method is the basis on the improvement of thin-film poly-Si properties and most of starting materials has the structure consisting of a nucleus generation layer and a crystal growth layer, as shown in Figure 3.1-2.

To enlarge grain size, it is essential to find an a-Si structure well-suited to solid-phase crystallization. The relationship between the structure of a-Si films before the SPC process and the average grain size of thin-film poly-Si after the SPC process was investigated. To elucidate the growth kinetics, the nucleation rate and velocity of solid-phase crystallization, and the detailed structure of a-Si films were analyzed. Growth kinetics for the enlargement of grain size were thereby explained.

The surface morphology of substrates is also very important in solid-phase crystallization. It was found that textured substrates had a great effect on the achievement of thin-film poly-Si with large grains in the SPC method. There are a number of reports on the crystalline growth of materials such as silicon (Si)[1], germanium (Ge)[2], and gallium arsenide (GaAs)[3] using textured substrates. These investigations are commonly known as "graphoepitaxy". The surface morphology of textured substrates in these papers were precise, but that of textured substrates used in this study was at random.

Despite using different textured substrates from "graphoepitaxy", thin-film poly-Si with a large grain size were successfully grown in this study. Factors that facilitate the enlargement of grain size on textured substrates were also studied. Furthermore, the film properties of poly-Si were improved by combining partial doping and textured substrates.

Another candidate of starting material is the a-Si film including a crystalline phase to act as seed of solid-phase crystallization. Solid-phase crystallization using c-Si as seed[4] has also been reported. In this paper, heat treatment of a-Si in contact with mesa-striped (100)-oriented Si seed crystal was performed, as shown in Figure 3.1-3. This method is called by external seeding technique. In external seeding technique, there are problems as following.

(1) It is necessary to remove impurities such as oxygen (O), carbon (C), and nitrogen (N) on both Si surfaces of the seed and a-Si.

(2) Both Si surfaces of the seed and a-Si must be flat.

(3) The surface of the a-Si must be brought into contact with the seed at a pressure of about 1 kg/cm^2, for a good contact with the seed.

So, it is difficult to prepare large-area thin-film poly-Si using the external seeding technique and to apply it to a textured surface. The reproducibility for the preparation of thin-film poly-Si is poor. Thus, I have developed internal seeding technique using grain made of single-crystalline phase as a seed. This internal seeding technique is a way of fabricating thin-film poly-Si by the SPC method using a-Si films containing a single-crystalline phase. The merits of this internal seeding technique are follows.

(1) The concentrations of impurities such as O, C, and N are very low at the interface between the seed and a-Si.

(2) The incubation time for solid-phase crystallization is decreased because there is no nucleation process.

(3) It is easy to fabricate large-area thin-film poly-Si.

The internal seeding technique thus enables significant improvement in thin-film poly-Si properties.

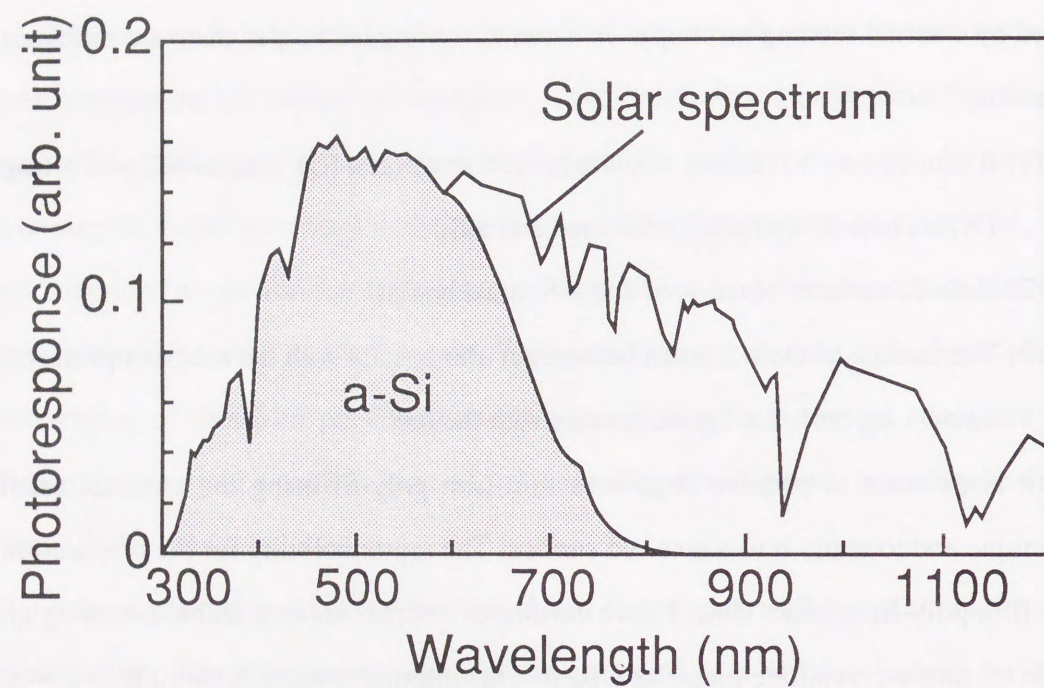


Fig. 3.1-1 Solar spectrum and photoresponse of a-Si solar cells.

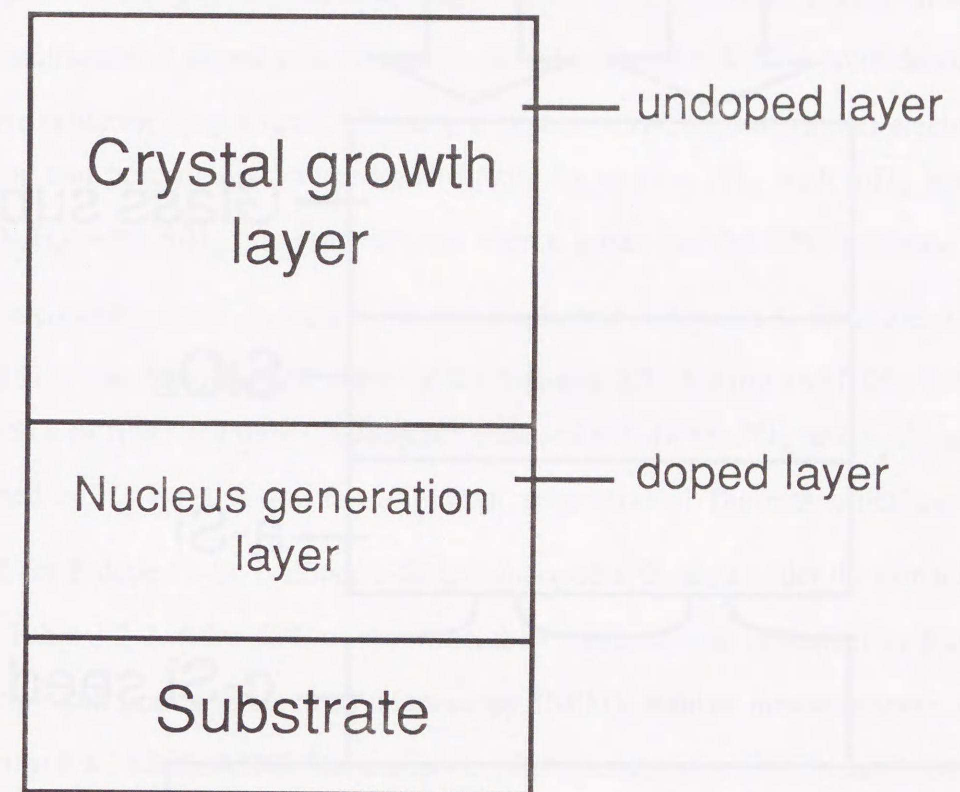


Fig. 3.1-2 The structure of starting material (a-Si) used in partial doping method.

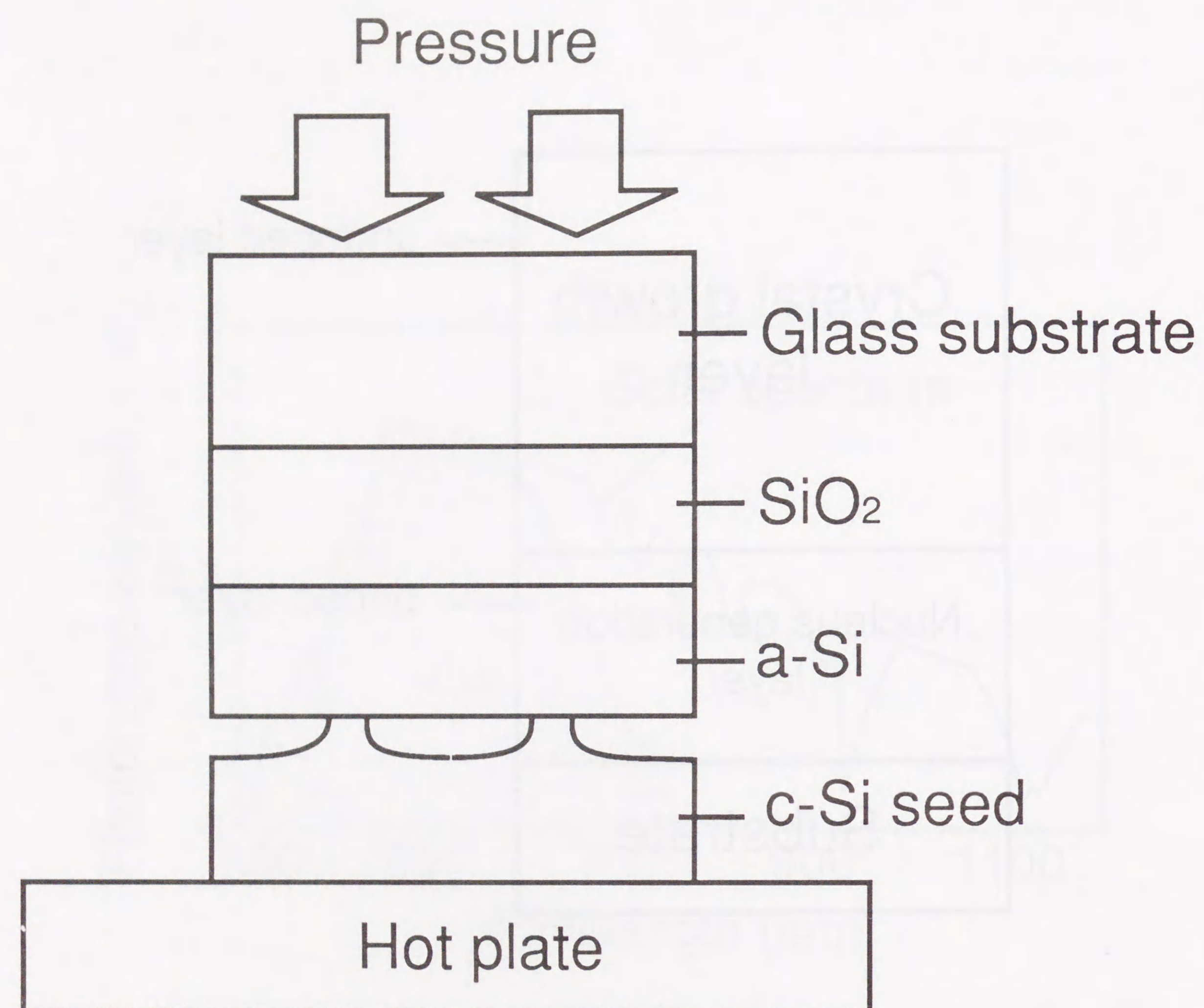


Fig. 3.1-3 A schematic illustration of the external seeding method for SPC. Stripes are formed on (100)-oriented Si seed crystal. The same chemical treatment is applied to the both Si surfaces of seed and substrate.

3.2 Effect of impurities (dopants)

This section describes the effects of dopant atoms (phosphorus and boron) on solid-phase crystallization as well as those of partial doping using phosphorus atoms.

3.2.1 Experimental technique

In order to investigate the effects of dopant atoms (phosphorus or boron) on solid-phase crystallization, P-doped a-Si, B-doped a-Si and undoped a-Si films were deposited on a quartz substrate by plasma-CVD using a capacitively-coupled parallel electrode. Phosphorus and boron atoms were doped in-situ by mixing PH_3 with SiH_4 and by mixing B_2H_6 with SiH_4, respectively, as source gases for the SPC process. The preparation conditions of P-doped a-Si, B-doped a-Si and undoped a-Si films are shown in Table 3.2-1. The thickness of P-doped a-Si films was 0.2 - 3.0 μm and 0.09 - 0.4 μm for B-doped a-Si films and 0.09 - 3.0 μm for undoped a-Si films. PH_3 and B_2H_6 gases were diluted by H_2 for 1 % and for 1000 ppm, respectively. Thermal annealing was performed for P-doped a-Si, B-doped a-Si and undoped a-Si films under the conditions shown in Table 3.2-2. After SPC of the films, their structure was evaluated by Raman spectroscopy and scanning electron microscopy (SEM). Raman measurements were carried out with a JASCO R800T Raman spectrophotometer with a triple monochrometer and a cooled photomultiplier. The exciting light is a 488 nm line from an Ar-ion laser. Wavenumbers were calibrated by using the natural emission lines of the laser. Hall mobility was measured. In the Hall effect measurements, the intensity of the magnetic field was 5000 Gauss, the electrode was a van der Pauw configuration, and the temperature was 300 K.

To provide high-quality thin-film poly-Si using the partial doping method, a quartz/undoped a-Si (crystal-growth layer)/P-doped a-Si (nucleus-generation layer) structure was fabricated, where, in the nucleus generation layer, the density of nuclei generated during the SPC process was designed to be minimized.

Table 3.2-1 Preparation conditions of P-doped a-Si, B-doped a-Si and undoped films.

	P-doped a-Si	B-doped a-Si	undoped a-Si
SiH_4 (sccm)	1～30	5	30
PH_3 1% H_2 (sccm)	3～70	-------	-------
B_2H_6 0.1% H_2 (sccm)	-------	1～50	-------
Substrate temperature(℃)	200～500	200～300	650
Pressure (Pa)	36	40	36
R.F. power (mW/cm^2)	120	80	120

Table 3.2-2 SPC conditions of P-doped a-Si, B-doped a-Si and undoped a-Si films.

Annealing temperature (℃)	500～850
Annealing time (hour)	3～10
Annealing atmosphere	vaccum or N_2

3.2.2. Phosphorus and boron

(1) Effect of phosphorus atoms on SPC

In order to investigate the effect of phosphorus atoms on solid-phase crystallization, the SPC process was performed at a temperature of 600 °C, using P-doped and undoped a-Si films as starting materials. Figure 3.2-1 shows the Raman spectra of the films after SPC of undoped and P-doped a-Si films, whose thickness is 1.0 μm. After the SPC process, the film of undoped a-Si showed the broad peak at 480 cm^{-1} but did not show the peak at 520 cm^{-1}. On the other hand, the film after SPC of P-doped a-Si has the peak at 520 cm^{-1}. Figure 3.2-2 shows the cross-sectional SEM photographs taken after the SPC process of undoped and P-doped a-Si films at an SPC temperature of 600 °C, where the SPC time is 10 hours. The SPC of the undoped a-Si film does not occur and the cross section after the SPC process is of amorphous phase. On the other hand, SPC of P-doped a-Si film does occur and the cross section after SPC is of polycrystalline phase with a grain size of about 1μm. RHEED measurements also confirmed that the films after SPC of P-doped a-Si films were polycrystalline phase. Thus, it was found that SPC occurred easily at low temperature when phosphorus atoms were doped. Therefore, the phosphorus atom has the effect of promoting polycrystallinity with large grains at a relatively low temperature of 600 °C.

The influences of phosphorus concentration and SPC temperature on n-type poly-Si were investigated. Figure 3.2-3 shows cross-sectional SEM photographs of n-type poly-Si with phosphorus concentrations of 1.2 x 10^{20} - 1.7 x 10^{21} cm^{-3}, where the SPC conditions are chosen to be 700 °C for 10 hours to accelerate the crystallization. In Fig. 3.2-3, the grain size of n-type poly-Si drastically increases with the reduction in phosphorus concentration. This indicates that the reduction of phosphorus concentration leads to the decrease of the density of nuclei generated during SPC. As a result, polycrystalline Si of large grain size grew after SPC. In n-type poly-Si with a phosphorus concentration of 1.2 x 10^{20} cm^{-3}, a grain size of about 2.0 μm was obtained. Figure 3.2-4 shows the absorption coefficient of the films

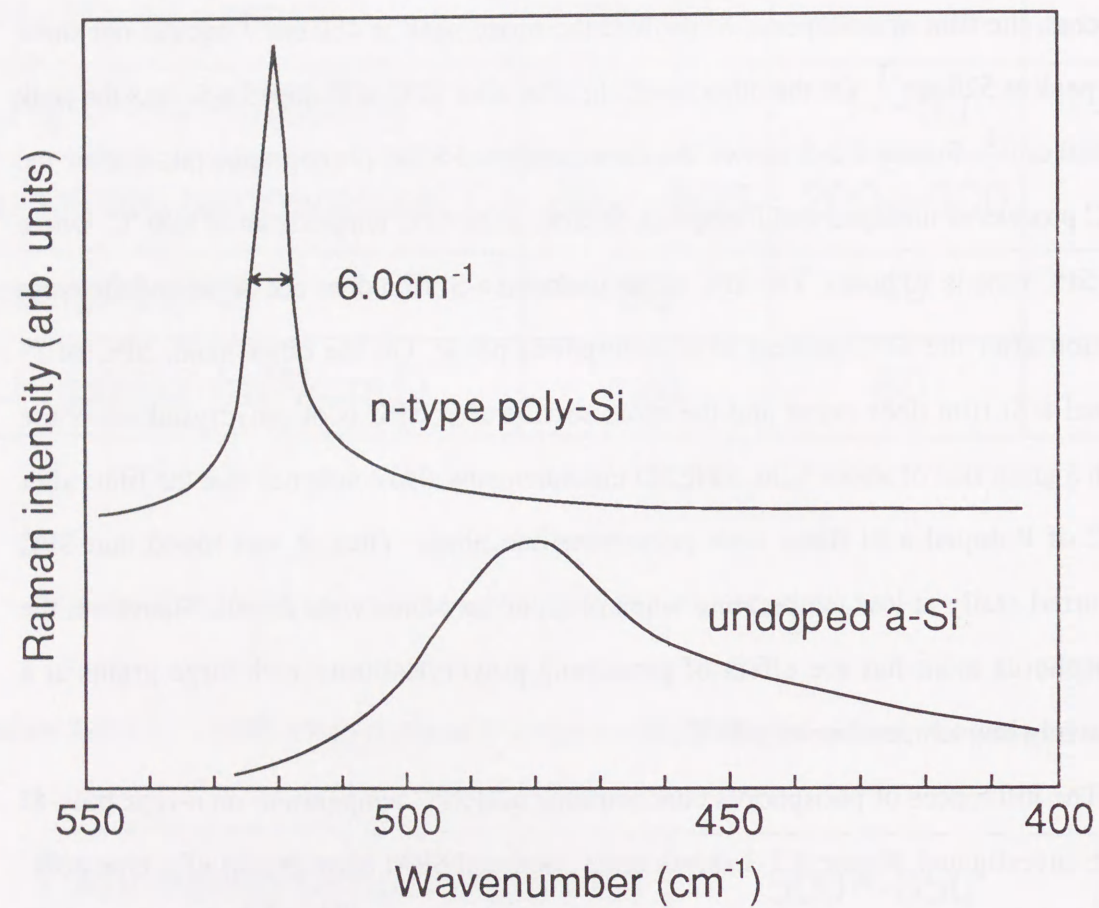


Fig. 3.2-1 Raman spectra of the films after SPC process of undoped a-Si and P-doped a-Si films at the SPC temperature of 600℃.

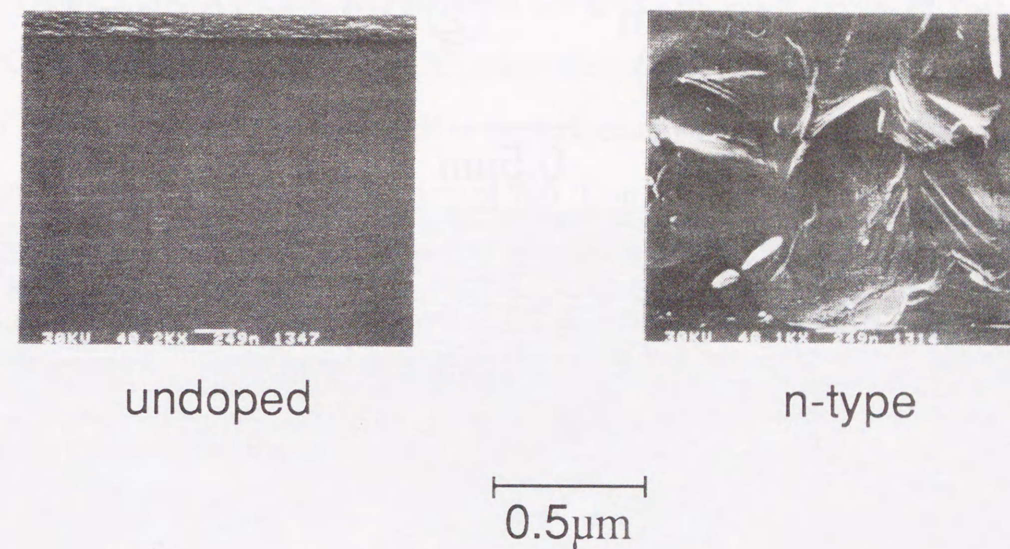


Fig. 3.2-2 The cross-sectional SEM photographs taken after SPC process of undoped a-Si and P-doped a-Si films at the SPC temperature of 600℃.

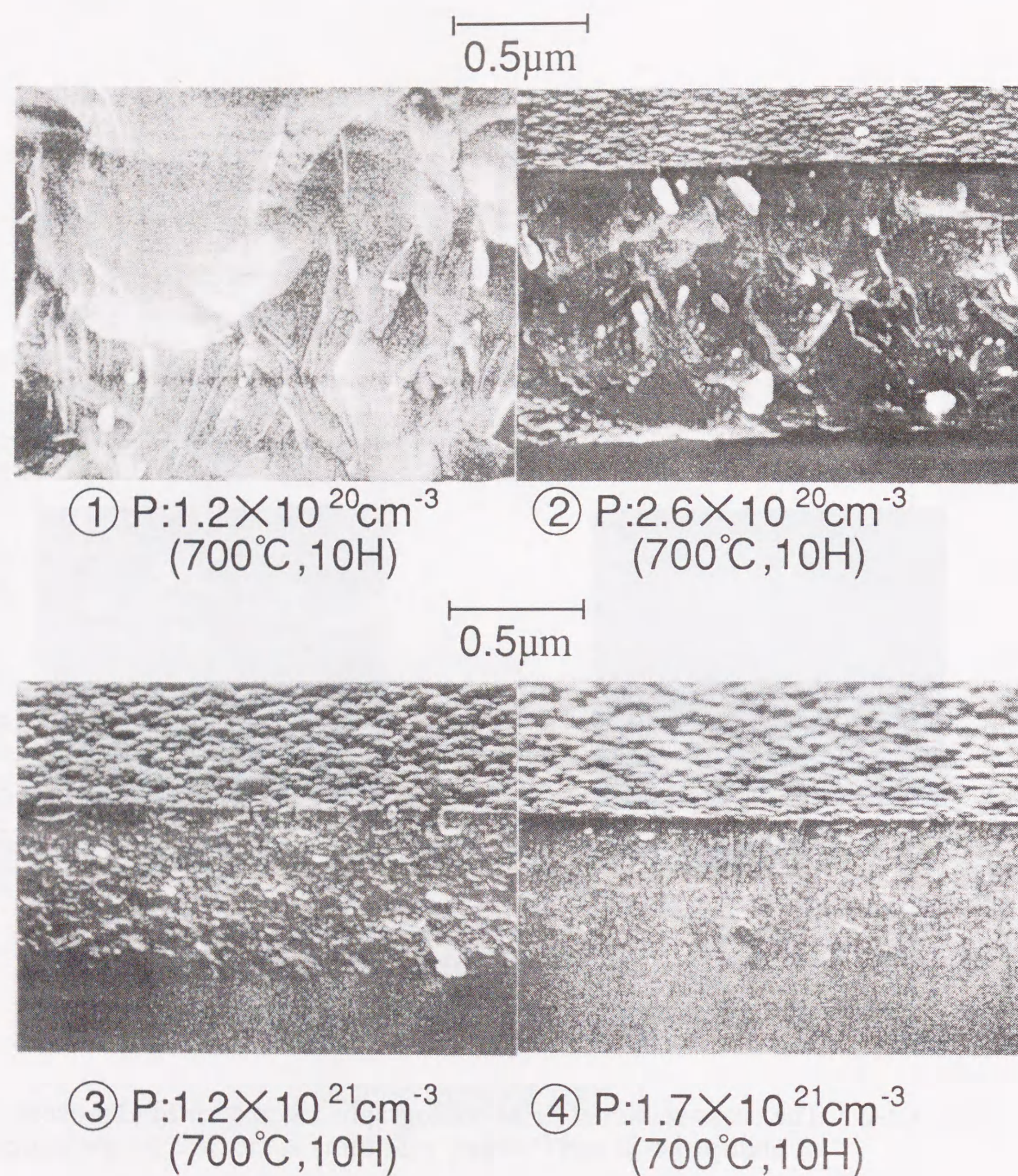


Fig. 3.2-3 The cross-sectional SEM photographs of n-type poly-Si with phosphorus concentration of 1.2×10^{20} cm^{-3} ~1.7×10^{21}cm^{-3}, where the SPC conditions are 700℃, 10hours.

after SPC of a-Si films with phosphorus concentrations of 1.2×10^{20} - 1.7×10^{21} cm^{-3}, compared with that of single-crystalline silicon (c-Si).[5] The absorption coefficient was determined precisely using transmittance and reflection spectra of the films.[6] The absorption coefficient increases with increasing the phosphorus concentration. Considering that thin-film poly-Si consists of grain and grain boundaries, this increase in the absorption coefficient is thought to be due to the increase in grain-boundary regions because the absorption coefficient of the grains are the same as that of c-Si. Thus, it was also confirmed by a optical measurement that grain size was enlarged by reduction of the phosphorus concentration.

Figure 3.2-5 shows the cross-sectional SEM photographs of n-type poly-Si for two SPC temperatures, 600 °C and 700 °C, where the phosphorus concentration is 1.2×10^{20} cm^{-3}. The n-type poly-Si fabricated at the temperature of 600 °C had the larger grains than that prepared at the temperature of 700 °C in the region near the substrate. This indicates that reducing the SPC temperature contributes to the growth of polycrystalline Si of large grain size as a result of the decrease in the density of nuclei generated during SPC. It was recognized that the control of nucleus generation led to growth of polycrystalline Si of large grain size.

Figure 3.2-6 shows the Hall mobility of n-type poly-Si prepared by the SPC at temperatures of 600 °C and 700 °C. The Hall mobility of n-type poly-Si crystallized at 600 °C was larger than that crystallized at 700 °C. This supports that n-type poly-Si crystallized at lower temperatures has the larger grain size, as shown in Fig. 3.2-5.

Minority carrier characteristics are very important for solar cell materials. Thus, the minority carrier trap density was analyzed in terms of a trapping model.[8] According to the trapping model, the following equation can be introduced:

$$\sigma T^{1/2} \propto \exp(-q^2 N_t^2 / 8\varepsilon N k T), \qquad (3.2\text{-}1)$$

where N_t is the minority carrier trap density, N the phosphorus concentration, σ the dark conductivity of poly-Si, q the electronic charge, ε the dielectric constant of silicon, k the Boltzmann's constant, and T the absolute temperature. In n-type poly-Si prepared by the SPC method, the dependence of dark conductivity on temperature was analyzed from the slope of the $\ln(\sigma T^{1/2})$-vs-$1/T$ relationship. Figure 3.2-7 shows the minority carrier trap

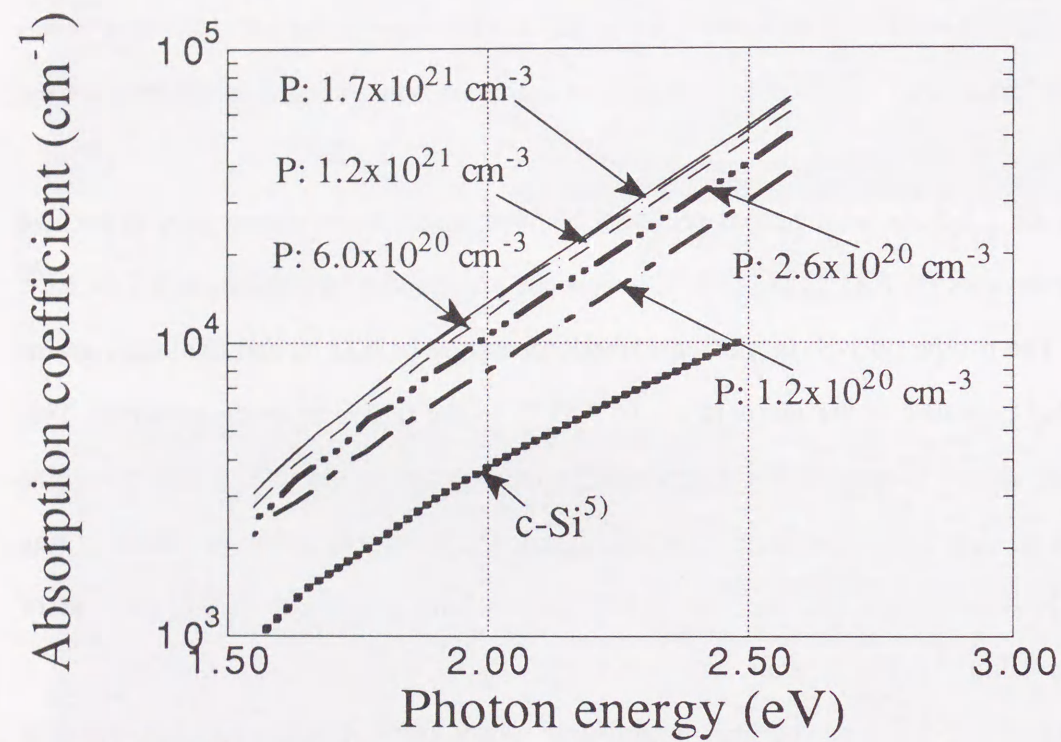


Fig. 3.2-4 The absorption coefficient of the films after the SPC process for the a-Si films with various phosphorus concentrations.

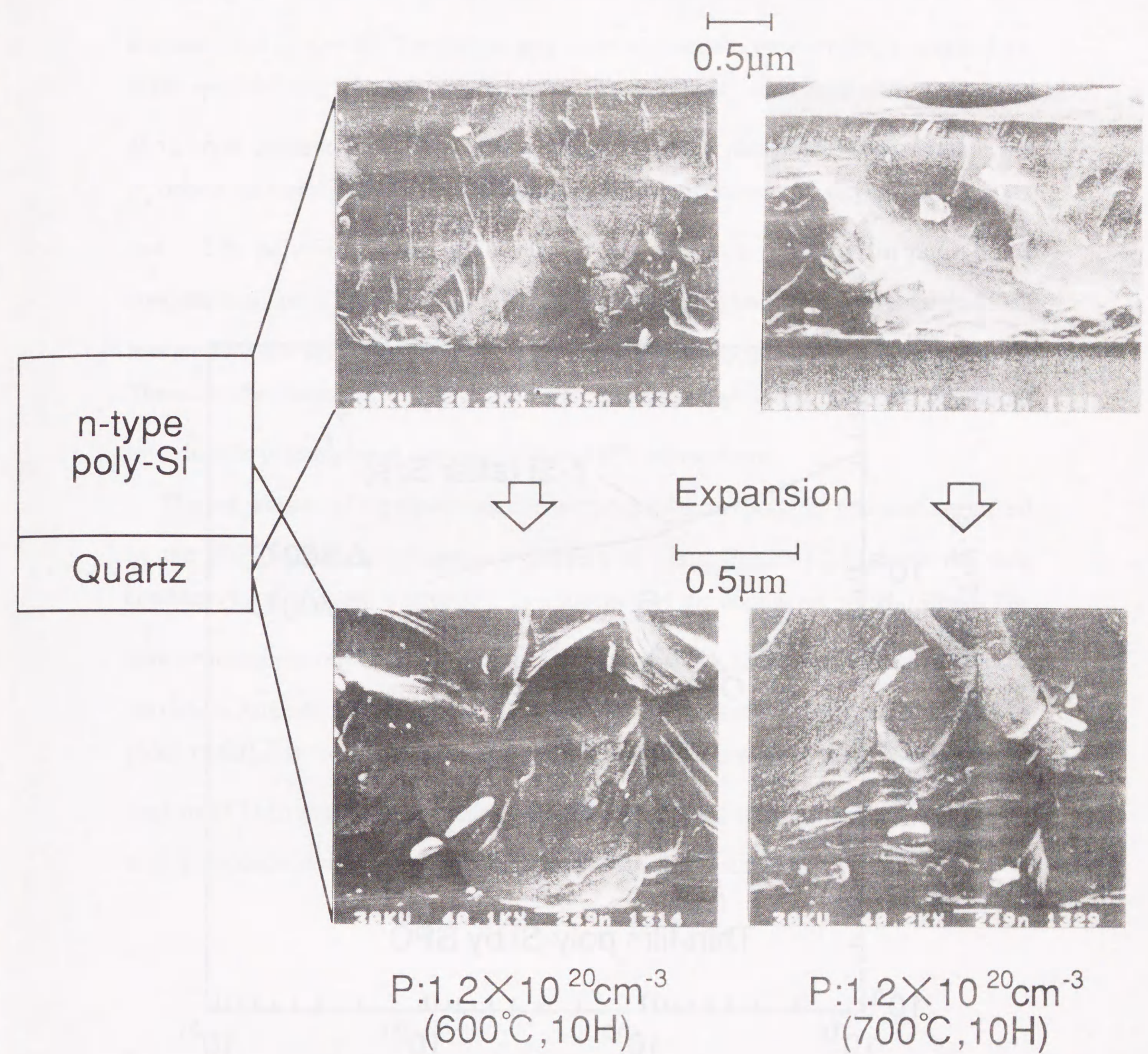


Fig. 3.2-5 The cross-sectional SEM photographs of n-type poly-Si for two temperatures of 600℃ and 700℃, where the phosphorus concentration is $1.2\times10^{20}cm^{-3}$. The upper part shows the whole portion in cross-sections, and the lower part shows a portion near the substrate for the temperatures.

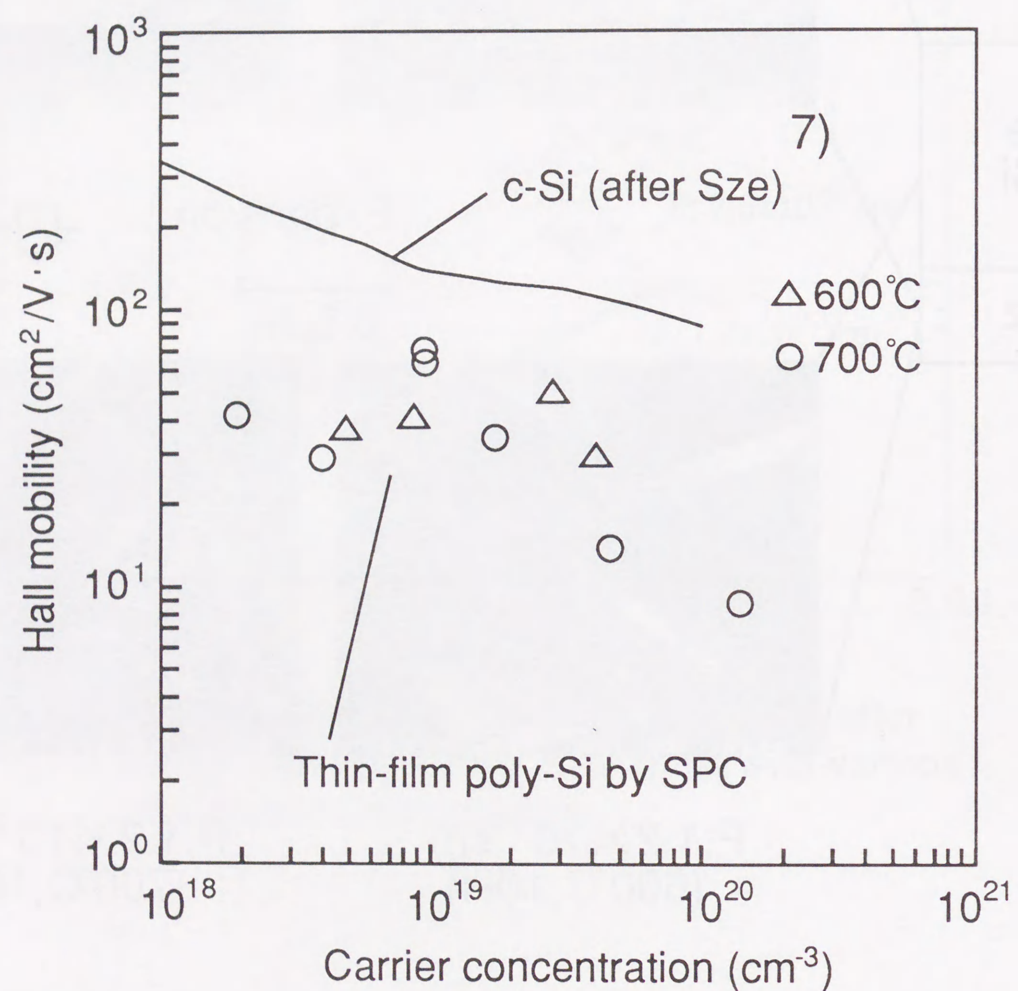


Fig. 3.2-6 The comparison of Hall mobility in the n-type poly-Si prepared at the SPC temperature of 600℃ and 700℃.

density N_t in n-type poly-Si prepared by the SPC method as a function of the phosphorus concentration in poly-Si. The phosphorus concentration was measured by secondary ion mass spectroscopy (SIMS). As shown in Fig. 3.2-7, N_t decreased with decreasing phosphorus concentration. Especially in the region of low phosphorus concentration, the N_t decreased significantly with a reduction in SPC temperature. As shown in Figs. 3.2-3 and 3.2-5, poly-Si of large grain size grows due to a reduction in phosphorus concentration and SPC temperature. Thus, when the phosphorus concentration and SPC temperature are decreased, poly-Si with a small grain boundary region is prepared. Therefore, the decreases in N_t coincide with the results of grain-size enlargement induced by reduction in phosphorus concentration and SPC temperature.

The preparation of highly conductive n-type poly-Si (n^+poly-Si) was also attempted by the SPC method, using highly P-doped a-Si films. Figure 3.2-8 shows the dark conductivity of n^+poly-Si after SPC as a function of the doping ratio (PH_3/SiH_4). The dark conductivity of n^+poly-Si increases with an increase in the doping ratio and has a maximum value of $1.5\text{x}10^3$ $(\Omega cm)^{-1}$. This conductivity is equal to a sheet resistance of about 10 Ω/□ at the thickness of 0.7 μm, and this value is close to that of SnO_2 which is used in TCO (transparent conductive oxide) electrode of solar cells. Thus, n^+poly-Si with high conductivity can be prepared by using the SPC method.

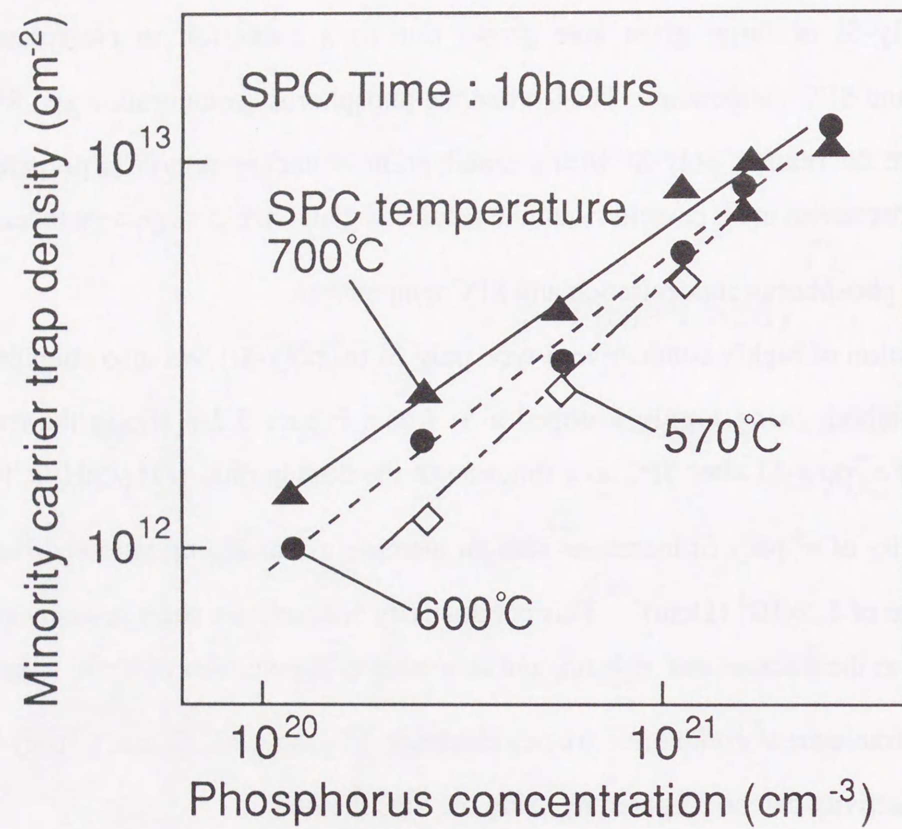


Fig. 3.2-7 The minority carrier trap density N_t in n-type poly-Si prepared by the SPC method as a function of the phosphorus concentration in poly-Si.

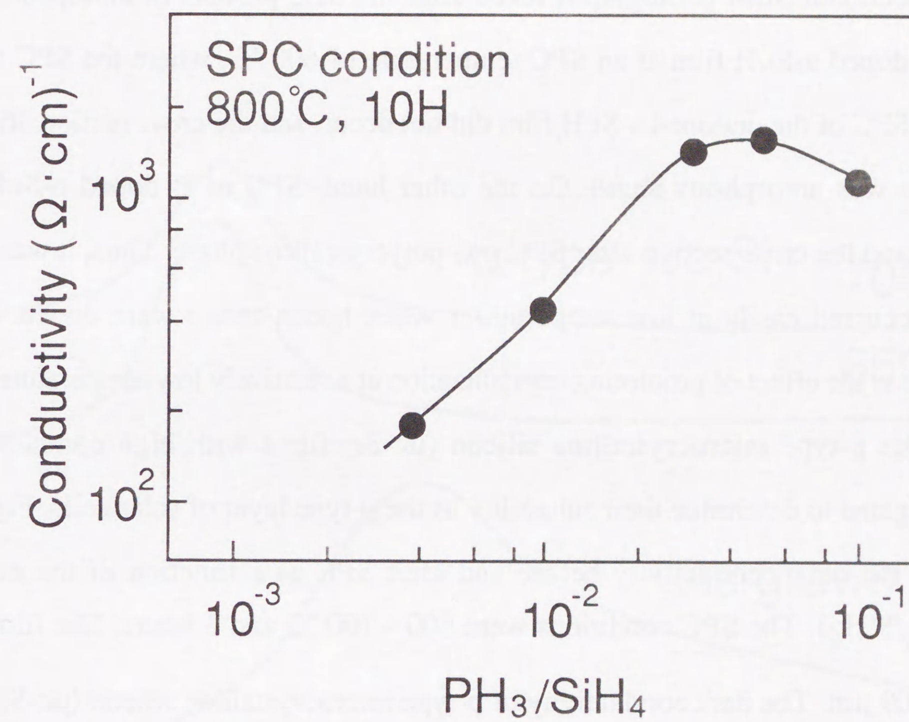


Fig. 3.2-8 The dark conductivity of n^+ poly-Si after SPC as a function of the doping ratio (PH_3/SiH_4)

(2) Effect of boron atoms on the SPC

In order to find the effects of boron atoms on solid phase crystallization, a B-doped hydrogenated amorphous silicon (a-Si:H) film was annealed at temperatures of 650 °C and 700 °C. Figure 3.2-9 shows the Raman spectra of the films before and after SPC of the B-doped a-Si:H films. Before SPC, a broad peak was observed at 480 cm^{-1}. The film before SPC was amorphous. After SPC, a peak was observed at around 512 cm^{-1} and no peak was observed in the 470 to 480 cm^{-1} region. Thus, it was confirmed that films after SPC of B-doped a-Si:H films had a crystalline phase. Figure 3.2-10 shows cross-sectional SEM photographs taken after the SPC process of undoped a-Si:H film and B-doped a-Si:H film at an SPC temperature of 600 °C, where the SPC time was 3 hours. SPC of the undoped a-Si:H film did not occur, and the cross section after the SPC process was amorphous phase. On the other hand, SPC of B-doped a-Si:H film did occur, and the cross section after SPC was polycrystalline phase. Thus, it was found that SPC occurred easily at low temperatures when boron atoms were doped. Therefore, boron has the effect of promoting crystallization at a relatively low temperature of 600 °C.

The p-type microcrystalline silicon (μc-Si) films with high conductivity were investigated to determine their suitability as the p-type layer of solar cells. Figure 3.2-11 shows the dark conductivity before and after SPC as a function of the doping ratio (B_2H_6/SiH_4). The SPC conditions were 600 - 700 °C and 3 hours. The film thickness was 0.09 μm. The dark conductivity of p-type microcrystalline silicon (μc-Si) increased as the SPC temperature was increased for each doping ratio, and reaching a maximum value at a doping ratio of 5×10^{-3}. Another prominent feature was an increase in dark conductivity by 9 to11 orders after SPC at a doping ratio of 5×10^{-3}, using the film with low dark conductivity. A maximum value of about 2.0×10^{3} $(\Omega cm)^{-1}$ was achieved, a value never before reported. In order to elucidate the reasons why p-type μc-Si films prepared by the SPC method have the highest conductivity at a doping ratio 5×10^{-3}, the quality of crystallinity for films after SPC was analyzed using their absorption coefficient. Figure 3.2-12 shows the dependence of the absorption coefficient of p-type μc-Si on the doping ratio, where the SPC conditions were 650 °C for 3 hours and 700 °C for 3 hours. The absorption coefficient of p-type μc-Si at a doping ratio of 5×10^{-3} was

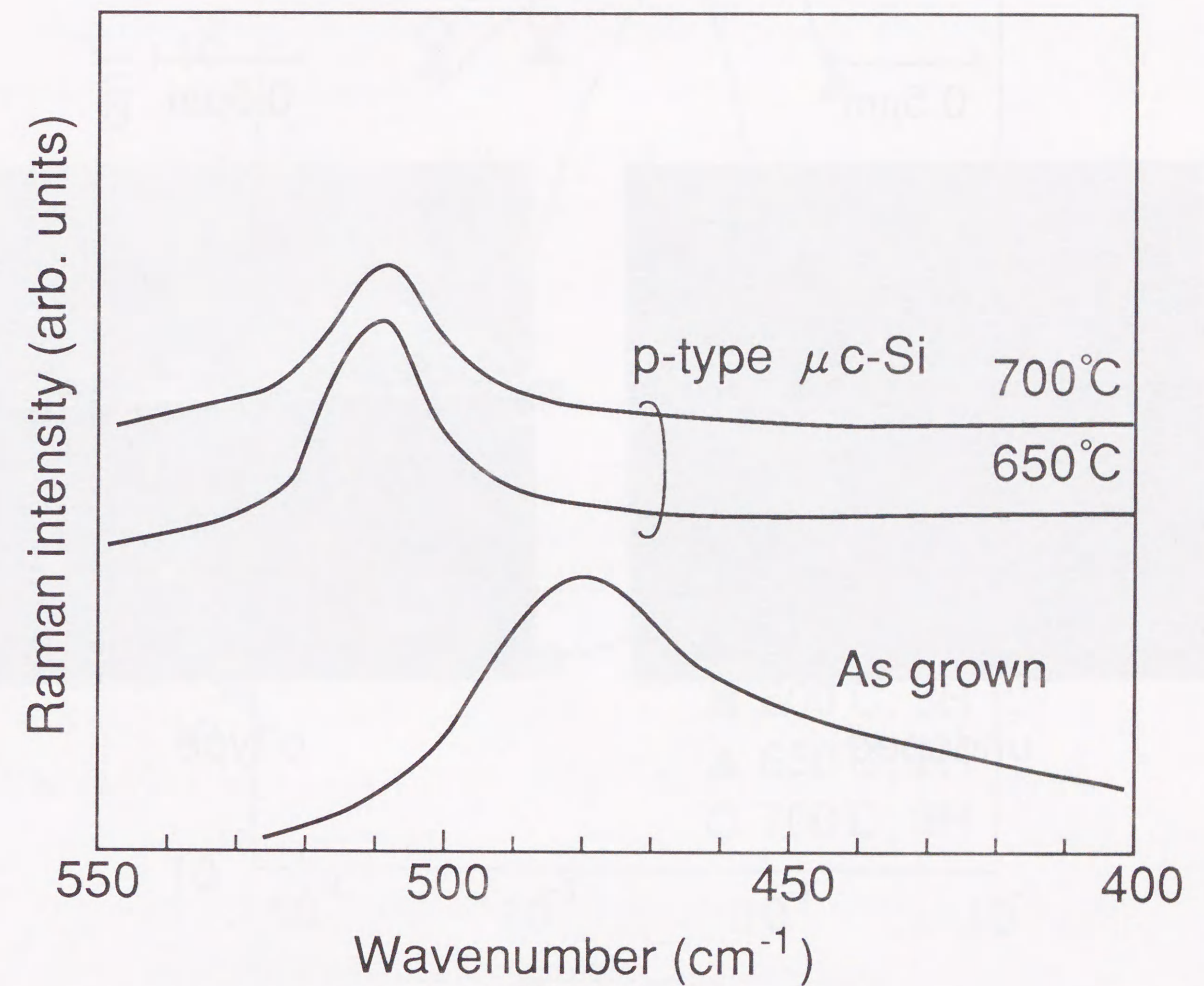


Fig. 3.2-9 Raman spectra of films before and after SPC of B-doped a-Si:H films, where SPC temperatures are 650℃ and 700℃.

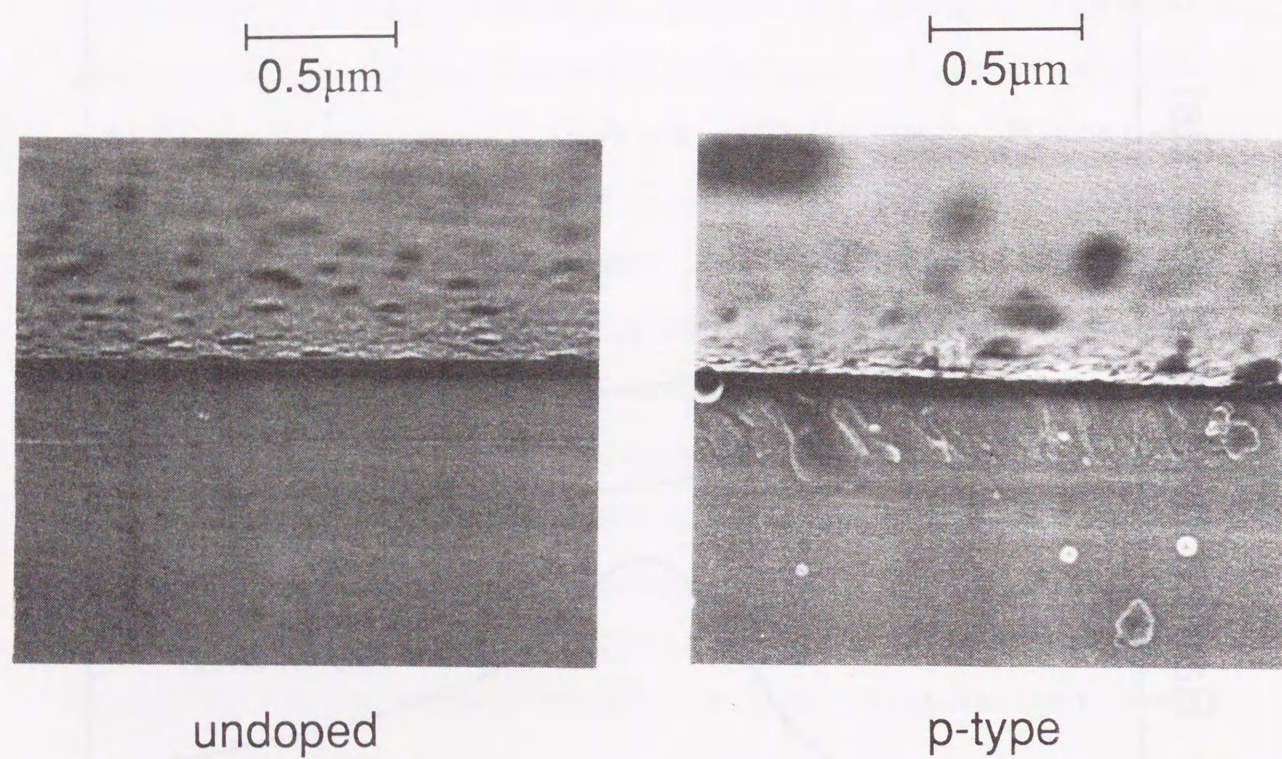


Fig. 3.2-10 The cross-sectional SEM photographs after SPC of B-doped a-Si and undoped a-Si films. Boron atoms were introduced in-situ into a-Si film.

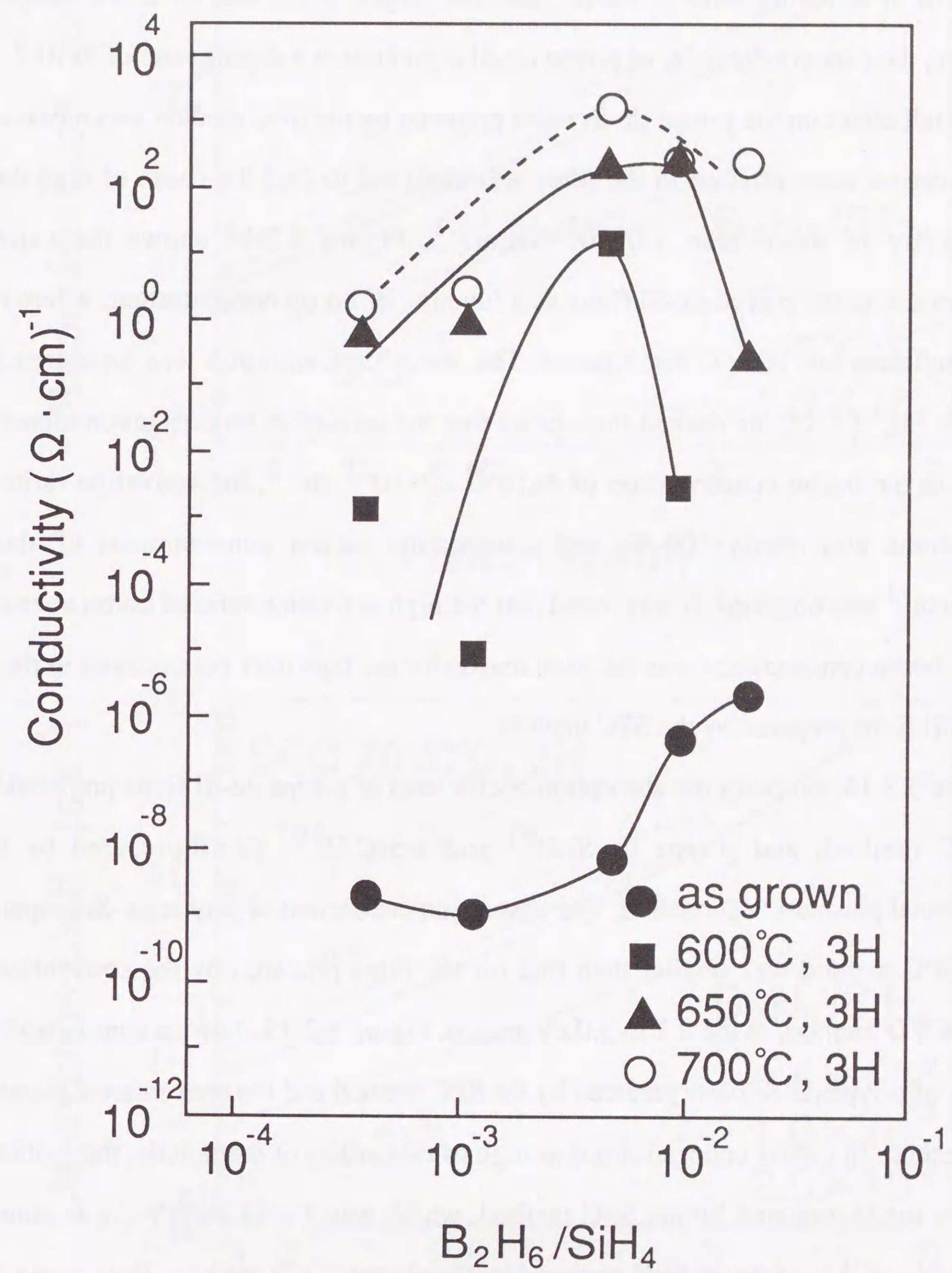


Fig. 3.2-11 Dark conductivity of the films before and after SPC as a function of doping ratio (B_2H_6/SiH_4), where SPC temperatures are 600℃, 650℃, and 700℃.

the lowest, and its value was nearest to that of c-Si.[5] Given that the absorption coefficient of n-type poly-Si increases as the phosphorus concentration increases, the p-type μc-Si at a doping ratio of 5×10^{-3} had the largest grain size of these samples. Therefore, the dark conductivity of p-type μc-Si is greatest at a doping ratio of 5×10^{-3}.

The Hall effect on the p-type μc-Si films prepared by the SPC method was measured and the carrier concentration in the films was analyzed to find the cause of high dark conductivity of more than 1.0×10^{2} $(\Omega cm)^{-1}$. Figure 3.2-13 shows the carrier concentration in the p-type μc-Si films as a function of boron concentration, where the SPC conditions are 700 °C for 3 hours. The boron concentration was measured by SIMS. In Fig. 3.2-13, the dashed line shows that the activation ratio of boron atoms is 100 %. In the boron concentration of 4×10^{20} - 2×10^{21} cm^{-3}, the activation ratio of boron atoms was nearly 100 %, and a maximum carrier concentration of about 2×10^{21} cm^{-3} was obtained. It was found that the high activation ratio of boron atoms at the high boron concentration was the main reason for the high dark conductivity in the p-type μc-Si films prepared by the SPC method.

Figure 3.2-14 compares the absorption coefficients of p-type μc-Si films prepared by the SPC method, and p-type μc-Si:H[9] and a-SiC:H[10] films prepared by the conventional plasma-CVD method. The absorption coefficient of p-type μc-Si prepared by the SPC method was smaller than that for the films prepared by the conventional plasma-CVD method, in the 2.1 to 3.0 eV region. Figure 3.2-15 shows a comparison of mobility of p-type μc-Si films prepared by the SPC method and the conventional plasma-CVD method. In carrier concentrations as high as two orders of magnitude, the mobility of p-type μc-Si prepared by the SPC method, which was 7 - 13 cm^2/Vs, was almost equal to that of the p-type μc-Si:H prepared by the plasma-CVD method. Thus, using the SPC method, p-type μc-Si films with a higher conductivity and lower absorption coefficient can be prepared.

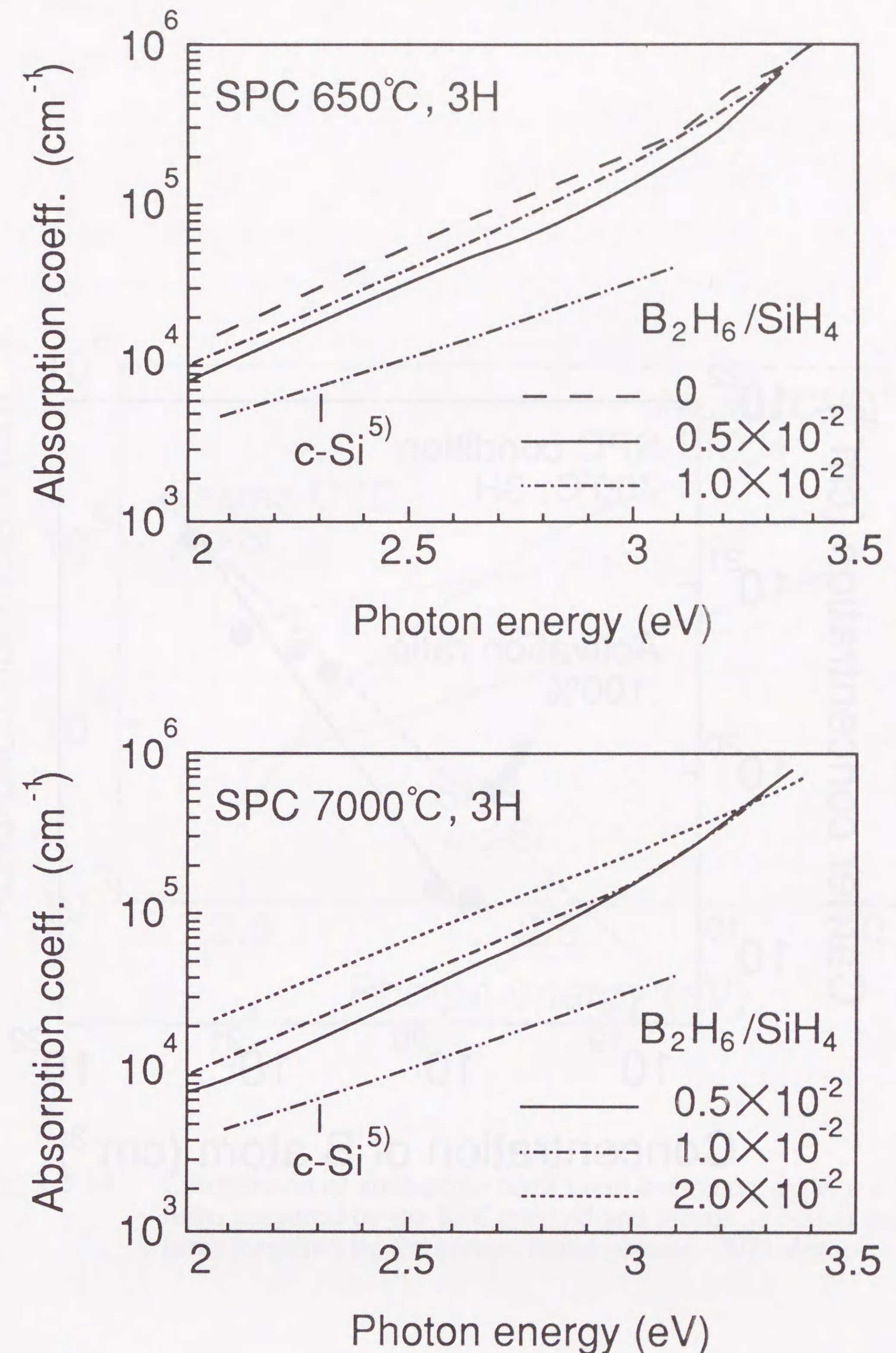


Fig. 3.2-12 The dependence of absorption coefficient of p-type μc-Si prepared by the SPC method on the doping ratio (B_2H_6/SiH_4), where SPC conditions are 650℃ for 3 hours and 700℃ for 3 hours.

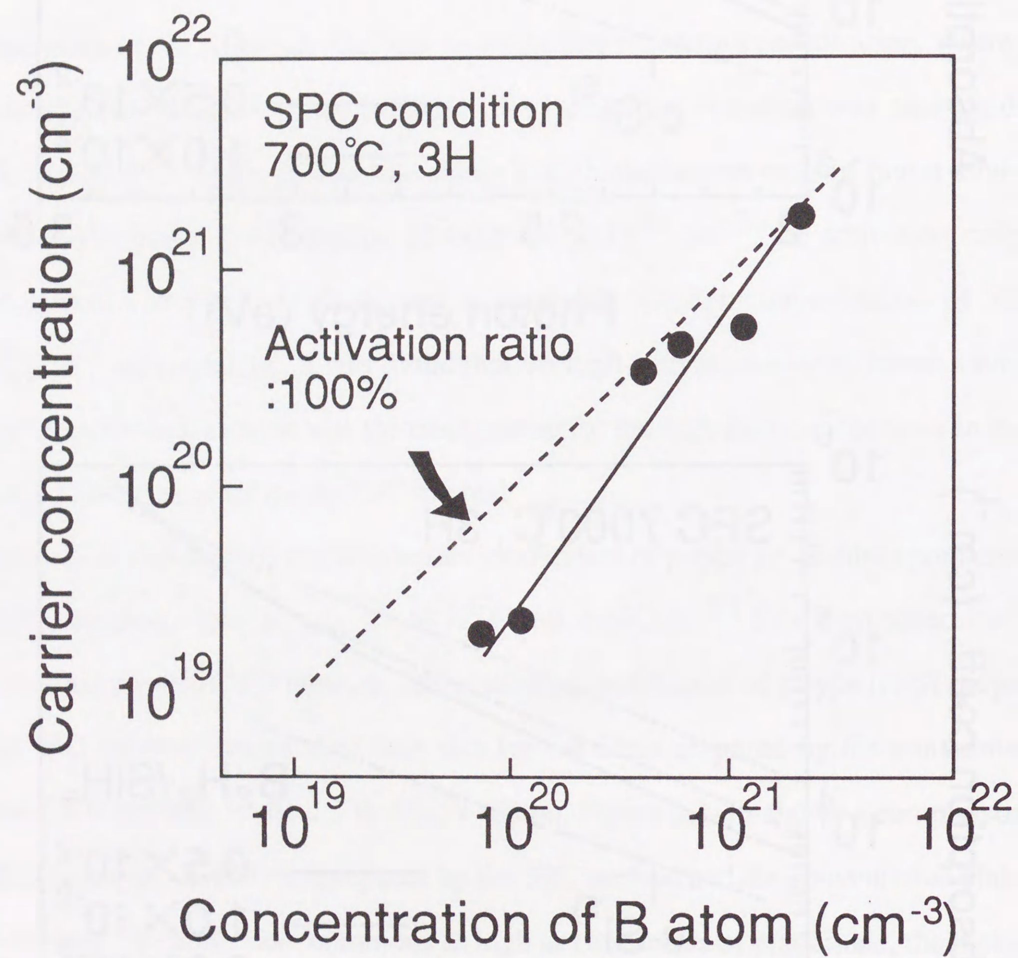


Fig. 3.2-13 Carrier concentraion in the p-type μ c-Si films as a function of boron concentration in the p-type μ c-Si films, where the SPC conditions are 700℃ for 3 hours and the boron concentraion was measured by SIMS.

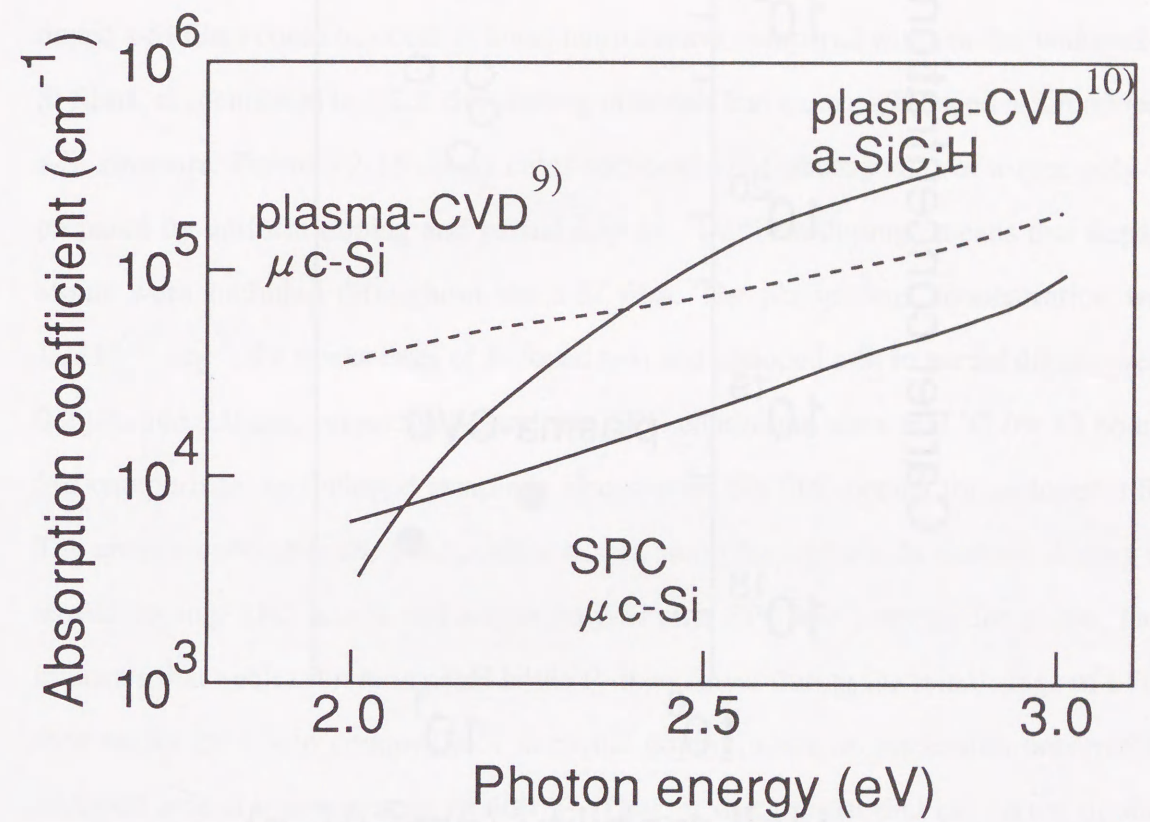


Fig. 3.2-14 Comparison of absorption coefficient between p-type μ c-Si films prepared by the SPC method and p-type μ c-Si:H and a-SiC:H films prepared by the conventional plasma-CVD method.

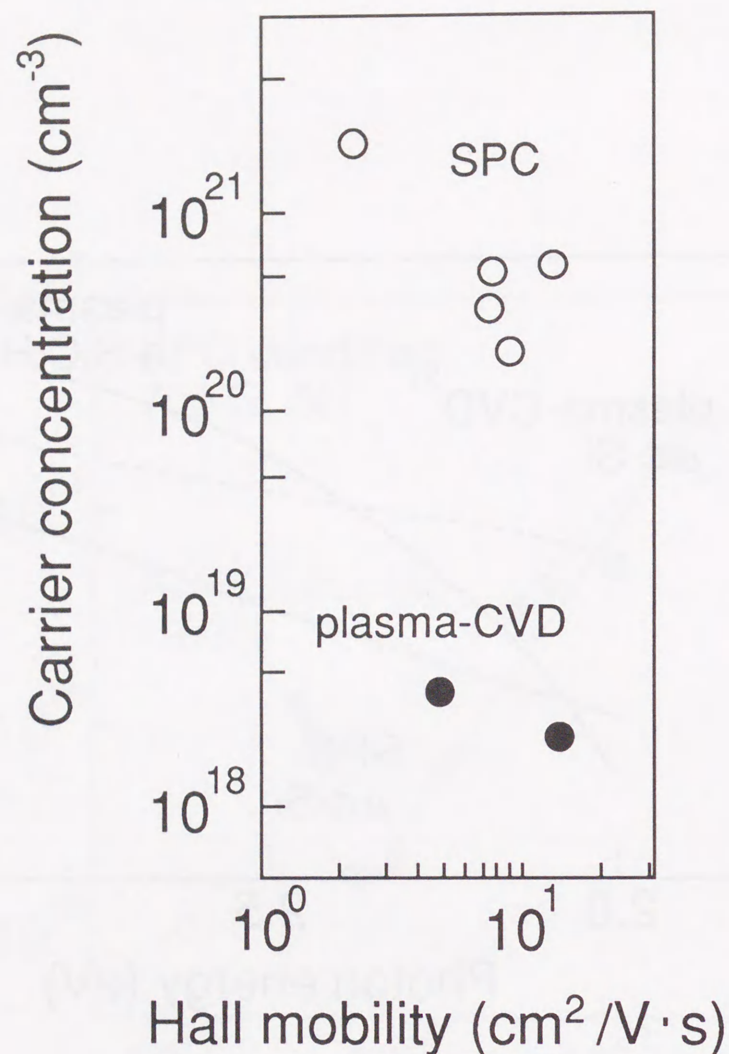


Fig. 3.2-15 Comparison of Hall mobility between p-type μ c-Si films prepared by the SPC method and the conventional plasma-CVD method.

3.2.3. Partial doping

It is necessary to control nucleus generation during the SPC process for the improvement of n-type poly-Si film properties. The partial doping method was developed to suppress nucleus generation. This method offers a means of preparing n-type poly-Si from starting materials separated nucleus generation and crystal growth layers. P-doped a-Si films were used as the nucleus generation layer, because the crystallization of P-doped a-Si films could be occur at lower temperatures compared with that for undoped a-Si films, as mentioned in 3.2.2. So, starting materials had a quartz/P-doped a-Si/undoped a-Si structure. Figure 3.2-16 shows cross-sectional SEM photographs of n-type poly-Si prepared by uniform doping and partial doping. "Uniform doping" means that dopant atoms were included throughout the a-Si film. The phosphorus concentration was 1.2×10^{20} cm^{-3}; the thicknesses of P-doped a-Si and undoped a-Si in partial doping were 0.2 μm and 2.0 μm, respectively; and, the SPC conditions were 600 °C for 10 hours. For comparison, an undoped sample is also shown. No SPC occurs for undoped a-Si. The cross section after the SPC process has an amorphous phase. In uniform doping or partial doping, SPC occurs and n-type poly-Si after SPC had a crystalline phase. This indicates that nucleation took place in the P-doped layer during the initial stage of SPC, then nuclei grew into undoped a-Si in partial doping, since no nucleation occurred in undoped a-Si at a temperature of 600 °C. Thus, it was proven that the partial doping method could control the position of nucleation. Another interesting feature was that the phosphorus concentration in the n-type poly-Si prepared by the partial doping method was uniformly about 2×10^{18} cm^{-3} in depth after SPC.

Figure 3.2-17 shows the N_t for n-type poly-Si prepared by partial doping and uniform doping. The N_t in n-type poly-Si prepared by partial doping decreased more than that for film prepared by uniform doping, dropping to a minimum value of 4.6×10^{11} cm^{-2}.

To clarify the effects of partial doping method on crystallization of a-Si films, nuclei density was analyzed in P-doped a-Si films (nucleus-generation layer) for various deposition temperatures (Ts) and SPC temperatures. Figure 3.2-18 shows the density of nucleus grown in the P-doped a-Si:H layer as a function of Ts, for SPC temperatures of 500, 550 and 600 °C. At each SPC temperature, the density of nucleus generation

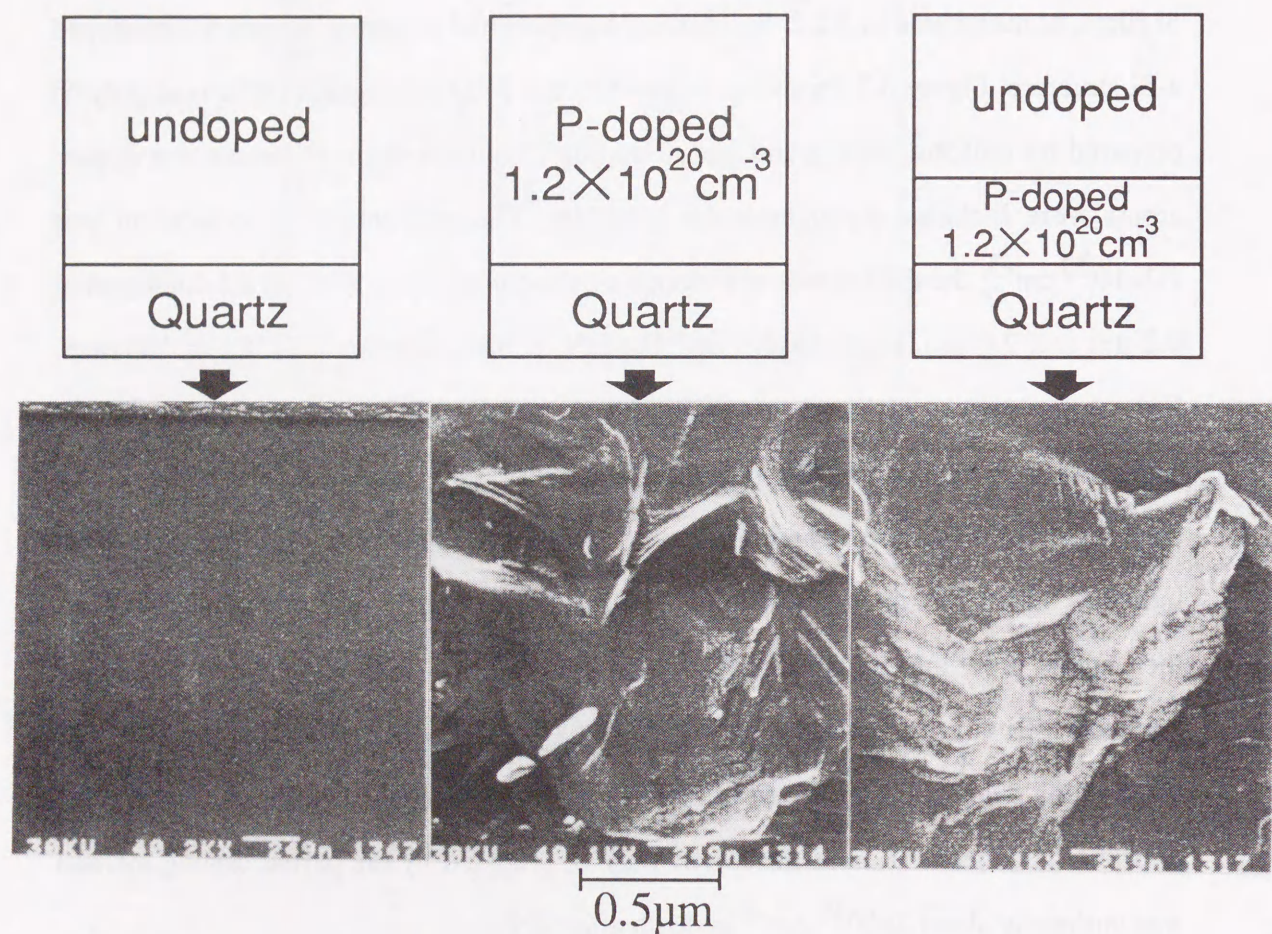


Fig. 3.2-16 The cross-sectional SEM photographs of n-type poly-Si prepared by uniform doping and partial doping and undoped a-Si after the SPC process, where the phosphorus concentration is $1.2\times10^{20}cm^{-3}$ and the SPC conditions are 600℃ for 10 hours.

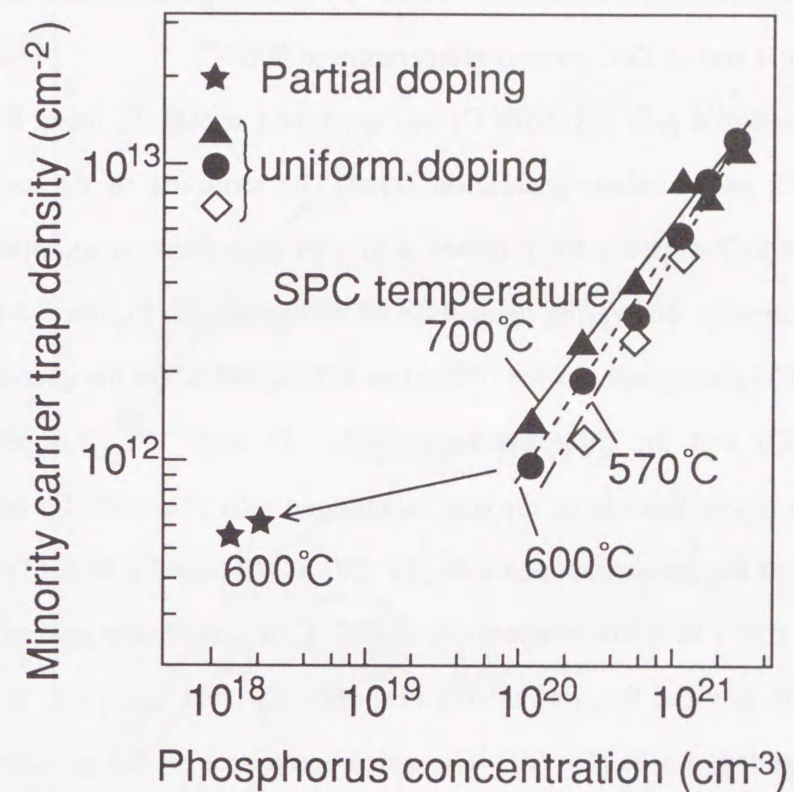


Fig. 3.2-17 The comparison of the minority carrier trap density Nt in n-type poly-Si prepared by partial doping and uniform doping.

increased as Ts increased and reach a maximum value at a Ts in the range of 300 - 350 °C. Finally, no SPC becomes to occur at 500 °C. For a-Si:H films prepared at the same temperature, the density of nucleus decreased with decreasing the SPC temperature. So, in order to minimize the number of nuclei, it is need to decrease both the Ts of P-doped a-Si:H and the SPC temperature. In this experiment, it was found that the density of nucleus could be decreased to 2 - 3 /μm^2 by choosing a deposition temperature of 200 °C for a-Si:H and an SPC process temperature of 500 °C.

The SPC of undoped a-Si (Ts: 650 °C) was examined at 500 °C, using P-doped a-Si:H (Ts: 200 °C) as a nucleus-generation layer. The structure of the sample was quartz/undoped a-Si/P-doped a-Si. P-doped a-Si was deposited on undoped a-Si to prevent thermal damage during the deposition of undoped a-Si. Figure 3.2-19 shows cross-sectional SEM photographs of the films after SPC at 500 °C for the quartz/undoped a-Si (Ts: 650 °C) and the quartz/undoped a-Si (Ts: 650 °C) /P-doped a-Si:H (Ts: 200 °C). No crystallization of the quartz/undoped a-Si (Ts: 650 °C) occurred at 500 °C. The SPC of the quartz/undoped a-Si (Ts: 650 °C) /P-doped a-Si:H (Ts: 200 °C), however, did occur at a very low temperature of 500 °C. It was proven again that nuclei were generated in only the P-doped a-Si:H (Ts: 200 °C) layer and grew to a size of 2 - 3 μm in the undoped a-Si (Ts: 650 °C), which acted as a crystal-growth layer, as illustrated in Figure 3.2-20. This experiment also showed an interesting result in that solid-phase crystallization occurred at a temperature lower than Ts. In order to investigate the influence of the number of nuclei generated in the P-doped a-Si:H (Ts: 200 °C), SPC of quartz/undoped a-Si (Ts: 650 °C)/P-doped a-Si:H (Ts: 200 °C) was performed at three different temperatures, 500, 550 and 600°C. Figure 3.2-21 shows cross-sectional SEM photographs of the films after SPC at the three different temperatures for 10 hours. At all SPC temperatures, SPC of undoped a-Si, which was the crystal-growth layer, occurred. It was also found that the grain size of poly-Si increased with decreasing the SPC temperature between 500 and 600 °C, because the density of nuclei generated in the P-doped a-Si:H (Ts: 200 °C) decreased with decreasing the SPC temperature as shown in Fig. 3.2-18. Therefore, it was proven that the poly-Si thin films with large grains could be grown by decreasing the density of nuclei generated during the initial stage of SPC,

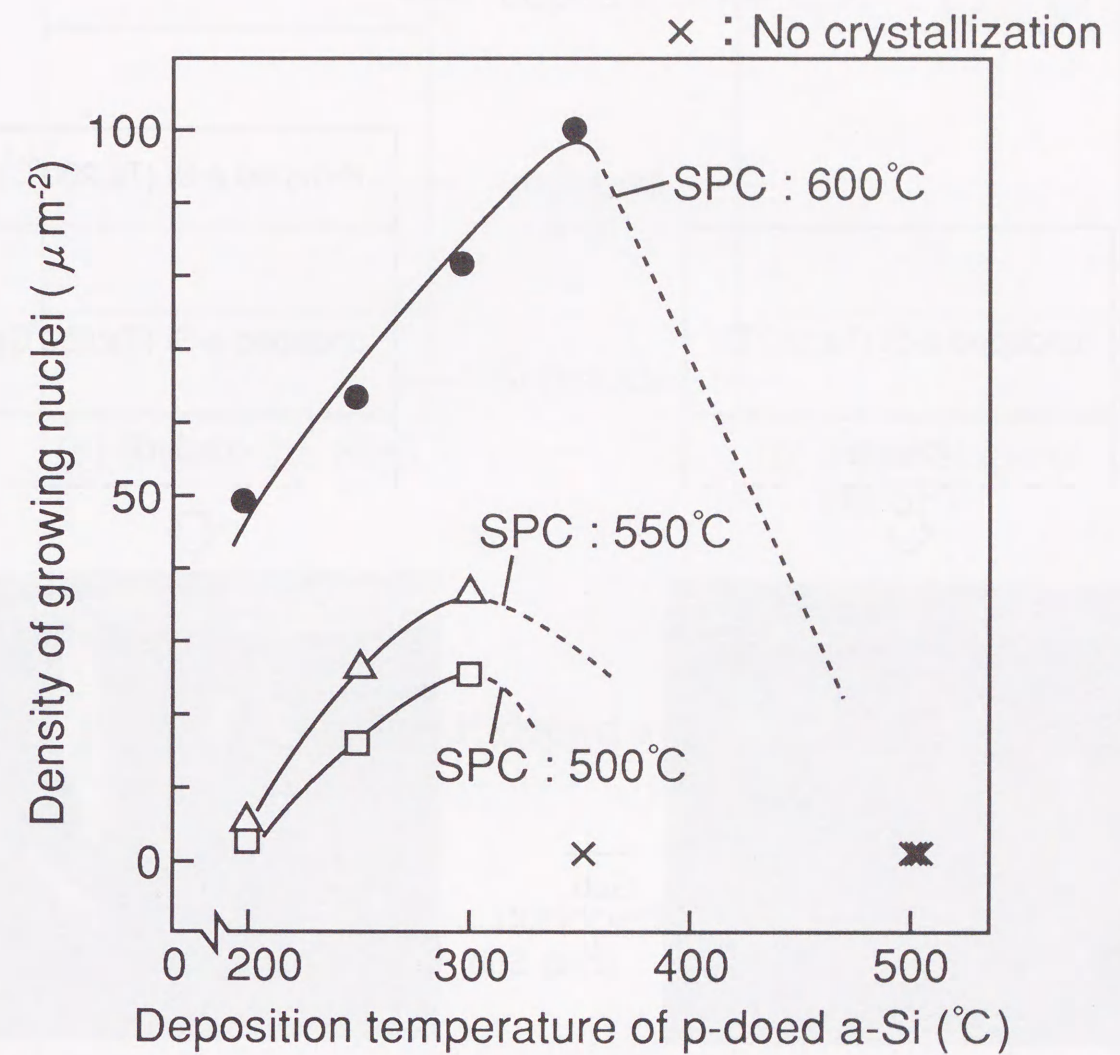


Fig. 3.2-18 The density of growing nuclei in P-doped a-Si:H layer as a function of its Ts, for various SPC temperatures of 500℃, 550℃ and 600℃.

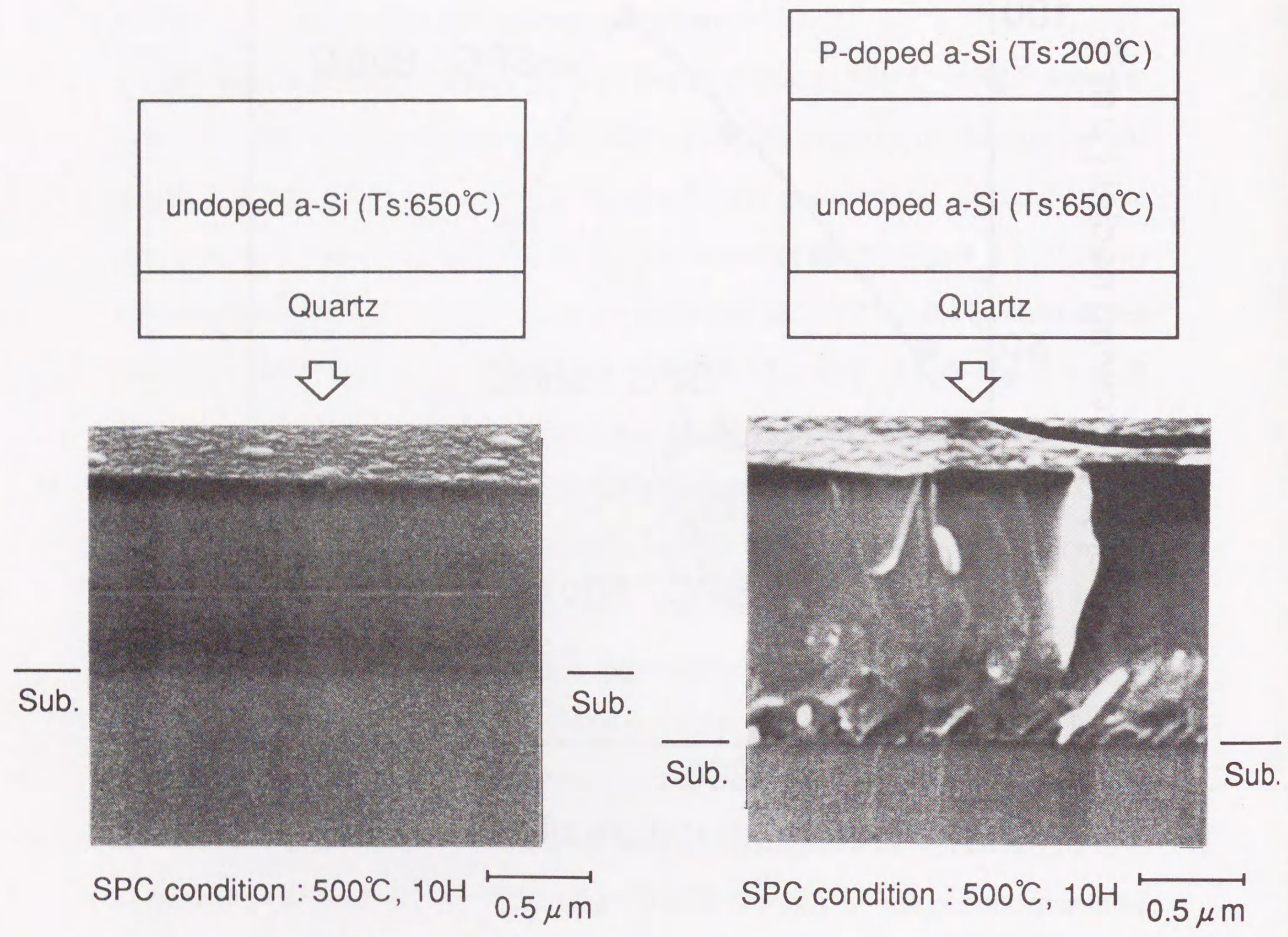


Fig. 3.2-19 The cross-sectional SEM photographs of the films after the SPC at 500℃ of the quartz/undoped a-Si (Ts:650℃) and the quartz/undoped a-Si(Ts:650℃) P-doped a-Si:H(Ts:200℃).

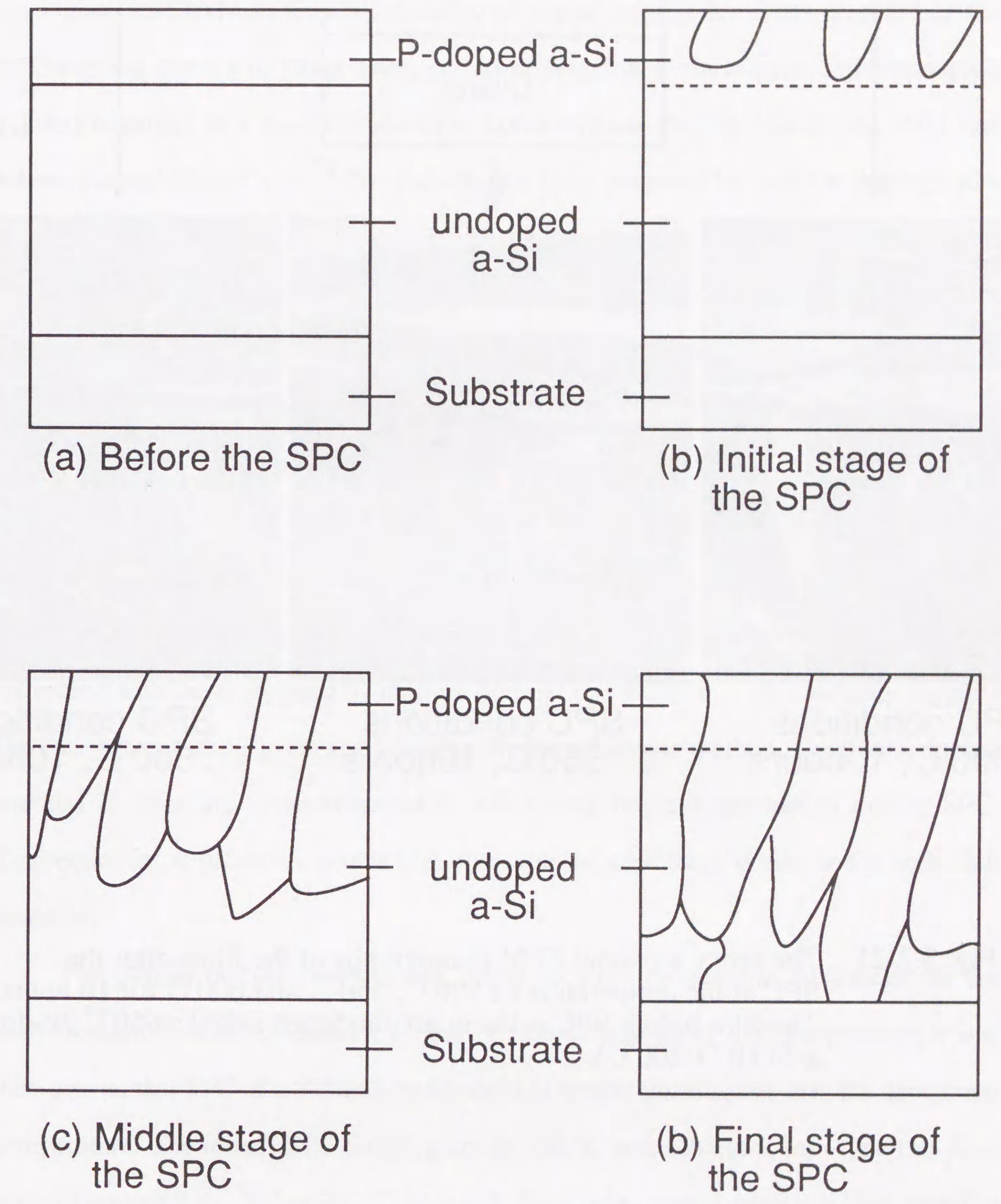


Fig. 3.2-20 The model for growth kineties in the SPC, using the a-Si film prepared by the partial doping method.

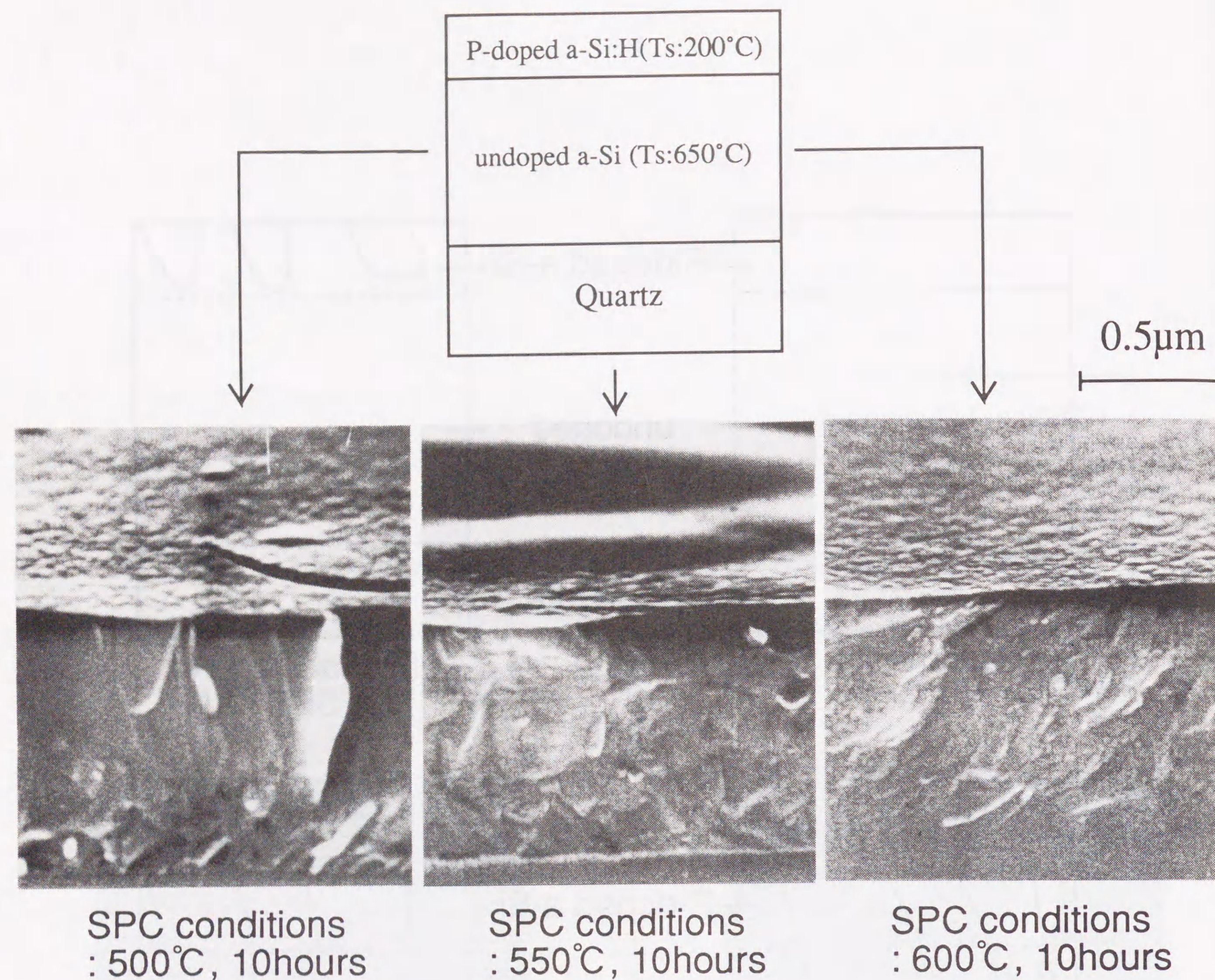


Fig. 3.2-21 The cross-sectional SEM photographs of the films after the SPC at the temperature of 500℃, 550℃ and 600℃ for 10 hours. The film before SPC is the quartz/undoped a-Si(Ts:650℃)/P-doped a-Si:H(Ts:200℃).

and that SPC of a-Si films prepared by plasma-CVD could occur at a temperature lower than the deposition temperature, if the partial doping method of separating the nucleus-generation and crystal-growth layers was used.

Figure 3.2-22 shows the Hall mobility of n-type poly-Si thin-films prepared by the SPC method from a-Si films using partial doping (open circle) and uniform doping (closed triangle) as a function of carrier concentration. In Fig. 3.2-22, the solid line shows the mobility of c-Si.[7] The poly-Si thin-films prepared by uniform doping had a mobility of 4 - 70 cm^2/Vs in the carrier concentration region of $2x10^{18}$ to $5x10^{20}$ cm^{-3}. The maximum mobility value was 70 cm^2/Vs at a carrier concentration of $1x10^{19}$ cm^{-3}. On the other hand, poly-Si thin-films prepared by partial doping have a mobility of 40 to 196 cm^2/Vs in the region of $1x10^{18}$ to $8x10^{18}$ cm^{-3}. Thus, carrier concentration in poly-Si thin films prepared by partial doping is reduced. The highest value obtained was 196 cm^2/Vs at a carrier concentration of $1x10^{18}$ cm^{-3}. This value is as high as about 60 % of value of c-Si at the same carrier concentration. So, it was found that the poly-Si thin-films prepared by partial doping have higher mobility at lower carrier concentrations, compared with those prepared by uniform doping. The increase of Hall mobility supports the enlargement of the grain size by using the partial doping method. The partial doping method is therefore more effective in controlling nucleus generation during SPC. Consequently, it promotes n-type thin-film poly-Si with large grains and a high Hall mobility.

The partial doping method was found to have remarkable advantage on the improvement in mobility, increase of grain size, and decrease of SPC temperature. It was also proven that SPC of a-Si films could occur at temperatures lower than the deposition temperature. The lowest SPC temperature of 500 °C was achieved. In n-type thin-film poly-Si prepared by SPC at 500 °C from a-Si films using partial doping, a high mobility of 196 cm^2/Vs was obtained at a carrier concentration of $1x10^{18}$ cm^{-3}.

In summary, it was found that phosphorus and boron used as dopants for silicon facilitated nucleation during the SPC process and consequently, decreased the critical temperature of solid-phase crystallization, compared with undoped films. The partial doping method that the nucleation occurred only in a nucleus-generation layer (doped a-

Si) and then, nuclei were grown up to crystal growth layer (undoped a-Si) was developed. As a result, thin-film poly-Si with large grains could be prepared, and the critical temperature of solid-phase crystallization was decreased to 500 °C. It was also confirmed that n-type poly-Si prepared by the partial doping method had mobility higher than that prepared by uniform doping.

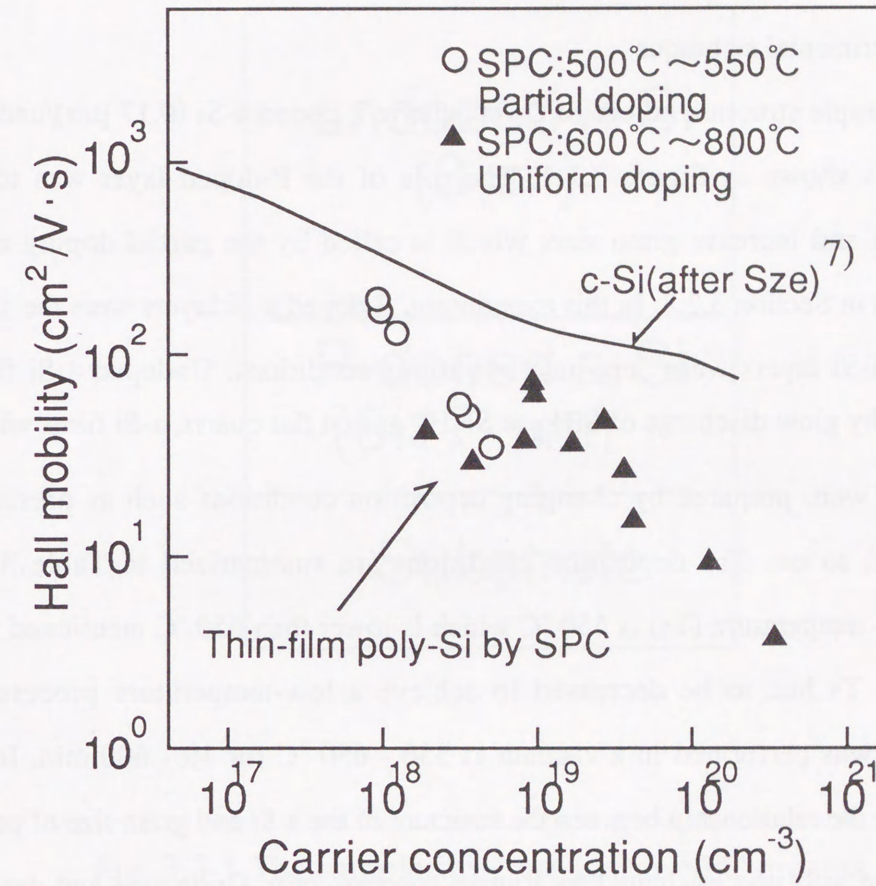


Fig. 3.2-22 The Hall mobility of n-type poly-Si thin-films prepared by the SPC method from a-Si films using the partial doping (open circle) and uniform doping (closed triangle) as a function of carrier concentration.

3.3 Optimum starting materials for the SPC method

In Section 3.2, it was shown that separating the nucleus-generation layer from the crystal-growth layer was effective for the improvement of thin-film poly-Si properties. In this section, the structural analysis of the undoped a-Si (crystal-growth layer) suited to solid-phase crystallization, and growth kinetics for thin-film poly-Si with large grains are described.

3.3.1 Experimental technique

The sample structure before SPC was quartz/P-doped a-Si (0.17 μm)/undoped a-Si (3 μm), as shown in Figure 3.3-1. The role of the P-doped layer was to enhance nucleation and increase grain size, which is called by the partial doping method as mentioned in Section 3.2.3. In this experiment, P-doped a-Si layers were the same; only undoped a-Si layers were deposited at various conditions. Undoped a-Si films were deposited by glow discharge of SiH_4 or Si_2H_6 gas on flat quartz. a-Si films with various structures were prepared by changing deposition conditions such as pressure, R. F. power and so on. The deposition conditions are summarized in Table 3.3-1. The deposition temperature (Ts) is 550 °C which is lower than 650 °C mentioned in section 3.2, since Ts had to be decreased to achieve a low-temperature process. Sample annealing was performed in a vacuum at 550 - 650 °C for 10 - 600 min. In order to investigate the relationship between the structure of the a-Si and grain size of poly-Si, the structure of a-Si was evaluated by Raman spectroscopy. Grain size and density were measured using SEM images after Secco's etching or from transmission electron microscopy (TEM) images.

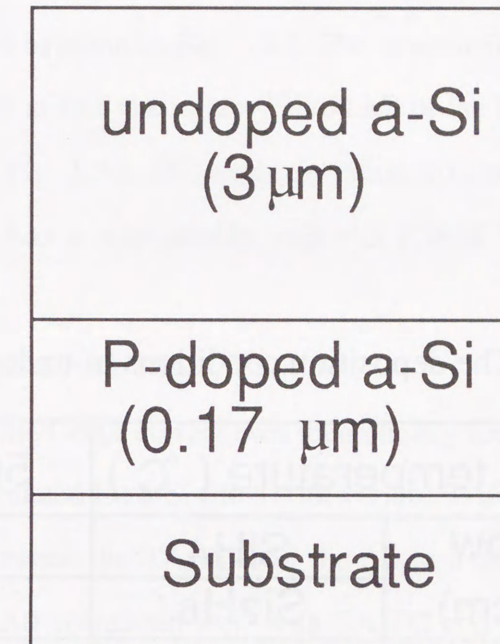


Fig. 3.3-1 The sample structure before SPC process.

Table 3.3-1 The deposition conditions of undoped a-Si films.

Substrate temperature (℃)		500 - 600
Gas flow rate (sccm)	SiH_4	30 - 50
	Si_2H_6	10 - 20
R. F. power (mW/cm^2)		100 - 300
Pressure (Pa)		30 - 70

3.3.2 Evaluation of structural disorder in starting materials

The structural disorder of a-Si films before SPC was analyzed. Figure 3.3-2 shows the typical Raman spectrum of the a-Si film. Two prominent peaks are observed at about 480 cm^{-1} and 150 cm^{-1}. These peaks are attributed to the transverse optical (TO) band and transverse acoustic (TA) band, respectively. It has been reported that the TA peak height divided by the TO peak height is the sensitive probe of the structural disorder of a-Si.[11] So, TA/TO was used as a parameter for structural disorder. The peak heights were measured from the dashed baseline in Fig. 3.3-2. The statistical error of TA/TO is less than $\pm$ 0.02. The full width at half maximum (F.W.H.M) of the TO peak was defined as $2x\Gamma$, using Γ as shown in Fig. 3.3-2. The angle deviation from bond angle 109.5° in the Si-Si bond of c-Si, $\Delta\theta$, has a relationship with the F.W.H.M. of the TO peak as follows:[12]

$$(\text{F.W.H.M.}=2x\Gamma)=15+6\Delta\theta. \qquad (3.3\text{-}1)$$

Equation 3.3-1 was confirmed to be correct both theoretically and experimentally. Using Eq. 3.3-1, the $\Delta\theta$ was calculated for a-Si films with various TA/TO values. Figure 3.3-3 shows the correlation between the TA/TO and the $\Delta\theta$ in a-Si films deposited under various conditions. The $\Delta\theta$ correlated well with TA/TO and its value was found to increase as TA/TO increased. The distortion energy in a-Si film was proportional to the square of $\Delta\theta$.[13] So, it was found that a-Si films with large TA/TO values stored large distortion energy.

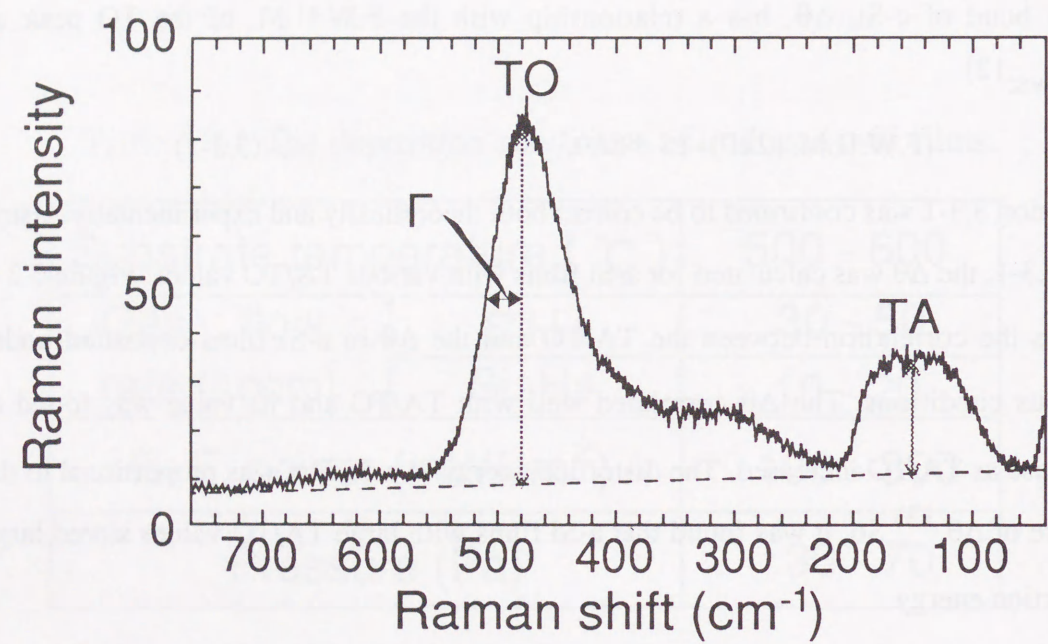


Fig. 3.3-2 The typical Raman spectrum of the a-Si film prepared by plasma-CVD method.

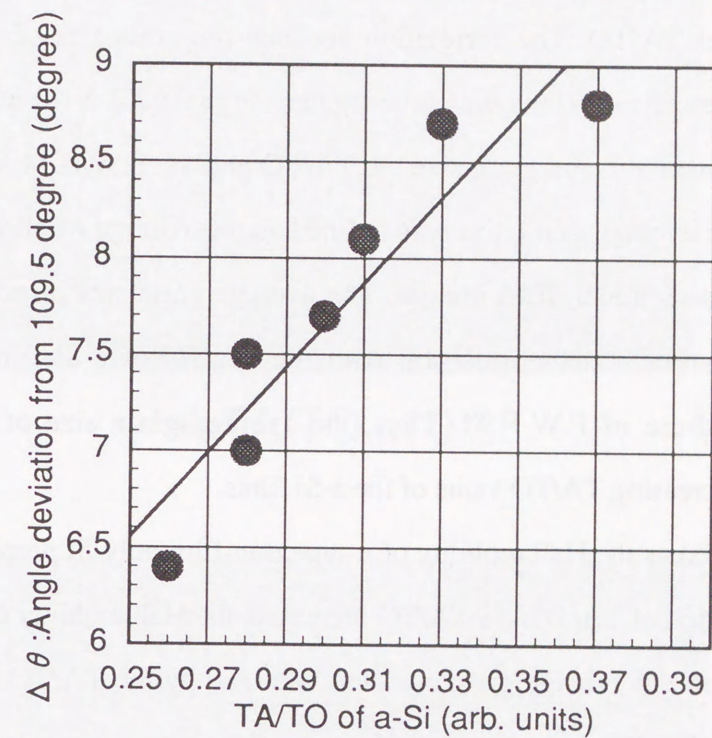
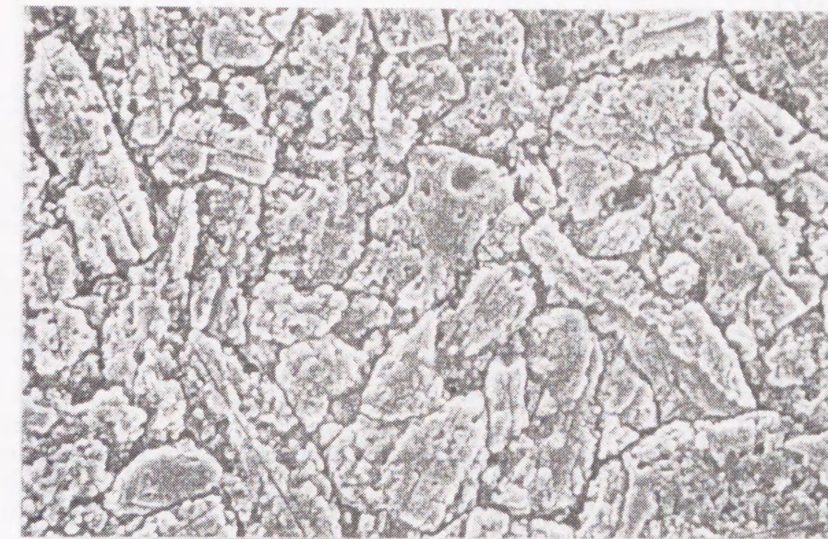


Fig. 3.3-3 The relationship between the TA/TO and the $\Delta\theta$ in a-Si films deposited under various conditions.

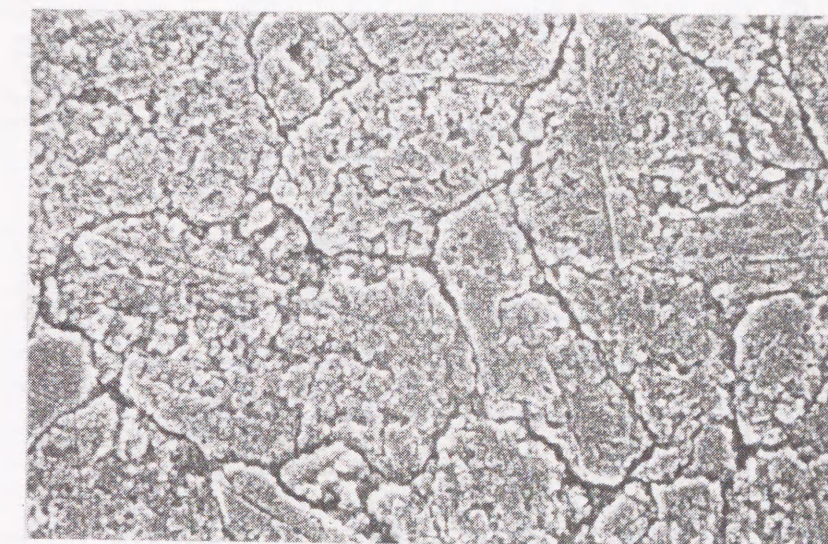
3.3.3 Correlation between grain size of polycrystalline silicon and structural disorder of starting materials

Figures 3.3-4 (a) and (b) show SEM images of thin-film poly-Si films after Secco's etching, the TA/TO of which are 0.28 and 0.37, respectively. The SPC conditions were 600 °C for 10 hours. The grain size after SPC clearly becomes large by using the a-Si film with a larger TA/TO. The correlation between the grain size of poly-Si and the structural disorder of a-Si films was investigated. Figures 3.3-5 (a) and (b) show the relationship between average grain size vs. TA/TO and vs. F.W.H.M. of the TO peak, respectively. The average grain size was defined as the average of all grains visible in surface and cross-sectional SEM images. The average grain size of poly-Si after SPC was found to have a better correlation with the TA/TO of a-Si films before SPC, compared with those of F.W.H.M. Thus, the average grain size of n-type poly-Si increased with increasing TA/TO value of the a-Si films.

Figure 3.3-6 shows the Hall mobility of n-type thin-film poly-Si prepared by the SPC method as a function of TA/TO. As TA/TO increased, the Hall mobility of n-type poly-Si increased, because the average grain size was enlarged by the TA/TO. Therefore, a-Si films with large TA/TO values have effects on the improvement of structural and electronic properties in the poly-Si after SPC.

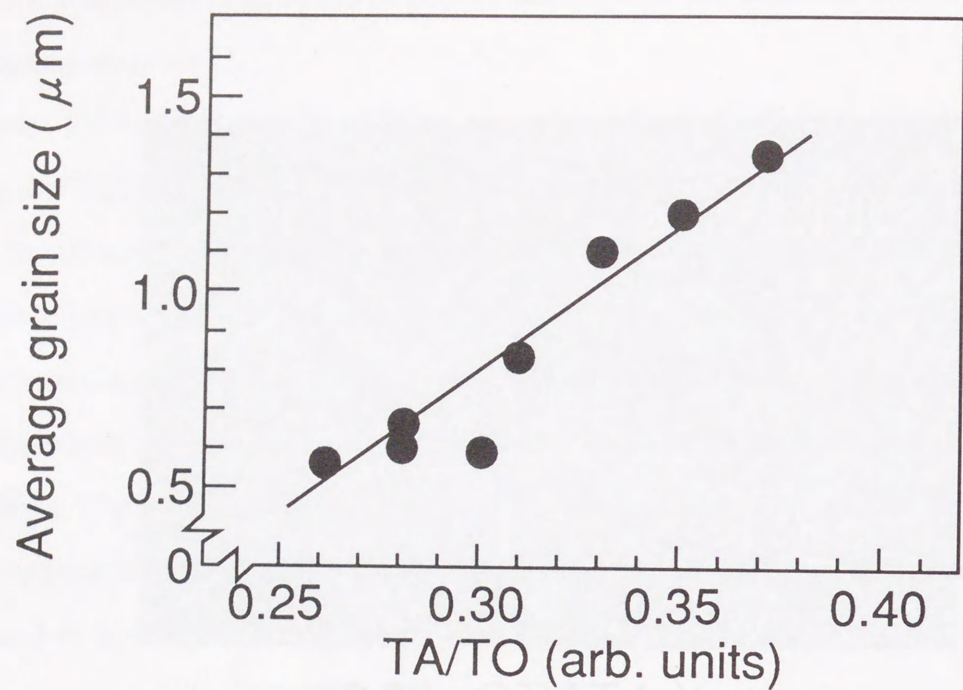


(a) TA/TO of 0.28

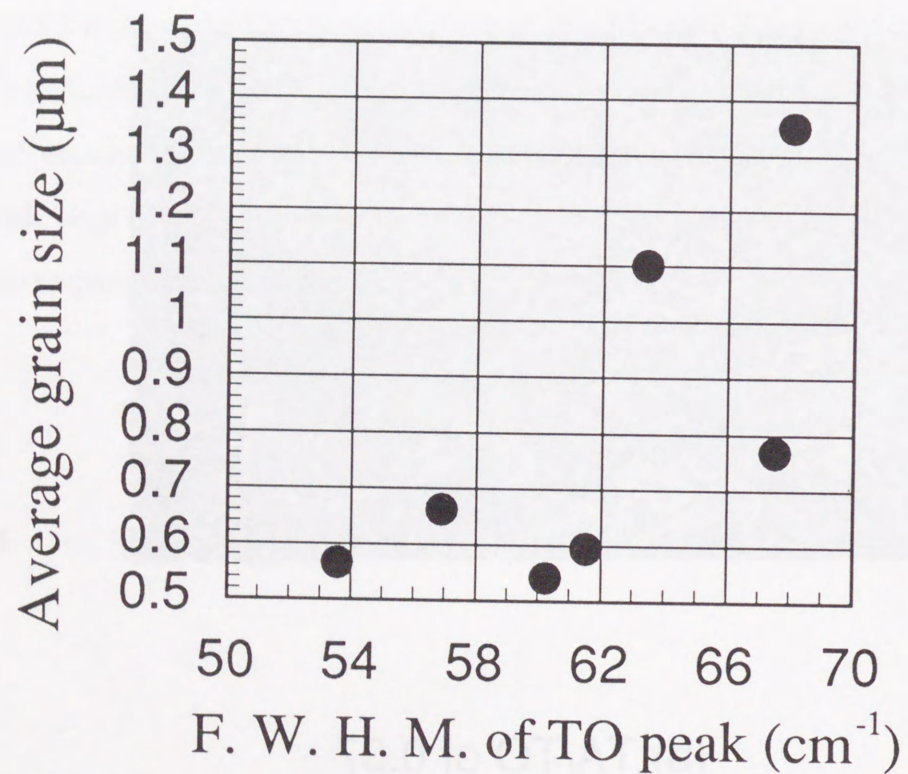


(b) TA/TO of 0.37

Fig. 3.3-4 SEM images of thin-film poly-Si films after Secco's etching, where (a) is the TA/TO of 0.28 and (b) is the TA/TO of 0.37.



(a) Average grain size vs. TA/TO



(b) Average grain size vs. F. W. H. M. of TO peak

Fig. 3.3-5 The relationship between the average grain size and TA/TO (a), and between that and the F. W. H. M. of TO peak (b).

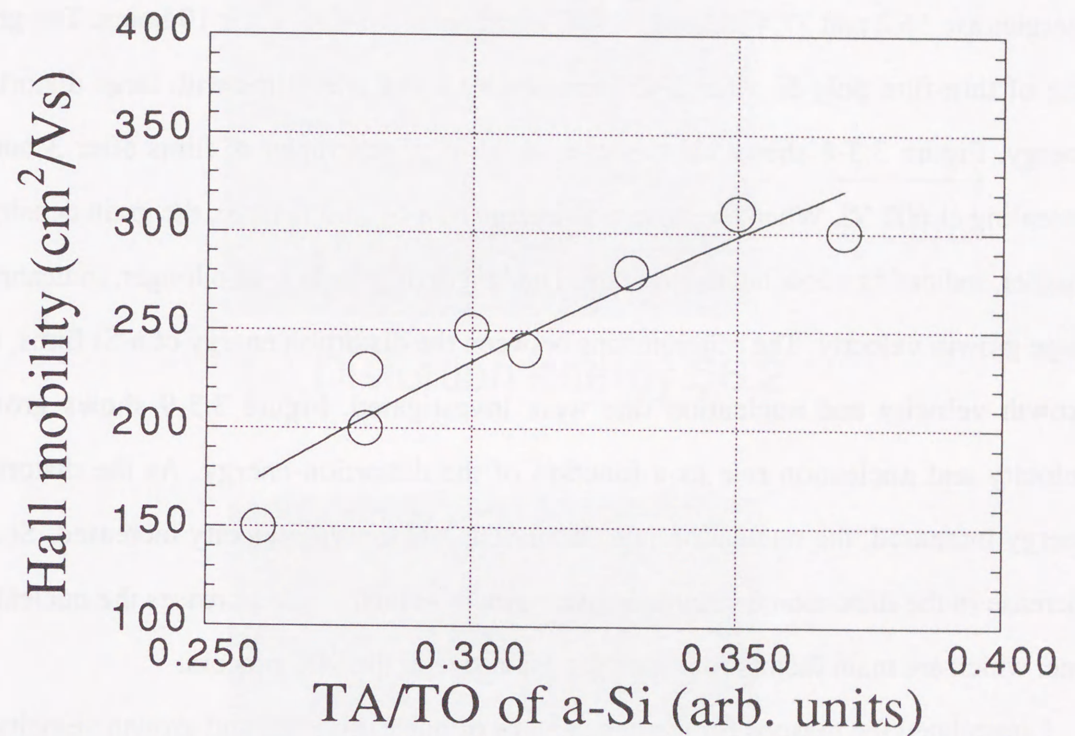


Fig. 3.3-6 The Hall mobility of n-type thin-film poly-Si prepared by SPC method, as a function of TA/TO.

3.3.4 Factors for enlarging grain size in polycrystalline silicon

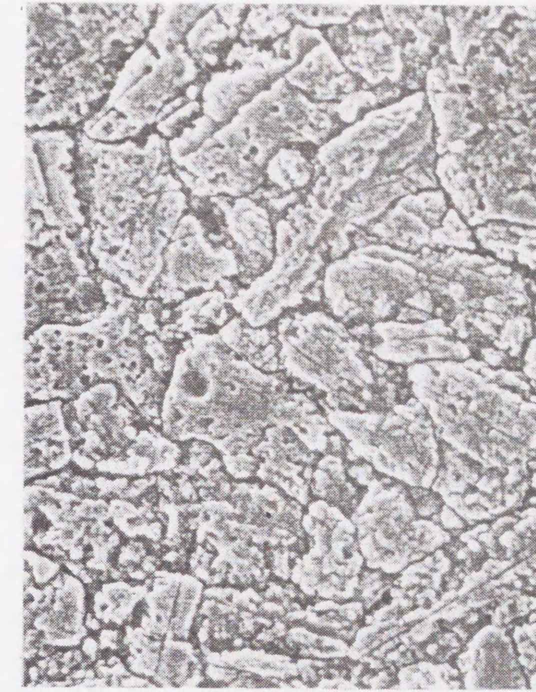
In 3.3.2, it was asserted that a-Si films with large TA/TO value stored large distortion energy. In order to investigate factors for the enlargement of grain size in SPC using a-Si films with large TA/TO values, the dependences of grain size, growth velocity and nucleation rate on distortion energy in a-Si films were examined. Figure 3.3-7 shows the SEM photographs of thin-film poly-Si after Secco's etching, where the distortion energies are 56.2 and 77.4 $(degree)^2$. SPC conditions are 600 °C for 10 hours. The grain size of thin-film poly-Si after SPC increases by using a-Si films with large distortion energy. Figure 3.3-8 shows cross-sectional TEM photographs of films after 3 hours' annealing at 600 °C. When the distortion energy of a-Si film is large, the grain density is smaller, indicating a low nucleation rate. The length of growth is also longer, indicating a large growth velocity. The relationships between the distortion energy of a-Si films, and growth velocity and nucleation rate were investigated. Figure 3.3-9 shows growth velocity and nucleation rate as a function of the distortion energy. As the distortion energy increased, the nucleation rate decreased, and growth velocity increased. So, an increase in the distortion energy increases growth velocity and decreases the nucleation rate, which are main factors for enlarging grain size in the SPC process.

I speculated the reasons for the dependence of nucleation rate and growth velocity on distortion energy. According to a statistical picture of the nucleation and the growth[14)], many clusters of a small size are always created, and some of them are annihilated during SPC. The free-energy change, ΔG_n, on the formation of a crystalline cluster having n atoms in a-Si is given by the following equation:

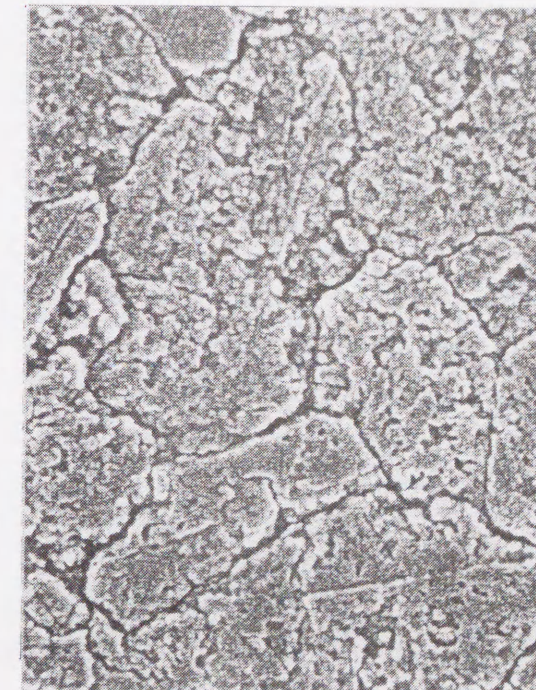
$$\Delta G_n = -n \cdot g + s_n \cdot f \qquad (3.3\text{-}2)$$

where g is the Gibbs free energy difference between the amorphous phase and the crystalline phase per atom (positive value), s_n is the surface area of a cluster of n atoms, and f is the interfacial free energy per unit area. ΔG_n has a maximum value of ΔG_n^* at cluster size of n* which is called the critical size. From Eq. 3.3-2, ΔG_n^* can be expressed analytically by assuming that both f and g are independent of cluster size n:

$$\Delta G_n^* = 4 \cdot \alpha^3 \cdot f^3 / 27 \cdot g^2 \qquad (3.3\text{-}3)$$



(a) Distortion energy:56.2



(b) Distortion energy:77.4

Fig. 3.3-7 The SEM photographs of thin-film poly-Si after Secco's etching, where the distortion energies are 56.2 and 77.4.

(a) Distortion energy:56.2

(b) Distortion energy:75.7

Fig. 3.3-8 The cross-sectional TEM photographs of films after 3hours' annealing at 600°C.

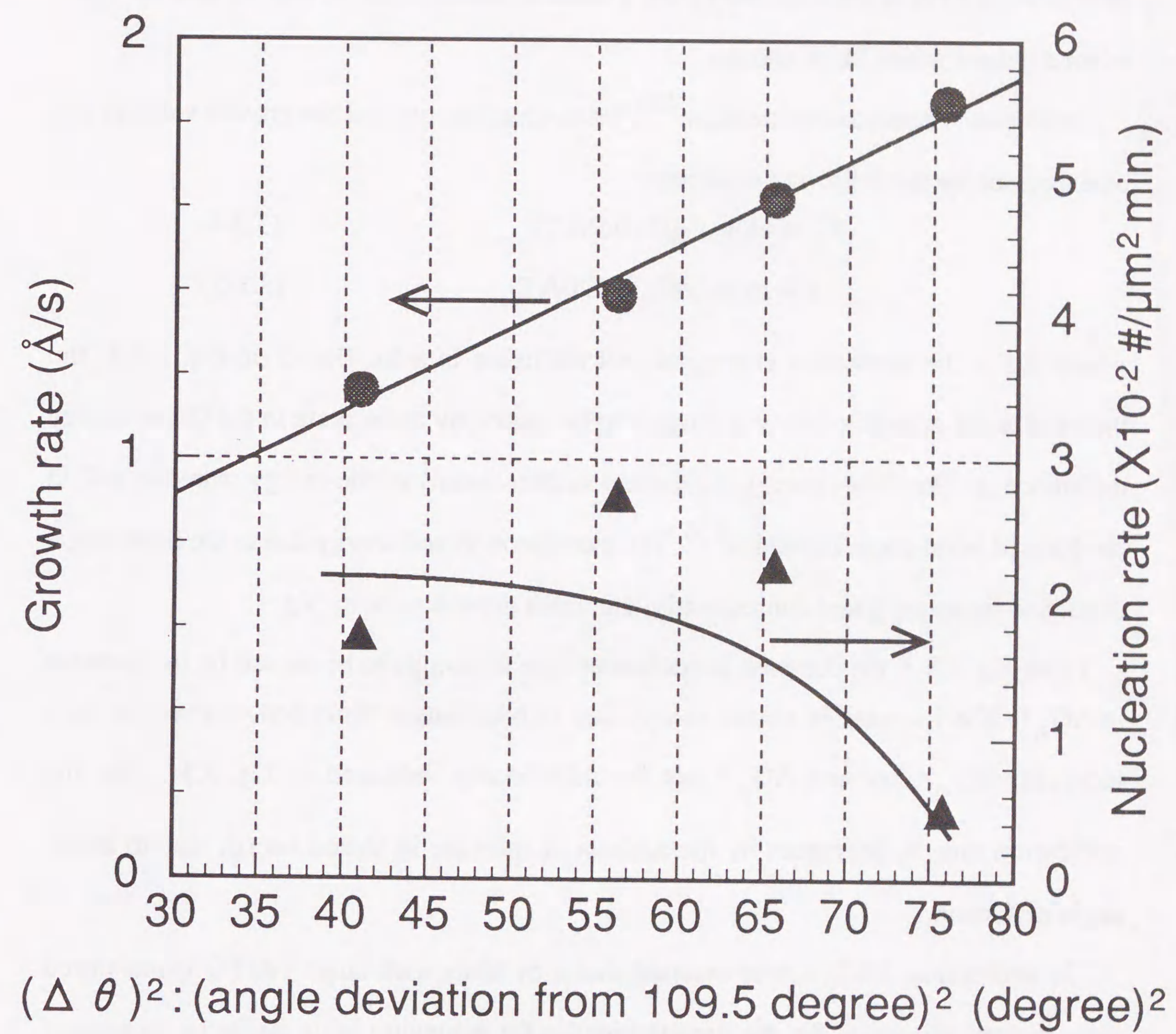


Fig. 3.3-9 The growth velocity and nucleation rate as a function of the distortion energy: $(\Delta\ \theta)^2$.

where α is the surface area factor ($s_n=\alpha \cdot n^{2/3}$). ΔG_n* represents the nuclear formation energy, which is the energy barrier to create stable nuclei. Smaller clusters (n < n*) tend to shrink, and larger clusters (n > n*) or nuclei tend to grow because growth is energetically favorable. Therefore, the nucleation rate is determined from ΔG_n*. The growth velocity is determined only from g because the first term in Eq. 3.3-2 is dominant when a cluster grows large enough.

From more detailed consideration[15], the nucleation rate and the growth velocity can be expressed by the following equations:

$$V_g \propto \exp(-(-g/2+Ed)/kT) \qquad (3.3\text{-}4)$$

$$n \propto \exp(-(\Delta G_n^*+Ed)/kT) \qquad (3.3\text{-}5)$$

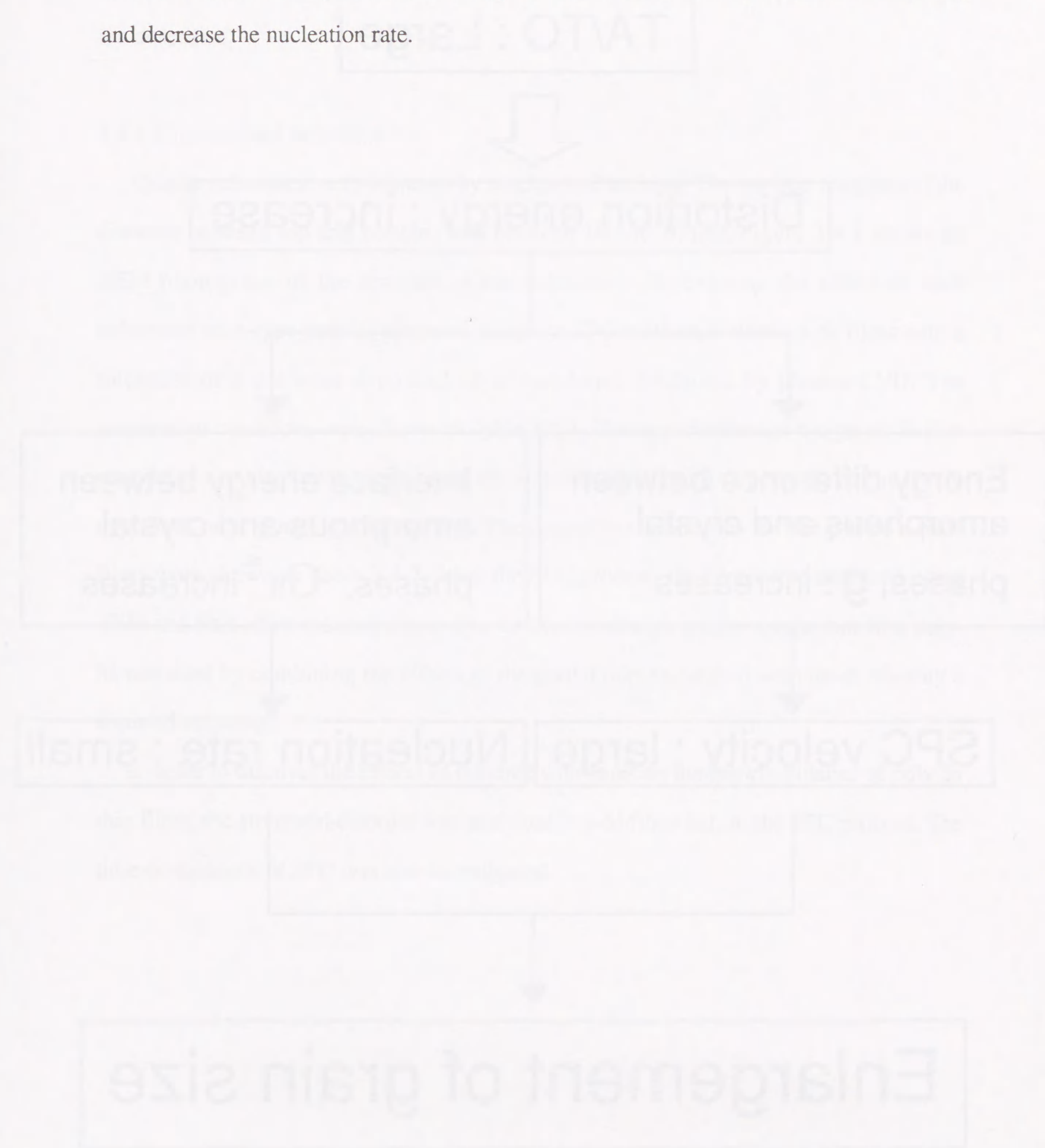
where Ed is the activation energy of self diffusion in a-Si. Based on Eq. 3.3-4, the increase in the growth velocity is thought to be caused by an increase in the Gibbs energy difference, g. The Gibbs energy difference consists mainly of the energy stored in a-Si in the form of bond-angle distortion[13]. The increase in stored energy due to the bond-angle distortion increases g and consequently, increases growth velocity Vg.

From Eq. 3.3-5, the decrease in nucleation rate is thought to be caused by the increase in ΔG_n*. The increase in stored energy due to bond-angle distortion increases f, then increases ΔG_n* because ΔG_n* has the relationship indicated in Eq. 3.3-3. So, the nucleation rate, n, decreases by the amount of increase in stored energy due to bond-angle distortion.

In subsection 3.3.2, it was asserted that a-Si films with large TA/TO value stored large distortion energy. So, the growth kinetics for achieving large grains by increasing TA/TO was proposed, as shown in Figure 3.3-10. The increases in TA/TO create large distortion energies stored in a-Si films. This large distortion energy has two effects on solid-phase crystallization. One is the increase of growth velocity caused by an increase in the Gibbs energy difference, g. The other is a decrease in the nucleation rate caused by an increase in ΔG_n*. The increase in growth velocity and decrease in nucleation rate enlarge the grain size after SPC process.

In summary, it has been found that the TA/TO of a-Si films before SPC correlated well with the average grain size of poly-Si after SPC, and that the average grain size

increased with increasing the TA/TO. Enlarged grain size results from increasing the TA/TO because the large distortion energy stored in a-Si film increase the growth velocity and decrease the nucleation rate.



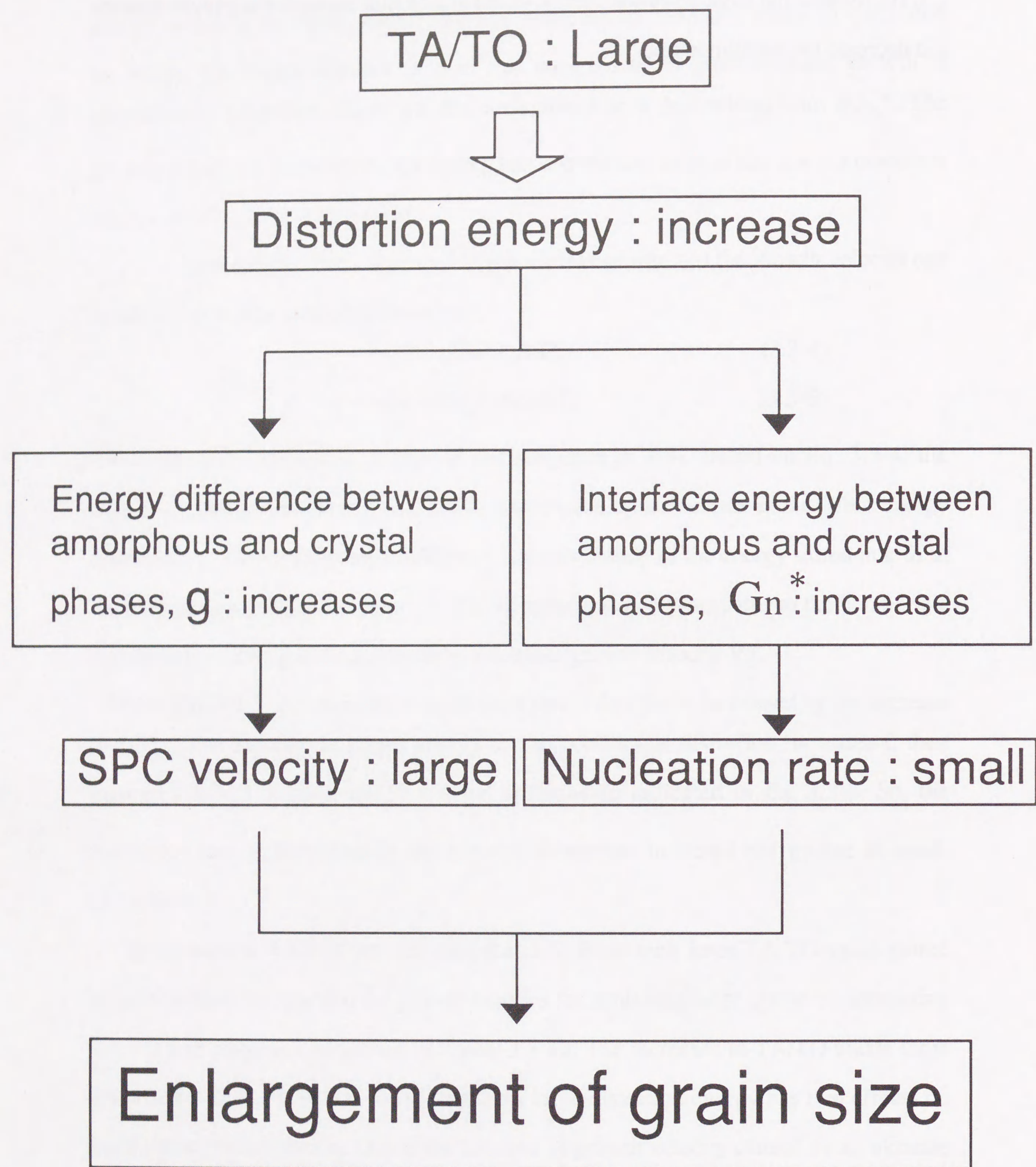


Fig. 3.3-10 The growth kinetics for large grain by increasing TA/TO.

3.4 Investigation of substrates

In this section, the effects of textured substrate and growth kinetics on such substrates are described.

3.4.1 Experimental technique

Quartz substrates were textured by mechanical etching. The surface roughness (the distance between top and bottom) was between 10 and 20 μm. Figure 3.4-1 shows an SEM photograph of the textured quartz substrates. To examine the effect of such substrates on n-type poly-Si prepared using the SPC method, P-doped a-Si films with a thickness of 2 μm were deposited on textured and flat quartz by plasma-CVD. The preparation conditions were shown in Table 3.4-1. The improvement of p-type μc-Si film properties was also investigated using the textured substrate. B-doped a-Si:H films were deposited on textured and flat quartz. The deposition conditions for the p-type a-Si:H films were shown in Table 3.4-2. After the SPC process, the films were analyzed using TEM and Hall effect measurements. The fabrication of high-quality n-type thin-film poly-Si was tried by combining the effects of the partial doping method with those of using a textured substrate.

In order to discover the effects of textured substrates on the growth kinetics of poly-Si thin films, the structural disorder was analyzed in a-Si films before the SPC process. The time dependence of SPC was also investigated.

Fig. 3.4-1 An SEM photograph of the textured quartz substrates

Table 3.4-1 The preparation conditions of n-type a-Si films deposited on the textured quartz substrate

SiH_4 (sccm)	40
PH_3 0.1%/H_2 (sccm)	10
Substrate temperature (℃)	500
Pressure (Pa)	27
R.F.power (mW/cm^2)	120

Table 3.4-2 The preparation conditions of p-type a-Si films deposited on the textured quartz substrate

SiH_4 (sccm)	2.5～10
B_2H_6 0.1%/H_2 (sccm)	4～50
Substrate temperature (℃)	200～350
Pressure (Pa)	13.3
R.F.power (mW/cm^2)	100

3.4.2 Effects of surface morphology

It was discovered that textured substrates greatly improve mobility and grain size in poly-Si thin films prepared by the SPC method. Figure 3.4-2 shows the mobility of n-type poly-Si thin-films prepared by the SPC method on textured and flat substrates, as a function of carrier concentration. P-doped a-Si films deposited using uniform doping were used as a starting material. The SPC conditions were 550 °C for 10 hours changing the ramp rate from 10 to 40 °C/s. The poly-Si thin-films on textured and flat substrates were found to have almost same carrier concentration of $1x10^{18}$ to $1x10^{19}$ cm^{-3}, and the carrier concentration increased with increasing the ramp rate. In this region, the mobility of the poly-Si on the textured substrate was about seven times higher than that on flat substrate. A maximum value of 217 cm^2/Vs was obtained at a carrier concentration of $1x10^{18}$ cm^{-3}. Figure 3.4-3 shows cross-sectional TEM photographs of n-type poly-Si thin-films with a thickness of 2 μm prepared by the SPC method on textured and flat substrates. The SPC conditions were 550 °C for 8 hours. The grain size of poly-Si was between 4 and 6 μm on both textured substrates, and between 2 and 3 μm on the flat substrates. These grain sizes were confirmed by measuring the films after Secco's etching using SEM. Furthermore, the grain boundary of poly-Si on textured substrates could not be observed clearly. In the case of the flat substrates, however, a grain boundary was clearly visible. Consequently, it is apparent that poly-Si thin films on textured substrates have a higher mobility, larger grain size and a more rigid grain boundary than those on flat substrates. The larger grain size of 4 to 6 μm contributes on the achievement of the seven-times-higher mobility.

In 3.2.3, it was mentioned that the partial doping method effectively improved mobility in the lower carrier concentration, compared with uniform doping. So, the possibility of further improving the mobility of n-type poly-Si thin-films prepared by the SPC method was examined by combining the effects of partial doping with those of a textured substrates. Figure 3.4-4 shows the mobility of n-type poly-Si thin films prepared by the SPC method as a function of carrier concentration, where n-type poly-Si thin films were fabricated under various conditions: namely, partial doping on **textured substrates** (star), uniform doping on **textured substrates** (open circle), partial

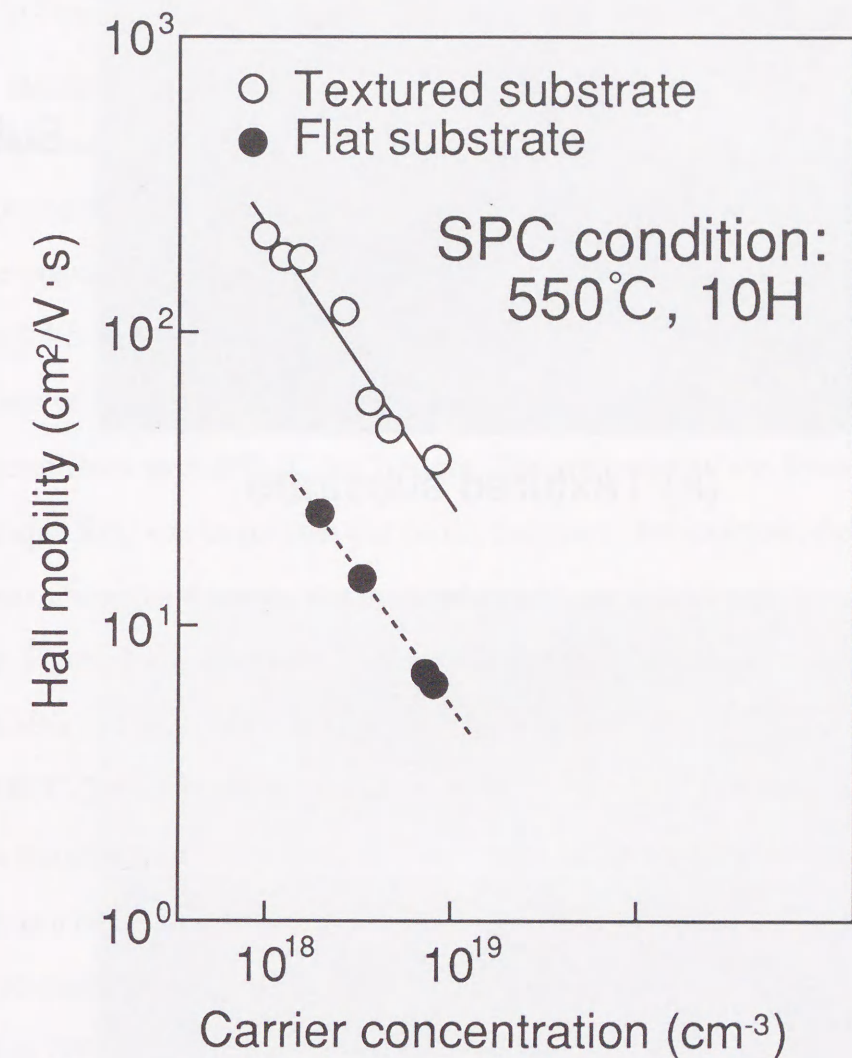
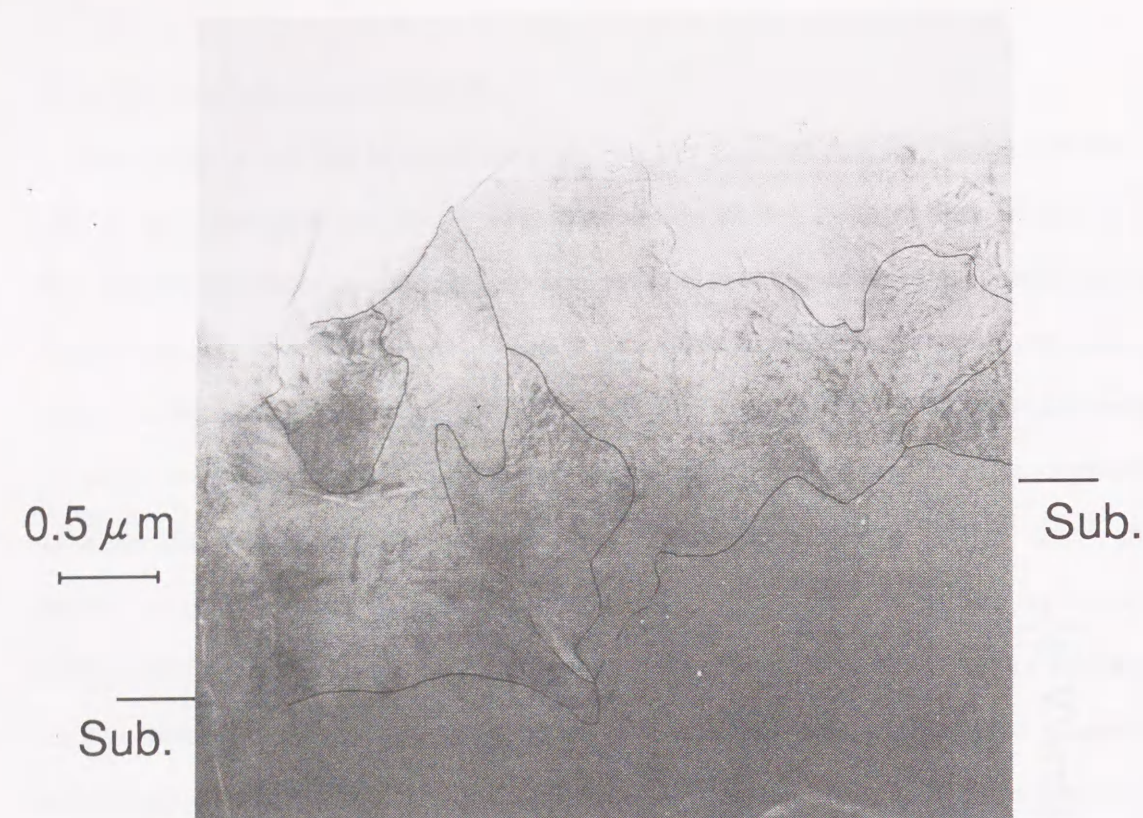
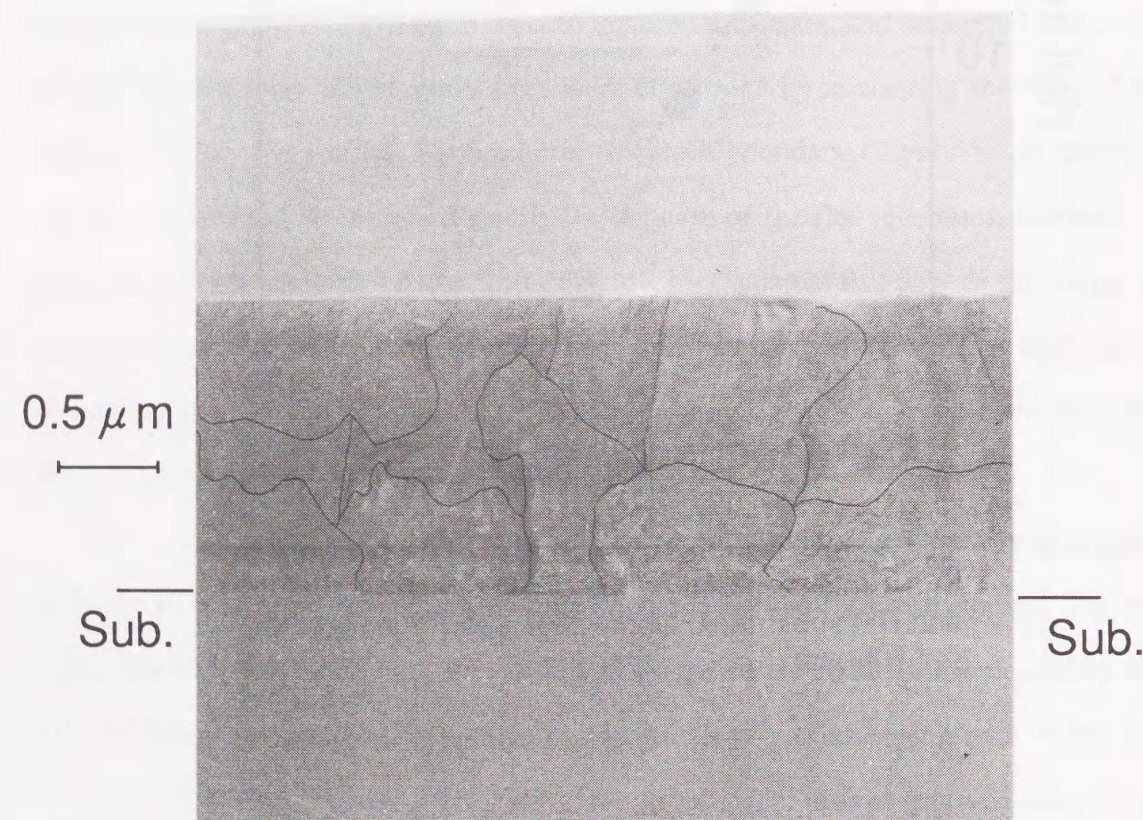


Fig. 3.4-2 The comparison of Hall mobility of n-type poly-Si thin-films prepared by the SPC method on textured and flat substrates, where SPC conditions are 550℃ for 10hours



(a) Textured substrate



(b) Flat substrate

Fig. 3.4-3 The cross-sectional TEM photographs of n-type poly-Si thin films prepared by the SPC method on textured and flat substrates

doping on **flat substrates** (closed circle) and uniform doping on **flat substrates** (open triangle). The n-type poly-Si thin films fabricated by the SPC method from a-Si films using partial doping on textured substrates (star) were found to have low carrier concentrations, ranging from 1.5×10^{15} to 3.5×10^{15} cm^{-3}. In these poly-Si thin films, a maximum mobility of 623 cm^2/Vs was achieved at a carrier concentration of 3.0×10^{15} cm^{-3}, for the first time. This value was highest in the poly-Si thin-films on glass substrates and was about 50 % the value for c-Si at the same carrier concentration.[7)] So, it was proven that high-quality poly-Si thin-films could be obtained by applying the partial doping method to films on textured substrate.

The preparation of p-type μc-Si films was also investigated using the textured quartz. Figure 3.4-5 shows cross-sectional TEM photographs of n-type poly-Si thin films with a thickness of 0.5 μm prepared by the SPC method on textured and flat substrates. The SPC conditions were 650 °C for 7 hours. The grain size of the films on the textured quartz after SPC was larger than that on the flat quartz. For example, the maximum grain size was about 3 - 4 μm on the textured quartz, compared with 1 - 2 μm on the flat quartz. Figure 3.4-6 shows the Hall mobility of the films on both the textured and flat quartz after SPC as a function of carrier concentration. The SPC temperatures were 650 and 700 °C. The ramp rate was in the range of 1 - 40 °C/s. The Hall mobility of the films on the textured quartz was three to seven times larger than that of the films on the flat quartz, at a high carrier concentration of 2×10^{20} - 2×10^{21} cm^{-3}. Most of the films on the textured quartz prepared at 650 °C had a greater mobility than that of the films on the flat quartz at 700 °C. The maximum mobility was 32.2 cm^2/Vs at a carrier concentration of 2×10^{20} cm^{-3} on the textured quartz. This value is 64 % that of c-Si with the same carrier concentration. Therefore, it was also confirmed for p-type μc-Si films that using a textured quartz was an effective means for enlarging grain size and improving Hall mobility.

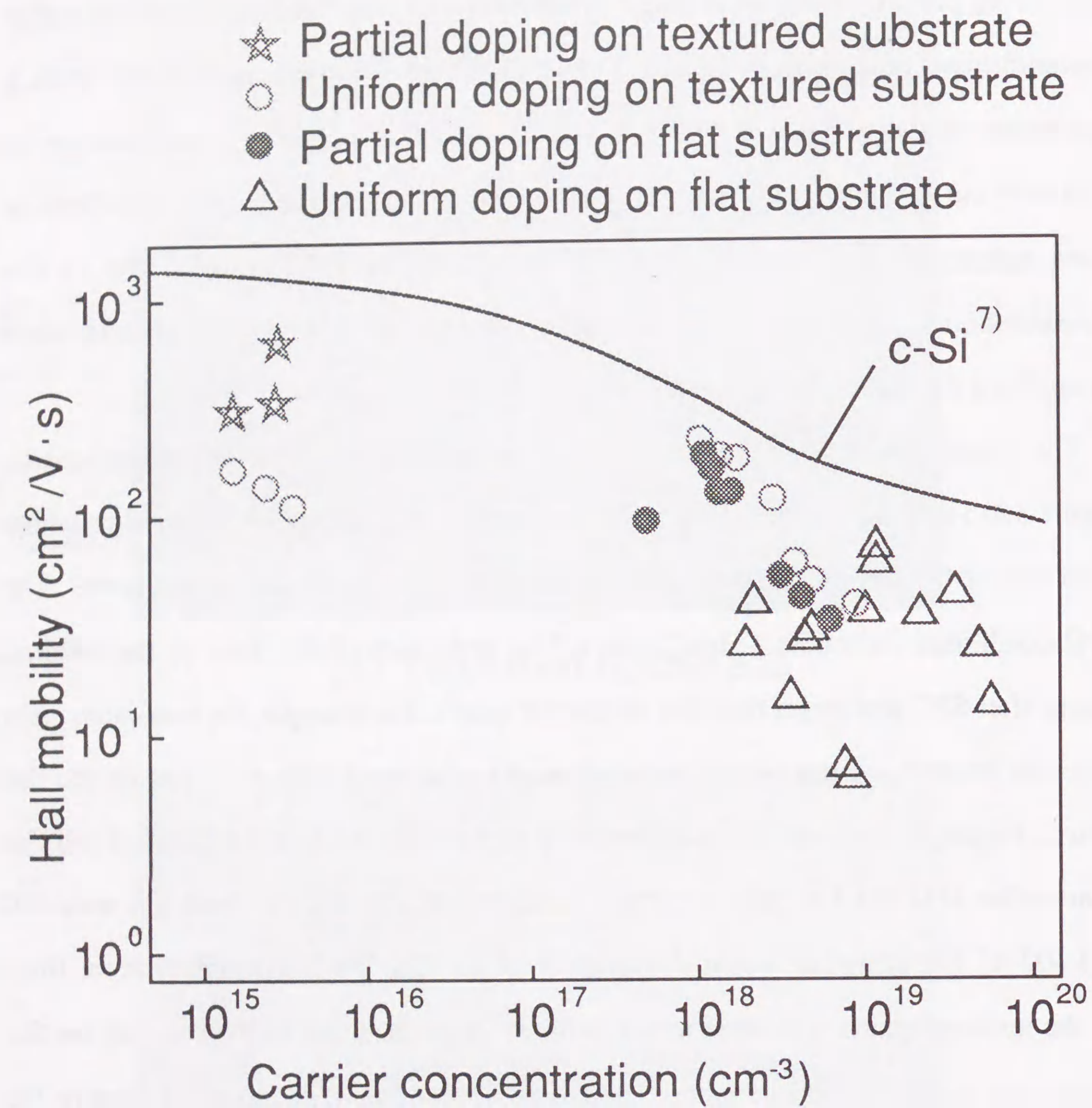
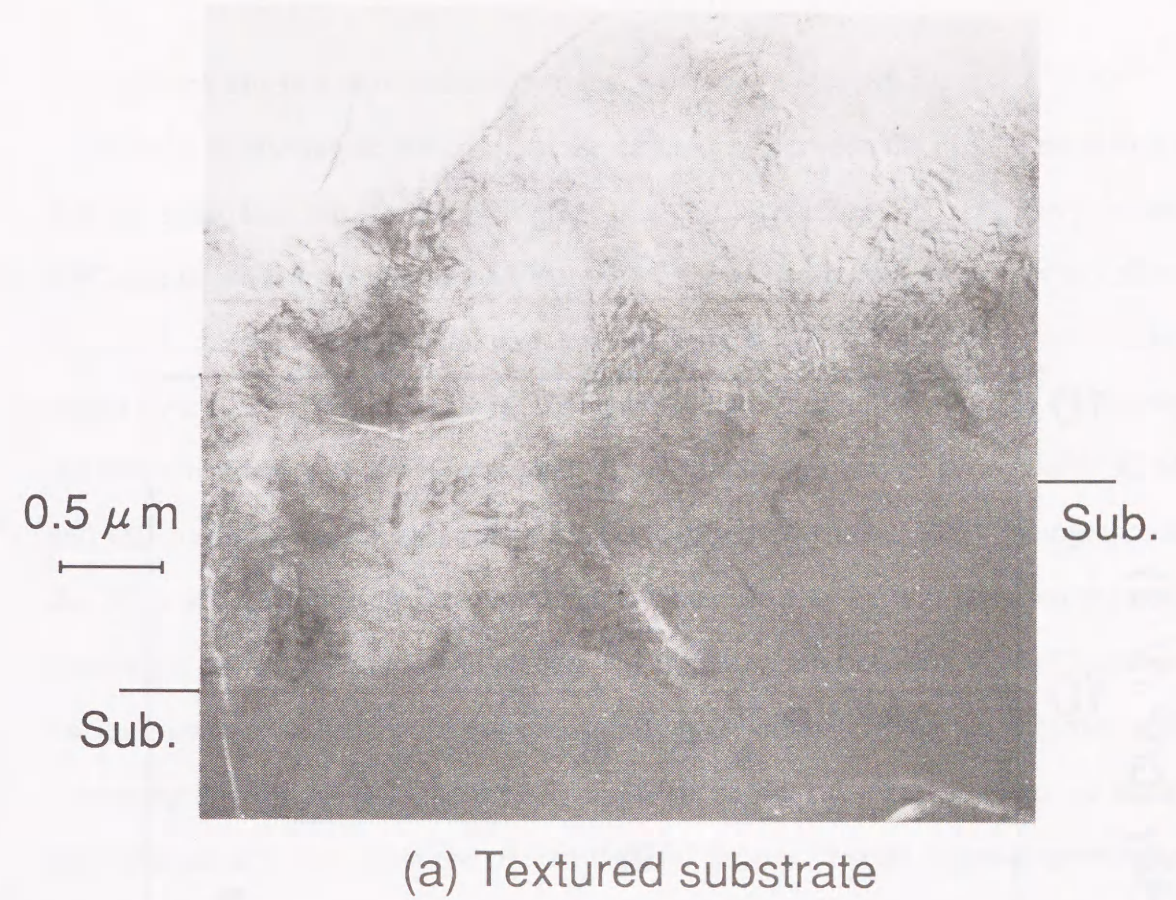
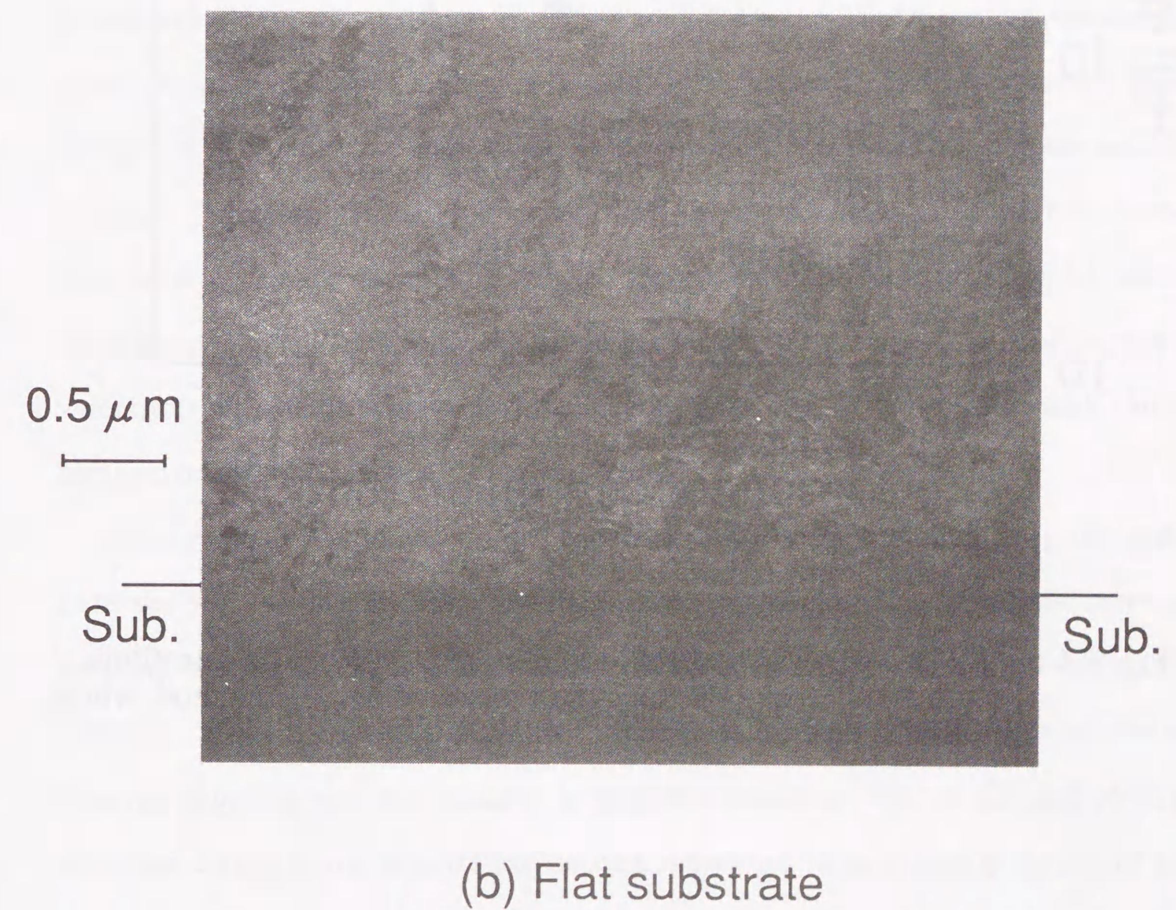


Fig. 3.4-4 The Hall mobility of n-type poly-Si thin-films prepared by the SPC method as a function of carrier concentration, where n-type poly-Si thin-films were fabricated under the various conditions: namely, partial doping on textured substrates, uniform doping on textured substrates, partial doping on flat substrates and uniform doping on flat substrates



(a) Textured substrate



(b) Flat substrate

Fig. 3.4-5 The cross-sectional TEM photographs of p-type μc-Si thin films prepared by the SPC method on textured and flat substrates

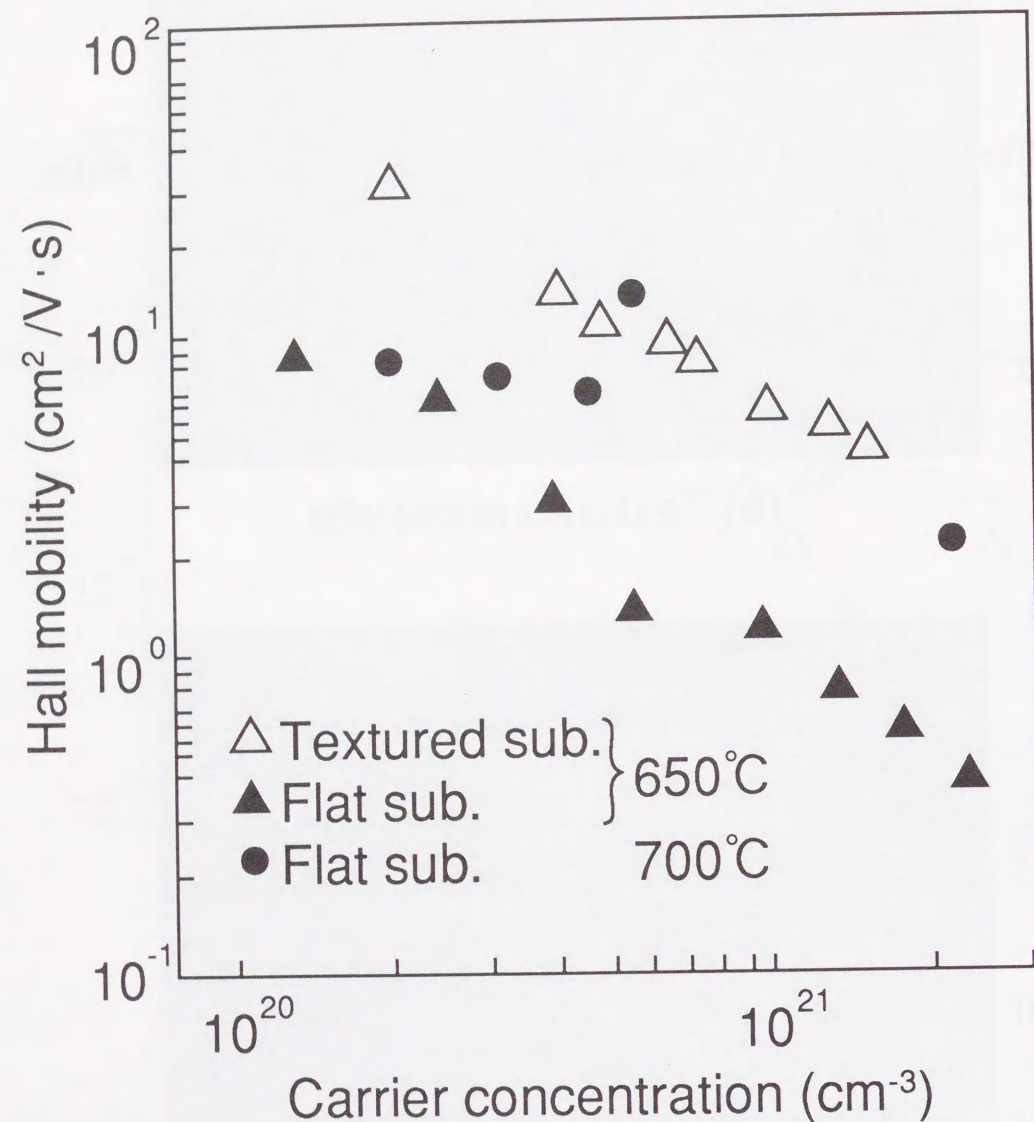


Fig. 3.4-6 The comparison of Hall mobility of p-type μ c-Si thin-films on textured and flat substrates prepared by SPC method, where SPC temperatues of 650℃ and 700℃

3.4.3 Growth kinetics on textured substrates

In order to investigate the origin of the differences between the poly-Si on textured and flat substrates, the structural disorder of a-Si films before SPC was analyzed and SPC time dependence was studied. Figure 3.4-7 shows the Raman spectra for a-Si films deposited under the same conditions on textured and flat quartz. The a-Si film on textured quartz have a larger distortion energy, compared with that of a-Si film on the flat quartz. An SPC temperature of 550 °C was used. The SPC time was varied: periods of 3, 30, 60 and 480 min. were performed. Figure 3.4-8 shows cross-sectional TEM photographs of the films after SPC using the various SPC times. In poly-Si thin films on textured substrates, nuclei generation had already begun 3 min. after starting the SPC process, nuclei growth proceeded both perpendicularly and horizontally on the substrate with increasing the SPC time. In the poly-Si thin films on flat substrate, however, no nuclei had emerged at 3 min. from the start of the SPC process. Nuclei began to generate at 30 min. then grew perpendicular to the substrate with increasing the SPC time. The growth velocities estimated from Fig. 3.4-8 are 8.4 Å/s and 3.6 Å/s for textured and flat quartz, respectively. This high growth velocity on textured quartz was caused by an increase in the distortion energy stored in the a-Si films as a result of using the textured substrate. Therefore, it was found that the films on textured substrate had shorter incubation times and especially, had the higher growth velocities in the horizontal direction compared with those for films grown on flat substrate. This high growth velocity is one factor accounting for the large grain size of 4 to 6 μm which can be obtained on textured substrates.

I discovered that textured substrate had the effect on the growth of high-quality poly-Si by the SPC method. By using textured substrates, the grain size of poly-Si increased by about two times, and mobility increased to about seven times that of poly-Si on flat substrate. It was found that one factor accounting for enlargement of grain size on textured substrate was the increase in growth velocity in SPC as a result of large distortion energy stored in a-Si films on such substrates. Thus, a large grain size of 4 to 6 μm and high mobility of 217 cm^2/Vs were obtained without using partial doping. In a

poly-Si thin-film combining partial doping and a textured substrate, a maximum mobility of 623 cm^2/Vs was achieved at a carrier concentration of 3.0×10^{15} cm^{-3}.

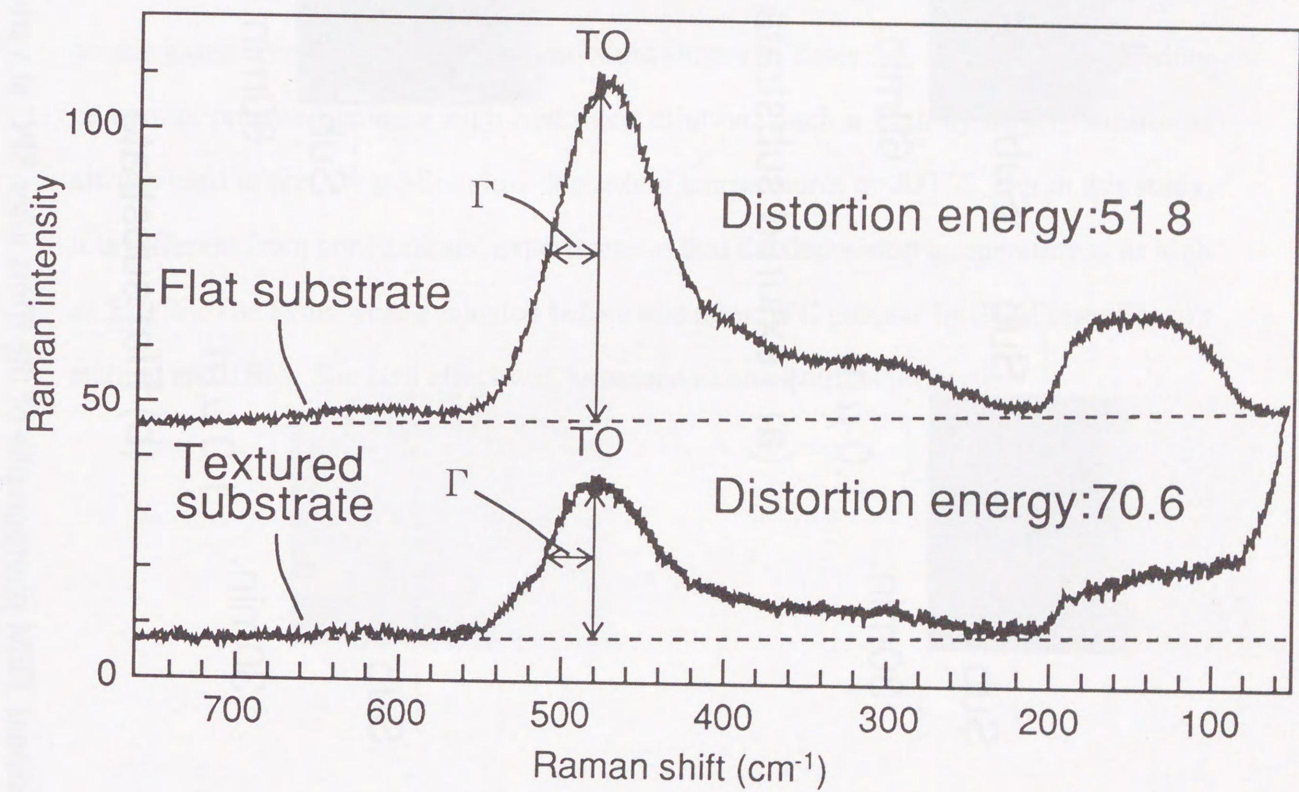


Fig. 3.4-7 Raman spectra of a-Si films deposited on textured and flat substrates under a same cndition by plasma-CVD.

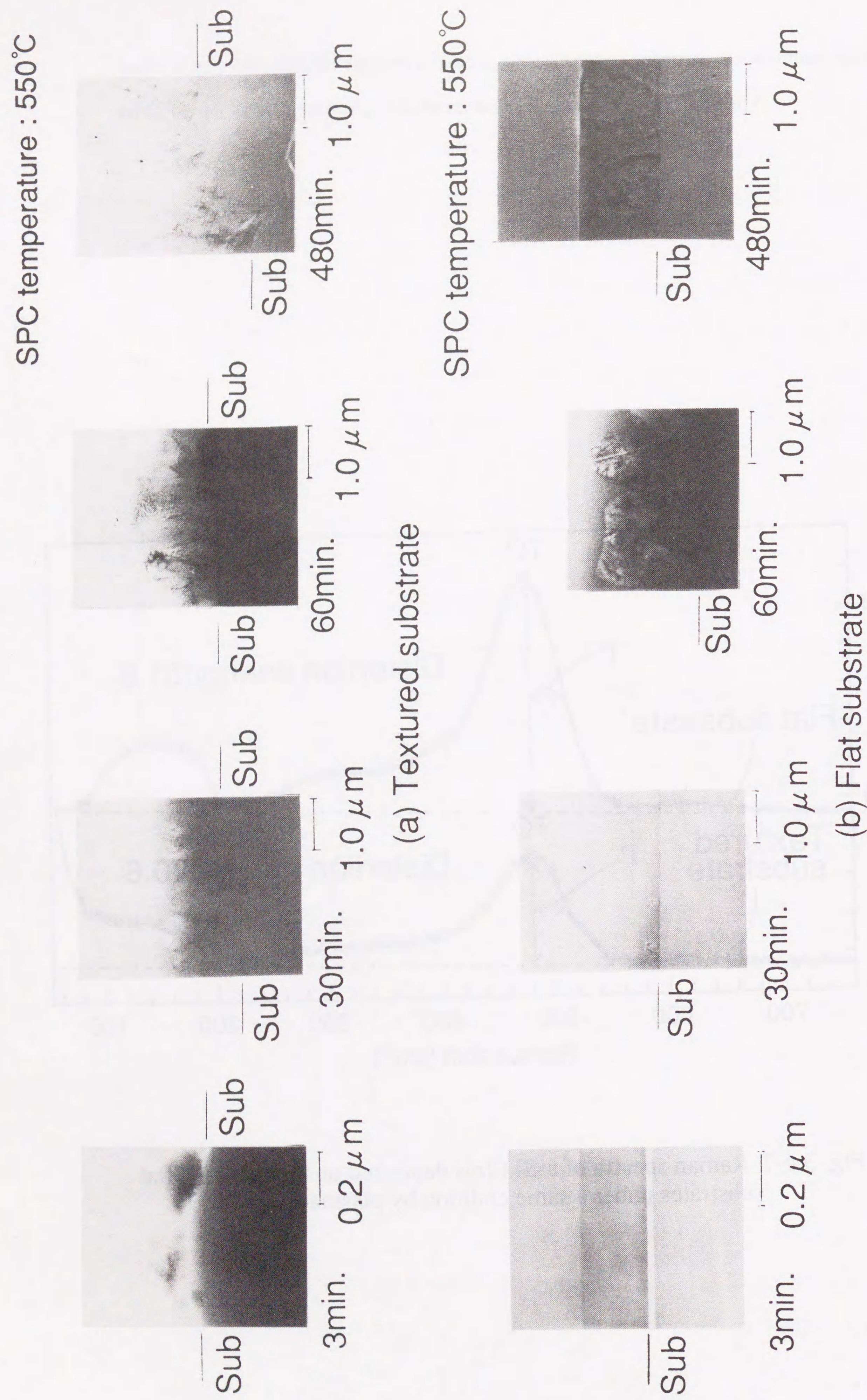


Fig. 3.4-8 The cross-sectional TEM photographs of the films after SPC at various SPC times on flat and textured substrates

3.5 Solid phase crystallization using crystal silicon as seed

The improvement of thin-film poly-Si properties have been succeeding on the basis of modifying the structure of the substrate/nuclei generation layer/crystal growth layer. So, in this section, I propose SPC using a substrate/film containing crystal phase/a-Si as a new structure of starting material.

3.5.1 Experimental technique

It was tried to fabricate crystal phase in P-doped a-Si as nuclei generation layer. Here, I define the films containing crystal phase as an internal seeding layer. The internal seeding layer was deposited on quartz substrates by the plasma-CVD. The quartz/the internal seeding layer/undoped a-Si was also fabricated. SiH_4, PH_3 and H_2 were used as source gases. The fabrication conditions were shown in Table 3.5-1. The internal seeding layer was prepared using a high hydrogen dilution. Such a high hydrogen dilution is always used to prepare μc-Si at low deposition temperatures of 200 °C. But in this study, it is different from conventional experiment in that the deposition temperature is as high as 550 °C. The films were evaluated before and after SPC process by SEM after Secco's etching and TEM. The Hall effect was measured as an electrical property.

Table 3.5-1 The deposition conditions of films under high hydrogen dilution.

Substrate temperature (°C)		500 - 600
Gas flow rate (sccm)	SiH_4	1 - 5
	PH_3	0.003 - 0.01
	H_2	40 - 300
R. F. power (mW/cm^2)		120
Pressure (Pa)		30 - 60

3.5.2 Effect of internal seeding

Figure 3.5-1 shows a SEM photograph of a film deposited under the conditions as shown in Table 3.5-1. It was found that this film consisted of two phases, where one was toothed in shape when viewed in cross section and the other was amorphous phase. In order to confirm the nature of these phases, the diffraction of the TEM was measured for a portion of the toothed and lattice images of TEM was measured for the films. Figure 3.5-2 shows the diffraction pattern of the TEM for the toothed portion. Figure 3.5-3 shows the lattice image for the film. The diffraction pattern shows a spot pattern which indicates single-crystal phase. The distance between two planes in the crystal phase calculated from this pattern is 1.90 Å. This value is almost same as the value of 1.92 Å for c-Si. Fig. 3.5-3 shows silicon atoms arranged regularly and arranged at random. So, it was found that this film had a crystalline phase structure existing in the amorphous phase. The size of the grain with a single-crystalline phase was about 1000 Å, estimated from Figs. 3.5-1 and 3.5-3.

A quartz/internal seeding layer/undoped a-Si structure was fabricated. The thicknesses of the internal seeding layer and undoped a-Si layer were 0.2 μm and 3 μm, respectively. Figure 3.5-4 shows cross-sectional SEM photograph of the film after the SPC process. For comparison, that of a film after SPC of quartz/P-doped a-Si/undoped a-Si is also shown. In the film using the internal seeding layer, the grain boundary is almost perpendicular to the substrate, but it is random in the film without seeding. The grain size is larger than that of the film without seeding. So, it was confirmed that the internal seed had the effect of enlarging the grain size and directional control of solid phase growth.

Figure 3.5-5 shows the Hall mobility for the films prepared by the SPC method, using a-Si films with internal seed as a function of carrier concentration. The quartz substrates are flat and textured. In this SPC method using internal seed, the effect of texture was also shown. The Hall mobility of n-type poly-Si prepared using internal seed was found to be higher than that of poly-Si without internal seed, and a maximum value of 808 cm^2/Vs was achieved at a carrier concentration of 1.3×10^{16} cm^{-3}. So, from the viewpoints of both structural and electrical properties, this internal seeding method is clearly effective in improving solid phase crystallization.

I described the innovative technologies for the improvement of thin-film poly-Si properties prepared by SPC method, above. I show the comparison between thin-film poly-Si prepared by SPC method with c-Si seeds and thin-film poly-Si prepared by the conventional SPC method. Figure 3.5-6 shows the resistivity of the n-type thin-film poly-Si described in this study and that prepared by the conventional SPC method[16] as a function of phosphorus concentration, compared with c-Si[17]. The resistivity of n-type thin-film poly-Si prepared by the SPC method is almost the same as that of c-Si when the phosphorus concentration exceeds 10^{15} to 10^{21} cm^{-3}. The resistivity of films prepared by the conventional SPC method, on the other hand, shows values higher by six to seven orders than that of c-Si at phosphorus concentrations of 10^{17} - $10^{19} cm^{-3}$. Figure 3.5-7 shows the resistivity of p-type μc-Si prepared by the SPC method and conventional SPC method[16], compared with c-Si[17]. The p-type films prepared by the SPC method show resistivity lower than that prepared by conventional SPC method, and their values are close to those of c-Si. So, the n- and p-type thin-film Si prepared by the SPC method offer good properties, and the SPC method proposed in this study is well-suited to the preparation of thin-film Si materials at low temperatures.

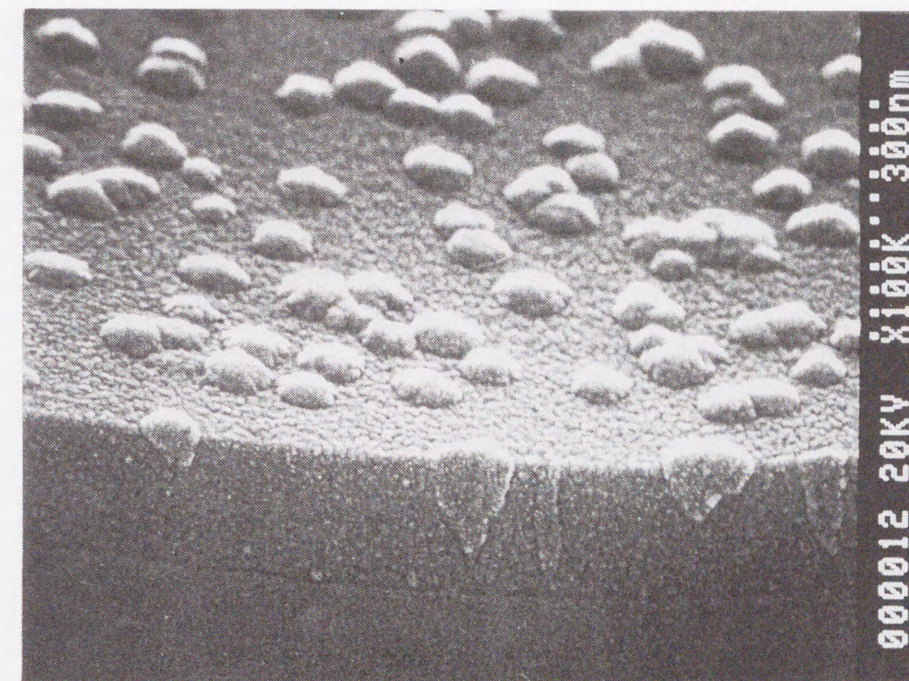


Fig. 3.5-1 The SEM photograph of a film deposited under the high hydrogen dilution.

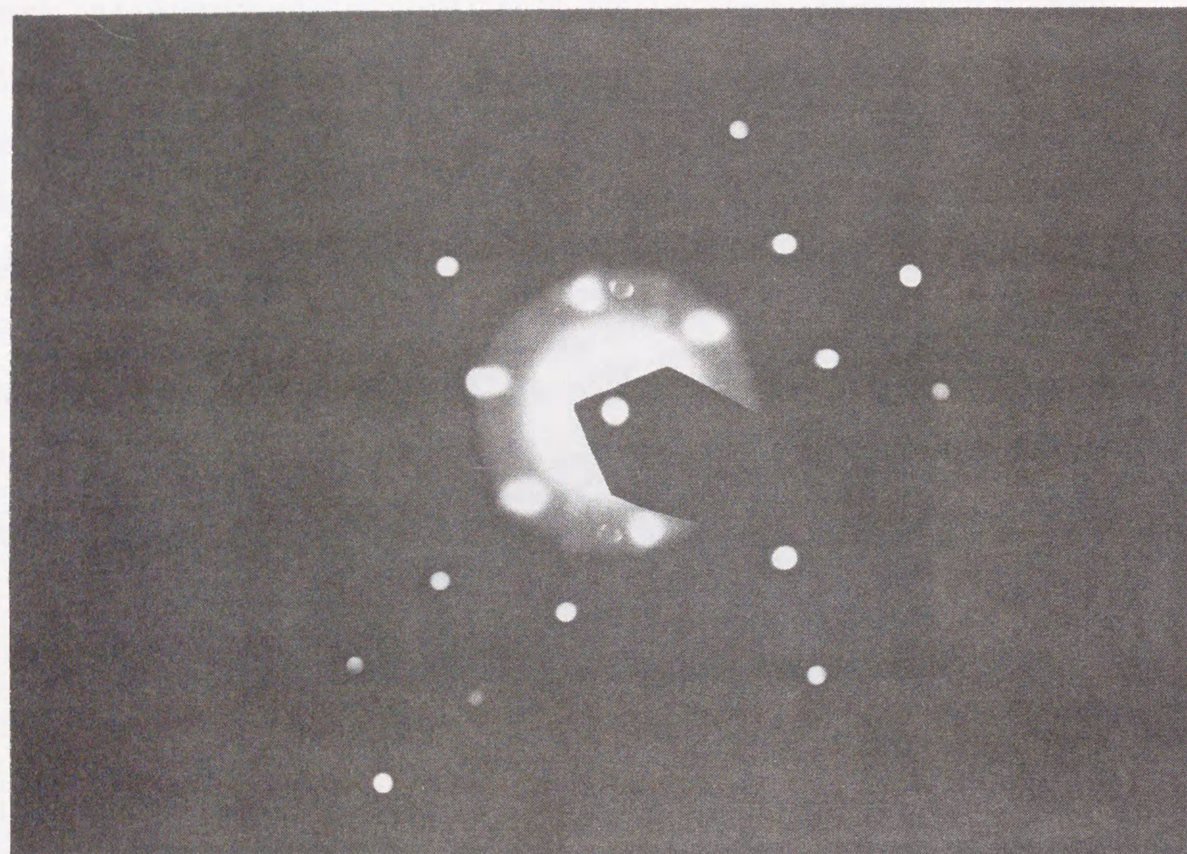


Fig. 3.5-2 The difraction pattern of TEM for a film deposited under the high hydrogen dilution condition.

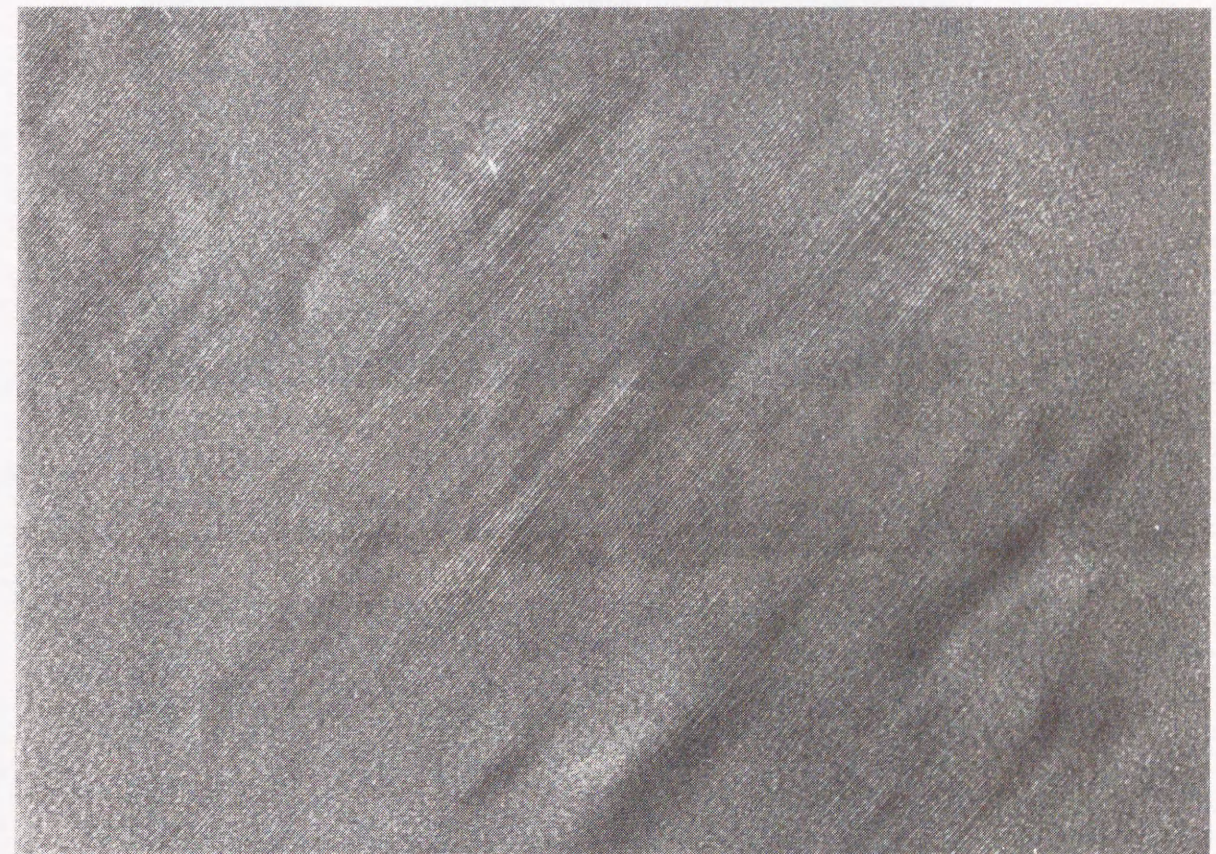


Fig. 3.5-3 The lattice image for the film deposited under high hydrogen dilution condition by plasma-CVD.

(a) quartz/internal seeding layer/undoped a-Si

(b) quartz/P-doped a-Si/undoped a-Si

Fig. 3.5-4 The cross-sectional SEM photographs of the films after SPC process of (a) quartz/internal seeding layer/undoped a-Si and (b) quartz/P-doped a-Si/ undoped a-Si. SPC conditions are 600°C for 10hours.

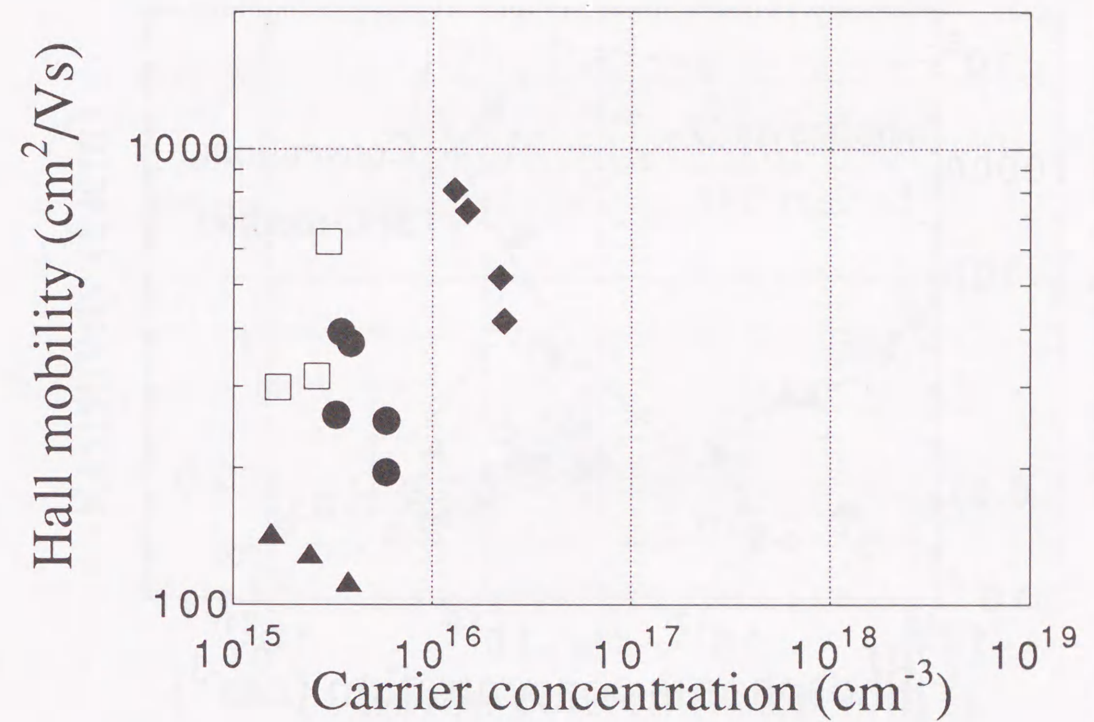


Fig. 3.5-5 The Hall mobility of the films prepared by SPC method using a-Si films with and without internal seed, as a function of carrier concentration. The substrates are f textured quartz.

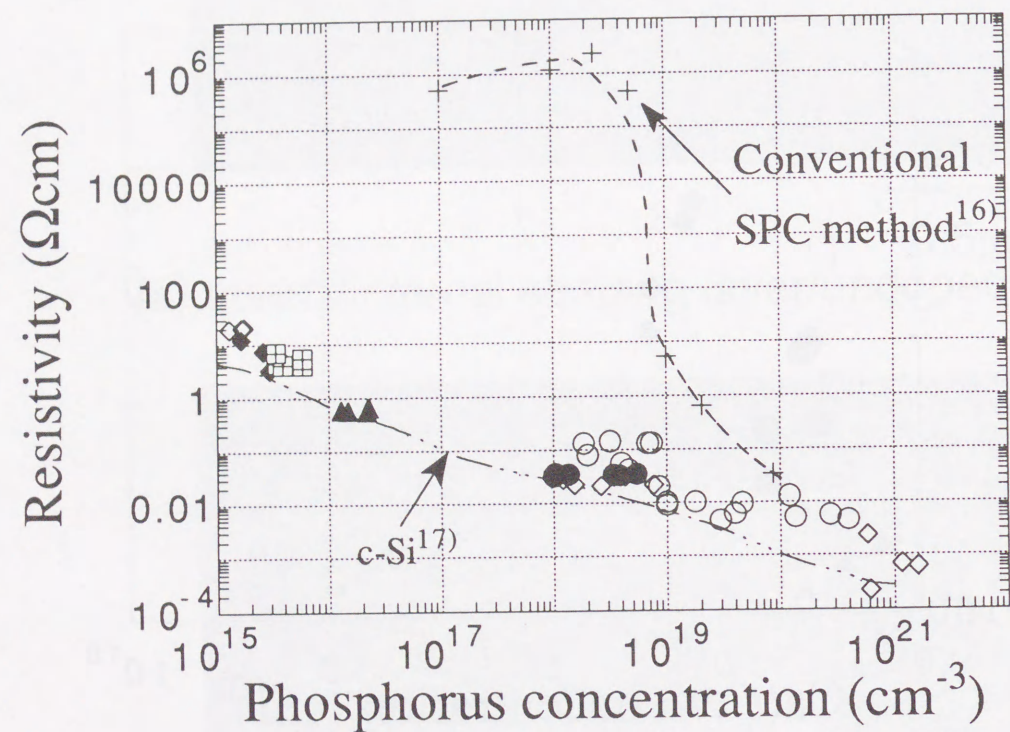


Fig. 3.5-6 The resistivity of n-type thin-film poly-Si prepared by various methods as a function of phosphorus concentration, compared with c-Si.

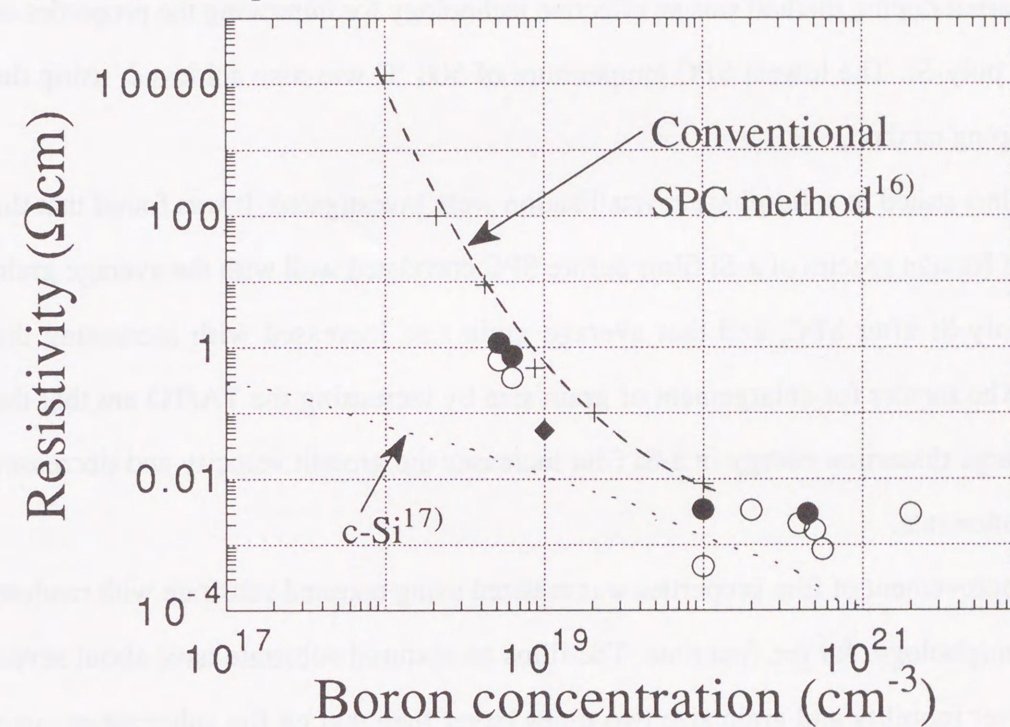


Fig. 3.5-7 The resistivity of the p-type films prepared by various methods as a function of boron concentration, compared with c-Si.

3.6 Summary

The n- and p-type thin-film Si materials were fabricated by the SPC method and film properties were improved by innovative technologies. The phosphorus and boron atoms as dopant for silicon have the effect of promoting the creation of crystalline phase and, decreasing the critical temperature of solid-phase crystallization.

The partial doping method which consists of separating the nucleus-generation and crystal-growth layers has been developed. By using this partial doping method, control of nucleus generation during the initial stage of SPC was performed and it was proven that the partial doping method was an effective technology for improving the properties of thin-film poly-Si. The lowest SPC temperature of 500 °C was also achieved, using the partial doping method.

a-Si films suited to solid-phase crystallization were investigated. It was found that the TA/TO of Raman spectra of a-Si films before SPC correlated well with the average grain size of poly-Si after SPC, and that average grain size increased with increasing the TA/TO. The factors for enlargement of grain size by increasing the TA/TO are that the store of large distortion energy in a-Si film increases the growth velocity and decreases the nucleation rate.

The improvement of film properties was realized using textured substrate with random surface morphology, for the first time. The films on textured substrate have about seven times higher mobility and grain size two times larger than that on flat substrate at same carrier concentration. It was found that a factor for enlargement of grain size on textured substrate was the increase in the growth velocity during SPC by storage of large distortion energy in the a-Si films. Combining the effects of the partial doping method with those of a textured substrate was also investigated and a high mobility of 623 cm^2/Vs was achieved.

The SPC using an internal seed was investigated. The grain with a single-crystalline phase can be fabricated in a-Si films by plasma-CVD method. The thin-film poly-Si prepared by the SPC method using an internal seed had grain boundary perpendicular to the substrate. The possibility of controlling the direction of solid-phase growth using this

method also became apparent. In this thin-film poly-Si, a maximum mobility of 808 cm^2/Vs was achieved at a carrier concentration of $1.3x10^{16}$ cm^{-3}.

In conclusion, n- and p-type thin-film Si prepared by the SPC method are materials offering good properties. The SPC method proposed in this study is well-suited to the preparation of thin-film Si materials at low temperatures.

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4 Development of solar cells using thin-film polycrystalline silicon

4.1 Introduction

In conventional c-Si and poly-Si solar cells, the p-n junctions are, in general, fabricated using popular methods such as the thermal diffusion[1] of P and B, and the implantation[2] of P^+ and B^- into c-Si and poly-Si. In these methods, dopant atoms, which are an opposite type of dopant contained in the host Si, are introduced into the host Si. For example, when the host Si was n-type, boron atoms were implanted. As a result, atoms of both boron and phosphorus exist in the host Si. So, these methods have the following problems.

(1) The process temperatures are higher than 800 °C.

(2) The quality of the c-Si and poly-Si is deteriorated, because opposite types of dopants are contained in the same host semiconductor.

a-Si solar cells are composed of three kinds of thin layers, i. e. p-type, i-type, and n-type layers, and these are deposited in order on the substrate. So, the junction is fabricated by depositing thin layers in a-Si solar cells. Using this technology, two kinds of junction fabrications by the deposition of thin layers were investigated at low temperatures of less than 700 °C to resolve problems (1) and (2) mentioned above. One was a homojunction consisting of p-type thin-film crystalline silicon and a c-Si wafer, and the other was a heterojunction composed of a-Si and a c-Si wafer.

There are few reports on homojunction fabrication by the deposition of thin layers in c-Si and poly-Si solar cells. Various researchers, however, have been working on a-Si/c-Si heterojunction solar cells. Hamakawa et al. developed a tandem solar cell containing both a-Si and poly-Si.[3] Their bottom cell (poly-Si cell) has an n-type poly-Si wafer/p-type μc-Si heterojunction structure. A conversion efficiency of more than 20% has been reported with the tandem cell.[4] Morikawa et al.[5] studied the characteristics of μc-Si/poly-Si wafer heterojunction solar cells. They found that μc-Si deposition after fabricating a thin layer of silicon oxide (SiO_2) improved solar cell characteristics such as the open circuit voltage (V_{oc}). Mimura and Hatanaka[6] and Matsuura et al.[7] investigated the junction properties of a-Si/c-Si wafer heterojunctions, but they made no reports on their application in solar cells.

In spite of the above studies, the conversion efficiencies of heterojunction solar cells are lower than those of conventional homojunction cells; the maximum efficiency of conventional cells is about 24 %.[8)] So, the heterojunction using a-Si and c-Si was investigated to improve the junction properties.

By applying new junction fabrication technologies to the thin-film poly-Si described in Chapter 3, thin-film poly-Si solar cells were fabricated on a metal substrate, and attempts were made to improve solar cell performance.

This Chapter mentions these new junction fabrication technologies and the development of thin-film poly-Si solar cells using those technologies.

4.2 Experimental technique

To fabricate a homojunction composed of p-type thin-film crystalline silicon and c-Si wafer by the SPC method, B-doped a-Si:H films were deposited by the plasma-CVD method on n-type c-Si (ρ: 1.35 - 2.25 Ωcm) and then, thermal annealing was performed for a solid-phase crystallization of B-doped a-Si:H layer. Boron atoms were in-situ doped by mixing B_2H_6 with SiH_4 as a source gas for the SPC process. The deposition conditions are shown in Table 4.2-1. Thermal annealing conditions were 600 - 700 °C and for 1 - 7 hours in a vacuum or nitrogen atmosphere.

For the fabrication of a heterojunction consisting of thin a-Si films and c-Si wafer, B-doped a-Si:H and undoped a-Si:H films were also deposited on n-type c-Si (ρ: 1.35 - 2.25 Ωcm) by the plasma-CVD method. Table 4.2-2 shows the preparation conditions for these films.

Thin-film poly-Si solar cells were fabricated using the n-type poly-Si thin-films as an active layer. The p-n junction was an a-Si/poly-Si heterojunction. a-Si films were deposited by plasma-CVD. In the solar cells, an indium tin oxide (ITO) transparent electrode was fabricated on a-Si/poly-Si by a sputtering method at a substrate temperature of 150 °C.

The output characteristics of the solar cells were measured under AM-1.5, 100 mW/cm^2. Collection efficiency spectra were also measured at a "constant-photon density

mode" with a monochromatic light of 2 x 10^{14} photons/(cm^2·s), under illumination with a white light bias of AM-1.5, 100 mW/cm^2.

Table 4.2-1 The deposition conditions of B-doped a-Si:H for the fabrication of homojunction by the SPC method.

Substrate temperature (°C)		200 - 350
Gas flow rate (sccm)	SiH_4	2.5 - 10
	B_2H_6	0.004 - 0.05
	H_2	40 - 50
R. F. power (mW/cm^2)		95.5
Pressure (Pa)		13.3

Table 4.2-2 The deposition conditions of a-Si:H films for the fabrication of heterojunction by plasma-CVD.

		p-type	i-type	n-type
Substrate temperature (°C)		120	120	180
Gas flow rate (sccm)	SiH_4	5	5	10
	B_2H_6	0.03 - 0.3	-------	-------
	PH_3	-------	-------	0.2
	H_2	0 - 70	-------	0 - 100
R. F. power (mW/cm^2)		25 - 75	25 - 75	55
Pressure (Pa)		15 - 27	5 -27	8 - 27

4.3 A new junction fabrication technology

This section describes new junction fabrication methods using film deposition.

As mentioned in Chapter 3, p-type μc-Si films prepared by the SPC method have high conductivity of more than 1×10^2 $(\Omega cm)^{-1}$. A homojunction fabrication method was developed using these films. The junction fabrication method consists of two processes. Figure 4.3-1 shows a diagram of this junction fabrication method. In the first process, B-doped a-Si:H films were deposited on n-type c-Si by the plasma-CVD method. In the second process, B-doped a-Si:H/n-type c-Si was annealed at temperatures of 600 - 700 °C, and consequently p-type SPC-Si/n-type c-Si was fabricated. This method offers following features.

(1) The impurity atom (B) is in-situ doped into a-Si:H.

(2) This process is very simple.

(3) The distribution of impurity atoms is sharp at the interface of the p-n junction.

(4) The process temperature is low.

Figure 4.3-2 shows the structure of a solar cell with a homojunction prepared by the SPC method. The thicknesses of the n-type c-Si, p-type SPC-Si and ITO were 400 μm, 0.2 μm and 700 Å, respectively. The SPC conditions were 650 °C for 7 hours. Aluminum was also evaporated for the front and back electrodes. Figure 4.3-3 shows the normalized collection efficiency (η_{coll}) of the p-type SPC-Si/n-type c-Si solar cell, compared with a conventional solar cell. The η_{coll} at 1000 nm showed a high value of 79.4 %. This ratio is almost equal to that of the conventional p-n junction solar cell, in which the p-n junction was prepared by a high-temperature process, such as a thermal diffusion or ion implantation method. The p-type SPC-Si/n-type c-Si solar cell shows a short circuit current (I_{sc}) of 34.3 mA/cm^2.

In order to evaluate the junction properties, the depth profile of boron concentration and the dark current-voltage characteristics were measured. Figure 4.3-4 shows the distributions in the depth of boron concentration, compared with thermal diffusion[9] and ion implantation methods.[10] In the thermal diffusion method, boron concentration C(x, t) is expressed by the following two equations. For a "limited source" condition, with the total amount of impurities S, C(x, t) is given by the Gaussian function

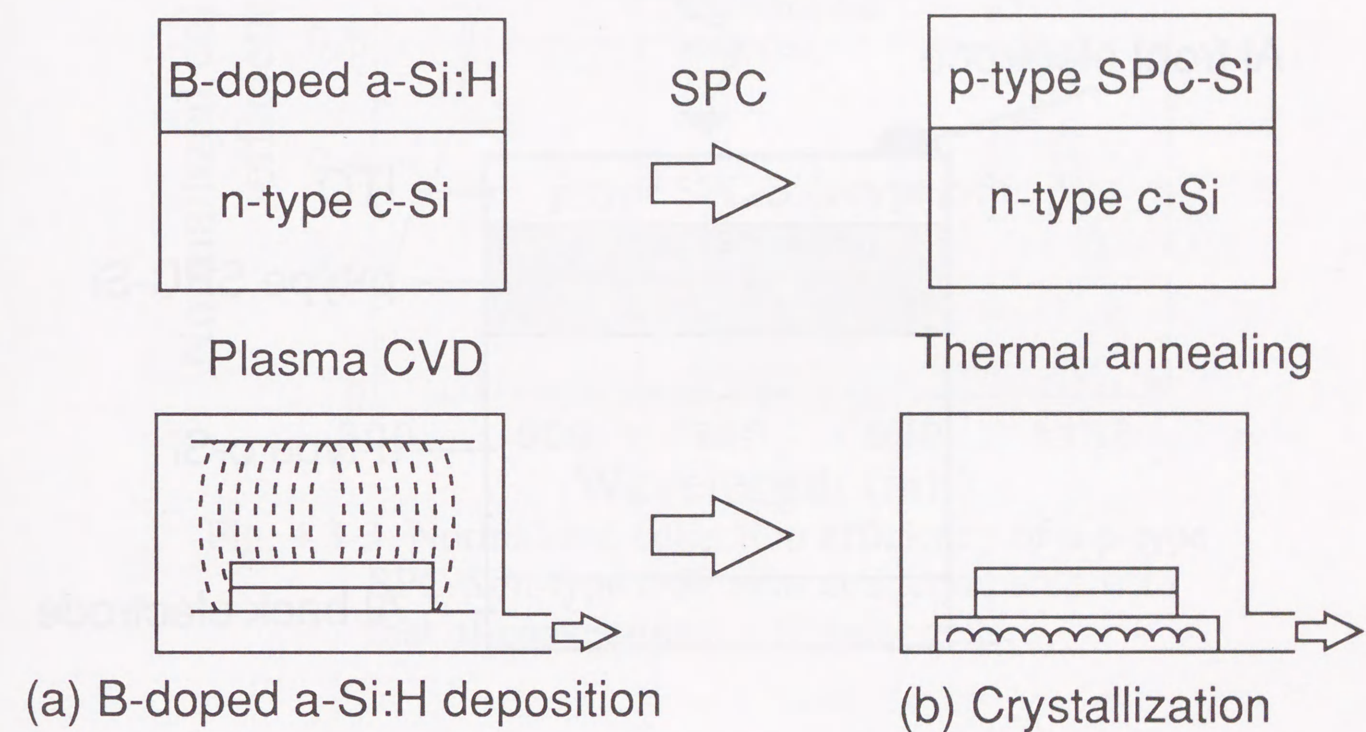


Fig. 4.3-1 Diagram of fabricating homojunction solar cells, using SPC method.

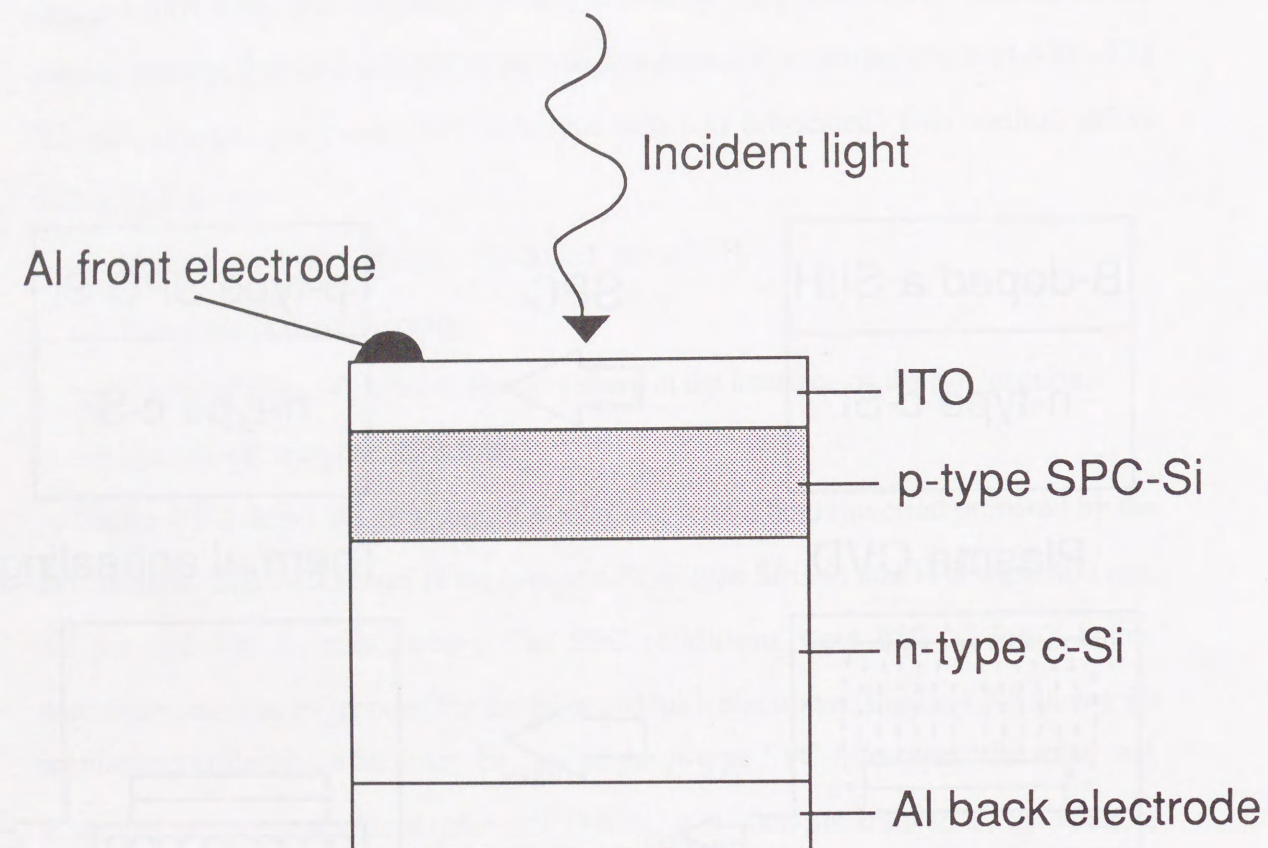


Fig. 4.3-2 The structure of a solar cell with homojunctn prepared by SPC method.

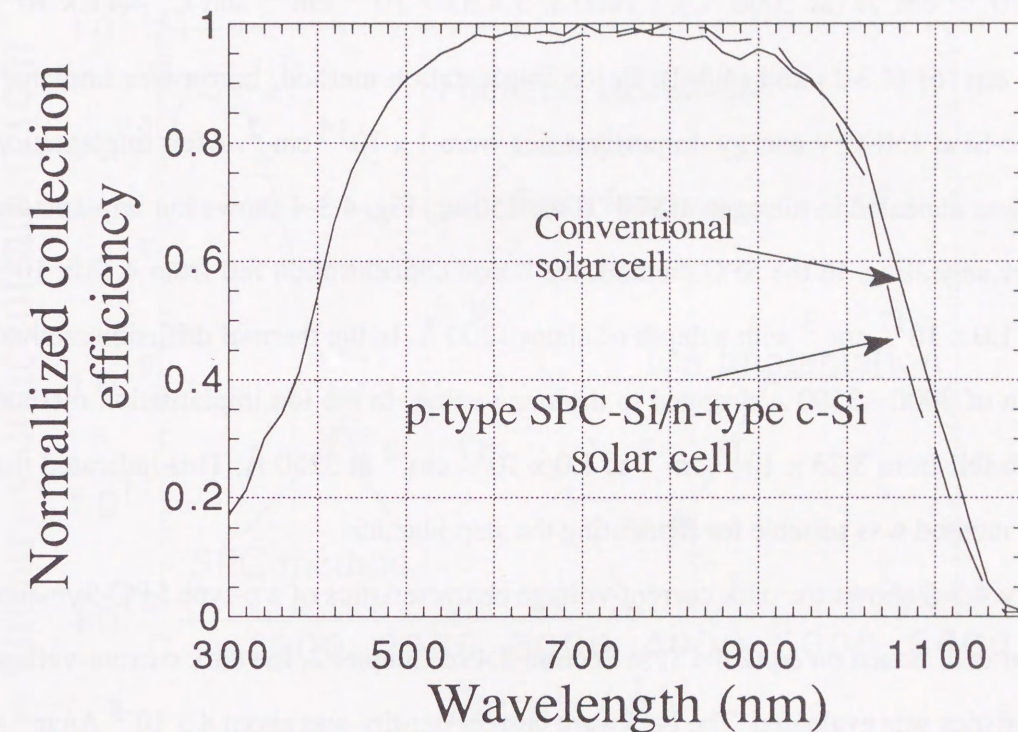


Fig. 4.3-3 Normalized collection efficiency of a p-type SPC-Si/n-type c-Si solar cell, compared with that of conventional c-Si solar cells.

$$C(x, t)=S\cdot(\pi Dt)^{-1/2}\cdot\exp\{-x^2/(4Dt)\} \qquad (4.3\text{-}1)$$

where D is the diffusion coefficient of boron atoms, t diffusion time, and x distance from the surface. For the "constant surface concentration" condition with a surface concentration C_s, C(x, t) is given by the error function compliment

$$C(x, t)=C_s\ \mathrm{erfc}[x/\{2(Dt)^{1/2}\}] \qquad (4.3\text{-}2)$$

In Fig. 4.3-4, C(x, t) for the two conditions was calculated introducing each value of D 1.96×10^{-14} cm^2/s (at 1000 °C), t 1800 s, S 4.33×10^{15} cm^{-2} and C_s 4.11×10^{20} cm^{-3} to eqs. of (4.3-1) and (4.3-2). In ion implantation method, boron was implanted into the c-Si at 150-keV energy. Impurity doses were 1×10^{14} cm^{-2}. After implantation, sample was annealed in nitrogen at 900 °C for 150sec. Fig. 4.3-4 shows ion implantation data after annealing. In the SPC method, the boron concentration fell from 4.11×10^{20} cm^{-3} to 1.0×10^{17} cm^{-3} with a depth of about 1200 Å. In the thermal diffusion method, the depth of 3000 - 3500 Å dropped to the same value. In the ion implantation method, the depth fell from 3.23×10^{18} cm^{-3} to 1.0×10^{17} cm^{-3} at 3250 Å. This indicated that the SPC method was suitable for fabricating the step junction.

Figure 4.3-5 shows the dark current-voltage characteristics of a p-type SPC-Si/n-type c-Si solar cell. Based on eq.(2.4-18) in Section 2.4 of Chapter 2, the dark current-voltage characteristics was evaluated. The backward current density was about 4×10^{-8} A/cm^2 at a bias voltage of 1 V, and the rectification ratio was of more than 5 orders. This showed that the p-n junction prepared by the SPC method had good junction properties, despite the low-temperature process of 650 °C.

From the viewpoint of solar cell performance, the textured substrate is effective for the increase of I_{sc}. On the other hand, it was mentioned in 3.4.2 of Chapter 3 that the p-type SPC-Si prepared on a textured substrate by the SPC method had large grains, and showed high mobility in the high carrier concentration range of 2×10^{20} - 2×10^{21} cm^{-3}. The p-type SPC-Si/n-type c-Si (textured) solar cells prepared by the SPC method are expected to have higher conversion efficiency. Figure 4.3-6 shows the illuminated I-V characteristics of the p-type SPC-Si/n-type c-Si (textured) solar cell, compared with that of the p-type SPC-Si/n-type c-Si (flat) solar cell. In the p-type SPC-Si/n-type c-Si (textured) solar cell, I_{sc}, fill factor (F. F.) and open circuit voltage (V_{oc}) increase,

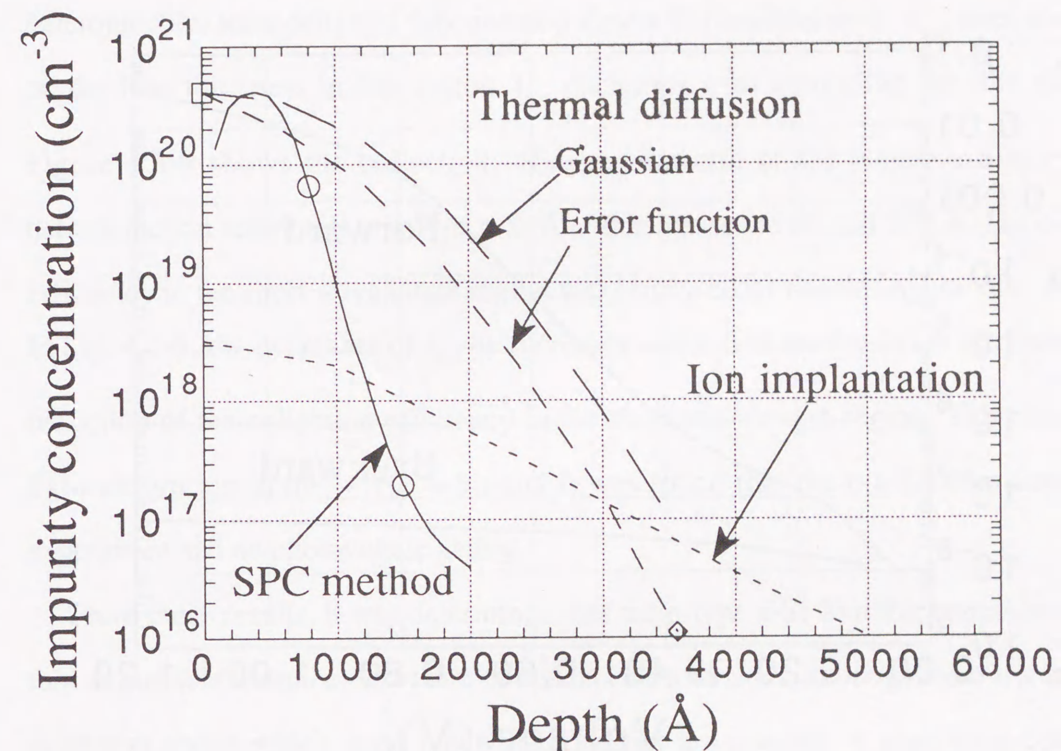


Fig. 4.3-4 The depth profiles of boron concentration in p-n junctions prepared by various methods.

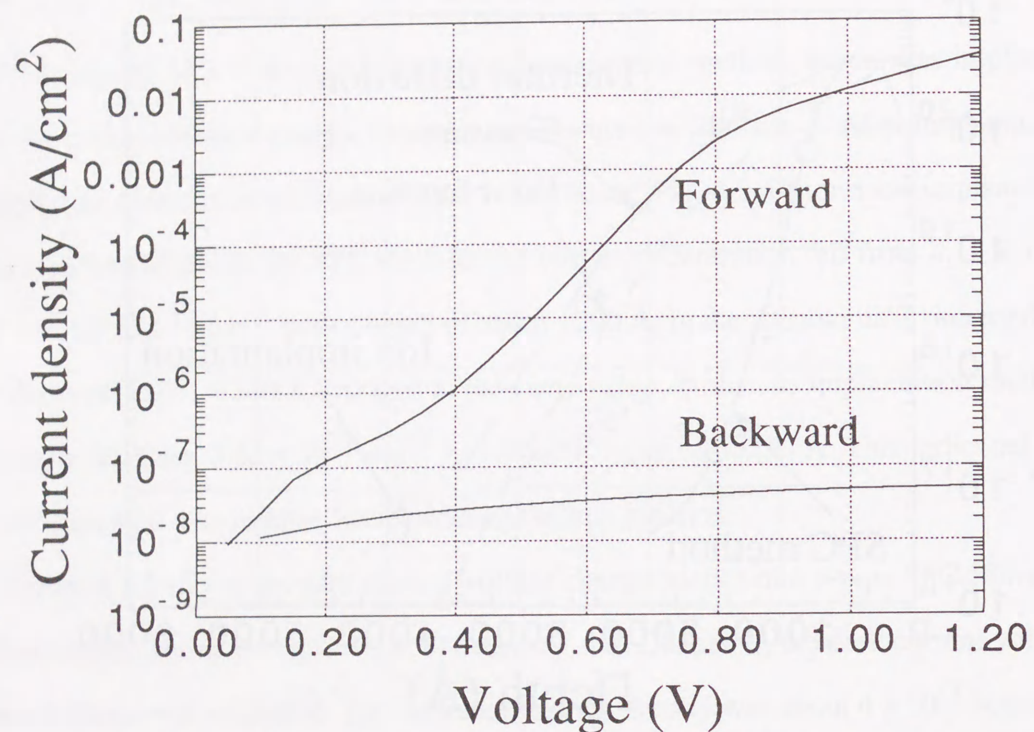


Fig. 4.3-5 Dark current-voltage characteristics of p-type SPC-Si/n-type c-Si solar cell.

compared with the p-type SPC-Si/n-type c-Si (flat) solar cell. In particular, I_{sc} was as large as 42 mA/cm^2. These improvements in solar cell performance are attributed to increases in mobility in the p-type SPC-Si films on a textured substrate. As a result, a high conversion efficiency of 14.2 % has been achieved with a size of 2 cm^2.

a-Si/c-Si heterojunction solar cells were also investigated using the structure as shown in Figure 4.3-7. Figure 4.3-8 shows the output characteristics of p-type a-Si/n-type c-Si heterojunction solar cells as a function of p-type a-Si film thickness. V_{oc} does not depend on the film thickness in this region. I_{sc} decreases with increasing the film thickness. Figure 4.3-9 shows the collection efficiency spectra of the p-type a-Si/n-type c-Si heterojunction solar cells at p-type a-Si film thicknesses of 50 and 270 Å. The collection efficiency in the short wavelength region was improved by decreasing the film thickness. In Fig. 4.3-8, the decreases of I_{sc} by increases in the film thickness are attributed to the reduction of the collection efficiency in the short wavelength region. This comes from light absorption in the p-type a-Si, and it was found that the p(a-Si) film used in this experiment had no photovoltaic ability.

From these results, it was determined that the p-type a-Si film thickness should be as thin as possible from the viewpoint of optical characteristics, although there is a minimum thickness above which good junction properties are assured. A maximum conversion efficiency of 12.3 % was achieved at a film thickness of under 100Å. In these heterojunction solar cells, however, V_{oc} and F. F. were somewhat lower than those of conventional c-Si homojunction solar cells.

In order to explain this inferiority, the junction properties of the p-type a-Si/n-type c-Si heterojunctions were investigated. The p-type a-Si/n-type c-Si heterojunction solar cells were evaluated by dark I-V characteristics, and low- and high-frequency C-V characteristics. The dark current-voltage characteristics was analyzed, based on eq.(2.4-18) in Section 2.4 of Chapter 2. As a result, it became clear that the dark I-V characteristics exhibited

prominent features. Figure 4.3-10 shows the dark I-V characteristics of a p-type a-Si/n-type c-Si heterojunction solar cell. The backward current density was about 10^{-6} A/cm^2 at a bias voltage of 1 V. This value for the backward current density is considerably

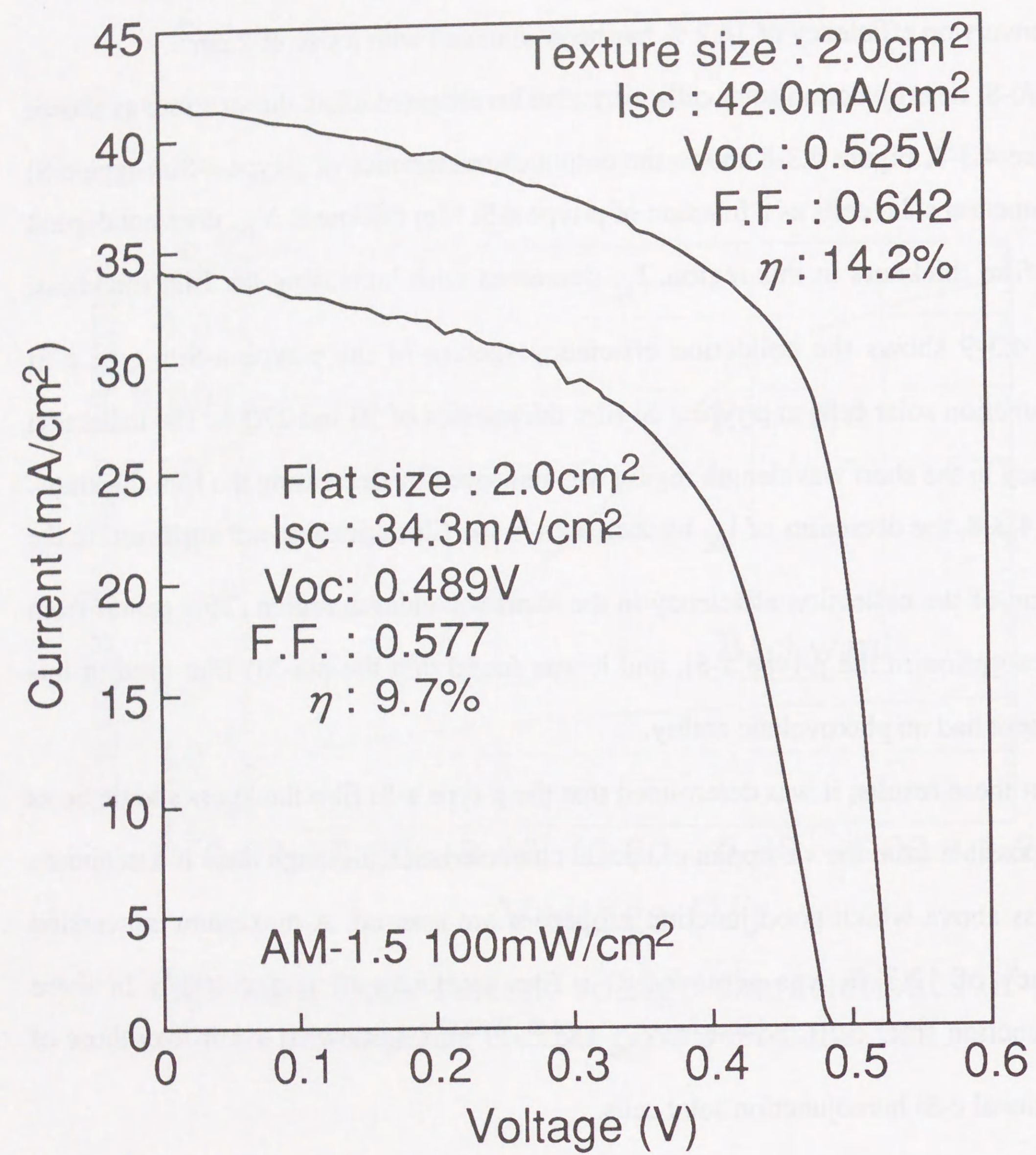


Fig. 4.3-6 Illuminated I-V characteristics of p-type SPC-Si/n-type c-Si solar cells prepared by the SPC method, where n-type c-Si substrates were flat and textured.

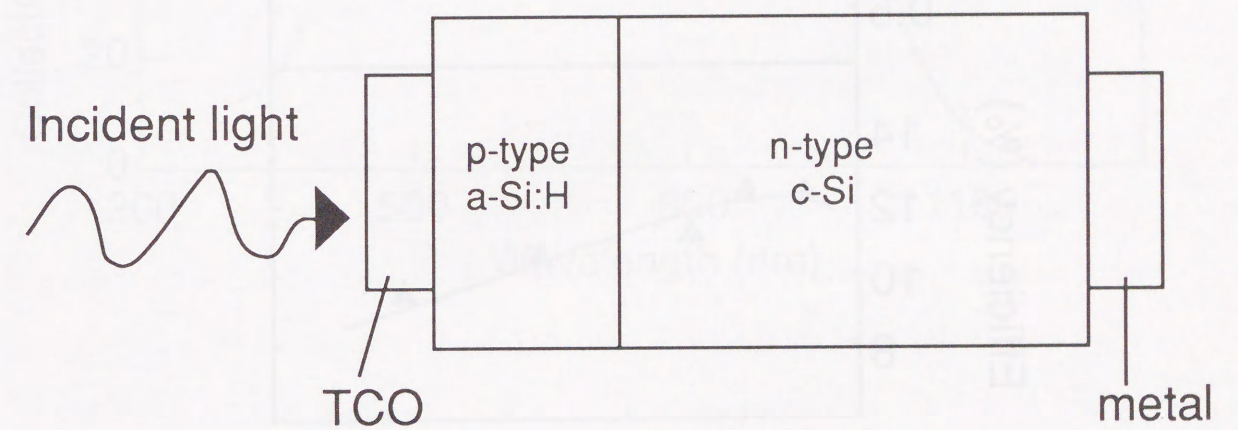


Fig. 4.3-7 Structure of a p-type a-Si/n-type c-Si heterojunction solar cell.

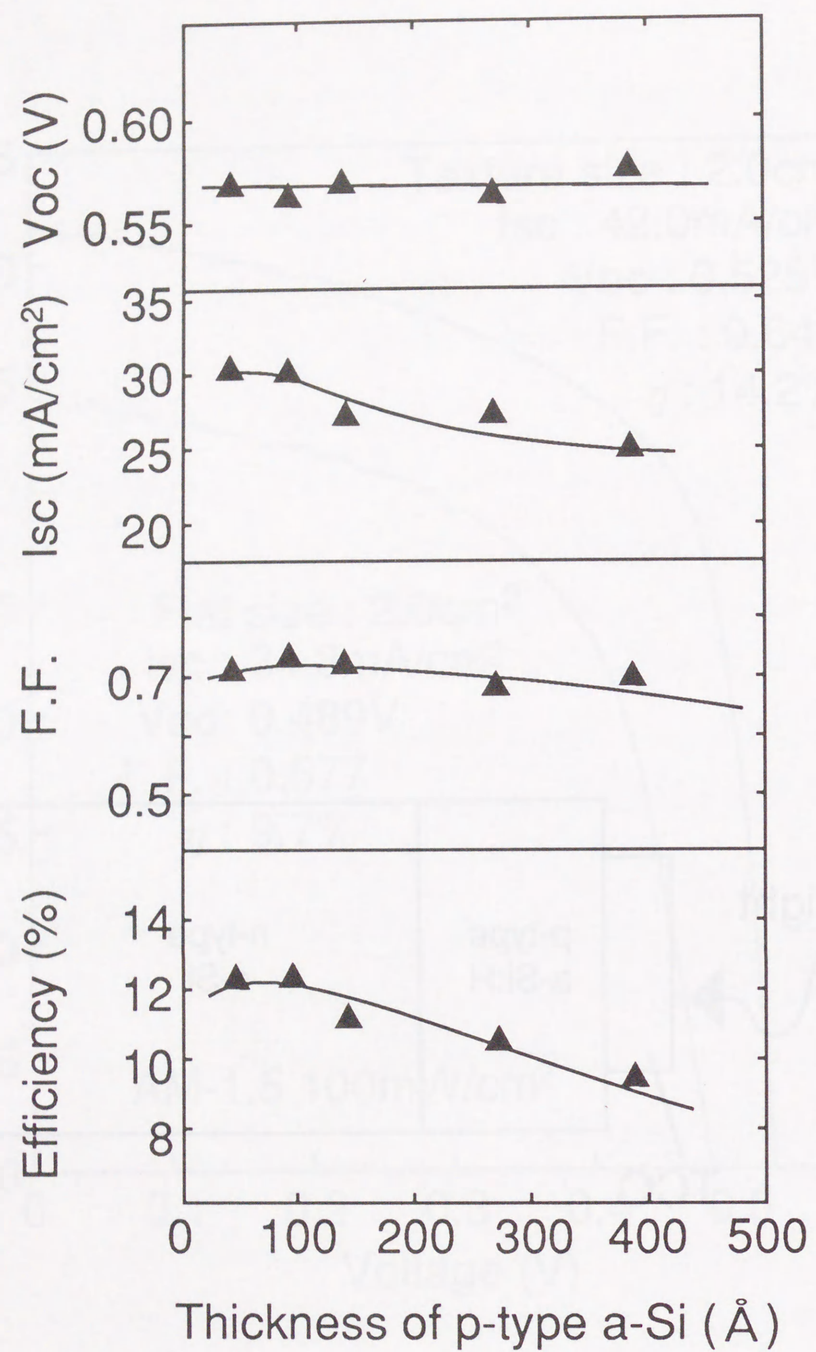


Fig. 4.3-8 Output characteristics of an a-Si/c-Si heterojunction solar cell as a function of p (a-Si) layer thickness.

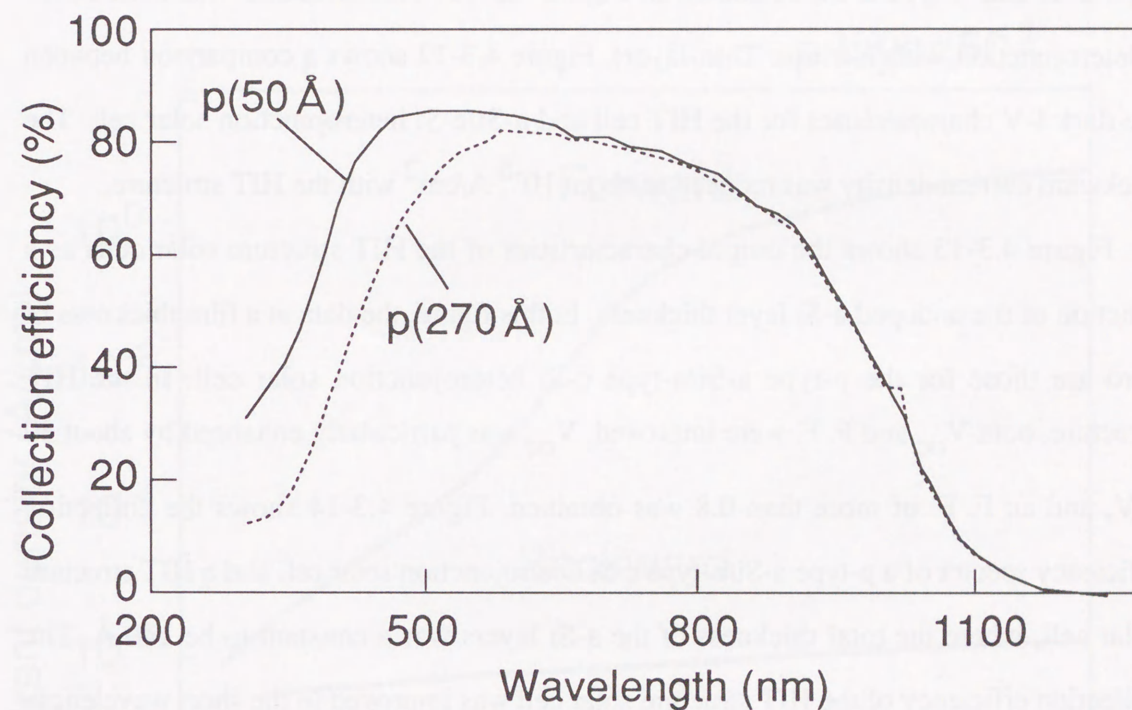


Fig. 4.3-9 Collection efficiency spectra of a-Si/c-Si heterojunction solar cells whose p (a-Si) layer thicknesses were 50 and 270Å.

larger than that of the c-Si homojunction, and seems to be caused by a large interface state density that originates from the heterojunction, and a localized state density in the a-Si layer.

In order to improve the junction properties, a new heterojunction technology was developed by thin-film deposition of less than 200Å. The decrease of the backward current in the p-n heterojunction was tried by inserting thin undoped a-Si film between p-type a-Si and n-type c-Si, as shown in Figure 4.3-11. This structure was called HIT (Heterojunction with Intrinsic Thin-layer). Figure 4.3-12 shows a comparison between the dark I-V characteristics for the HIT cell and a-Si/c-Si heterojunction solar cell. The backward current density was reduced to about 10^{-8} A/cm^2 with the HIT structure.

Figure 4.3-13 shows the output characteristics of the HIT structure solar cells as a function of the undoped a-Si layer thickness. In this figure, the data at a film thickness of zero are those for the p-type a-Si/n-type c-Si heterojunction solar cell. In the HIT structure, both V_{oc} and F. F. were improved. V_{oc} was particularly enhanced by about 30 mV, and an F. F. of more than 0.8 was obtained. Figure 4.3-14 shows the collection efficiency spectra of a p-type a-Si/n-type c-Si heterojunction solar cell and a HIT structure solar cell, where the total thickness of the a-Si layers was a constant to be 140 Å. The collection efficiency of the HIT structure solar cell was improved in the short wavelength region by inserting undoped a-Si (100 Å) between p-type a-Si and n-type c-Si. By using the HIT structure, a conversion efficiency of 14.8 % was obtained at the undoped a-Si layer thickness of 40 Å. It was found that the insertion of undoped a-Si contributed to the improvement of device properties such as the decrease of backward current, the enhancement of V_{oc}, and the increase of collection efficiency in the short wavelength region. These improvements indicate that undoped a-Si has an effect on the reduction of interface recombination between a-Si and c-Si.

To achieve a higher conversion efficiency, textured substrate and back surface field (BSF) technologies were applied to HIT structure solar cells. In the application of the textured substrate, it is important to deposit undoped a-Si thin layer uniformly and to obtain a clean surface before the fabrication of the a-Si film. It was found that a decrease in the deposition rate and the optimization of hydrogen dilution to silane gas were

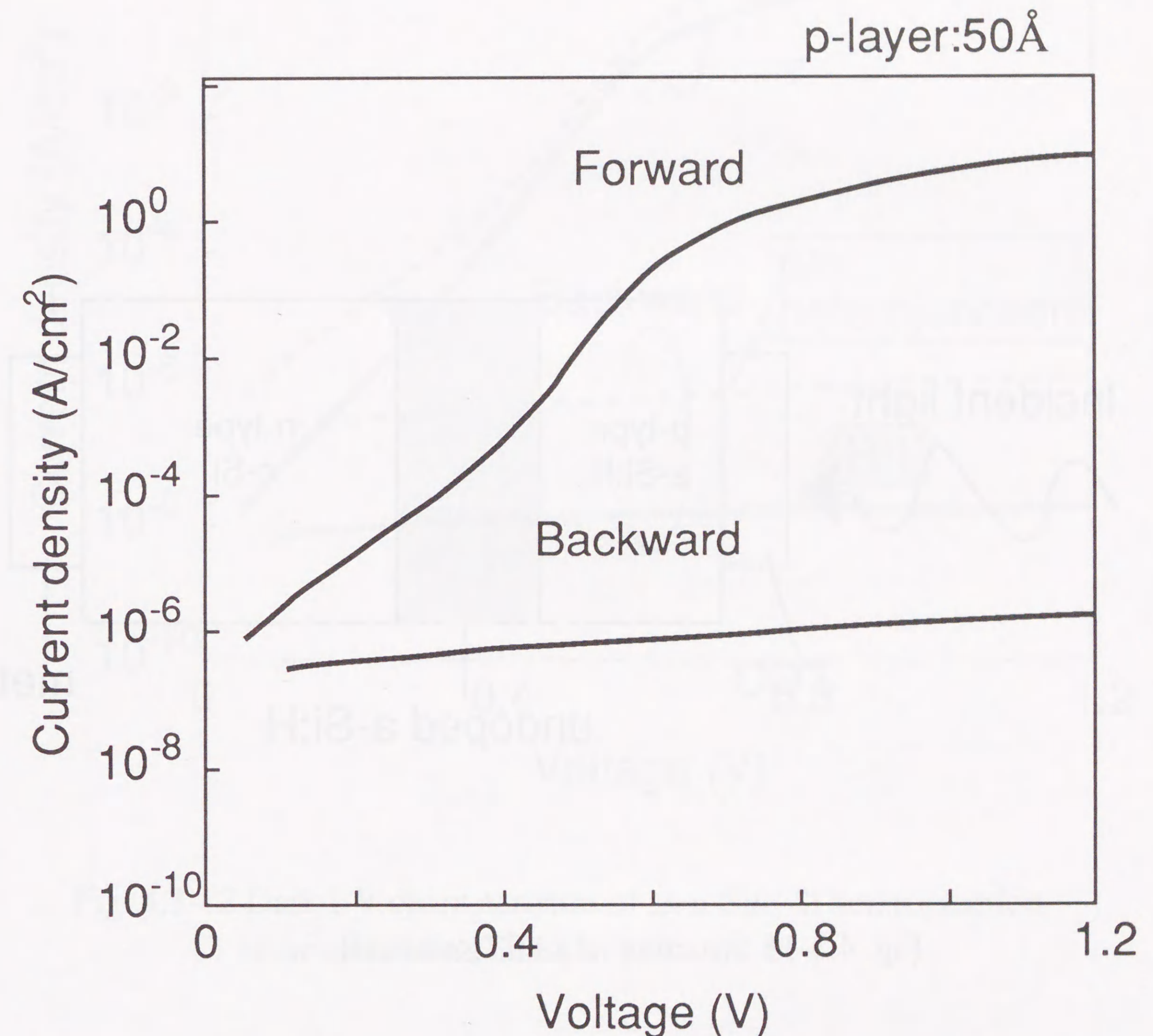


Fig. 4.3-10 Dark I-V characteristics of an a-Si/c-Si heterojunction solar cell.

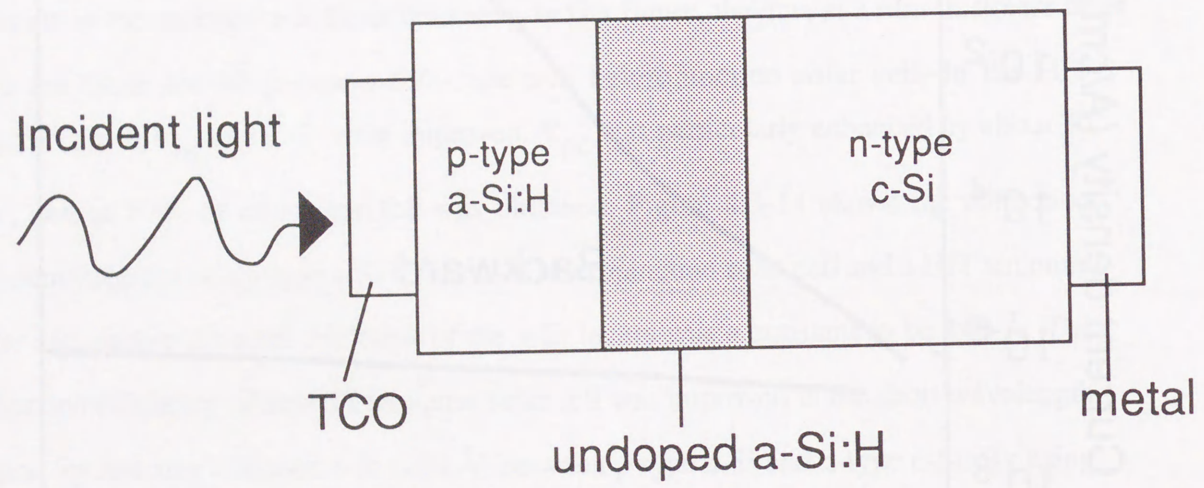


Fig. 4.3-11 Structure of a HIT solar cell.

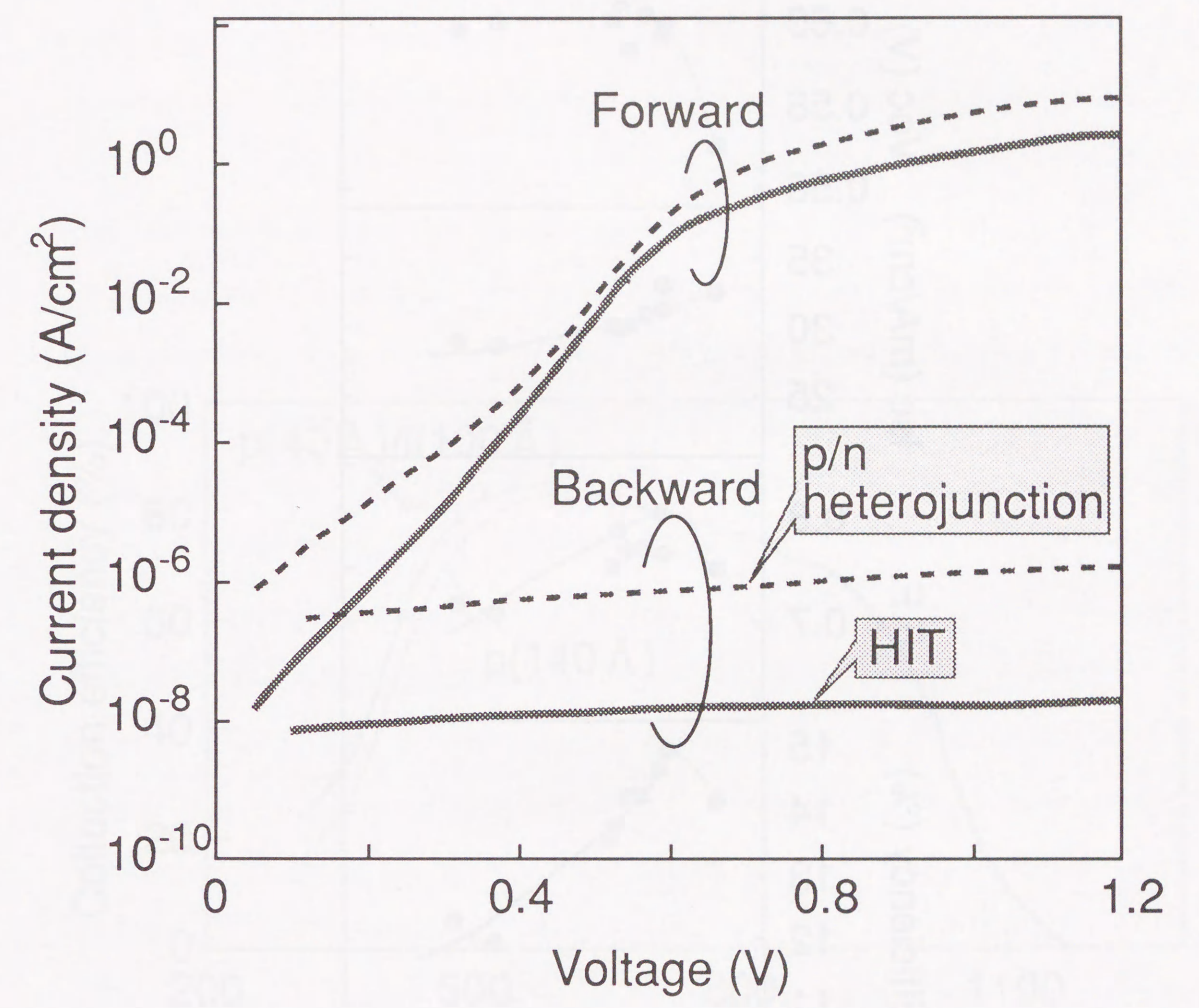


Fig. 4.3-12 Dark I-V characteristics of an a-Si/c-Si heterojunction solar cell and a HIT solar cell.

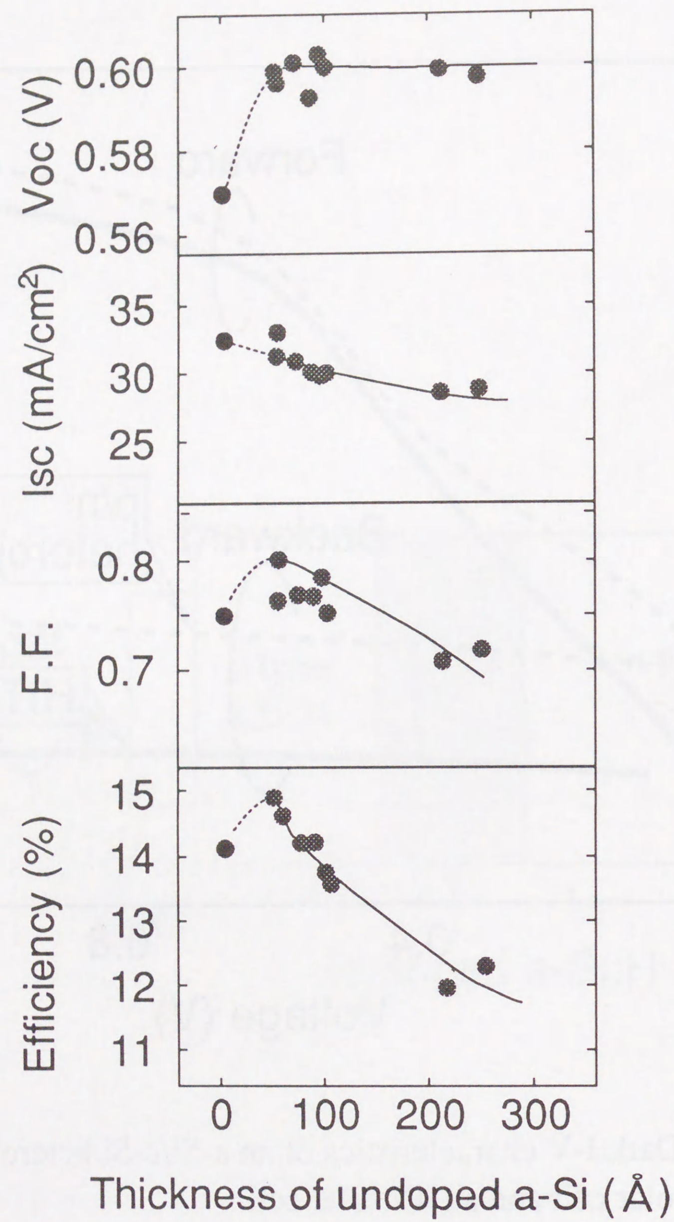


Fig. 4.3-13 Output characteristics of an a-Si/c-Si heterojunction solar cell and HIT solar cells as a function of undoped a-Si layer thickness.

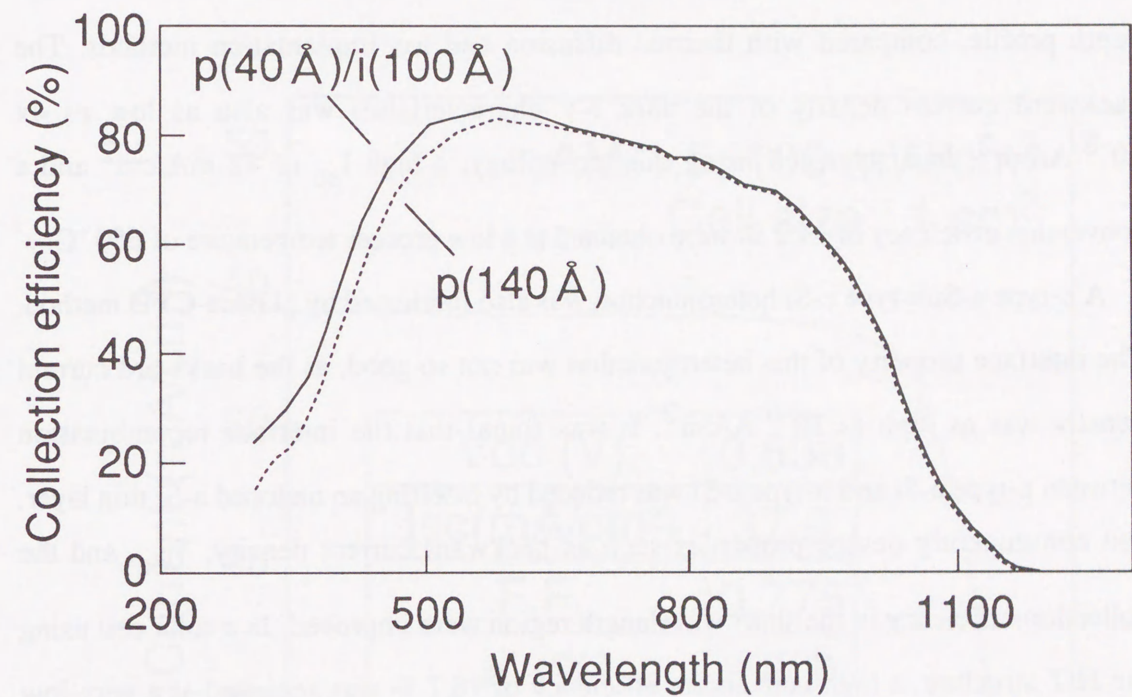


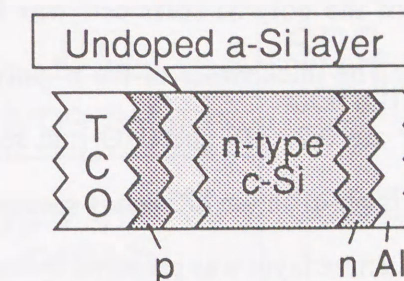
Fig. 4.3-14 Collection efficiency spectra of an a-Si/c-Si heterojunction solar cell and a HIT solar cell. The thicknesses of the a-Si layers are 140Å.

effective for the uniform deposition of a-Si films. Clean surfaces for the textured c-Si were obtained by using a hydrogen plasma treatment before the deposition of the a-Si layers. As a result, I_{SC} was improved by about 20 % in a solar cell using textured c-Si. In addition to the textured substrate, BSF structures using n-type a-Si were applied. Finally, a high conversion efficiency of 18.7 % was achieved, as shown in Figure 4.3-15. This is the highest value ever reported for solar cells in which the junction was fabricated at a low temperature of less than 200 °C.

The summaries in this Section are following. Homojunction and heterojunction formation by film deposition was investigated. A p-n homojunction was fabricated by the SPC method, and the junction had a sharp distribution of boron concentration in the depth profile, compared with thermal diffusion and ion implantation methods. The backward current density of the dark I-V characteristics was also as low as 4x 10^{-8} A/cm^2. In a solar cell using this technology, a high I_{SC} of 42 mA/cm^2 and a conversion efficiency of 14.2 % were obtained at a low process temperature of 650 °C.

A p-type a-Si/n-type c-Si heterojunction was also fabricated by plasma-CVD method. The interface property of this heterojunction was not so good, as the backward current density was as high as 10^{-6} A/cm^2. It was found that the interface recombination between p-type a-Si and n-type c-Si was reduced by inserting an undoped a-Si thin layer, and consequently device properties such as backward current density, V_{OC}, and the collection efficiency in the short wavelength region were improved. In a solar cell using the HIT structure, a high conversion efficiency of 18.7 % was achieved at a very low process temperature of less than 200 °C.

It was confirmed that junction fabrication by film deposition was effective for improving junction properties in both homojunctions and heterojunctions. A reduction in the process temperature was also achieved.



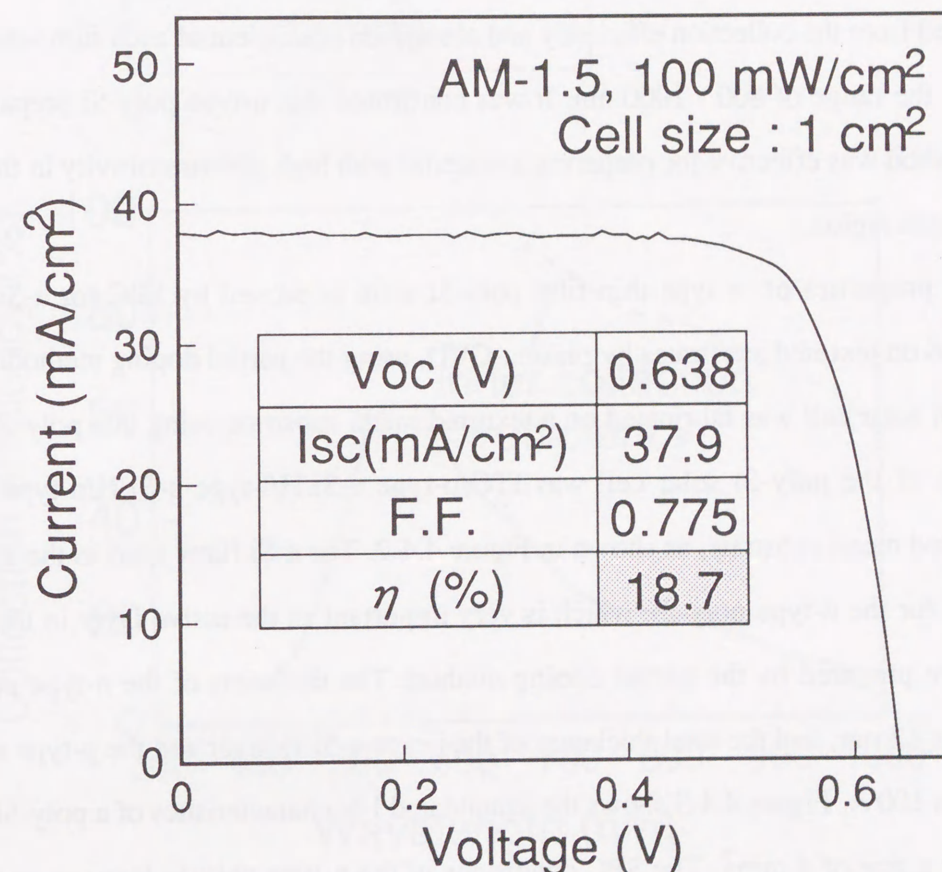


Fig. 4.3-15 Structure and illuminated I-V characteristics of a HIT solar cell.

4.4 Solar cells using thin-film polycrystalline silicon fabricated by the SPC method

In this Section, thin-film solar cells which combine the new junction formation technology and n-type poly-Si prepared by the SPC method are described.

A thin-film solar cell has been developed, using thin-film poly-Si prepared by the SPC method. The structure of the poly-Si solar cell was ITO/p-type a-Si:H/n-type poly-Si/n^+poly-Si/flat quartz. The thicknesses of the n^+poly-Si layer, n-type poly-Si layer, and p-type a-Si:H layer are 0.7, 3.0, and 0.09 μm, respectively. Figure 4.4-1 shows collection efficiency and inner quantum efficiency spectra of a thin-film poly-Si solar cell. The n-type poly-Si as an active layer was prepared by the partial doping method, and the SPC conditions were 600 °C for 9 hours. In the long wavelength region of 800 - 1000 nm, a collection efficiency of about 20 % was observed. The inner quantum efficiency calculated from the collection efficiency and absorption coefficient of each film was about 80 % in the range of 800 - 1000 nm. It was confirmed that n-type poly-Si prepared by SPC method was effective for preparing a material with high photosensitivity in the long wavelength region.

The properties of n-type thin-film poly-Si were improved by SPC for a-Si films deposited on textured substrates by plasma-CVD, using the partial doping method. Thus, a poly-Si solar cell was fabricated on a textured metal substrate using this poly-Si. The structure of the poly-Si solar cell was ITO/p-type a-Si:H/i-type a-Si:H/n-type poly-Si/textured metal substrate, as shown in Figure 4.4-2. The a-Si films used as the starting material for the n-type poly-Si, which is very important as the active layer in the solar cell, were prepared by the partial doping method. The thickness of the n-type poly-Si layer was 12 μm, and the total thickness of the i-type a-Si:H layer and the p-type a-Si:H layer was 100 Å. Figure 4.4-3 shows the illuminated I-V characteristics of a poly-Si solar cell with a size of 4 mm^2. The SPC conditions of the n-type poly-Si layer as an active layer were 600 °C for 60 hours. The I_{sc}, V_{oc}, and F. F. are 24.73 mA/cm^2, 0.548 V and 0.457, respectively. Consequently, a conversion efficiency of 6.2 % was obtained. Figure 4.4-4 shows the collection efficiency of the poly-Si solar cell. The dashed line shows the calculated collection efficiency assuming a c-Si thickness of 12 μm for comparison. In the long-wavelength region of more than 800 nm, the photovoltaic ability

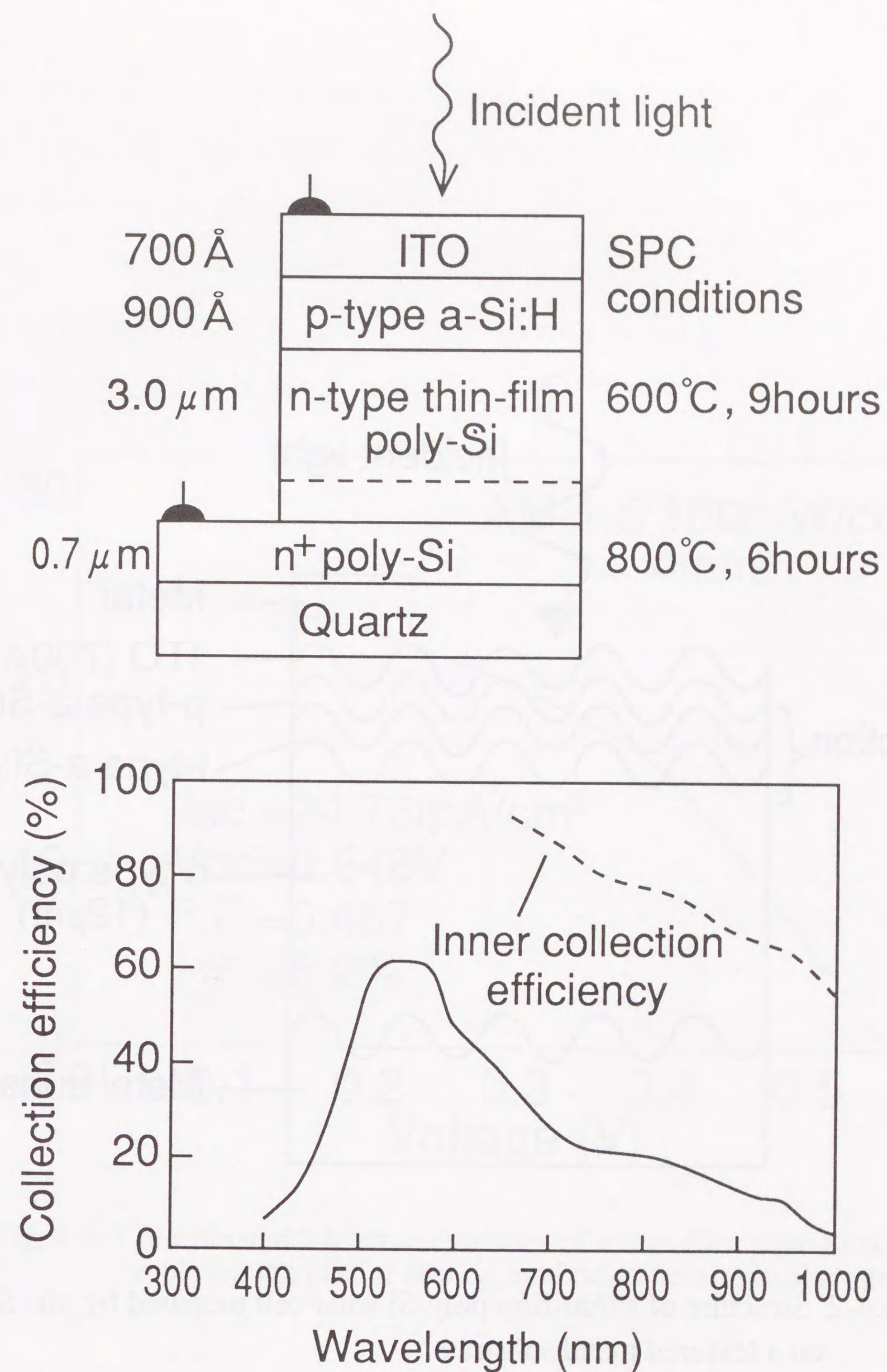


Fig.4.4-1 Collection efficiency and inner quantum efficiency spectra of a thin-film poly-Si solar cell prepared by SPC method. The cell structure was also shown.

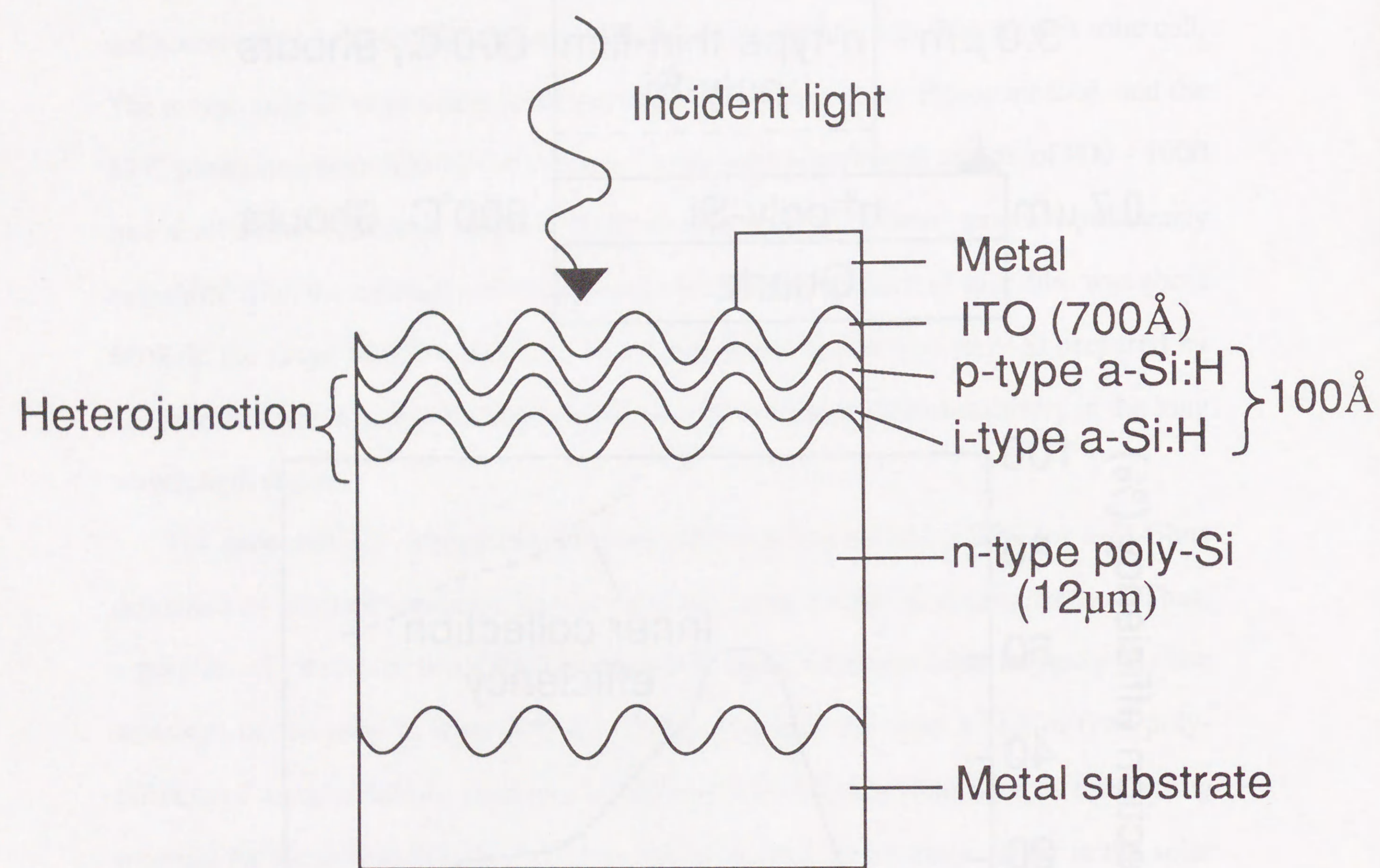


Fig. 4.4-2 Structure of a thin-film poly-Si solar cell prepared by the SPC method on a textured metal substrate.

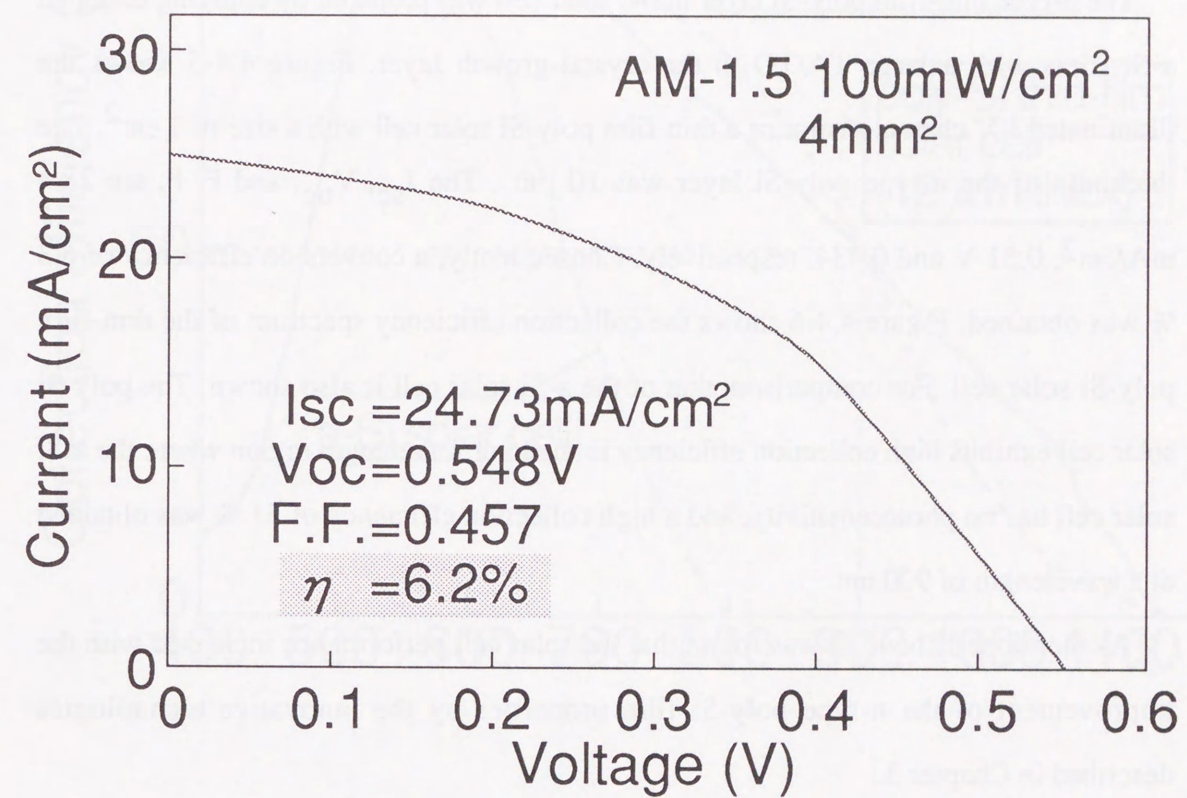


Fig. 4.4-3 Illuminated I-V characteristics of a thin-film poly-Si solar cell, applying the partial doping method to textured substrate.

of the solar cell was observed and a high collection efficiency of 50 % was obtained at the long-wavelength region of 900 nm in thin n-type poly-Si of 12 μm. This high value is attribnted to the large grain size of 4 to 6 μm. The collection efficiency in the region of more than 900 nm is higher than the calculated value. This is attributed mainly to the increase in light absorption by the effect of optical scattering at the interface between the n-type poly-Si and textured metal substrate. Therefore, it became clear that n-type poly-Si prepared by the SPC method on a textured substrate was high potential as a solar cell material with high photosensitivity in the long-wavelength region.

The n-type thin-film poly-Si layer in the solar cell was prepared by applying undoped a-Si films with a large TA/TO to the crystal-growth layer. Figure 4.4-5 shows the illuminated I-V characteristics of a thin-film poly-Si solar cell with a size of 1 cm^2. The thickness of the n-type poly-Si layer was 10 μm . The I_{sc}, V_{oc}, and F. F. are 28.4 mA/cm^2, 0.51 V and 0.434, respectively. Consequently, a conversion efficiency of 6.3 % was obtained. Figure 4.4-6 shows the collection efficiency spectrum of the thin-film poly-Si solar cell. For comparison, that of the a-Si solar cell is also shown. The poly-Si solar cell exhibits high collection efficiency in the long wavelength region where the a-Si solar cell has no photosensitivity, and a high collection efficiency of 51 % was obtained at a wavelength of 900 nm.

As mentioned above, it was found that the solar cell performance increased with the improvement of the n-type poly-Si film properties by the innovative technologies described in Chapter 3.

The diffusion length of the minority carrier of the poly-Si thin films prepared by the SPC method was estimated from short-circuit current measurements.[11] When a shallow-junction solar cell is illuminated with monochromatic radiation with a low absorption coefficient, such as that in the wavelength range of 0.8 to 1.03 μm for silicon, the measured current is essentially the photocurrent from the n-type poly-Si region and can be written[12]

$$I_{SC} = (qF_0L\alpha/\alpha^2L^2\text{-}1)[\alpha L\exp(-\alpha t)\text{-}\exp(-\alpha t)\coth\{(d\text{-}t)/L\} +\exp(-\alpha d)\mathrm{cosech}\{(d\text{-}t)/L\}], \quad (4.4\text{-}1)$$

where F_0 is the light intensity incident on the surface, L is the diffusion length, t is the

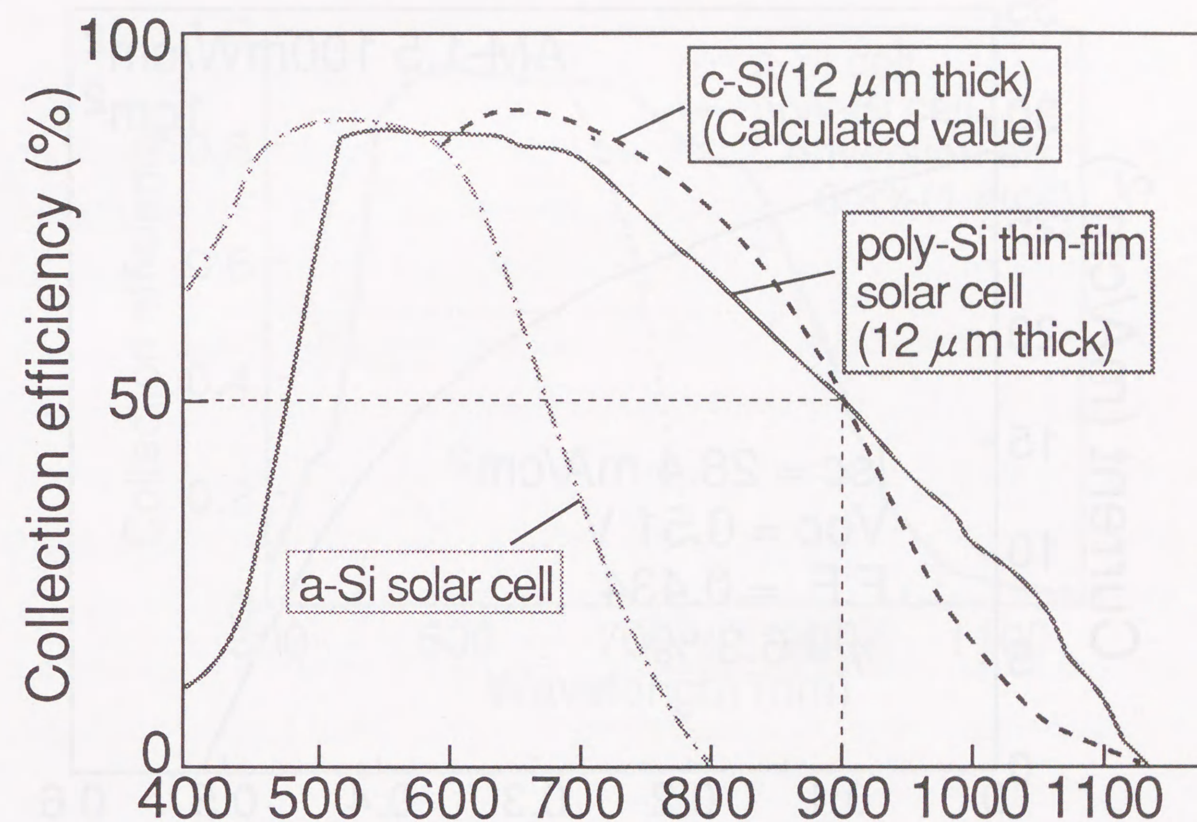


Fig. 4.4-4 Collection efficiency spectra of thin-film poly-Si solar cell and the typical a-Si solar cell. The calculated spectrum using c-Si with a thickness of 12μm was also shown.

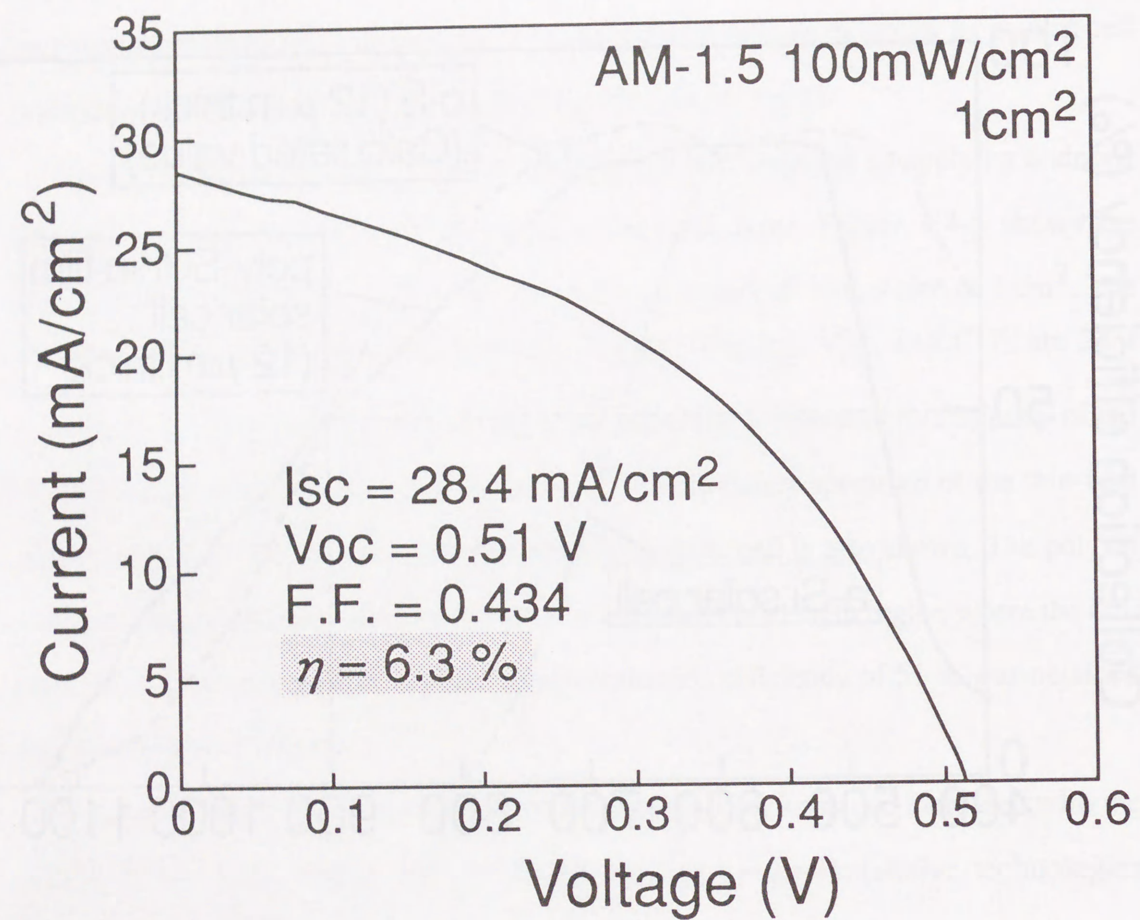


Fig. 4.4-5 Illuminated I-V characteristics of a thin-film poly-Si solar cell prepared by SPC method.

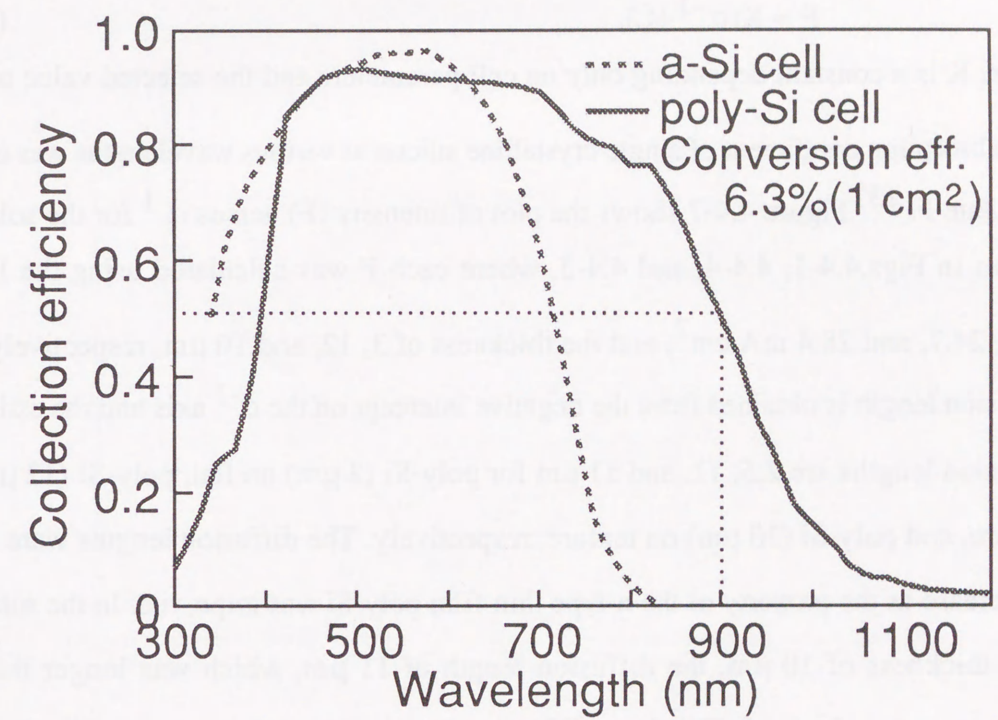


Fig. 4.4-6 Collection efficiency spectrum of the thin-film poly-Si solar cell prepared by SPC method.

depletion layer thickness, d is the specimen thickness and α is the optical absorption coefficient. When $\alpha d \geq 1$ and $d \geq 2L$, the term $\exp(-\alpha t)\mathrm{cosech}\{(d-t)/L\}$ becomes negligible, and $\coth\{(d-t)/L\}$ approaches unity. Equation (4.4-1) can then be written

$$I_{SC} = qF_0 L \exp(-\alpha t)/(\alpha^{-1}+L). \qquad (4.4\text{-}2)$$

If the incident light intensity on the n-type poly-Si, $F=F_0\exp(-\alpha t)$, is adjusted to maintain a given I_{SC} for all wavelengths, then eq. (4.4-2) is reduced to

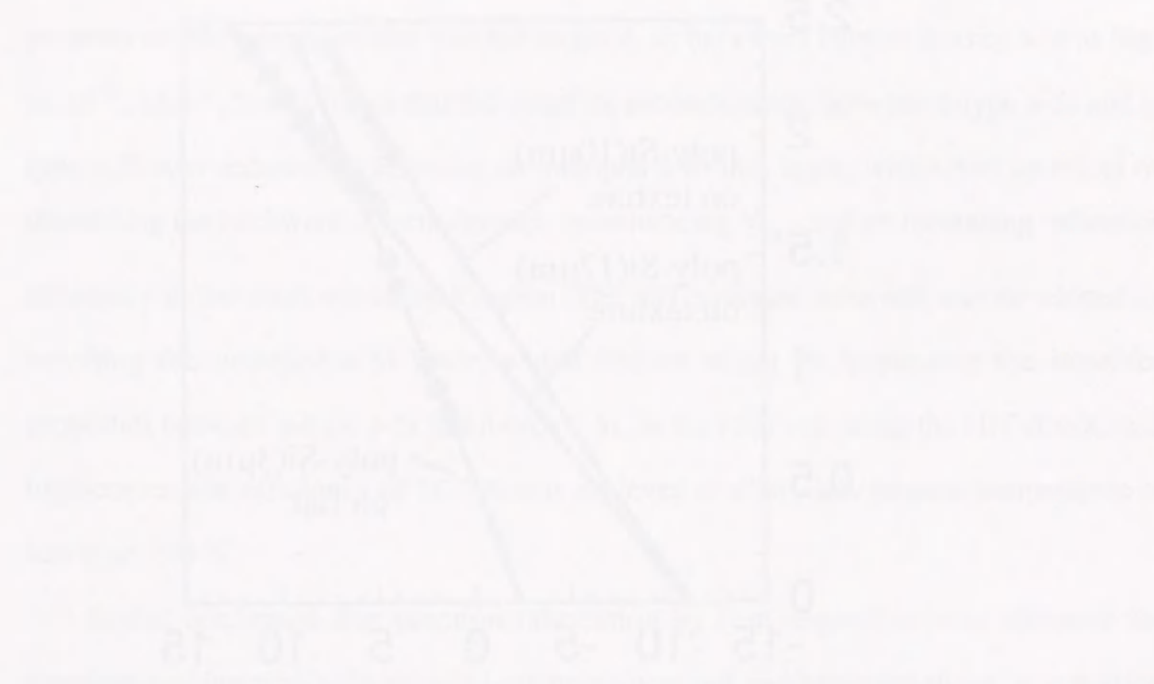
$$F = K(\alpha^{-1}+L), \qquad (4.4\text{-}3)$$

where K is a constant depending only on cell parameters and the selected value of I_{SC}. The absorption coefficient of single crystalline silicon at various wavelengths was used to calculate F. [13] Figure 4.4-7 shows the plot of intensity (F) versus α^{-1} for the solar cell shown in Figs.4.4-1, 4.4-4, and 4.4-5, where each F was calculated using the I_{SC} of 11.5, 24.7, and 28.4 mA/cm^2, and the thickness of 3, 12, and 10 μm, respectively. The diffusion length is obtained from the negative intercept on the α^{-1} axis and the estimated diffusion lengths are 2.5, 11, and 11 μm for poly-Si (3 μm) on flat, poly-Si (12 μm) on texture, and poly-Si (10 μm) on texture, respectively. The diffusion lengths were found to increase as the property of the n-type thin-film poly-Si was improved. In the solar cell with thickness of 10 μm, the diffusion length of 11 μm, which was longer than the thickness, was obtained. This long diffusion length contributes to the high collection efficiency of 51 % at a wavelength of 900 nm.

Thus, it was also confirmed from the result of solar cell characteristics that SPC method in used in this study was an effective fabrication method for solar cell materials.

The summaries in this Section are following. The thin-film poly-Si solar cells were developed, using n-type poly-Si prepared by the SPC method as an active layer. I succeeded in the fabrication of the poly-Si solar cells on the substrates except for silicon at the low temperature of 600 °C. It was proved that n-type poly-Si prepared by the SPC method exhibited high photosensitivity in the long wavelength region where a-Si solar cells have no photosensitivity. As the film properties improved, the solar cell characteristics were enhanced, and a conversion efficiency of 6.3 % was obtained in a solar cell with a size of 1 cm^2. This solar cell showed a high collection efficiency of 51 %

at a wavelength of 900 nm, despite its 10 μm thickness. The high value is attributed to a diffusion length of 11 μm, which is longer than the thickness.



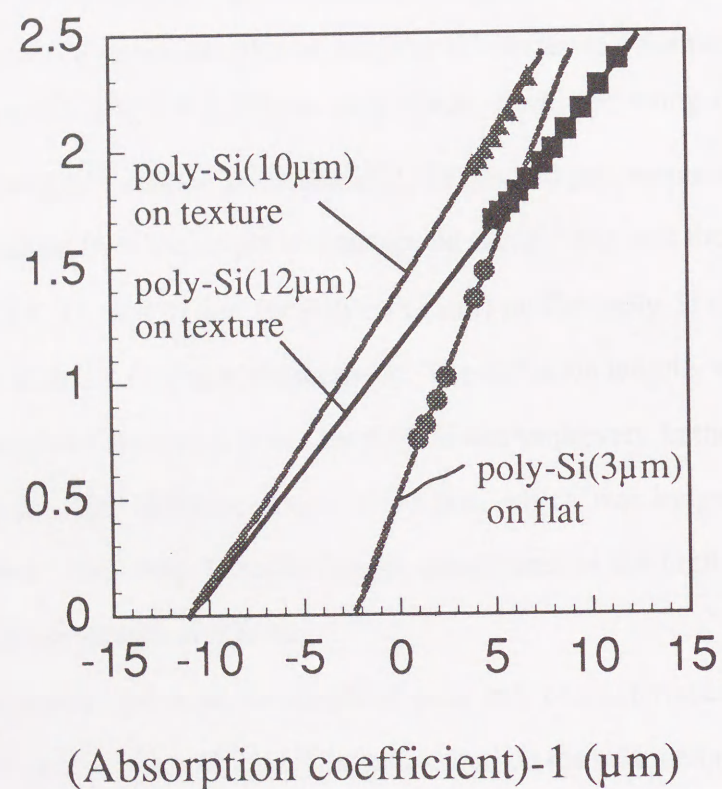


Fig. 4.4-7 Diffusion length estimated by the constant short-circuit current method, for solar cells msde of various n-type thin-film poly-Si prepared by SPC method.

4.5 Summary

Junction formation by film deposition was investigated for both homojunctions and heterojunctions. A p-n homojunction was fabricated by the SPC method, and the junction had a sharp distribution of boron concentration in the depth, compared with thermal diffusion and ion implantation methods. The backward current density of dark the I-V characteristics was also as low as 4×10^{-8} A/cm^2. In a solar cell using this technology, a high I_{sc} of 42 mA/cm^2 and conversion efficiency of 14.2 % were obtained at a low process temperature of 650 °C.

An a-Si/c-Si heterojunction was fabricated by plasma-CVD method. The interface property of this heterojunction was not so good, as backward current density was as high as 10^{-6} A/cm^2. It was found that the interface recombination between p-type a-Si and n-type c-Si was reduced by inserting an undoped a-Si thin layer, which had an effect on decreasing the backward current density, on enhancing V_{oc}, and on increasing collection efficiency in the short wavelength region. The HIT structure solar cell was developed by inserting the undoped a-Si layer, which had an effect on improving the interface properties between p-type a-Si and n-type c-Si. In the solar cell using the HIT structure, a high conversion efficiency of 18.7 % was achieved at a very low process temperature of less than 200 °C.

It was confirmed that junction fabrication by film deposition was effective for improving of junction properties in both homojunctions and heterojunctions. A reduction in the process temperatures was also achieved.

Using the new junction fabrication technology, thin-film solar cells applying n-type poly-Si prepared by the SPC method to the active layer were developed. It was revealed that the solar cells could be fabricated on the substrates except for silicon at the low temperature of 600 °C, by using the SPC method. It was proven that n-type poly-Si prepared by the SPC method exhibited high photosensitivity in the long wavelength region where a-Si solar cells have no photosensitivity. As the film properties improved, the solar cell characteristics were improved, and a conversion efficiency of 6.3 % was obtained in a solar cell with a size of 1 cm^2. This solar cell showed a high collection

efficiency of 51 % at a wavelength of 900 nm, despite its 10 μm thickness. The high value is attributed to a diffusion length of 11 μm, which is longer than the thickness.

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5. Summary

In this thesis, a systematic study was performed to develop thin-film solar cells with high photosensitivity in the long wavelength region where a-Si solar cells had no photosensitivity, through the approaches of the fabrication process and the junction formation technology.

Concerning the fabrication process, a new solid phase crystallization (SPC) method was developed, using a-Si films as a starting material. As for junction formation process, a new technology for p-n junctions (homo- and heterojunction) was developed using film deposition.

In Chapter 2, the theories on the growth and electrical transport of poly-Si, and on the current-voltage characteristics of p-n junction were described. In the growth theory, the kinetics of crystallization in solid phase was discussed and it was shown that transient time, nucleation, and growth velocity had the temperature dependence. The relationship between the conductivity and trap density was also introduced on the basis of the assumption which carrier trapping at grain boundary governed the electrical transport properties.

In Chapter 3, the effects of phosphorus and boron atoms, which are dopant for silicon, on solid-phase crystallization were investigated. These atoms were found to have the effects of promoting crystalline phase. A partial doping method of separating nucleus generation-layer and crystal-growth layer was developed using this feature of dopant, and it was shown that control of nucleation was a much effective means for improvements of thin-film poly-Si properties.

Based on the partial doping method, improvements of the film properties were attempted. As for crystal-growth layer, a-Si films suited to solid-phase crystallization were investigated. It was found that a-Si films with the large TA/TO value in Raman spectrum increased the average grain size of poly-Si after the SPC process. This enlargement of grain size attributed to the increase of growth velocity and the decrease of nucleation rate by the large distortion energy stored in a-Si films.

The film properties were further improved using textured substrate with at random surface morphology. The films on textured substrate had about 7 times higher mobility

and 2 times larger grain size than that on flat substrate. It was found that a factor for the enlargement of grain size was the increase of the growth velocity in SPC by the large distortion energy stored in a-Si films. By optimizations of the poly-Si films on textured substrate, the films with high mobility of 623 cm^2/Vs was obtained.

P-doped a-Si films containing the grains with single-crystalline phase were used as a nucleus-generation layer. By using this internal seeding technology, the films after the SPC process had grain boundary perpendicular to substrate and it was indicated to be able to control the direction of solid-phase growth. In this thin-film poly-Si, a maximum mobility of 808 cm^2/Vs was achieved at a carrier concentration of $1.3x10^{16}$ cm^{-3}.

So, it was proven through the innovative technologies that the decrease of nucleation and the increase of growth velocity in the SPC process were very effective for the improvements of the thin-film poly-Si properties.

In Chapter 4, a new junction formation technology and the thin-film poly-Si solar cells using this technology were studied. The formations of homo- and heterojunctions by film deposition were investigated for the purpose of preventing the existence of opposite types of dopants in a same semiconductor. In a p-n homojunction fabricated by the SPC method, the backward current density of dark I-V characteristics was as low as $4x10^{-8}$ A/cm^2. In the solar cell using this junction, a high I_{sc} of 42 mA/cm^2 and conversion efficiency of 14.2% were obtained at a low process temperature of 650°C. p-type a-Si/n-type c-Si heterojunctions were also fabricated by plasma-CVD. HIT structure solar cells, which undoped a-Si was inserted at interface between p-type a-Si and n-type c-Si, were also developed. This type solar cells had a low backward current density of $1x10^{-8}$ mA/cm^2, and a maximum conversion efficiency of 18.7 % was achieved at a very low process temperature of less than 200 °C. So, it was confirmed that the junction fabrication by film deposition was a considerably effective means for the improvements of junction properties in homo- and heterojunctions.

Since the thin-film poly-Si with good properties and the innovative technology for junction formation were developed, thin-film solar cells applying n-type poly-Si prepared by the SPC method to an active layer were fabricated using the new heterojunction fabrication technology. It was revealed that the solar cells could be fabricated on the

substrates except for silicon at a low process temperature of 600 °C. and, that the solar cells exhibited high photosensitivity in the long wavelength region where a-Si solar cells had no photosensitivity. As the poly-Si film properties improved, the solar cell characteristics was increased, and the conversion efficiency of 6.3 % was obtained in the solar cell with a size of 1 cm^2. This solar cell showed a high collection efficiency of 51 % at a wavelength of 900 nm despite 10 μm thickness. This high value is attributed to the diffusion length of 11 μm longer than the thickness. Thus, it was found that the thin-film poly-Si prepared by the SPC method was very suitable for solar cell materials.

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