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RF CMOS Integrated Circuit: History, Current Status and Future Prospects

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SUMMARY As great advancements have been made in CMOS process technology over the past 20 years, RF CMOS circuits operating in the microwave band have rapidly developed from component circuit levels to multiband/multimode transceiver levels. In the next ten years, it is highly likely that the following devices will be realized: (i) versatile transceivers such as those used in software-defined radios (SDR), cognitive radios (CR), and reconfigurable radios (RR); (ii) systems that operate in the millimeter-wave or terahertz-wave region and achieve high speed and large-capacity data transmission; and (iii) microminiaturized low-power RF communication systems that will be extensively used in our everyday lives. However, classical technology for designing analog RF circuits cannot be used to design circuits for the abovementioned devices since it can be applied only in the case of continuous voltage and continuous time signals; therefore, it is necessary to integrate the design of high-speed digital circuits, which is based on the use of discrete voltages and the discrete time domain, with analog design, in order to both achieve wideband operation and compensate for signal distortions as well as variations in process, power supply voltage, and temperature. Moreover, as it is thought that small integration of the antenna and the interface circuit is indispensable to achieve miniaturized micro RF communication systems, the construction of the integrated design environment with the Micro Electro Mechanical Systems (MEMS) device etc. of the different kind devices becomes more important. In this paper, the history and the current status of the development of RF CMOS circuits are reviewed, and the future status of RF CMOS circuits is predicted.
key words: RF, CMOS, transceiver, integrated circuit, MEMS, future

1. Introduction

There has been rapid progress in the development of wireless communication systems such as portable radio telephones or the wireless LAN, owing to digitization of systems and advancements in CMOS LSI technology over the past 20 years. Current mobile radio terminals can support various functions in addition to simple voice calls; for example, they support wireless LAN (WiFi or Bluetooth) and RFID, and they are equipped with TV receivers, music players, and cameras.

The RF circuit transmits and receives RF signals in that digital data are modulated. Mobile phones and wireless LAN systems use microwave frequency bands from 0.8 to 10 GHz. For a main application, there are GSM systems (0.8-, 0.9-, 1.8-, 1.9-GHz bands), DCS (1.8-GHz band), W-CDMA (1.9-, 2.1-GHz bands), wireless LAN (2.5-, 5-GHz bands), and UWB applications (3.1–10.6-GHz band). In order to operate circuits in these high-frequency bands, research and development until the 1990s was primarily based on the use of integrated circuits consisting of high-speed compound semiconductor devices or bipolar transistors with superior high-frequency characteristics.

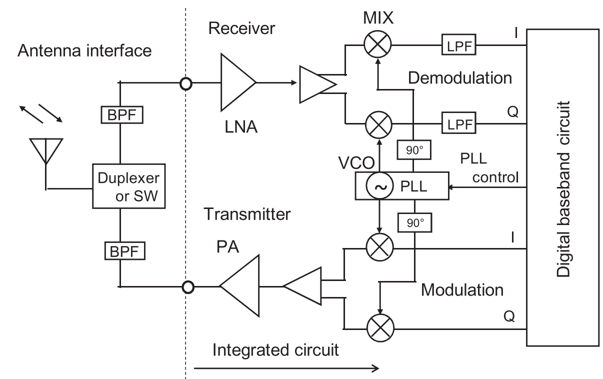

Fig. 1 Basic block diagram of a direct conversion RF transceiver.

However, as the high frequency operation in the GHz band having been enabled even in the CMOS circuit along with the CMOS technology advancement according to Moore's Law smoothly and appearance of short distance radio standard (Bluetooth system) which is easy to comparatively realize performance with the CMOS, the research and development of the RF CMOS circuit got into full-scale [1], [2].

The greatest merit of the RF CMOS circuit is that it can be integrated with the CMOS digital processing circuit, which is a circuit used for baseband processing. It is expected that a very wide range of functions will be facilitated by the use of the so-called system on chip (SoC), which has high reliability, low cost, and a small size. Initial development was focused on component circuits such as a low noise amplifier (LNA), power amplifier (PA), mixer (MIX), or voltage control oscillator (VCO) consisting of an RF transceiver (cf. Fig. 1); subsequently, there was a need to develop one-chip transceivers. Recently, RF transceivers that facilitate multiband/multimode operation covering the services of multiple frequency bands have been reported.

In addition, circuit technologies for overcoming the problems arising from advancements in CMOS technology were developed; these technologies involved more than sim-

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ply replacing rearranging classical analog RF circuits with compound semiconductor devices or the bipolar transistors. While classical analog RF circuits were capable of treating continuous voltage and continuous time signals, design that is based on the use of discrete voltages and the discrete time domain and that facilitates digital control was combined with RF transceiver design. A direct sampling mixer with the high speed and wideband characteristics of CMOS technology was proposed. For the phase locked loop (PLL) circuit in the RF transceiver, an all-digital feedback control technique and circuit topologies were investigated. Furthermore, a calibration technique based on the use of a digitally assisted circuit was adopted as a countermeasure against signal distortions as well as variations in process, power supply voltage, and temperature.

Scalable RF circuits that can help to achieve higher performance using chips with smaller areas as the CMOS process scaling continues are currently being studied. Further, versatile transceivers such as those used in the software-defined radio (SDR), cognitive radio (CR), and reconfigurable radio (RR) have been proposed as systems to be used in the near future.

It is expected that by 2020, the minimum processing dimensions in CMOS technology will be less than 11 nm. In this paper, we review the development history of the RF CMOS circuit technology and survey the technical developments that will occur ten years from now.

First, in Sect. 2, we review the developments since 1990, when RF CMOS circuit technology began to attract attention as CMOS technology scaling continued. In Sect. 3, we present important RF CMOS circuit technologies, including technologies that resulted from our research and development. In Sect. 4, we discuss the future prospects for RF CMOS circuit technology. We conclude the paper in Sect. 5.

2. RF Circuit Consisting of MOS Transistors

2.1 Relation between Performance of RF Circuits and MOS Transistor Scaling

A characteristic feature of a basic RF amplifier circuit as shown in Fig. 2 is that it is capable of narrow-band operation because it includes a resonant circuit consisting of a load inductor L_L and a capacitor C_L. The voltage gain Av of the circuit is expressed as

$$Av = -gm \cdot r_L \cdot Q_L^2 \tag{1}$$

Here, gm is the transconductance of the transistor, and Q_L and r_L are the Q value and loss resistance of L_L, respectively. Equation (1) can be rewritten by using an equation that relates the transition frequency f_T and Q_L (shown in Fig. 2).

$$Av = -2\pi f_T \cdot C_{in} \cdot \frac{1}{r_L} \cdot \frac{L_L}{C_L} \tag{2}$$

where C_{in} is the input capacitance of the transistor. From this equation, it is clear that the amplifier gain increases as the value of f_T increases. Even if f_T is small, the gain can be obtained by using an inductor with a large inductance, if C_{in} is almost equal to C_L. As f_T is inversely proportional to the gate length, the RF amplifier gain can be easily obtained as advancements are made in CMOS technology.

2.2 History of RF CMOS Circuits

The changes in RF CMOS circuit technology with changes in CMOS technology are shown in Fig. 3.

The first RF CMOS circuit was a differential amplifier with a gain of 14 dB at a center frequency of 770 MHz, as reported in 1993 [3]. At that time, the gate length of a MOS transistor was 2 μm, and the value of f_T was thought to be around 1 GHz. Therefore, a 127-nH inductor was integrated with this circuit by the micro electro mechanical systems (MEMS) process in order to achieve a high self-resonance frequency and high Q value. As a result of advancements made in CMOS technology in accordance with Moore's Law, f_T became large, and it became easy to achieve a gain even when an inductor with a small inductance was used; this can be easily understood by considering Eq. (2). After the mid 1990s, an ambitious study of RF CMOS component circuits was carried out. The inductance of the inductor used in the chip was decreased to several nanohenries, and the Q value was on the order of several tens; even in these cases, the gain can be obtained by using Eq. (2).

In a low noise amplifier (LNA) that limits the sensitivity of the RF receiver, a circuit for inductive source degeneration, as shown in Fig. 4(a), was often used in order

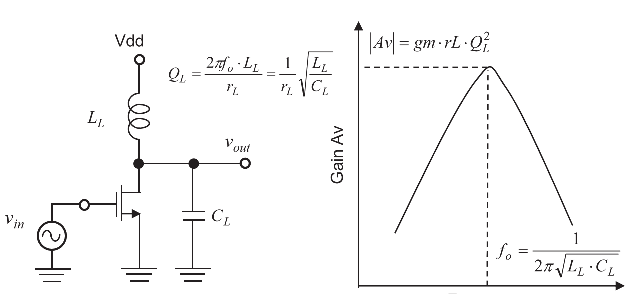

Fig. 2 Common source amplifier with an inductor as a load.

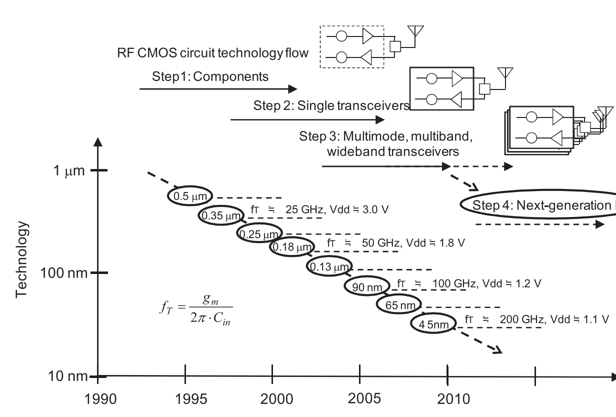

Fig. 3 Microwave RF CMOS circuit technology flow.

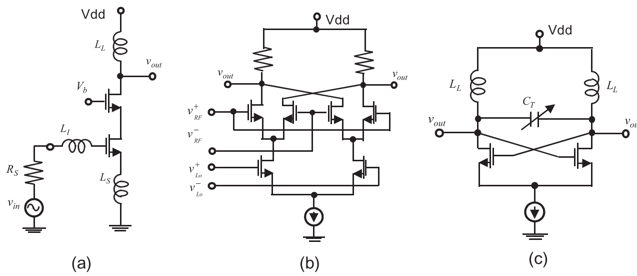

Fig. 4 Basic RF CMOS component circuits: (a) Low noise amplifier (LNA), (b) Mixer (MIX), (c) Voltage controlled oscillator (VCO).

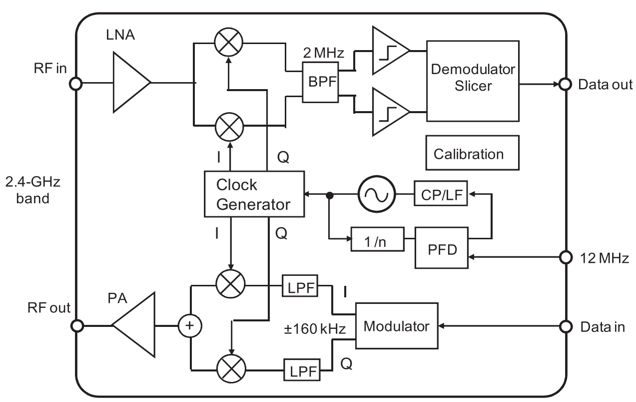

Fig. 5 Single-chip Bluetooth transceiver with direct conversion transmitter and low-IF receiver [18].

to achieve both input matching and low-noise performance without using resistors that generate thermal noise. There are many reports on such LNAs, e.g., the LNA operating in the 0.9-GHz band (GSM) and the LNA operating in the 1.8-GHz (DCS) band [4]–[6]. For a mixer (MIX), the Gilbert cell circuit that was often used in a bipolar transistor circuit was introduced into the CMOS circuit, as shown in Fig. 4(b), [7]–[9]. A differential cross-couple type circuit with an LC resonant circuit (Fig. 4(c)) was used as a VCO. The main design objective was to decrease the phase noise [10]–[15]. During the period in which these studies were carried out, no studies such as [16] were carried out on CMOS power amplifiers, because it was believed that a high RF output with high conversion efficiency cannot be achieved when CMOS technology is adopted. In the 1990s, RF CMOS circuits were developed by adopting RF bipolar circuits or using circuits comprising compound devices.

In the late 1990s, the process generation developed was researched to a 0.35-μm technology. Further, the short-range wireless LAN (Bluetooth; 2.5-GHz band) that can be easily implemented was standardized. The specifications were acceptable for the CMOS circuit. Integrated transceiver chip was introduced [17], [18]. Figure 5 shows a block diagram of a Bluetooth one-chip transceiver that was introduced in 2001 [18]. The conventional super heterodyne architecture was not used as the transceiver architecture; instead, a direct conversion technology [19] was adopted in the case of the transmitter and a Low IF technology was adopted in the case of the receiver in order to omit external IF filters.

When process technology advances to the deep submicron (0.25–0.13 μm) region, operation at more than 5 GHz can be targeted. The research and development of a transceiver for wireless LAN, WCDMA, and GMS systems was also initiated. However, the following new problems surfaced with the CMOS technology advancement in an RF CMOS circuit.

(i) Low-voltage operation: A power supply voltage of 3 V can be applied until the process technology advances to 0.35-μm technology. Therefore, it was possible to replace conventional RF circuits with CMOS circuits without changing the topology. However, it became difficult to achieve noise tolerance and a dynamic range using a low-voltage power supply, especially in the case of stacked transistor topologies such as that in the Gilbert cell. In the current 90-nm or 65-nm CMOS technology, the power supply voltage is around 1 V.

(ii) Tolerance to variations: The variations in transistor characteristics increase as CMOS technology advances. It is important to compensate for the increasing influence of variations not only in the fabrication process but also in the power supply voltage and temperature variations (PVT variations).

(iii) Scalability in RF circuits: The area occupied on the chip by the inductor that is commonly used in the RF circuit is large (the area is normally several hundred square microns) in comparison with the area occupied by transistors. The area occupied by the inductor cannot be reduced as the technology advances. Therefore, the fraction of the area on the SoC chip that is occupied by RF circuits increases, and thus, costs become high. There was a expectation to realize a scalable RF circuit that both occupies a small area on the chip and helps to achieve higher performance as the technology advances.

(iv) Wideband operation: It was expected that the wide band RF circuit that enables multiband/multimode operation and supports several radio services would be developed. Recently, there has been a demand for an RF circuit that is capable of large-scale digital processing and can thus be used to support multiple applications with the help of software programs or software control. SDR, CR, and RR are examples of systems in which such a circuit is used.

After 2001, studies aimed at solving these problems were promoted. In particular, the one-chip Bluetooth transceiver (Fig. 6), reported in 2004 [20], [21], attracted attention as a RF transceiver circuit technology of digital rich. For transceiver design, conventional analog designs developed for continuous voltage and continuous time signals were replaced by a discrete-time design. In the case of the PLL circuit, digital feedback control based on the use of a digitally controlled oscillator (DCO) and a time to digital converter (TDC) was carried out. The operation of the MIX in the receiver part was based on a digital direct sampling technique (these circuit techniques are briefly described in the next section). Thereafter, there was progress in research and development of the RF circuit technology that can be adopted for employing not only the analog circuit but also the digital technology in which the time domain can be exploited, and current RF circuit designs are based on this technology.

There are two methods for realizing a multiband/multimode function: (i) integrating multiple transceivers on a chip, as shown in Fig. 7, and (ii) realizing a programmable transceiver that can be controlled for carrying out multiple applications, as shown in Fig. 8. Examples of transceivers that were recently developed by the former method are the one-chip transceiver that supports WCDMA and 4-band GSM functions [22], as well as the transceiver that supports 2.4- and 5-GHz LAN along with FM radio [23].

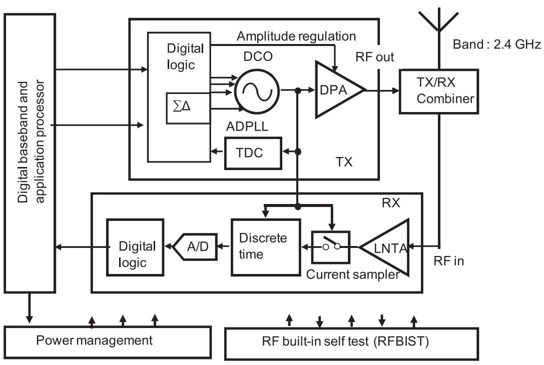

Fig. 6 Single-chip Bluetooth radio with an all-digital transmitter and a discrete-time receiver [20], [21].

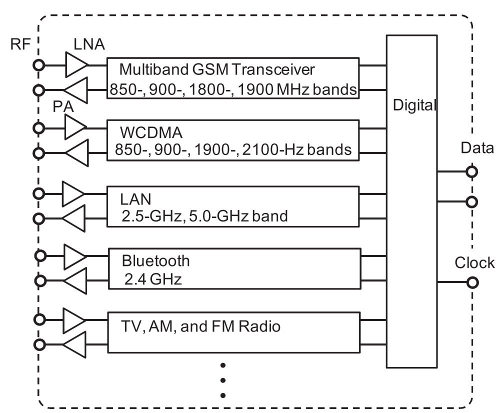

Fig. 7 Multi-transceiver structure for multimode/multiband communication.

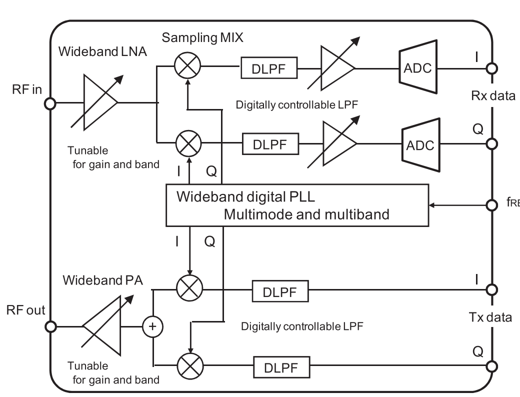

Fig. 8 Digitally controllable software defined radio.

An example of a transceiver developed by the latter method is an SDR one-chip transceiver that supports WCDMA/LTE, WiMAX, and digital TV (DVB-H). This transceiver is based on 40-nm CMOS technology; this transceiver was reported recently [24]. Although this transceiver is also equipped with a number of LNA and output amplifiers, RF signal modulation/demodulation and PLL circuits are communized for plural applications. It is believed that by adopting new transceiver architectures based on advanced CMOS technology, versatile transceivers such as those used in SDR, CR, and RR will be realized [25].

Thus, we have reviewed the development history of RF CMOS circuits with the scaling of CMOS technology. The current CMOS process technology already reaches 100-nm node and enters in the nanoscale era, greater integration and support for a large number of functions are expected in the case of RF CMOS transceivers. In the following section, we introduce circuit technologies that form the basis of current research and development, and we present our study on the technologies for developing scalable RF CMOS circuits.

3. RF CMOS Circuit Technique in Nanoscale Era

In the present design of microwave RF CMOS integrated circuits, it is important to consider the four categories of circuit design as shown in Table 1 [26]. It is believed that digitally controllable discrete voltages and time domain techniques will be useful for realizing the integration of fully monolithic wideband transceivers and for achieving tolerance to the PVT variations. Therefore, researchers studying circuit design are now trying to consider the four design categories.

3.1 Design Technique Based on Time Domain Control

As the techniques for time domain design which was carried out to obtain the circuit shown in Fig. 6 have already been introduced in many papers [e.g. 27], these techniques are briefly reviewed in this section.

(1) All-Digital PLL

In the conventional PLL circuit, the output of an analog

Table 1 Four categories of circuit design [26].

Time Domain / Voltage Domain	Continuous	Discrete
Continuous	R1 Analog	R2 Sampling SCF
Discrete	R3 TDC, PWM	R4 Digital

VCO is compared with the phase of the reference signal and the result is fed back in order to control the oscillation frequency of the VCO. However, in the circuit shown in Fig. 6, digital feedback control is performed by using the DCO and the TDC. The DCO circuit is shown in Fig. 9(a). This is the cross-coupled oscillator with LC resonant, but there are a number of small-sized varactors; for example, more than 1024 varactors are used for achieving a resolution of 10 bits, and these varactors are switched digitally for frequency tuning. The output signal is compared with the reference signal using the TDC, as shown in Fig. 9(b). The signal from the DCO is input to the delay line of the cascaded inverter. By reading out the signal status at each tap of the delay line using the flip-flop operated with the reference signal, a digital thermometer code can be obtained. The feedback to the DCO is implemented by processing the code digitally. In order to carry out the processing illustrated in Fig. 6, a delta-sigma modulation is adopted to suppress the spurious generation caused by the digital tuning operation for the DCO.

(2) Direct Sampling Mixer

An example of a direct sampling mixer used in the receiver part of the circuit illustrated in Fig. 6 is shown in Fig. 9(c). In this circuit, a modulated RF signal is sampled by directly switching the MOS transistor M_s according to the signal at the RF carrier frequency, L_o. The phase information of the modulated RF signal is stored in a capacitor C_R and is given by the amount of charge. Information can be extracted by observing the change in the amount of stored charge. However, if the sampling operation is continued for a long time, C_R is full filled with charge. To avoid this, eight capacitors identical to C_R are placed in parallel; C_R that is being charged is selected by the DCU. When four capacitors in Bank A are charged, the charging operation is shifted to Bank B. When the capacitors in Bank B are charging, information is extracted on the basis of the charge in the frequency can be decreased by a factor of 32. If the frequency of the RF signal is 2.4 GHz, the carrier frequency can be decreased to 75 MHz that this frequency is acceptable for the AD converter used for demodulation. C_H is called a history capacitor, and it filters high-frequency components.

The circuit offers the following advantages: (i) wideband operation can be achieved by changing the sampling frequency; (ii) the circuit is suitable for circuit integration because it is a digitally controlled circuit that does not have analog filters.

(3) RF Signal Generator Based on Time to Analog Conversion

Figure 10 shows the circuit that generates the sinusoidal RF signal from a digital square pulse signal by summing the outputs at the taps of a delay line. The operation principle of this circuit is opposite to that of the TDC. For example, the delay cell includes a two-stage inverter. A signal with an arbitrary waveform can be obtained by choosing the delay tap signal that should be added by a control circuit. A triangle waveform can be obtained by summing all the tap signals belonging to one period. Figure 10(b) shows a mea-

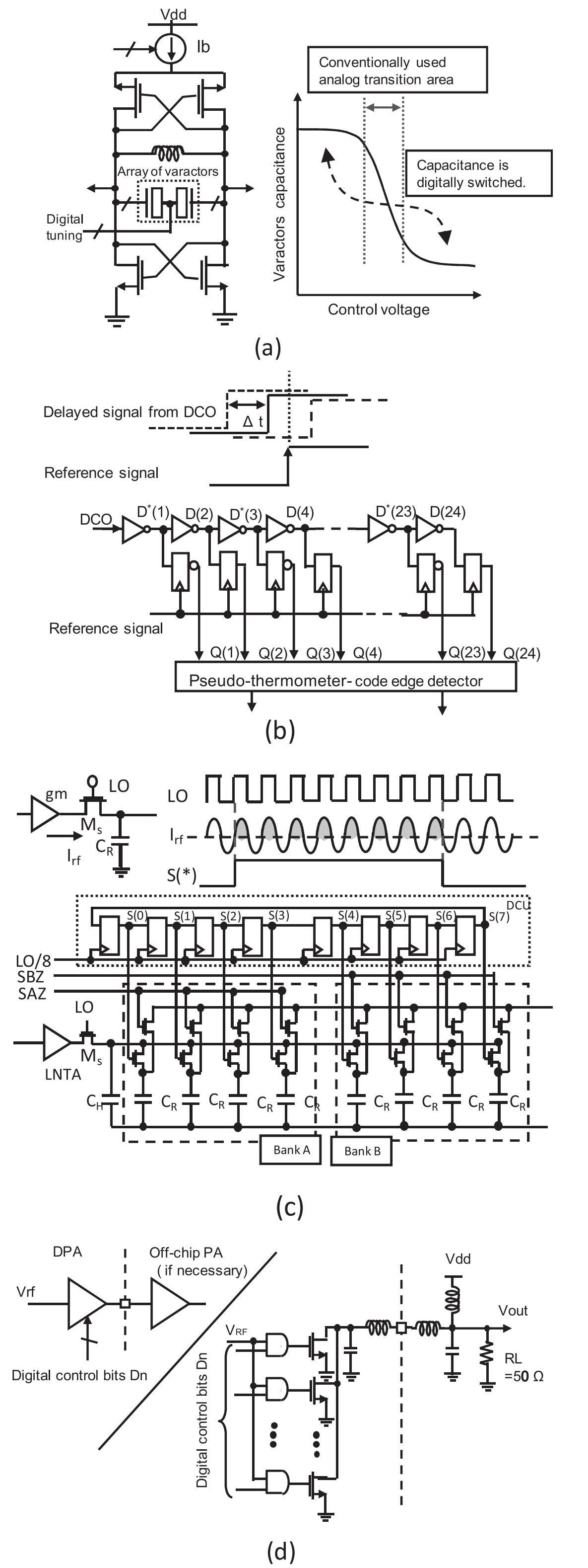

Fig. 9 Circuit technologies used in an all-digital transceiver: (a) Digitally controllable oscillator (DCO), (b) time to digital converter (TDC), (c) direct sampling mixer, (d) digitally controlable PA, [20], [21].

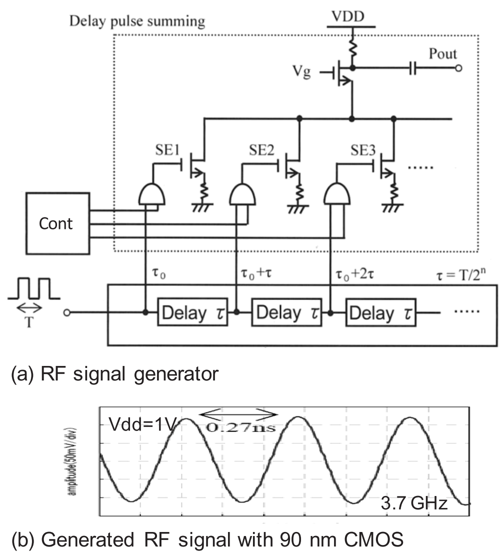

Fig. 10 Time to analog conversion circuit for RF signal generation: (a) RF signal generator, (b) Generated RF signal with 90 nm CMOS.

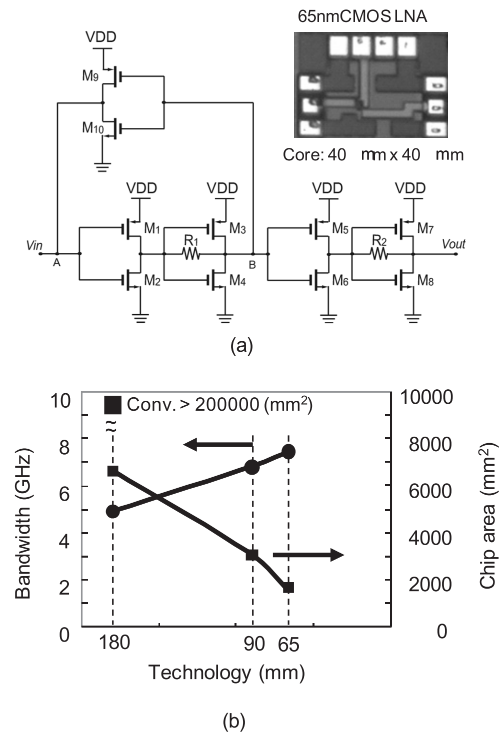

Fig. 11 CMOS inverter base wideband LNA, (a) 65 nm circuit, (b) technology dependency for bandwidth and chip area.

sured waveform generated by a chip fabricated by adopting 90-nm CMOS technology. A sinusoidal 3.7-GHz RF signal was generated by the fabricated chip when appropriate delay taps of 5 bits were selected. The third harmonic could be limited to −50 dBc via precise delay control [28].

3.2 Scalable Wideband RF Circuit

As described in Sect. 2, there are two methods for realizing the multiband/multimode function: (i) integrating multiple transceivers on a chip and (ii) realizing a programmable transceiver that can be controlled for carrying out several applications. The disadvantages of the former method are that the circuits occupy a large area on the chip and that the range of applications is limited by the specific transceivers that are integrated. Therefore, a programmable wideband RF circuit with a small chip area is required.

Furthermore, the circuit should be operated at a low power supply voltage, should not contain inductors so that it occupies a small area on a chip, and should be scalable as CMOS technology advances. A "scalable" circuit is a circuit whose performance improves and size decreases as the technology advances. In order to develop a scalable RF circuit that satisfies these requirements, a circuit consisting of inverters is considered. An advantage of the conventional RF circuit with inductors is that high-frequency operation can be achieved by exploiting the resonance between the inductor and the capacitive components of the transistors and wire lines. The inverter circuit with a resistive load can be operated in a wideband frequency region from DC to high frequencies, but as the bandwidth in the high-frequency region is limited by the RC low-pass filtering characteristics, the operation frequency cannot be increased such that it lies in the frequency band corresponding to the operation of the circuit with an inductor. An appropriately designed circuit with an inductor can be operated at frequencies greater than f_T. In the case of the resistive load circuit, if a 20-dB gain is assumed, the 3-dB-down frequency bandwidth is about 10% of the value of f_T. However, as a result of advancements in the technology, the value of f_T exceeded 100 GHz, and the inverter circuit without inductors was capable of operation in the microwave frequency region, e.g., at frequencies between 1 and 10 GHz.

(1) Wideband LNA Consisting of CMOS Inverters

Figure 11(a) shows an LNA consisting of CMOS inverters [29], [30]. In this circuit, two kinds of broadbanding techniques are applied: In the first technique, the Cherry-Hooper topology [31] is extended to CMOS inverters. By cascading a transconductor amplifier stage consisting of M_1 and M_2 and a transimpedance stage consisting of M_3, M_4, and R_f, the influence of the Miller capacitance can be reduced, and thus, wideband operation can be achieved. In the second technique, active feedback is implemented by using an inverter consisting of M_9 and M_{10} in order to achieve input impedance matching and a further wideband operation. In the high-frequency region, since the feedback inverter acts as a low-pass filter, the influence of feedback decreases in the high-frequency region, and thus, the gain attains a high value in this region. To evaluate the circuit technology, the circuit was fabricated by adopting 180-, 90-, and 65-nm CMOS technology. The measured bandwidth and circuit area are shown in Fig. 11(b). The gains of the circuits used in each LNA ranged from 15 to 20 dB. The area of this circuit is 5% that of the circuit consisting of inductors. It is clear that a wider bandwidth and smaller circuit were obtained for more advanced technologies. The power supply voltages for the circuits fabricated by the 180-nm and 65-nm CMOS technologies were 1.8 V and 1.2 V, respectively. The noise figure (NF) was about 3 to 5 dB. Further improvement of the design is now being studied for lowering the NF into consideration. Nevertheless, this simple LNA consisting of CMOS inverters is attractive for realizing versatile transceivers fabricated by nanoscale CMOS technology.

(2) Low Phase-Noise Ring VCO

The ring-type oscillator is well known as an inductor-less scalable oscillator. However, the phase noise generated by the oscillator is very large compared to the noise generated by the circuit consisting of inductors. As communication systems, decreasing the phase noise is an important goal in oscillator design. In general, in mobile communications, a phase noise of less than −120 dBc at an offset frequency of 1 MHz is required. However, the phase noise generated by the conventional ring oscillator is 20–30 dB greater than that generated by the circuit consisting of inductors. Therefore, the ring VCO circuit has not been used in RF communication.

To improve the phase-noise characteristics, an injection locking technique for RF applications is being studied [32]. By injecting a low-phase signal generated by the crystal oscillator in the system into the ring oscillator, the phase noise can be reduced by the synchronizing operation. The injection locking operation is shown in Fig. 12(a). As the output phase of the oscillators is corrected whenever the signal pulse for injection, f_{REF}, is input, the RF signal with low phase noise can be obtained from the ring VCO.

Figure 12(b) shows an example of the ring VCO with a terminal for signal injection [33]. Because orthogonal signals with a phase difference of 90° are required for the RF transceiver, the ring VCO is constructed using differential delay cells. In addition, the circuit of the differential delay cell includes a latched inverter structure that can output a signal with a rail-to-rail voltage swing rather than a differential circuit that includes a tail-current transistor. The latched inverter structure is employed because the large voltage swing can help to reduce the phase noise according to model given by Leeson's equation [34].

Figure 12(c) shows the measured phase-noise characteristics of the chip fabricated by 90-nm CMOS technology. By inputting the 500-MHz injection signal, f_{REF}, the phase noise can be reduced dramatically by 46 dB at an offset frequency of 1 MHz.

The disadvantage of injection locking is that the lock range is narrow and the output signal frequency should be an integral or half-integral multiple of f_{REF}. When the VCO is used as a frequency synthesizer, a circuit with the PLL structure [34] for setting the frequency or a circuit for controlling f_{REF} may be necessary. However, the circuit can be fabricated with in a small area because inductors are not necessary.

The use of a multilayer inductor structure has been studied as another means of reducing the VCO circuit area

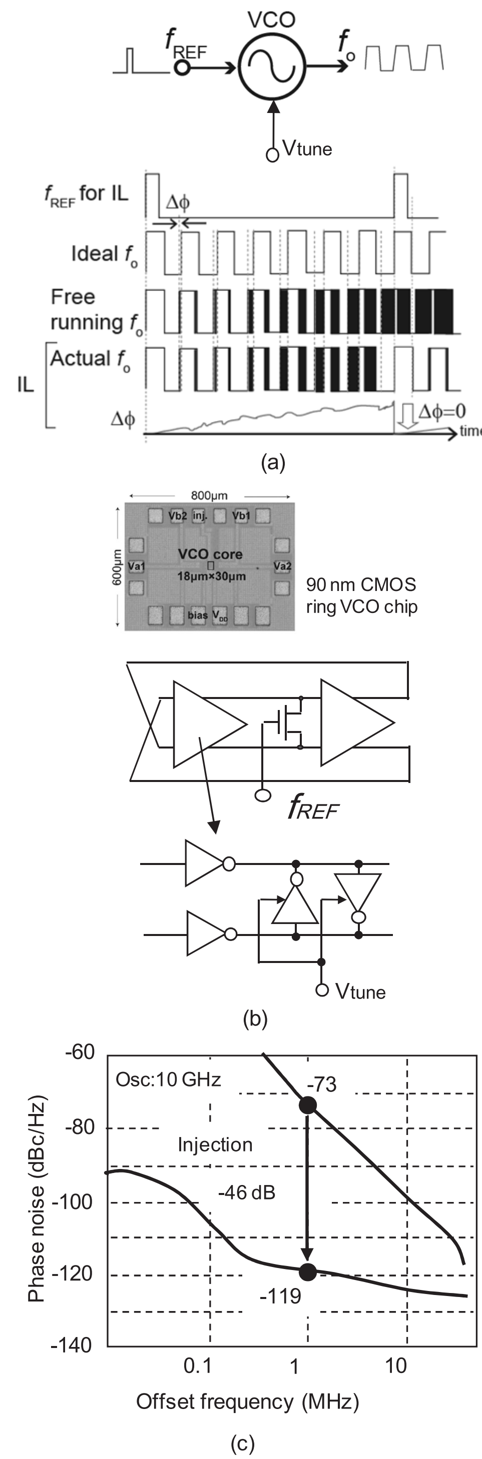

Fig. 12 Injection-locked ring VCO: (a) Injection locking operation, (b) circuit configuration, (c) phase-noise characteristics.

[36].

(3) CMOS Inverter PA Consisting of Stacked Transistors

A CMOS power amplifier is also being studied [37]–[40]. In order to use a CMOS circuit operating at a low voltage of 1 V to obtain a high output power that is comparable to the power output by a 1 W-class amplifier, it is only necessary to increase the signal currents. However, as a large current on the order of an ampere is necessary, it is difficult to output a power of more than 1 W because the resistance loss of the circuit wiring in the chip degrades the power efficiency.

Therefore, a CMOS PA consisting of stacked transistors has been proposed in order to realize a large voltage swing in the output by using a high-voltage power supply while not exceeding the breakdown voltage of the transistors [41], [42]. Figure 13(a) shows an example of such a circuit. As the gates of the cascaded common-gate transistors are self biased by connecting the gate and the drain terminals with resistors, the power supply voltage is automatically divided across the number of transistors. In the output stage, if the maximum voltage between the drain and the source terminal is Vdd, a voltage equal to five times of Vdd can be supplied. Figure 13(b) shows the measured input and output characteristics of the chip fabricated by 65-nm CMOS technology. Even if a power supply voltage of 6 V is induced, the circuit operates without being damaged. The saturation voltage swing at 0.8 GHz was 4 Vpp (17 dBm for 50Ω) [42].

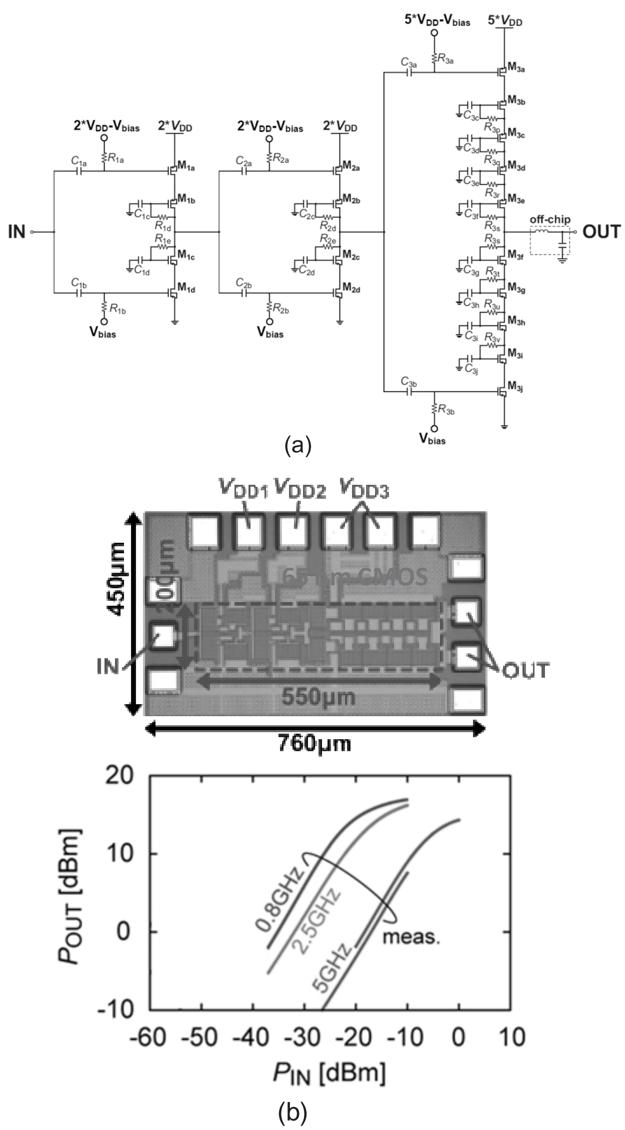

Fig. 13 Stacked power amplifier: (a) Circuit configuration, (b) chip microphotograph and measured input-output characteristics.

3.3 Digitally Assisting Circuit

(1) Digitally Controllable Gain Amplifier

Figure 9(d) shows a digitally controllable gain amplifier that is also used as an output PA in the circuit shown in Fig. 6. A number of common-source transistors are placed in parallel. By digitally controlling the number of activated transistors using AND gate, the gain and power of the output signal can be changed. The output waveform is rectangular, but external LC filters including parasitic impedances in packaging as shown in Fig. 9(d) converts it into a sinusoidal waveform.

(2) Calibration of Non-Linearity

Linearity is important issue in RF circuit design. In the transmitter circuit, the Cartesian feedback technique is often adopted to achieve highly linear operation, as shown in Fig. 14(a). However, it is difficult to control the high-frequency RF signals because the feedback delay generally increases. To overcome this, a digitally assisted circuit, as shown in Fig. 14(b), has been proposed [43]. In a calibration mode, when the feedback loop is active, the status of the transmitter is recorded in the lookup table using analog-to-digital converters (ADCs). After the status is recorded, the feedback loop is switched to an inactive state. Calibrated data are directly sent from the lookup table to up-conversion mixers through digital-to-analog-converters (DACs). There-

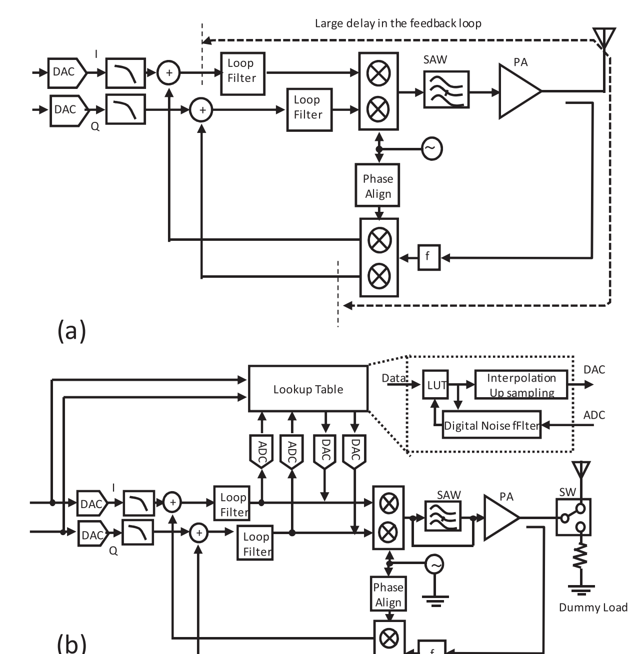

Fig. 14 Cartesian feedback in an RF transmitter: (a) analog feedback structure, (b) digitally assisted structure [43].

fore, high-speed operation becomes possible because the feedback loop does not exist in the operation mode.

4. Future Prospects of RF CMOS Circuit

In the next ten years, the main objectives of research are as follows: (1) realization of versatile RF CMOS transceivers; (2) systematization using the millimeter-wave and terahertz band; and (3) development of microminiaturized RF systems, as shown in Fig. 15.

4.1 Toward Versatile RF Transceiver Systems

In the next ten years, it is highly likely that versatile transceivers such as those used in SDR, CR, and RR systems will be developed by exploiting the advancements in CMOS technology. As shown in Table 1, the importance of an integrated design technique covering four regions will increase; such a technique will help accommodate advancements in the technology. In particular, it will help to compensate for the PVT variations and non-linearity and will facilitate low-voltage operation. In particular, the time domain design will be given more emphasis than the voltage domain design. Further, a method for controlling electric charge in circuits in such a manner that high-speed and low-power operation is achieved is an important component of future design methods. Thus, circuits will consist of several new architectures, which will in turn indicate future prospects.

4.2 Expansion to Millimeter- and Terahertz-Wave Systems

The main focus of this paper was microwave circuit technology, but as speed of the CMOS transistor is increased, the research and development of the CMOS of the millimeter wave region (30–300 GHz) is already being carried out.

In the RF circuitry operating in the millimeter-wave region, operation in the high-frequency region is achieved by using inductors or distributed passive devices such as stub lines. In 2001, a 50-GHz VCO fabricated by 0.25-μm CMOS technology was reported [44].

Recently, a transmitter [40], receiver [46], and a transceiver [47] for high-speed data transmission have been reported; a transmitter and a receiver for a high-speed interconnection [48] and a power amplifier [49] operating in the 60-GHz band have also been reported. Further, millimeter-wave radar systems operating in the 77-GHz band [50] have been demonstrated. Furthermore, research and development of millimeter-wave circuits operating at over 100 GHz has recently been reported [51].

The value of f_T for transistors fabricated by the 11-nm CMOS technology is expected to be 1 THz, and research and development ten years from now will be focused on the terahertz region rather than the millimeter-wave region. In addition, the circuits currently operating in the microwave region will operate in the millimeter-wave region, and this will help to support a wider range of RF communication functions.

4.3 Microminiaturized RF Systems

RF CMOS and MEMS systems must be combined in order to realize an extremely small microminiaturized RF system [52].

The size of computers can be reduced as LSI technology advances. Current mobile telephones (especially smart phones) are regarded as portable computers. It may be assumed that practically everybody carries a computer. Furthermore, with the progress of miniaturization, the portability of computers can be increased and computers can be used in a wide range of locations for communication and evaluation; for example, we can use computers to monitor our health, to preserve the environment, to assist people in agriculture, to monitor production in factories, and to achieve higher comfort levels in society and in our personal lives. Miniaturized systems for such applications must include wireless communication interfaces.

However, when the RF circuit is used in order to develop such systems, miniaturization of an antenna interface circuit consisting of RF duplexers and switches is difficult. Currently, desecrate devises are used for duplexers, which have a large size. Versatile transceivers include several such devices for supporting multiband/multimode wideband operation. Therefore, integration of the wideband duplexer with the CMOS chip was recently attempted [53], but the chip area was large because inductors were required.

Another approach to miniaturization is to combine RF CMOS and MEMS circuits. By using the MEMS circuit and adopting semiconductor production technology, a microminiaturized passive element, sensor, and actuator can be realized. Figure 16(a) shows an airsuspended inductor; the Q value of this inductor is higher than that of the inductor on the CMOS chip. The MEMS inductor has wideband characteristics, as shown in Fig. 16(c). In addition, the inductor value can be adjusted if a MEMS actuator is designed and integrated with the inductor. Furthermore, since this circuit is compatible with the CMOS integrated circuit, the integra-

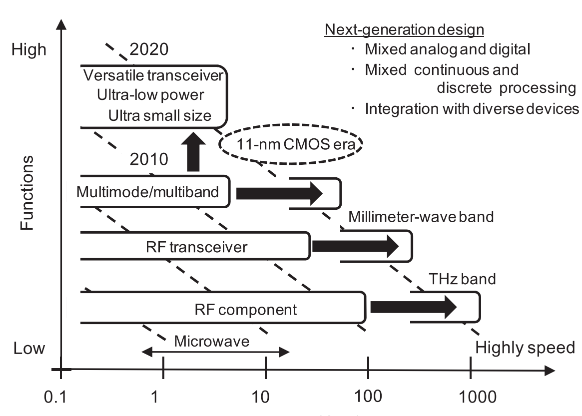

Fig. 15 Trend in RF CMOS circuit technologies.

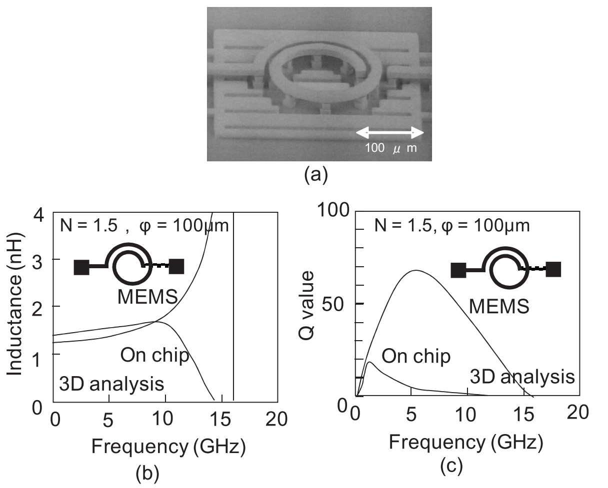

Fig. 16 MEMS inductor: (a) Microphotograph, (b) frequency dependence of inductance, (c) frequency dependence of Q value.

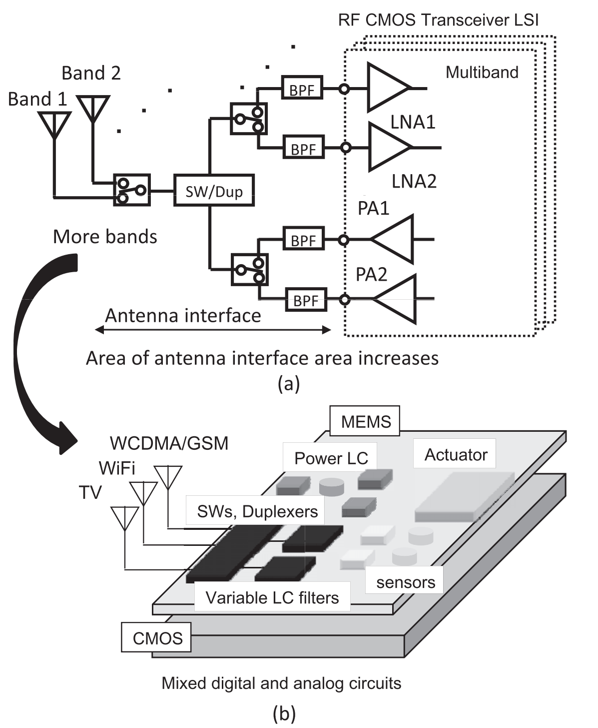

Fig. 17 Advanced micro RF system integrated with CMOS and MEMS: (a) Antenna interface, (b) Schematic of micro RF.

tion of RF CMOS and MEMS circuits is expected.

Figure 17 shows an image of the RF MEMS on CMOS LSI. Of course there are candidates of the multi-chip implementation in a package, CMOS on MEMS and multi stacked structure using 3D implementation technology by considering the big devices and small devices relations in a CMOS IC and the MEMS device.

To realize microminiaturized next-generation RF systems with a wide range of functions, it is important to construct a design platform for combining an RF CMOS circuit and a MEMS device. From the viewpoint of circuit design, the following issues are important: (1) standardization of the MEMS process, (2) expansion of the model library, (3) development of the MEMS control circuit along with the CMOS circuit. (4) Construction of the fusion design environment is necessary.

In particular, it is important to construct the fusion design environment for realizing a complicated microminiaturized system. It is necessary to carry out a coherent design process from the device level to the module level by performing dynamic analysis, heat analysis, electronic network analysis, electromagnetic field analysis, operation inspection, etc. The utility of an integrated design of microminiaturized systems starting at the device level will extend beyond the design of RF CMOS circuits.

5. Conclusions

The development history of technologies for developing microwave RF CMOS circuits was reviewed and future prospects were estimated. It is believed that in the next ten years, circuit speeds will increase and a high degree of integration will be continued as a flow of the necessity by enjoying a benefit of the CMOS production technology for ten years of the future. The main objectives of research are as follows: (1) realization of versatile RF CMOS transceivers; (2) systematization using the millimeter-wave and terahertz band; and (3) development of microminiaturized RF systems.

However, conventional circuit technologies cannot be adopted to achieve these objectives because they are analog design technologies that can applied only in the case of conventional continuous voltage and time domain signals. It is imperative to combine analog and digital technologies involving design for discrete voltages and discrete time. Furthermore, to realize microminiaturized integration, e.g., integration of an antenna and the interface circuit, it is necessary to carry out a coherent design from the device level to the module level by performing dynamic analysis, heat analysis, electronic network analysis, electromagnetic field analysis, operation inspection, etc. The importance of creating an integrated design platform extends beyond the design of RF CMOS circuits.

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