博士論文

Thermal Propagation and Device-Temperature Prediction Techniques for Power Semiconductor Modules with Circuit Simulators

（回路シミュレータを用いたパワー半導体モジュールにおける熱伝搬と素子温度予測技術）

小 島　　崇

広島大学大学院先端物質科学研究科

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主論文

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Chapter 1

Introduction

Si power devices are widely used for output controls of electronic control units in automotive applications. For example, motors, solenoids and lamps are the representative applications. The temperature increase of the Si power devices are the most important issue for the design of such applications. Si power devices have long history of using in railroad trains for power modules. However, Since electrical characteristics of Si devices are again strongly dependent on these temperature, electro-thermal coupling simulation techniques are required to estimate the thermal behavior accurately. Thermal simulations by Finite Element Methods (FEMs) are widely used for predicting temperature distribution.[14] However, the operation environment of Si power modules in railroad trains is different from that in automobiles. The temperature change of Si devices in the railroad trains is limited to the range of 20 - 40 K because of their rich cooling systems.[15] And the rate of temperature change in the railroad trains is quite

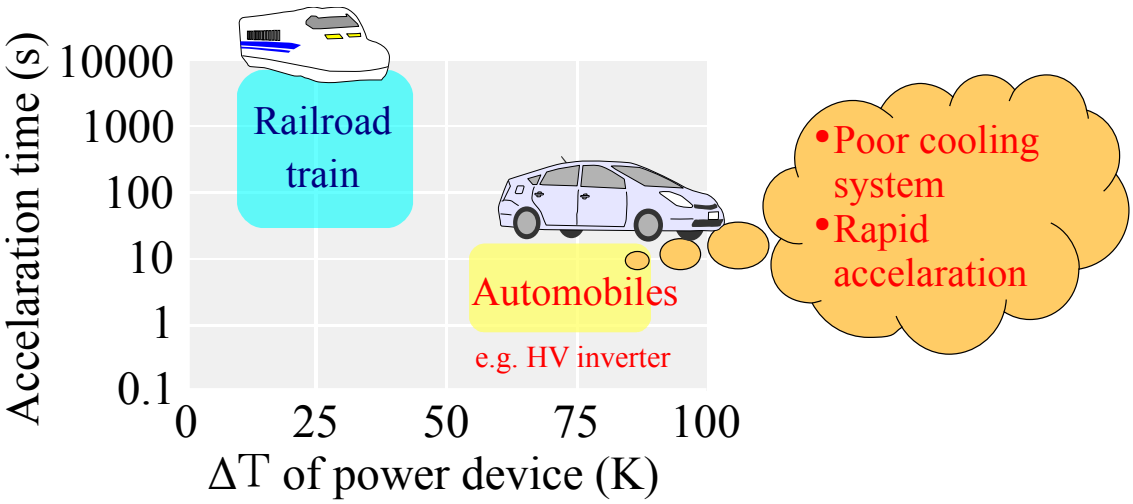


Figure 1-1. Target domain of electro-thermal coupling simulations.

slower than that in the automobiles, because the railroad trains are always gently increase and decrease speed. Therefore, the target domain of electro-thermal coupling simulation for automotive applications is different from that for the railroad trains as shown in Fig. 1-1. Figure 1-2 shows the trends of power applications in the automobiles, which are small size and high power.[17] As a result, the power density of the applications may become higher, and it cause failure of semiconductor devices such as metal oxide semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs) and diodes because of the temperature rise.

FEMs are not suitable for the electro-thermal coupling simulation because of their long calculation time.[7] Also conventional approaches using simple thermal models based on circuit simulators[7, 15] have encountered significant difficulties in accurately predicting the transient behavior of complex automotive power modules. Because the conventional approaches can't consider important features of automotive power modules, they are lateral heat spreading and thermal interference.

On the other hand, electro-thermal coupling simulation technique based on

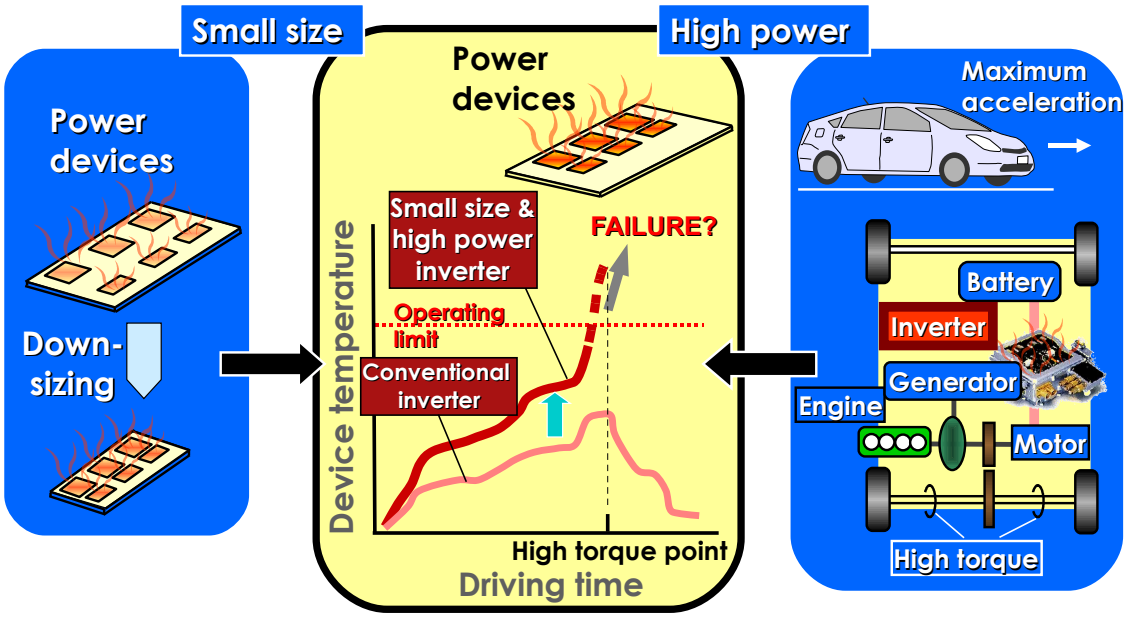


Figure 1-2. Trends of power applications in automobiles, and problem.

electrical circuit simulators were developed.[9,18-23] However, evaluation results of complicated power application such as hybrid vehicle (HV) inverters using electro-thermal coupling simulation technique hardly be reported.

The purpose of this study is achieving the practical use of electro-thermal coupling simulation techniques based on a circuit simulator. This paper describes following novel proposals to achieve the electro-thermal coupling simulation;

- A novel compact thermal model suitable for power modules. The compact thermal model can take into account lateral heat spreading within the modules and thermal interference among power devices.
- A novel electro-thermal coupling simulation technique using table look-up method mainly focused on a dynamic analysis of a HV inverter during real driving operations such as wide open throttle (WOT).
- Stable and fast simulation methodology using surface-potential-based semiconductor device model.

The background of this study is described in the first chapter, Especially, automotive applications are mentioned.

In the second chapter, basic principle of the electro-thermal coupling simulation technique is explained.

A novel resistance and capacitance (RC) compact thermal model (CTM) which has the capability of representing thermal behavior of multi chip inverter module are described in the third chapter. The proposed RC compact thermal model of inverter modules can take into account lateral thermal spreading and thermal interference. The thermal model is particularly suitable for representing thermal behavior of HV inverter.

In the fourth chapter, fast calculation technique, which is called “Table look-up method” is demonstrated. Various information and conditions such as motor current,

motor rotation speed, switching frequency and variable direct current (DC)-link voltage are applied to the simulation for carrying out a dynamic operation of power semiconductor devices mounted on a power module. This technique is the first electro-thermal coupling simulation in the world which has capability of predicting the power loss and the junction temperature of the device in the dynamic operation such as WOT acceleration of a HV.

An application for electro-thermal coupling simulation using Hiroshima University STARC IGFET model for high voltage (HiSIM_HV) model is described in the fifth chapter. Since HiSIM_HV is extension of HiSIM which is a surface-potential-based compact model, it is expected that HiSIM_HV realizes stable and high speed circuit simulations. Evaluation of the HiSIM_HV model is performed on three aspects in this paper. Firstly we have evaluated stability of the electro-thermal coupling simulation on SPICE3 with long simulation time. Next, comparison of calculation speed between HiSIM_HV and MOS Level 3 on SPICE3 has been done. Finally, we have compared calculation speed between HiSIM_HV on SPICE3 and Power MOSFET model on another simulator. The result verifies that methodology provides stable and fast simulation for real automotive applications with power devices where thermal interference occurs.

Chapter 2

Principle of Electro-thermal Coupling Simulation with a Circuit Simulator

Figure 2-1 shows transient temperature rise of surface of power semiconductor device for step power response[1]. A fixed value can be set for the device temperature in the calculation of about 10 ms because the temperature change is not large in this time range. On the contrary steady thermal analysis should be done by 3D FEM after power loss simulation using circuit simulator in the calculation of over 10 sec because the temperature is saturated in this time range. Electro-thermal coupling simulation is especially required for a few seconds simulation because the temperature change of device is particularly large, therefore temperature-dependent semiconductor device characteristics is required to calculate power loss within the device.

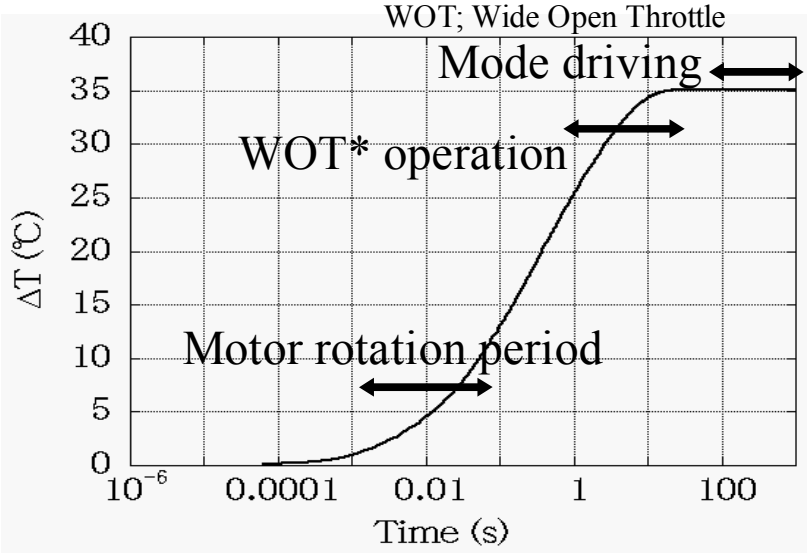


Figure 2-1. Example of Transient temperature rise of surface of power device for step power response.

2.1 Electro-thermal Coupling Simulation

In order to evaluate the accurate temperature increase of power Si semiconductor chips consisting of devices such as metal oxide semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBT) or diodes, which are embedded into automotive applications, electro-thermal coupling simulation[1-5] is provided in circuit simulators. The electro-thermal coupling simulator includes an electrical circuit model, which represents the electrical behavior of automotive applications, as well as a resistance and capacitance (RC) compact thermal model, which describes the thermal behavior of the automotive applications. These components are included in the circuit simulator, so that thermal coupling simulation can be realized. Figure 2-2 shows a schematic diagram of the electro-thermal coupling simulation technique using the following procedure:

1. Instantaneous device power loss is generated by applied current and voltage into the power device.
2. The device power loss is applied to the thermal model and an instantaneous device temperature is generated.
3. The temperature dependent device model parameters are determined using the device temperature.

These calculations are performed simultaneously using a circuit simulator. Heat flow is expressed using electrical circuit topology in the electro-thermal coupling simulation, because there is a relationship between the thermal quantities and electrical quantities. The thermal resistance, thermal capacitance, heat flux and temperature correspond to electrical resistance, electrical capacitance, electrical current and voltage, respectively. The accuracy of the device models and the thermal models are essential components for accurate electro-thermal simulations.

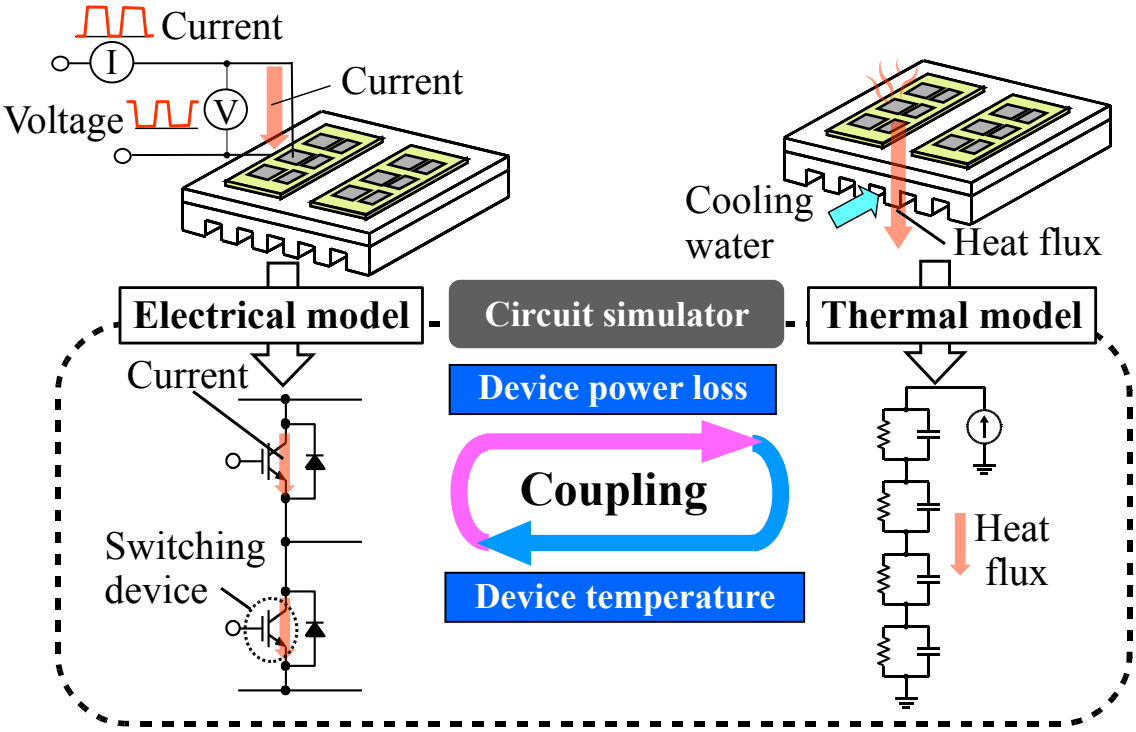


Figure 2-2. Schematic diagram of the electro-thermal coupling simulation.

2.2 Conventional Techniques and Problems

Thermal simulations by Finite Element Methods (FEMs) are widely used for predicting temperature distribution. However, FEMs are not suitable for the electro-thermal coupling simulation because of their long calculation time. Dynamic electro-thermal effects have been included in some of compact device models in several circuit simulators. However, physics based mathematical models have difficulties in converging due to their complexity of equations.[6] Additionally, conventional approaches using simple thermal models based on circuit simulators have encountered significant difficulties in accurately predicting the transient behavior of complex applications such as automotive power modules[7].

Chapter 3

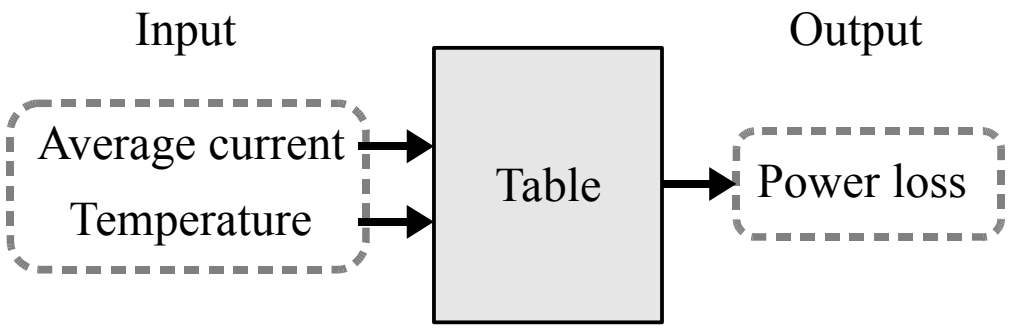
Components of Electro-thermal Coupling Simulation

In this chapter, details of semiconductor device models and thermal models, which are main components of the electro-thermal simulation, are described.

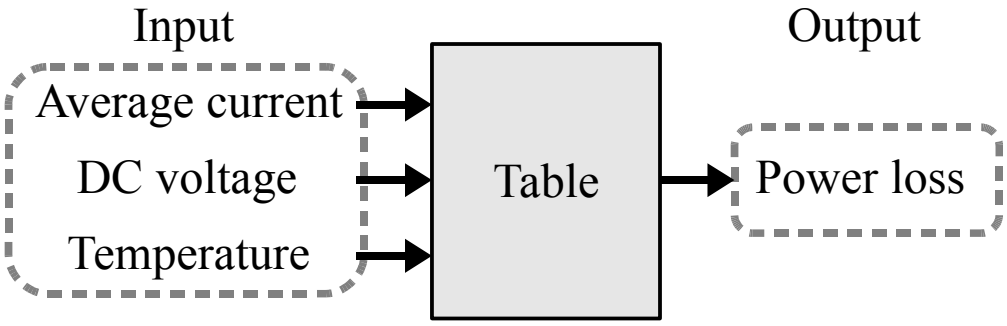
3.1 Semiconductor Device Models

The role of the electrical circuit in the electro-thermal coupling simulation is calculating the power loss in the semiconductor device models and passing it to the thermal circuit. The power loss is expressed as the product of the device voltage and current. Electrical characteristics of the device strongly depends on the junction temperature of the device[8]. therefore the power loss of the device also depends on the temperature. There are two major methods to implement the temperature dependency of electrical characteristics of the device in electro-thermal coupling simulation, they are the table look-up method[1, 9] and the method which uses device models with self-heating effect.

In the table look-up method, the device power loss is obtained by referring to "loss tables". For example, a steady state device power loss is defined in a look-up table as a function of current and junction temperature as shown in Fig. 3-1(a), and a switching power loss is defined as a function of current, voltage and junction temperature as shown in Fig. 3-1(b). The power loss values in the look-up tables are obtained from measured or simulated switching waveforms.



(a) Example of look-up table for a steady state power loss



(b) Example of look-up table for a switching power loss

Figure 3-1. Power loss look-up tables for a power device

The self-heating effect has been implemented into existing compact power device models, as shown Fig. 3-2[10,25]. Both internal and external thermal networks composed of thermal resistance and/or thermal capacitance are provided in those models. The device temperature is obtained at the temperature node *T*. The internal thermal circuit topology of a power device is fixed in many cases. An external thermal circuit is available if the internal thermal circuit has insufficient accuracy to perform thermal functions of the power device including its cooling system.

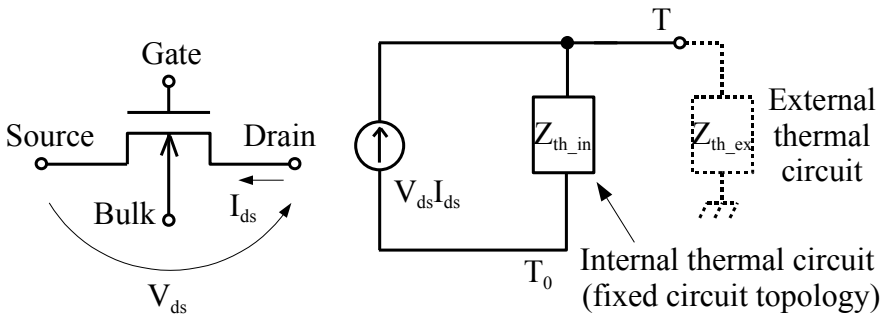


Figure 3-2. Power device model that includes self-heating effect.

3.2 Thermal Models

Thermal conduction inside a solid structure is described by the heat conduction equation as follows;

$$c_p(T)\cdot\rho\frac{\partial T}{\partial t}=\nabla\{\lambda(T)\cdot\nabla T\}+w(\vec{x},t) \tag{3.1}$$

where c_p, ρ, λ, w and T represent specific heat, material density, temperature dependent thermal conductivity, thermal power density and temperature, respectively.[22,26] Solving the equ (3.1) for the 3D structure of a power module employing FEM is of very high computational effort.

The RC compact thermal model is a lumped parameter network represented with R equivalent to thermal resistance, C equivalent to thermal capacitance and current source equivalent to the heating source. The RC compact thermal model is strongly required for carrying out the electro-thermal coupling simulation, because the model can be implemented using a circuit simulator easily. The difficulties of the RC compact thermal model for a poor cooling system (e.g. HV inverter system) are described in this subsection.

3.2.1 Difficulties of thermal analysis

The Photograph of an example for a commercialized HV inverter module (Multi chip module) is shown in Fig. 3-3 where many Si chips are packaged. Figure 3-4 shows the cross section of the inverter module. A heat flux generated by heating of each Si chip transfers from Si chip down to a convection cooler mainly. Also, it spreads in the lateral direction in the inverter module. Interference of each heating from each Si chip occurs among many Si chips which contributed to the temperature rise of individual Si chip each other. Therefore in order to build the accurate RC compact thermal model which represents the thermal behavior of the inverter module, it is important to represent the transient heat propagation behavior from Si chip down to the convection cooler and thermal interference behaviors among many Si chips due to the heat spreading in the module accurately.

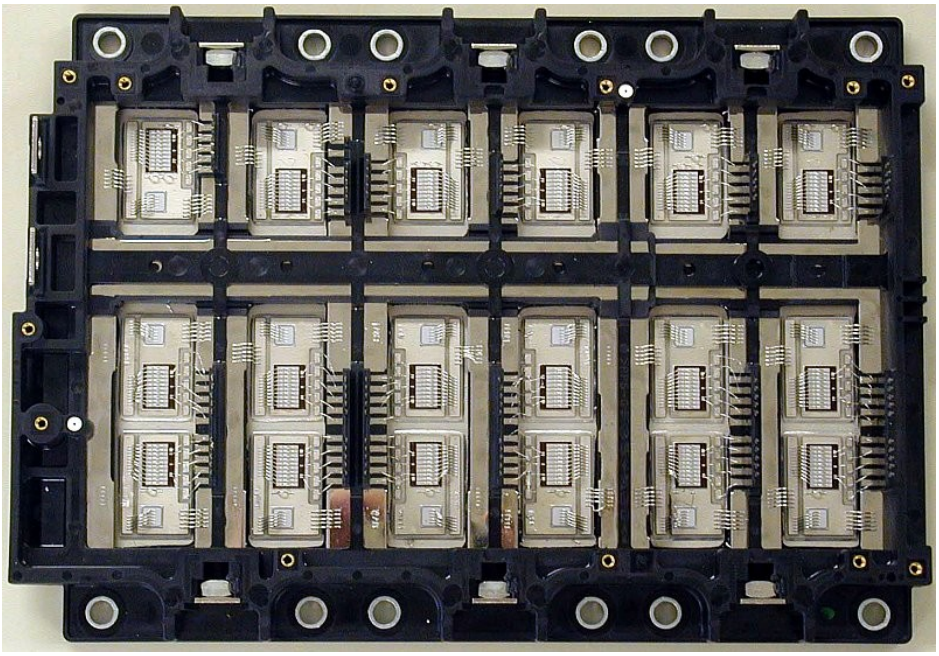


Figure 3-3. Photograph of commercialized HV inverter module.

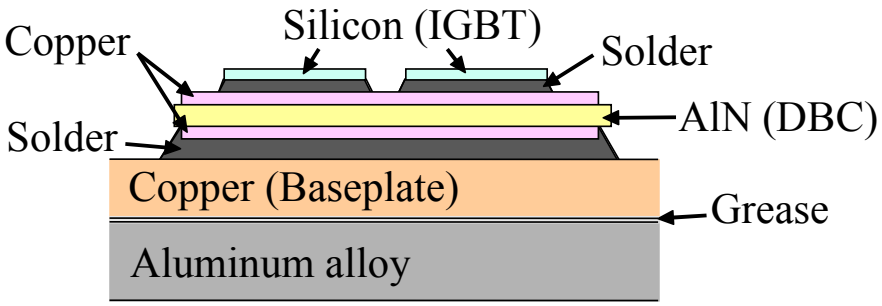


Figure 3-4. Cross section of the inverter module.

3.2.2 Lateral heat spreading model

The circuit employed as the RC compact thermal model is one called Foster network as shown in Fig. 3-5. It has the configuration consisted of the parallel resistance and capacitance sub-circuits connected in series. Although the Foster network thermal model is the behavior model having no physical meaning for R and C, It has the advantages of easiness of RC parameter extraction and high accuracy compared to the conventional thermal model of Cauer network circuit, shown in Fig. 3-6, having physical meaning for R and C. Because, one-dimensional Cauer network circuit can't represent lateral thermal spreading behavior of inverter module which has three-dimensional structure[7].

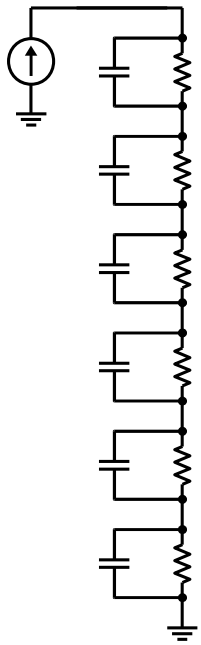


Figure 3-5. Foster network.

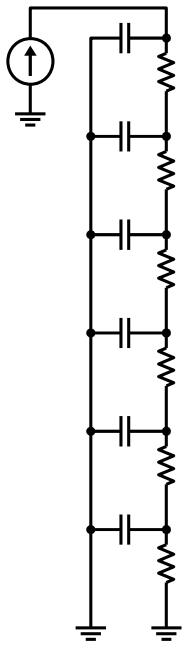


Figure 3-6. Cauer network.

A new compact thermal model based on Foster network is proposed to overcome these problems. Figure 3-7 shows the "cell" for each physical domain, which consists of the thermal resistance and capacitance. In the cell, two paralleled thermal resistance and capacitance are connected in series. The thermal impedance ($Zth(t)$) of the cell can be expressed by the following equation,

$$Z_{th}(t) = R_1\left(1 - e^{-\frac{t}{R_1 C_1}}\right) + R_2\left(1 - e^{-\frac{t}{R_2 C_2}}\right) \tag{3.2}$$

The parameters (R_1, R_2, C_1, C_2) related to every node within the network are computed basing on a single transient thermal FEM simulation (step response, Fig. 3-8) of the whole system, i.e. module and heat sink (Fig. 3-4).

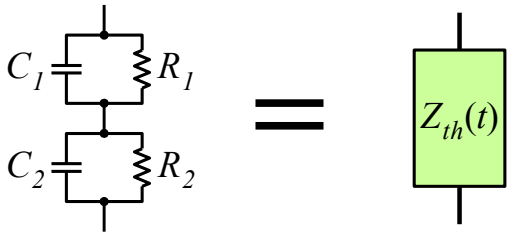


Figure 3-7. Unit cell of proposed compact thermal model.

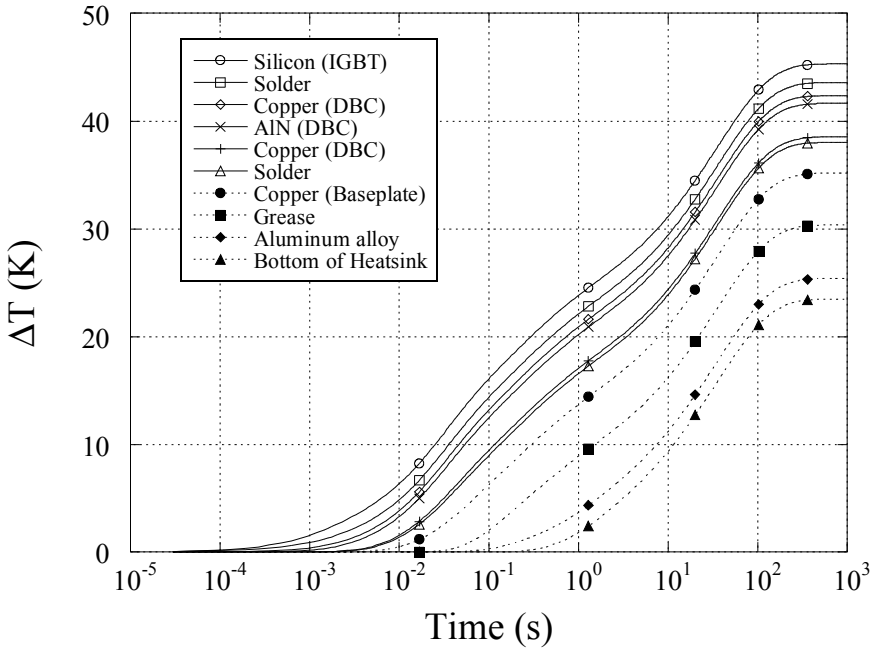


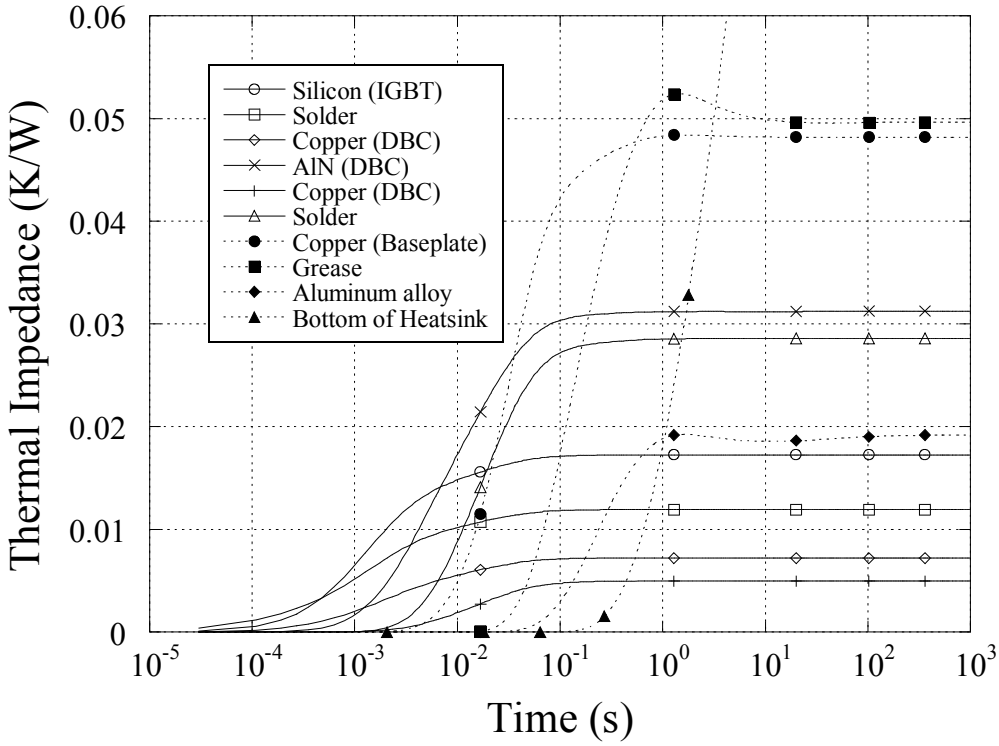
Figure 3-8. Step response of temperature at each layer of the power module (by FEM).

Thermal impedance for each layer can be calculated by following equation (Fig. 3-9(a)).

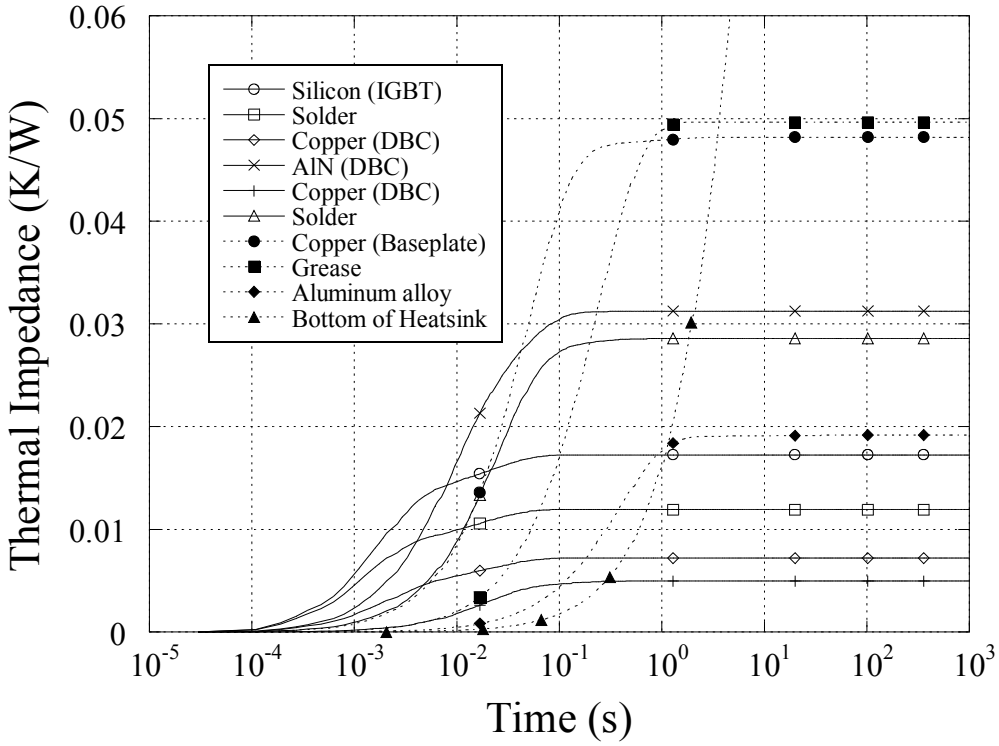
$$Z_{th\_i}(t)=\frac{T_{in}-T_{in-1}}{P_i} \tag{3.3}$$

Where T_{in} represents the temperature at nth layer and P_i represents applied power where the parameters R_1, R_2, C_1 and C_2 are determined to minimize errors in comparison with results calculated by FEM.

Figure 3-9(b) shows the time dependence of thermal impedances calculated using the optimum compact thermal model and the transient heat FEM (the transient response to the heat unit step) using equ. (3.3). The thermal impedance from the compact thermal model agrees with that from FEM.



(a) Calculated by FEM



(b) Calculated using the proposed model

Figure 3-9. Thermal impedance for each layer.

3.2.3 Thermal interference model

The temperature distribution for the inverter module (Fig. 3-3) is shown in Fig. 3-10, when all Si chips have steady state heating. All Si chips are found to have the thermal interference from Fig. 3-10. The thermal impedance matrix which is expressed as the equ (3.4) is used to represent the thermal interferences among many Si chips inside the inverter module.

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_j \\ \vdots \\ T_n \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1j} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2j} & \cdots & Z_{2n} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ Z_{i1} & Z_{i2} & \cdots & Z_{ij} & \cdots & Z_{in} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ Z_{n1} & Z_{n2} & \cdots & Z_{nj} & \cdots & Z_{nn} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_i \\ \vdots \\ P_n \end{bmatrix} \tag{3.4}$$

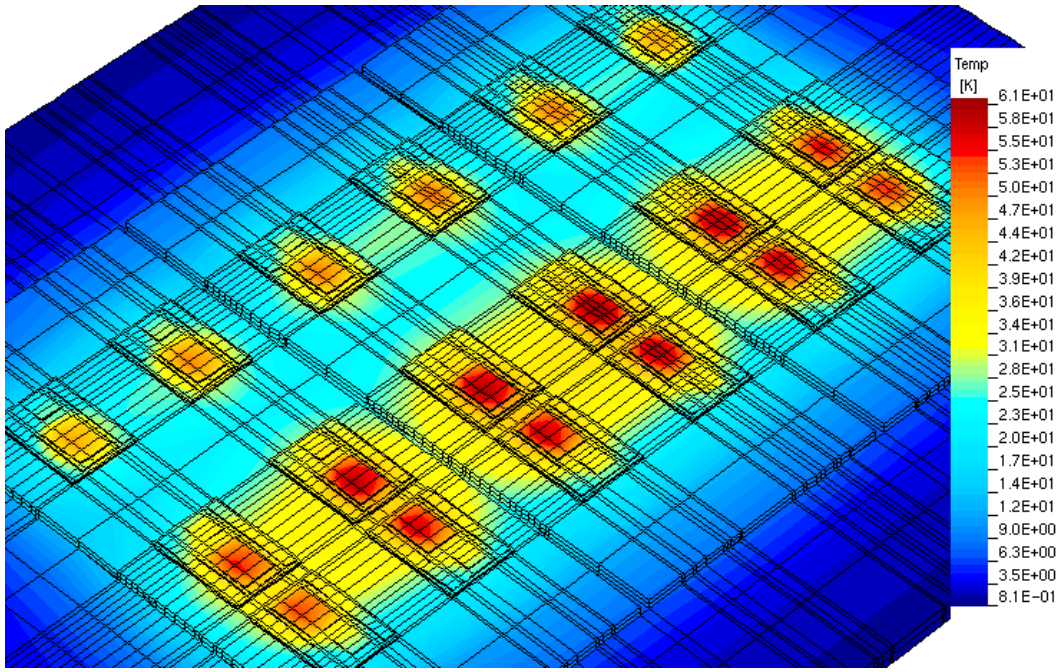


Figure 3-10. Static thermal analysis result of a power module under thermal interfering condition by 3D FEM.

In the equ (3.4), P_i is the loss generated by the ith Si chip and T_j is the temperature rise of the jth Si chip. T_j is related to P_i by the thermal impedance matrix element Z_{ij} which means the thermal interference between the ith Si chip and the jth Si chip. The diagonal element in the thermal impedance matrix, for example Z_{ii}, means self heating of the ith Si.

When the "device one" shown in Fig. 3-11 generates heat, heat flux flows from "device one" to bottom of this power module. Because this "cooling block" layer cool down the inverter by the water flow. The temperature of the "device one" is risen by the heat flux. The relation between the temperature (T_1) and the heat flux (P_1) is expressed by following equation;

$$T_1 = Z_1 P_1 \tag{3.5}$$

where Z_1 represents the self thermal impedance for "device one." Because cooling performance of the power module for automotive applications not very high, the heat flux spreads under the adjacent devices. Then temperatures of device 2, 3 and 4 are risen. This effect is the thermal interference. The thermal impedance matrix among these four devices can be expressed by following equation;

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} \tag{3.6}$$

The thermal impedance of each physical domain can be expressed by the same equation as equ (3.2). In the case that thermal interference occurs, to define the values of parameter R_1, R_2, C_1 and C_2 for Z_{ij}, firstly, step heat generation is applied to a Si chip and surface temperature rises of all Si chips and temperature observation points insides of the module are observed. The temperature observation points are normally placed at the boundaries of physical domains as shown in Fig. 3-12. Secondly, the values of

parameters R and C are determined by least square method to fit equ (3.2) to FEM result. This procedure is carried out for each Si chip which is under the thermal interference. As a result, thermal impedances based on the Foster network are defined to all temperature rises. These thermal impedances are the thermal impedance matrix elements. For example, Z_{ij} means that it is determined from the *j*th Si chip temperature rise when step heat generation is applied to *i*th Si chip.

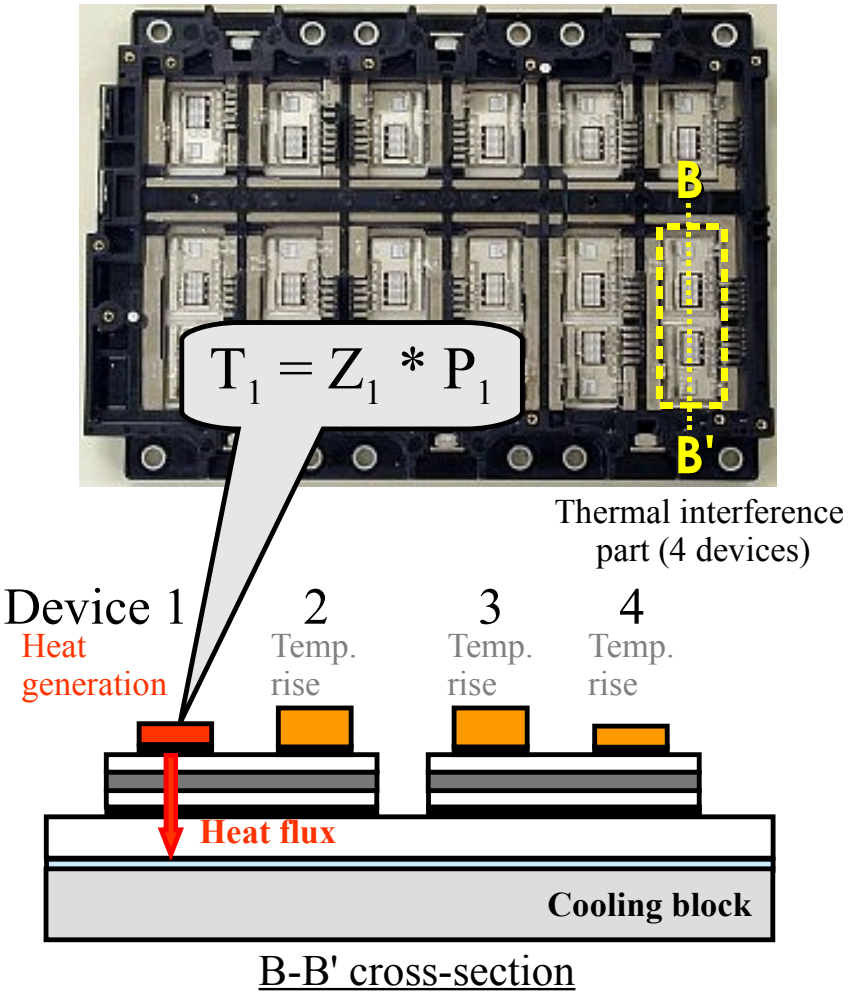


Figure 3-11. Thermal interference.

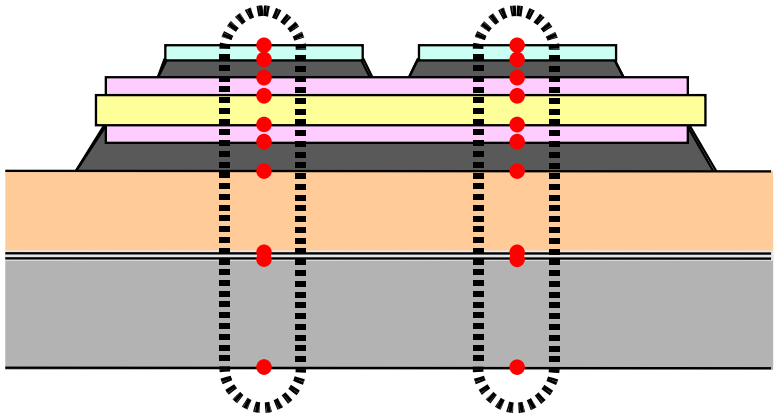


Figure 3-12. Temperature observation points for determination of the RC compact thermal model parameters.

Figure 3-13 shows the example to determine the thermal impedances for calculating the temperature rise of "device-one." These thermal impedances are determined from the calculation result by 3D transient thermal FEM. To define the Z_{11}, step heat generation is applied to the device-one, and surface temperature of the device-one is observed. The value of RC are determined by least square method to minimize errors in comparison with FEM result. To define the Z_{12}, step heart generation is applied to the device-two in this case, and also surface temperature of the device-one is observed. Z_{13} and Z_{14} are determined by the same manner as Z_{12}. The temperature of the device-one (T_1) is expressed by equ (3.7);

$$T_1 = Z_{11} P_1 + Z_{12} P_2 + Z_{13} P_3 + Z_{14} P_4 \qquad (3.7)$$

Thermal interference is included in the last three terms.

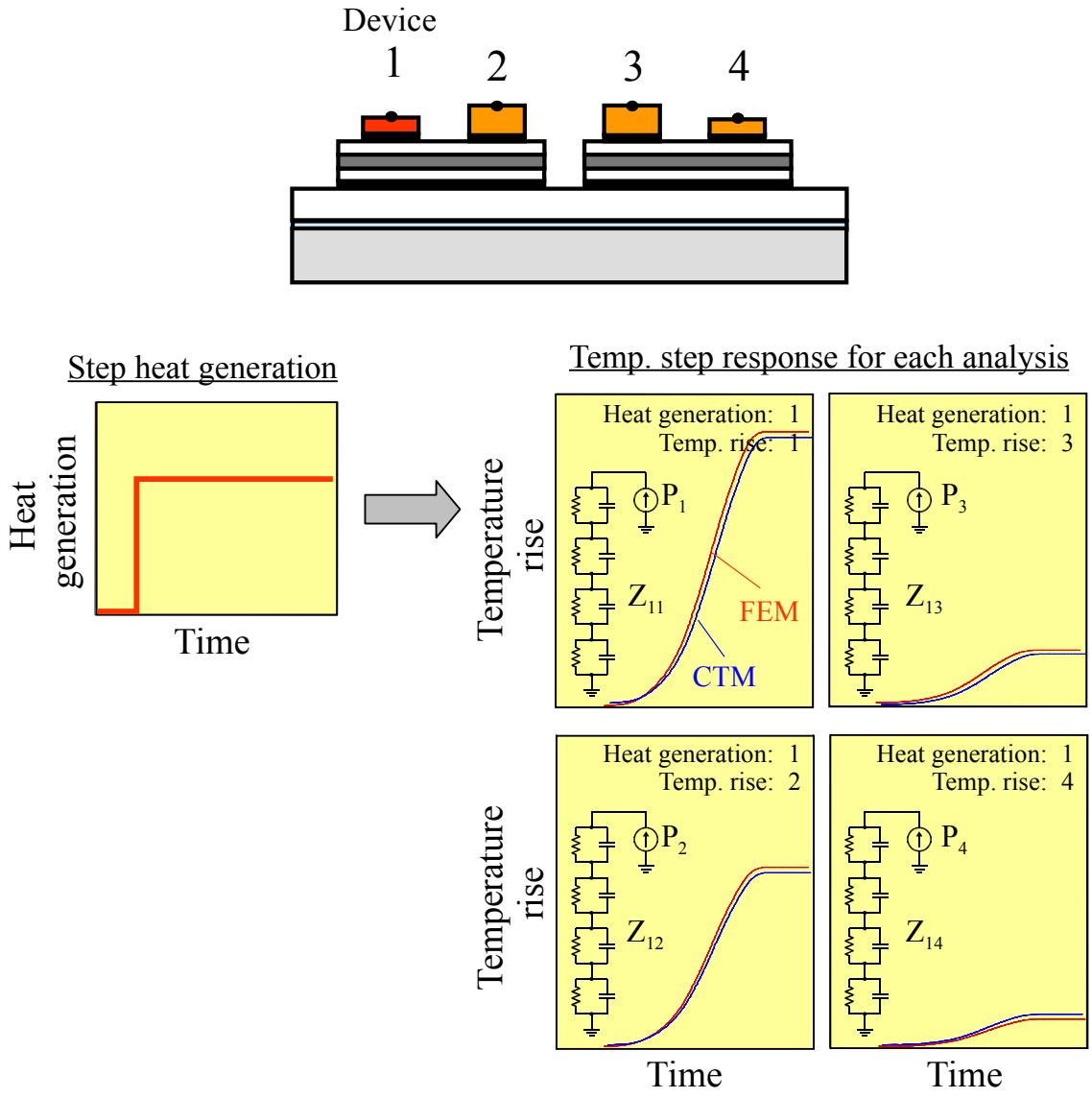


Figure 3-13. Example to determine the thermal impedances
for calculating the temperature rise of "device-one."

3.2.4 Accuracy verification of the thermal models

The accuracy of the proposed RC thermal model is demonstrated for two examples of actual inverter module structures. And example of electro-thermal coupling simulation using proposed RC compact thermal model is also demonstrated.

A. Unit step responses without thermal interference

Figure 3-14 shows the temperature transient responses to the heat unit step during a cooling period calculated using the proposed compact thermal model in the case that thermal interference did not occur (operation of one IGBT). The lateral thermal spreading is accurately modeled, because the result calculated using the proposed model is in agreement with those calculated by the FEM and measured.

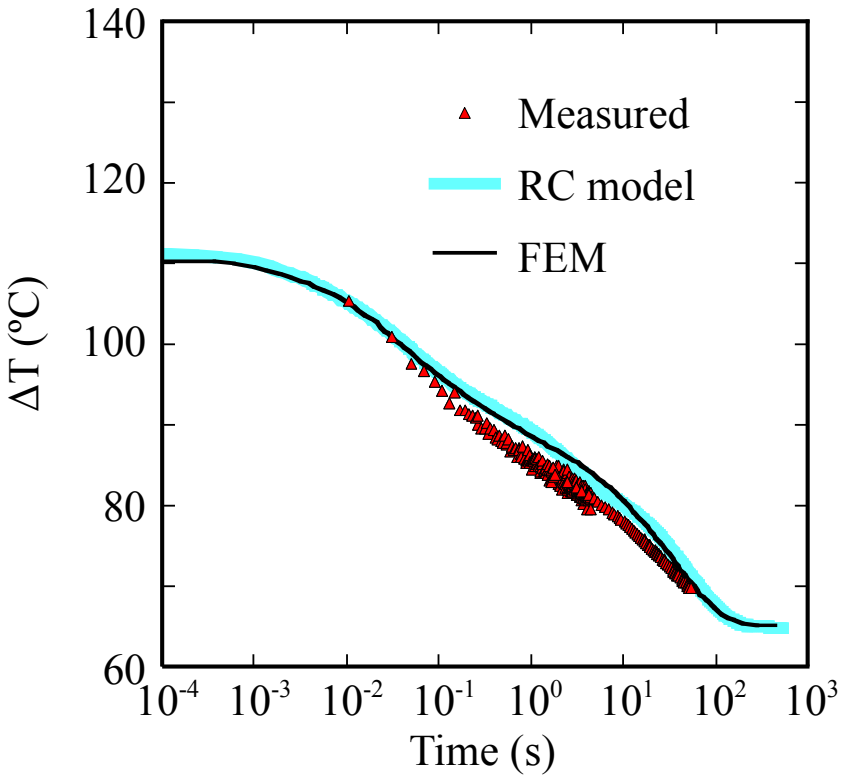


Figure 3-14. Calculated (lines) and measured (symbols) pulse response without thermal interference. Power loss at the steady-state (before turn-off) is 93.7 W.

Figure 3-15 shows the comparison of temperature transient responses to the heat unit step during heating period between the Cauer and the Foster network circuits. From this figure, the result calculated using the Foster network circuit is in agreement with that calculated by the 3D-FEM. The Cauer model shown in Fig. 3-6 cannot exactly represent a three-dimensional structure having temperature transient[7]. Therefore certain disagreement occurs on a transient response shown in Fig. 3-15. Specifically, the Cauer model cannot represent lateral thermal spreading on the real IGBT module mounted on the water cooler because the model is only applicable for a single exponential phenomenon.

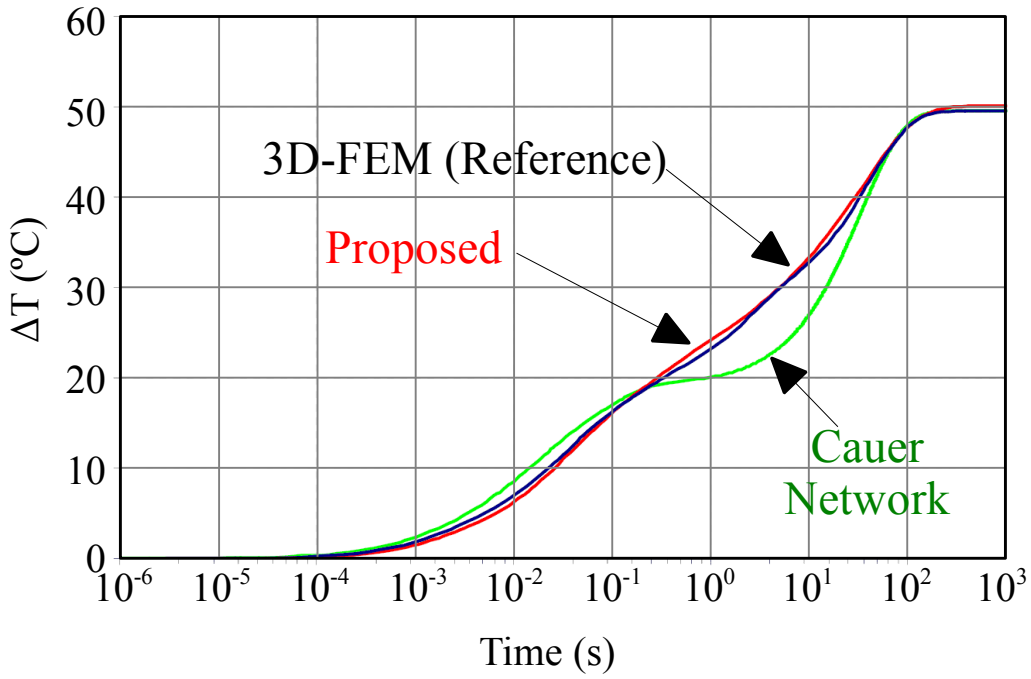


Figure 3-15. Comparison of calculated results among proposed model, one-dimensional Cauer model and 3D-FEM for step response. Power loss of the device is 100 W.

B. Unit step responses with thermal interference

In this case, strong thermal interference occurs among neighboring 4 devices shown in Fig. 3-10. The temperature transient responses to the heat unit step calculated using the proposed compact thermal model is shown in Fig. 3-16. The result calculated using the proposed model is in agreement with that calculated by the FEM for every device, showing that the thermal interference is accurately modeled.

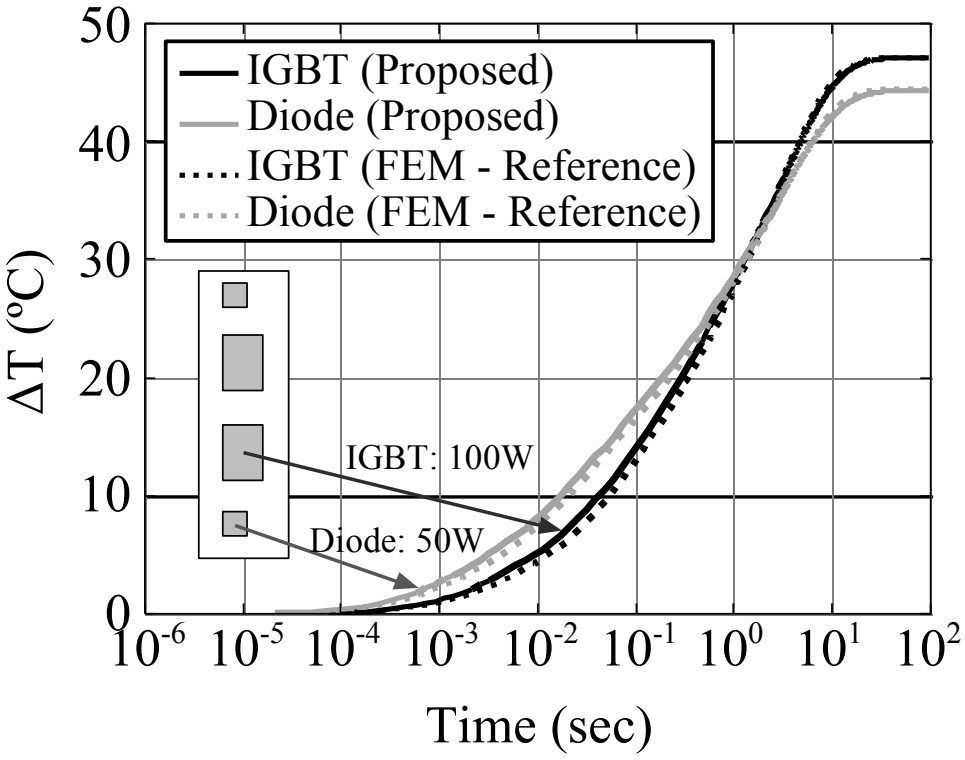


Figure 3-16. Comparison of calculated results between proposed model and 3D-FEM for step power response with thermal interference.

C. Periodical square wave responses

Three IGBT chips and three diode chips are packaged on the same substrate in the inverter module as shown Fig. 3-17, where the heating pattern with the periodical square wave is applied to the three IGBT chips and the inverted heating pattern to the three diode chips simultaneously as shown in Fig. 3-18. To evaluate the suitability of the proposed model for thermal calculation of inverter module, it assumes that the frequencies of the heating pattern correspond to motor speed. Figure 3-19 shows the temperature waveform for IGBT chips calculated by FEM thermal analysis and that by the RC compact thermal model corresponding to this inverter module. Because the temperature waveform for IGBT chips calculated by the RC compact thermal model agrees with that by FEM, it is found that the proposed RC compact thermal model is suited to represent the inverter module.

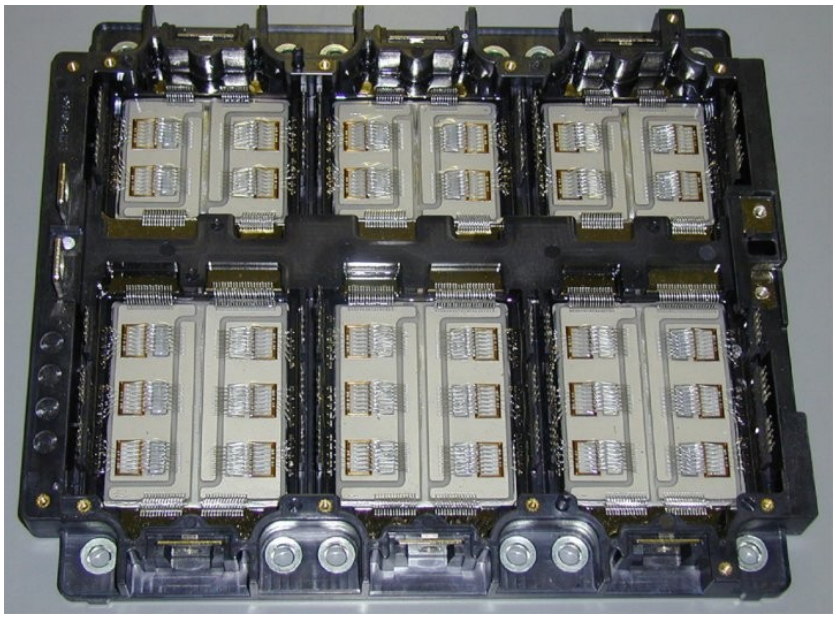


Figure 3-17. Photograph of a test module for the evaluation of the proposed thermal model for periodical square wave responses.

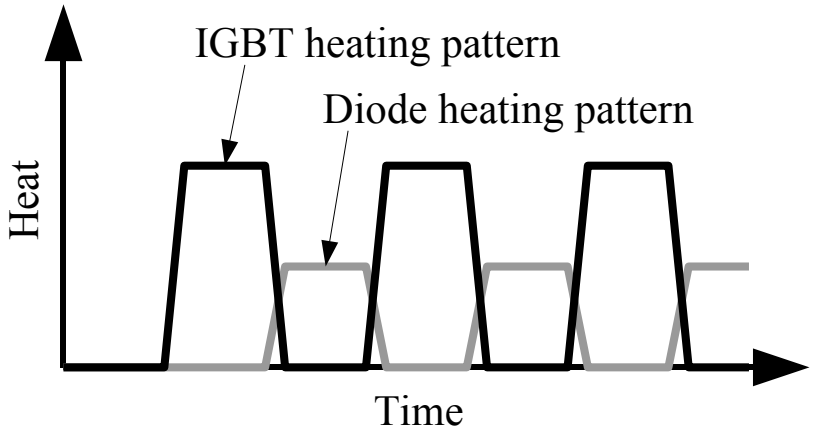
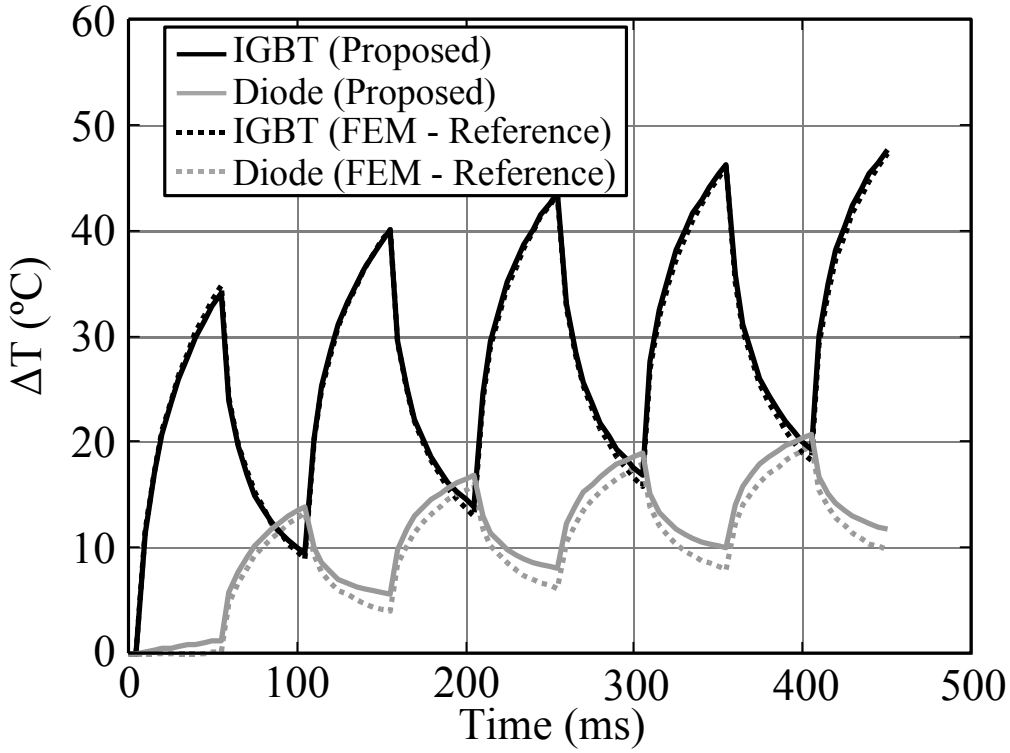
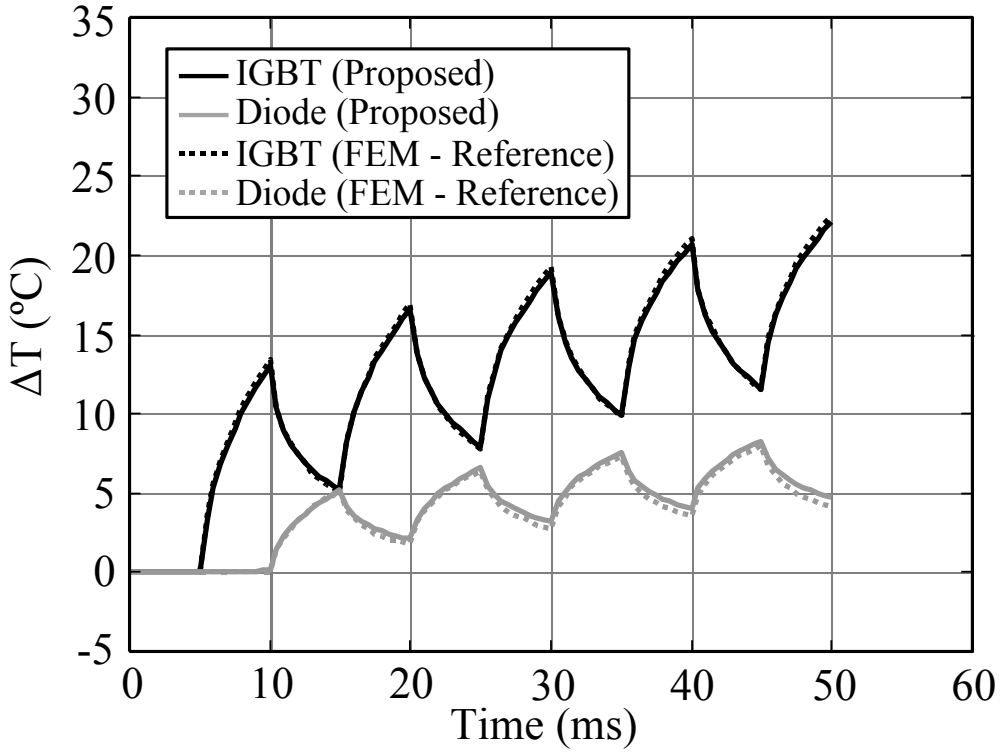


Figure 3-18. Heating patterns of IGBT chips and diode chips.

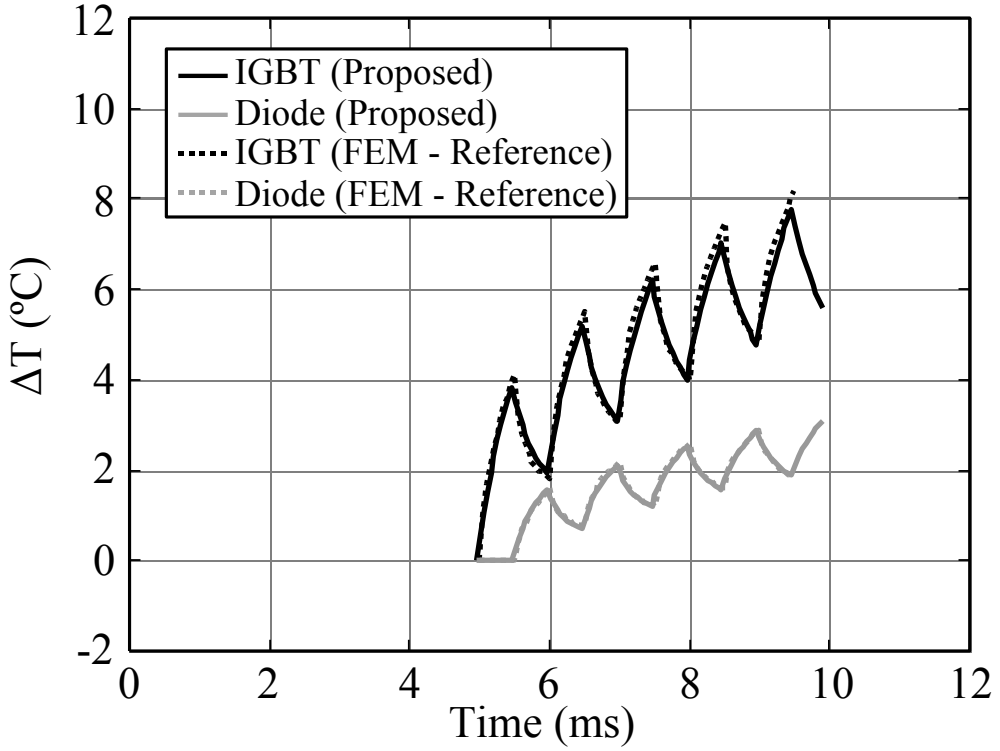


(a) Frequency of heating is 10 Hz.

Figure 3-19. Comparison of calculated results between proposed model and 3D-FEM for periodical power response with thermal interference.



(b) Frequency of heating is 100 Hz.



(c) Frequency of heating is 1 kHz.

Figure 3-19. (Continued from previous page)

Chapter 4

Detail of Table Look-up Method

A dynamic temperature prediction technique under real driving condition was achieved in combination with the RC thermal compact model and the table look-up method. This technique is mainly focused on the wide open throttle (WOT) operation of HV. The technique is going to be explained with specific examples in this chapter.

4.1 Preparation of Look-up Tables

A Circuit simulation using the power device model described in subsection 3.1 requires short time increments on the order of nanoseconds. However, conventional physics based mathematical or semi-mathematical (e.g. combines simple bipolar junction transistor (BJT) and modified MOSFET models with voltage dependent C_{gc} and C_{ce}) device models are not adequate for transient temperature simulation such as WOT operation, because unrealistic calculation time is required.[11] I developed a method to look-up prepared device power loss tables to reduce the calculation time. Parameters of the power loss look-up tables are device current, device temperature and DC-link voltage of inverter. Figure 4-1 shows a example of look-up table for switching power loss of HV inverter at 650 V. One of the best ways to make accurate look-up tables of power loss is executing simulations using accurate simulation models (driving circuit of power device, smoothing capacitor on the power supply, stray inductance of power module, and so on). The WOT operation simulation was able to be finished within realistic calculation time using developed look-up table method.

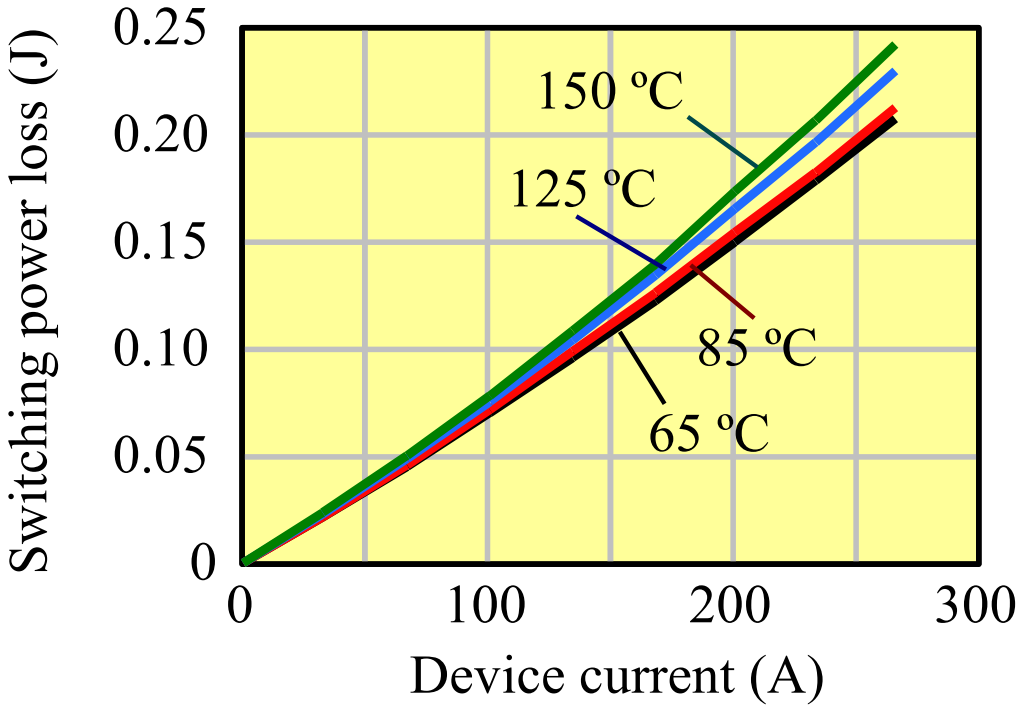


Figure 4-1. Example of look-up table for switching power loss
at 650 V of DC-link voltage.

4.2 Implementation Technique of Table Look-up Method into Circuit Simulator

The electro-thermal coupling simulation is carried out for prediction of the IGBT chip temperature in a “6 in 1 module” where three IGBT chips and three Diode chips are connected in parallel on each arm (shown in Fig. 3-17). Initially, motor frequency is zero in this simulation, and it is monotonically increased. The simulation is finished when the motor torque is changed to decrease. Following time-series data (see Fig. 4-2) are applied as simulation conditions;

- Motor torque
- Motor frequency (revolution)
- DC-link voltage of inverter
- Carrier frequency of inverter

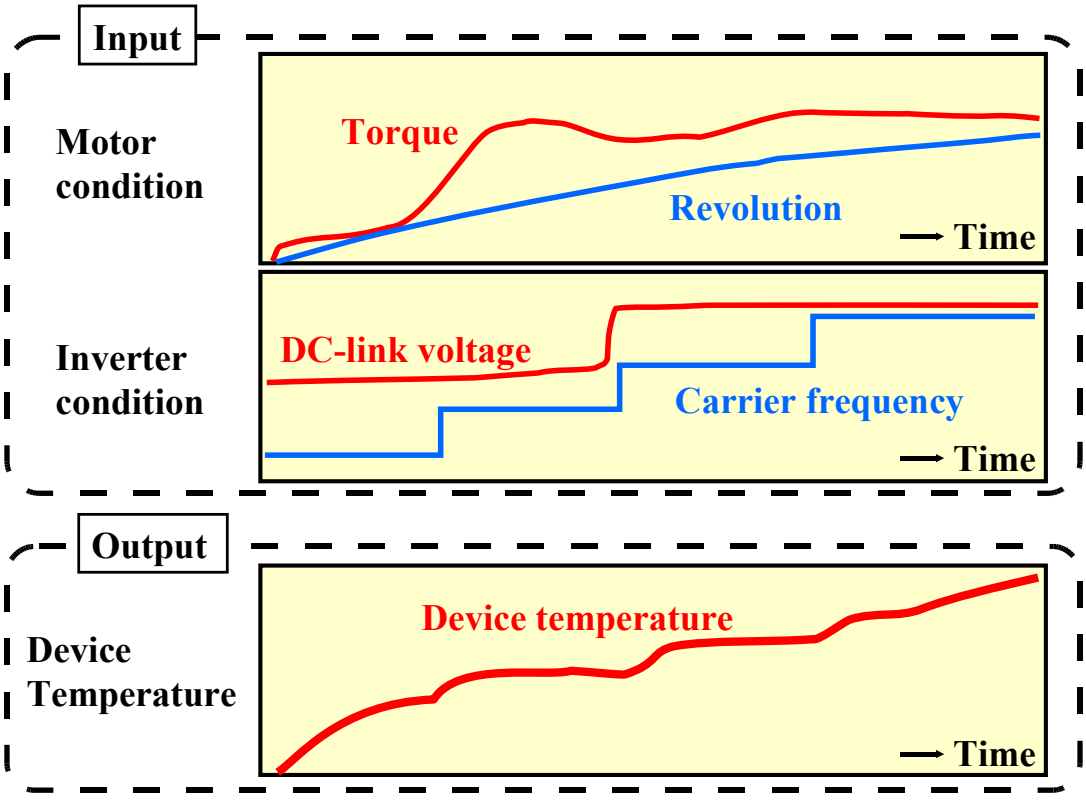


Figure 4-2. Input and output of electro-thermal coupling simulation for real driving simulation.

The block diagram of the electro-thermal coupling simulation is shown in Fig. 4-3. Power losses generated in power semiconductor devices are obtained from look-up tables. I implemented the block diagram in SIMPLORER.[10] The look-up table element available in SIMPLORER automatically provides linearly interpolated value corresponding to the current, DC-link voltage and junction temperature. It contributes to the accuracy improvement of the simulation.

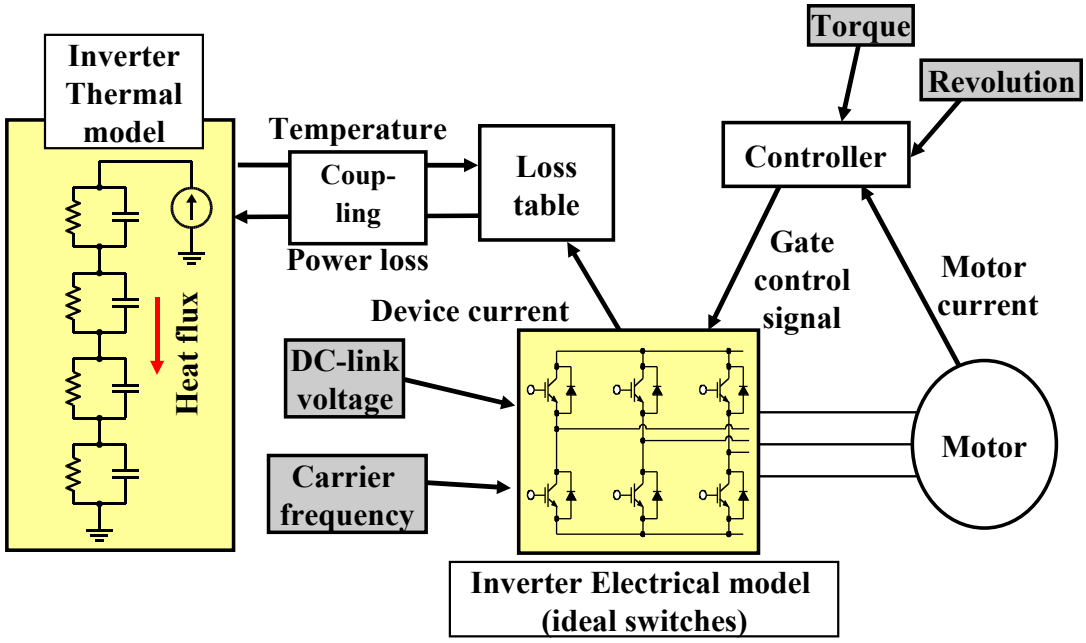


Figure 4-3. Block diagram of electro-thermal coupling simulation for a real driving condition.

4.3 Accuracy Verification of Table Look-up Method

The simulated and measured results are compared to determine the accuracy of the simulation technique in Fig. 4-4. The comparison between the simulated and measured results indicates that this method offers reasonable accuracy for the IGBT temperature estimation as shown in the figure where the worst case error in the IGBT temperature is less than 5 %. The fundamental advantage of this simulation technique is the CPU time efficiency compared to conventional electric-thermal coupling simulation. In the inverter simulation above, the time step is chosen to be 1 ms and it takes 210 minutes to complete the WOT simulation with duration of 4 seconds.

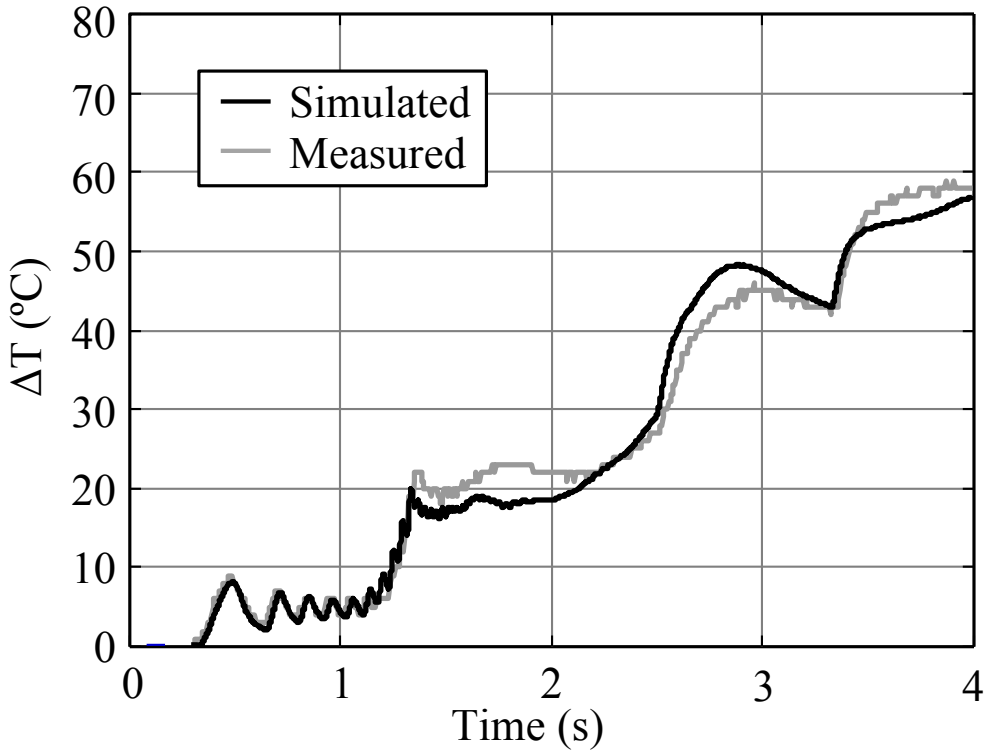
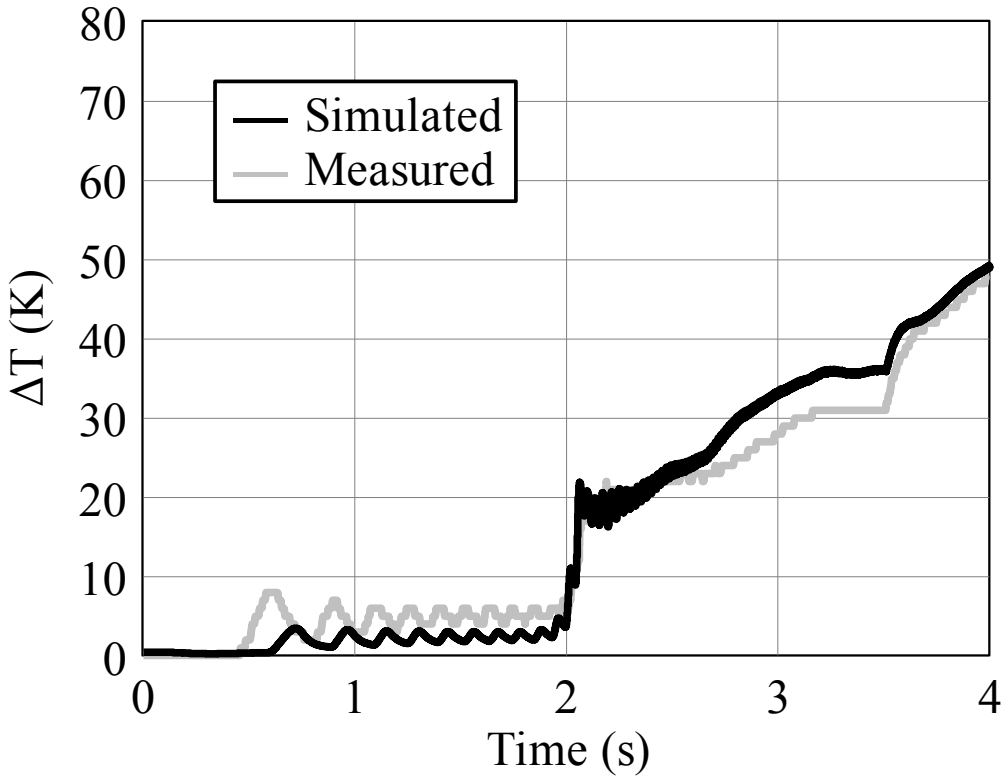


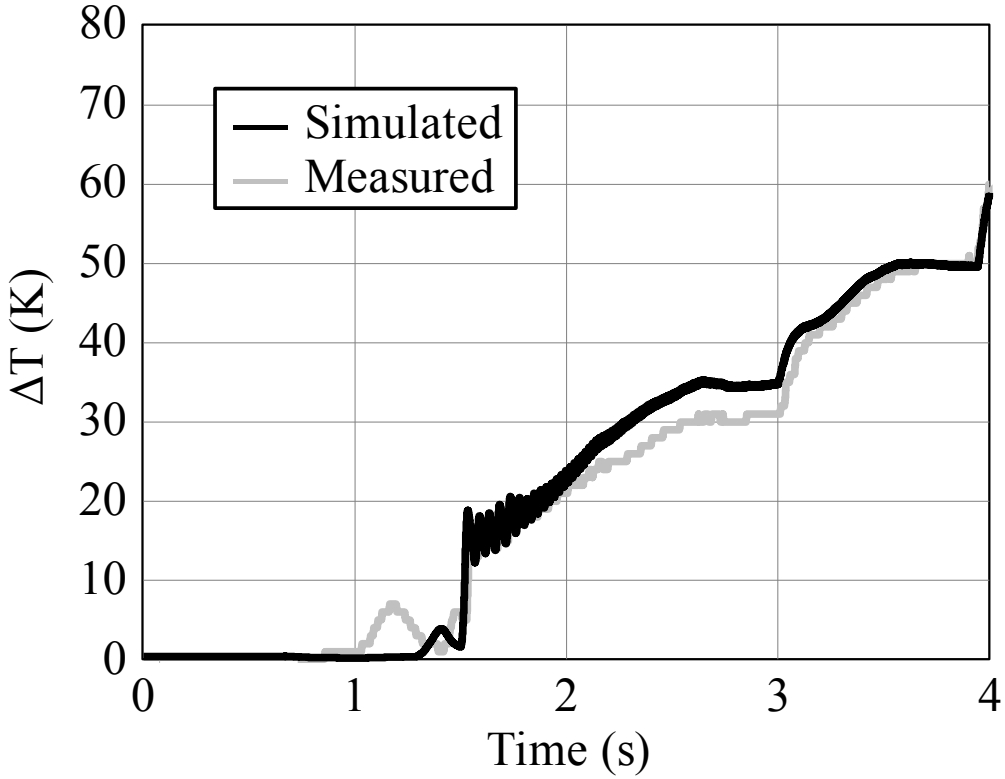
Figure 4-4. Simulated temperature rise profile of IGBT chip
for WOT operation of HV.

Verification of driving pattern modification for WOT operation of HV were performed. Figure 4-5 shows simulation results for the temperature waveforms on several driving pattern. The most notable differences among the driving pattern is slope angles of the tested road. The inverter temperature dependence of HV system control pattern on road condition can be calculated well with different control signal such as current, voltage and career frequency. The simulation errors are less than 5 %. This study of modifications verified that models are practical tools for optimum inverter design to evaluate inverter system performance for several driving conditions.

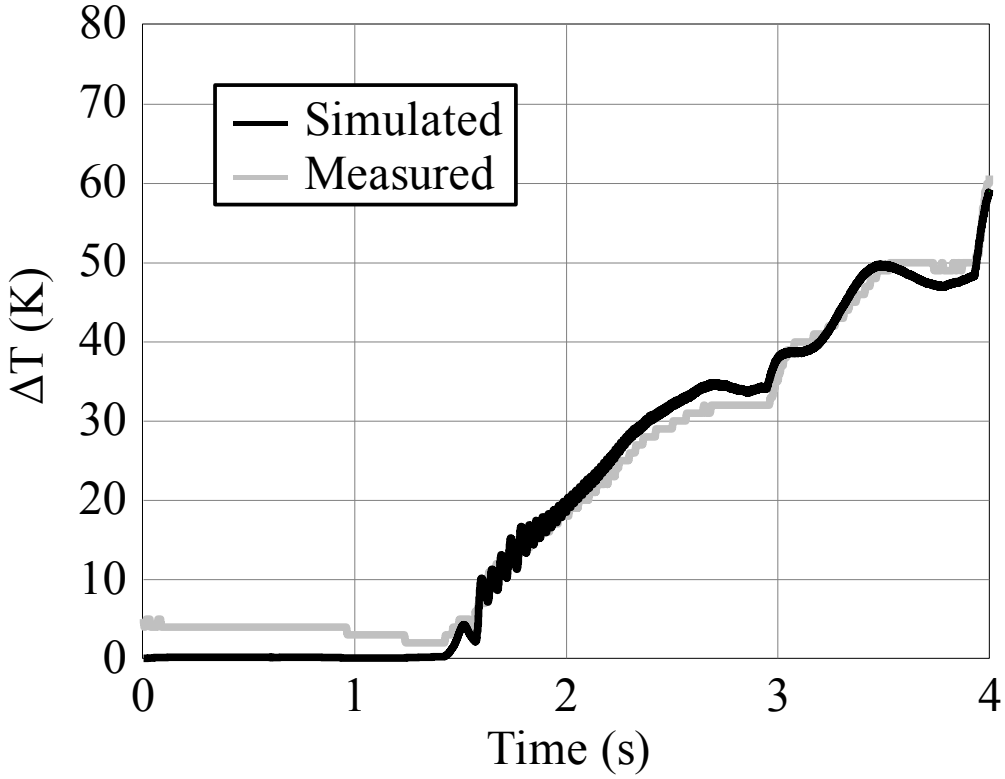


(a) Road condition A

Figure 4-5. Simulation results of IGBT Temperature at WOT on several road conditions



(b) Road condition B



(c) Road condition C

Figure 4-5. (Continued from previous page)

Chapter 5

Consistent Thermal Simulation in Semiconductor Modules with a Surface-Potential-Based Model

5.1 Advantage of Surface-Potential-Based Model

The existing power device models require enormous calculation times for electro-thermal coupling simulation[11]. The reason for the slow calculation with the existing models is that the equations for the DC characteristics are dynamically calculated according to the instantaneous voltage condition. However, due to the lack of model quality, discontinuities of device current easily occur in the existing threshold voltage based models. On the other hand, a surface-potential-based model requires only a single equation to describe the device characteristics for any bias conditions. HiSIM is the first simulation based on this method[12]. It is expected that this surface-potential-based model can realize stable and high speed circuit simulations. The key feature of the HiSIM_HV model, which is an extension of HiSIM, is the accurate and consistent modeling of the resistance effect in the resistive drift region[13]. In addition, the self-heating effect has been implemented into the HiSIM_HV model. The self-heating model of HiSIM_HV is also illustrated in Fig. 3-2. The internal thermal circuit of HiSIM_HV is simply implemented as a single stage parallel-connected resistance and capacitance. The external thermal circuit is also available in HiSIM_HV. The basic electrical characteristics of HiSIM_HV have been verified[13]; therefore, this study has focused on the applicability of HiSIM_HV to electro-thermal simulation.

5.2 Basic Characteristics of HiSIM_HV model

Basic information and characteristics of HiSIM_HV model are described in this section.

5.2.1 Characteristics of Laterally Diffused Metal Oxide Semiconductor (LDMOS) Device

Figure 5-1 shows the studied LDMOS structure. The channel is formed by the out diffusion of the impurity concentration from the source contact region. The resistive region, called the drift region, is typically formed with the substrate. The length and impurity concentration of the drift region, L_{drift} and N_{drift}, respectively, determine the features of the LDMOS structure. The impurity concentration in the drift region N_{drift} is varied while keeping the length L_{drift} and other device parameters constant. Figures 5-2(a) and 5-2(b) show the current–voltage (I–V) and g_m characteristics simulated with a two-dimensional device simulator for N_{drift} = 1 * 10^{17} and 1 * 10^{16}. The corresponding C_{gg} characteristics are shown in Fig. 5-2(c). Anomalous spikes are observed with a reduced N_{drift} of 1 * 10^{16}, and a clear correlation between g_m and C_{gg} is also observed.

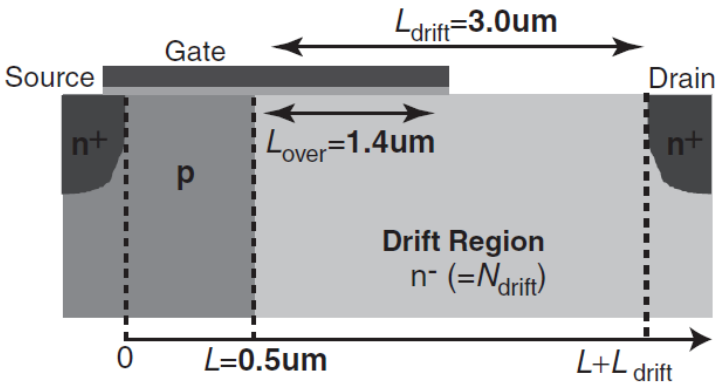


Figure 5-1. Cross section of LDMOS

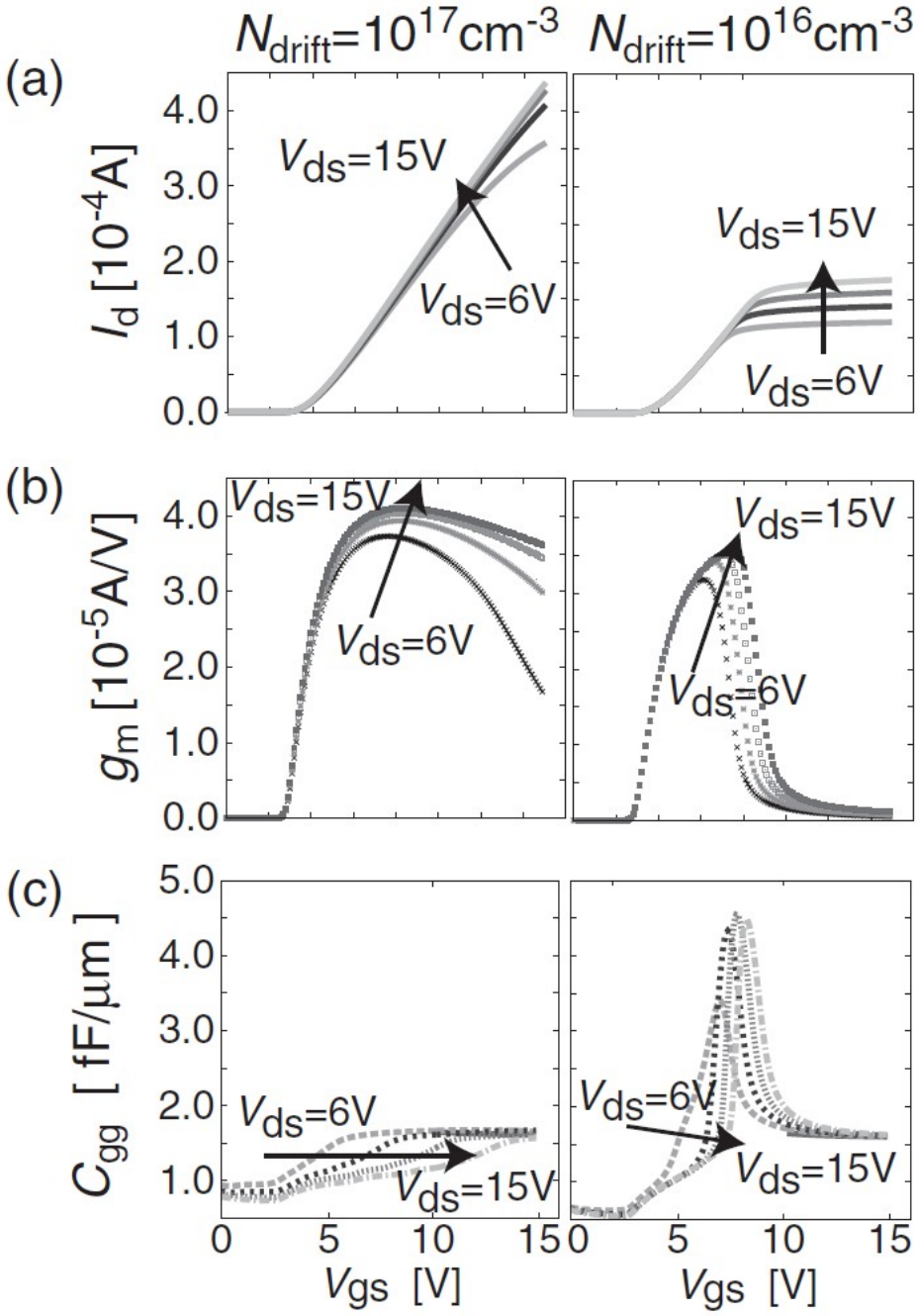


Figure 5-2. Simulated (a) drain current, (b) transconductance, and (c) gate capacitance for two impurity concentrations of drift region with 2D device simulator.

When g_m decreases abruptly with the increased V_{gs}, spikes in C_{gg} are formed, as observed in Figs. 5-2(b) and 5-2(c). For such a case current does not increase as a function of the gate voltage V_{gs}, as typically observed, for MOSFET, however, it enters the saturation condition.

The doped impurity concentration of the channel region, fabricated by the out diffusion of the impurity from the source, is not homogeneous, however, it decreases gradually from the source to the drain. It is believed that the C_{gg} spikes are caused by this impurity gradient of the channel doping concentration.[27] For the simulation results shown in Fig. 5-2, a homogeneous impurity concentration is applied to focus on the essence of the LDMOS features, namely, the effect of the drift region. Figure 5-3 shows a comparison of simulation results with and without the gradient. It is observed that the impurity gradient enhances the LDMOS features observed in g_m and Cgg. However, the features themselves are not changed, but the same effect can be achieved by reducing N_{drift}.

Since the abrupt reduction in gm and the anomalous spike observed in C_{gg} are observed only for the resistive drift region with N_{drift} = 1 * 10^{16}, it was concluded the features are caused by the resistance effect of the drift region. Thus, the key for a good compact model is the accurate modeling of the resistance effect of the drift region.

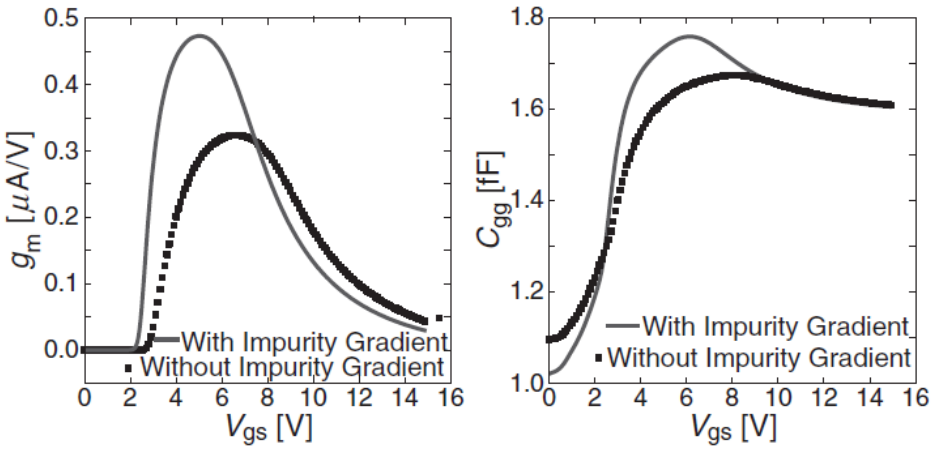


Figure 5-3. Comparison of simulated gm and C_{gg} with (solid line) and without (dotted line) impurity gradient of channel region.

5.2.2 Modeling Approach

A. Resistance effect

For modeling the resistance effect of the drift region consistently, the bulk MOSFET model HiSIM have been extended, which solves Poisson's equation for surface potentials iteratively.[29] Despite the iteration, it has been proved that HiSIM is at least as fast as conventional threshold voltage-based models, such as BSIM.[30] The potential distribution calculated with HiSIM is shown in Fig. 5-4. The potential increase within the drain drift region is exactly the essence of the LDMOS features; thus, the accurate calculation of the increase caused by the resistance effect is an important task for modeling LDMOS.

The original HiSIM provides different approaches that include the resistance effect consistently.[28] One approach is the introduction of additional nodes for resistances and the solution of potential drop using circuit simulators. Another approach is the iterative solution of potential drop with internal nodes within HiSIM. For LDMOS modeling, the second approach is extended. The reason for this is that the resistance effect cannot be solved as the external resistance, because the potential drop in the drift region affects not only the drain current, which is a function of external voltage, but also the overlap capacitance and the charge induced in the drift region simultaneously.

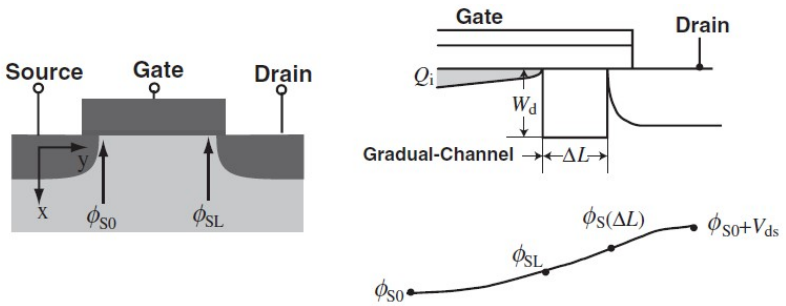


Figure 5-4. Calculated important surface potentials in HiSIM for bulk MOSFET.

The potential drop caused by the resistance effect is written as

$$\Delta V = I_{ds} R_{drift} \tag{5.1}$$

where I_{ds} is the drain current and R_{drift} is the resistance in the drift region, where I_{ds} must be known prior to the ΔV calculation. However, to calculate Ids, the potential drop ΔV must be known. Therefore, this is solved iteratively in HiSIM, as schematically shown in Fig. 5-5. The iteration procedure for the surface-potential calculation is included in the iteration for the potential-drop calculation. This approach ensures the consistent inclusion of the resistance effect of the drift region. It is expected, however, that this approach results in unstable calculations for circuit simulation. It has been proved, however, that calculation stability depends on surface-potential accuracy. If Poisson's equation is solved consistently with a high accuracy of 1 * 10^{-13} V, a very stable calculation is obtained even for such complex devices.

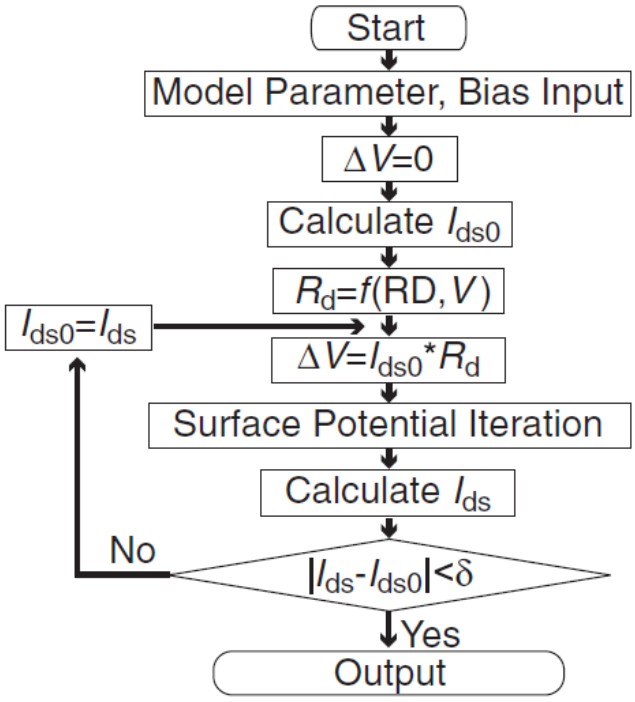


Figure 5-5. Calculation flow chart of HiSIM_HV.

B. Charges induced in drift region

In comparison with the bulk MOSFET, the overlap length in the drift region L_{over} is relatively large. When the gate voltage V_{gs} induces the inversion condition in the channel, the overlap region is typically under the accumulation condition; thus, the overlap charge gives a non-negligible contribution to the total capacitance. HiSIM_HV includes the overlap charge Q_{over} model as a function of the surface potential, calculated by solving Poisson's equation within the overlap region under the inversion, depletion, and accumulation conditions. Here, the potential distribution along the overlap length L_{over} is neglected to simplify the calculation procedure.

Another charge induced in the drift region is called the drift charge Q_{drift} due to current flow. To obtain a closed form for Q_{drift}, approximations are introduced. One is that the carrier density in the drift region is calculated with the drain current I_{ds} (= $qn\mu E$, q: electron charge; n: carrier concentration; μ: carrier mobility), at which the electric field E is replaced with that in the drift region modeled as

$$E = (V_{ds} + Vbi - \phi_{sdl}) / L_{drift} \tag{5.2}$$

where V_{ds} and V_{bi} are respectively the drain voltage and built-in potential between the channel and the drift region. ϕ_{sdl} is the potential at the channel/drift region junction calculated as

$$\phi_s(\Delta L) = CLM1(V_{ds} + \phi_{s0}) + (1 - CLM1)\phi_{sl} \tag{5.3}$$

where *CLM1* is the model parameter describing the junction condition. Figure 5-6 shows the simulated potential distributions along the LDMOS surface calculated with a two dimensional (2D) device simulator for the studied cases of N_{drift} = 1 * 10^{17} and 1 * 10^{16} with a negligible overlap length. The calculated surface potentials with HiSIM_HV are also depicted. All device features are written as a function of these potentials; thus, model consistency is preserved.

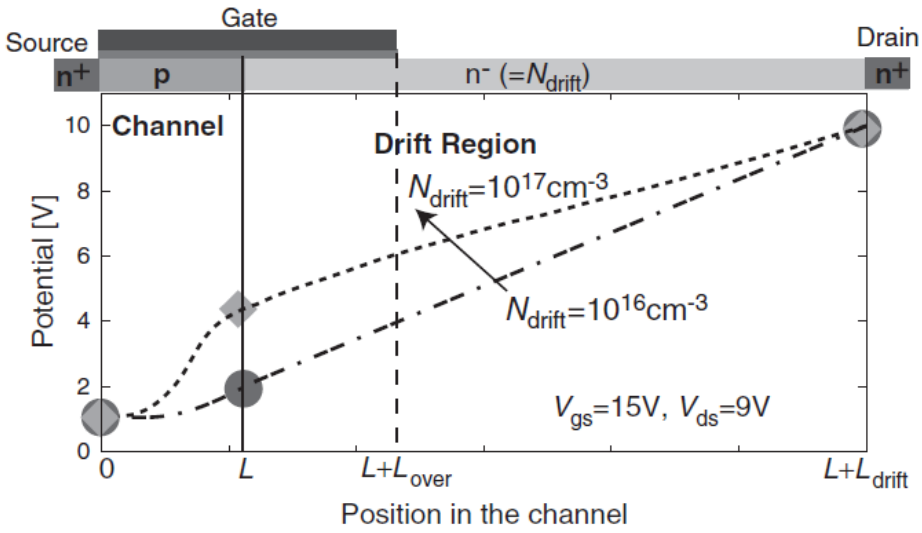


Figure 5-6. Calculated potential distribution along channel with developed HiSIM-HV (symbols) for two N_{drift} concentrations compared with 2D device simulation results (line).

5.3 Implementation Technique for Consistent Thermal Simulation

Figure 5-7 shows the structure of the virtual power module that was studied. Thermal interference occurs among three devices in this structure (Fig. 5-8). In order to conduct the electro-thermal coupling simulation, the RC compact thermal model (CTM) must be implemented into a circuit simulator. The Foster network was selected as the RC CTM, which has a configuration consisting of parallel resistance and capacitance sub-circuits connected in series[5]. The reason for this choice is that with this model the RC parameters can be easily extracted and it requires only a small circuit size to achieve the required accuracy for complicated cooling systems such as an IGBT module. The circuit shown in Fig. 5-9 was proposed to realize the electro-thermal coupling simulation on SPICE3 with thermal interference. The main circuit part, which consists of MN1-3, DFWD, LLOAD, etc., is a basic switching circuit for an inductive load. MN1-MN3 are the switching devices investigated in this study, DFWD is the free wheeling diode and LLOAD is the load. In Fig. 5-9, the value of the current source ILOSS2 connected to the MN2 temperature node is equal to the power consumption in MN2. The current controlled current source (CCCS) F22 copies the current value from the current value that flows in V2. The thermal impedance Z22 is the self thermal impedance of MN2, so that the temperature caused by the self-heating effect at node n22 appears as a voltage. Z21 and Z23 are the mutual thermal impedances of MN2. Because of the thermal interference, the temperature increase at MN2 caused by MN1 and MN3 appears on nodes n21 and n23, respectively. All temperature values are added using the voltage controlled voltage sources (VCVSs) E21, E22 and E23, and the thermal interference among the three chips is then calculated. These calculations are performed simultaneously at each simulation time step.

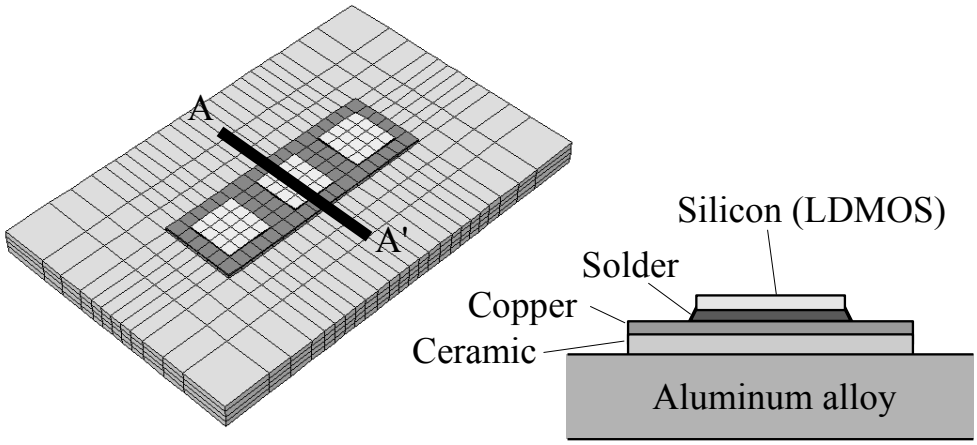


Figure 5-7. Cooling structure of the virtual power module.

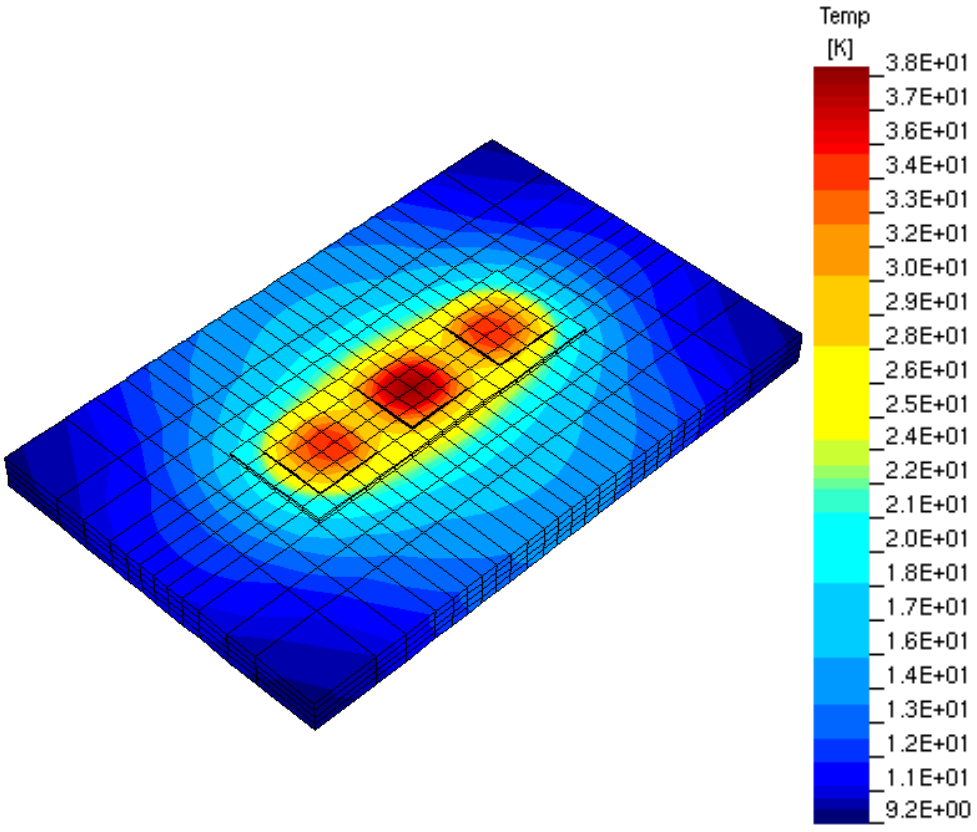


Figure 5-8. Example of thermal analysis that includes thermal interference.

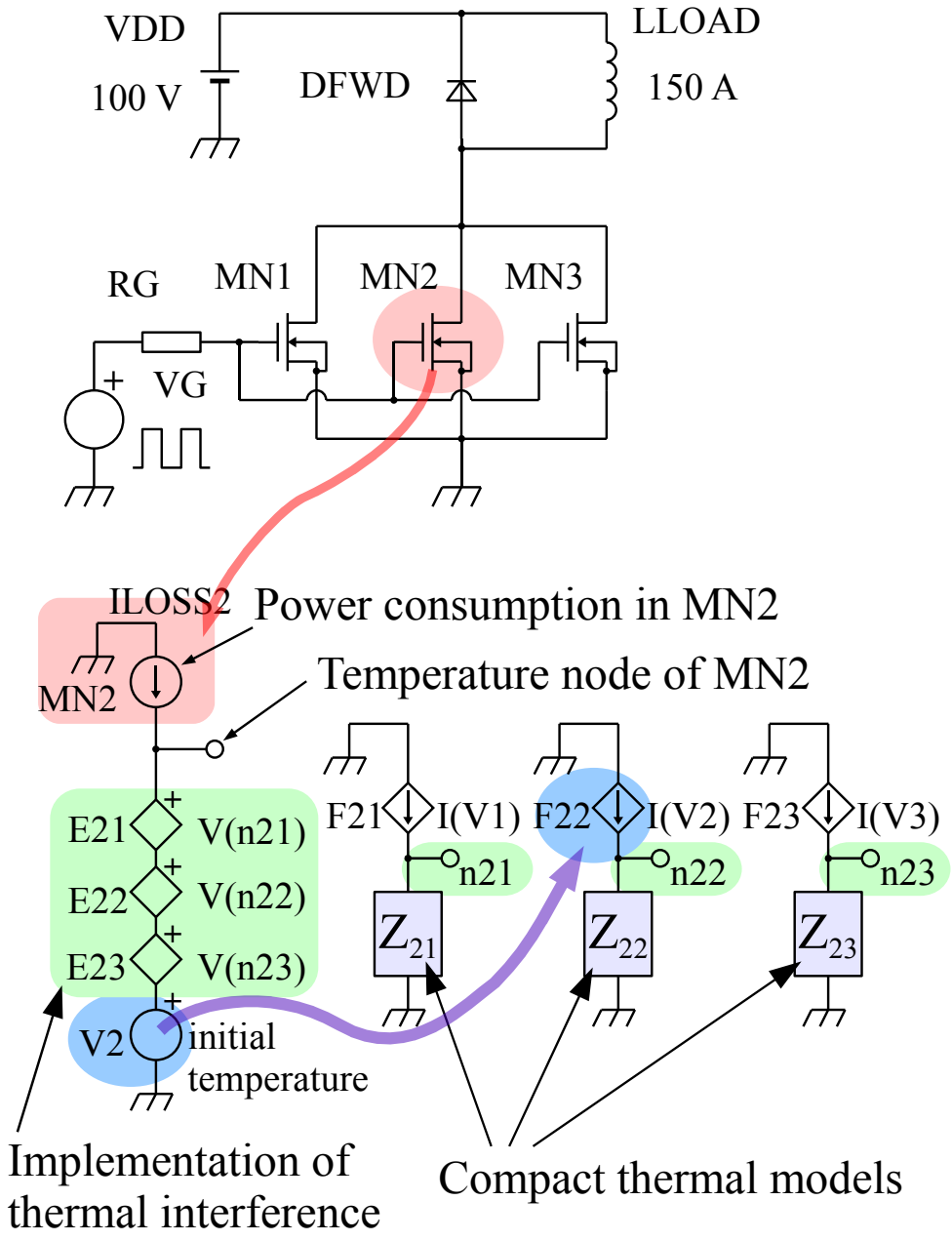
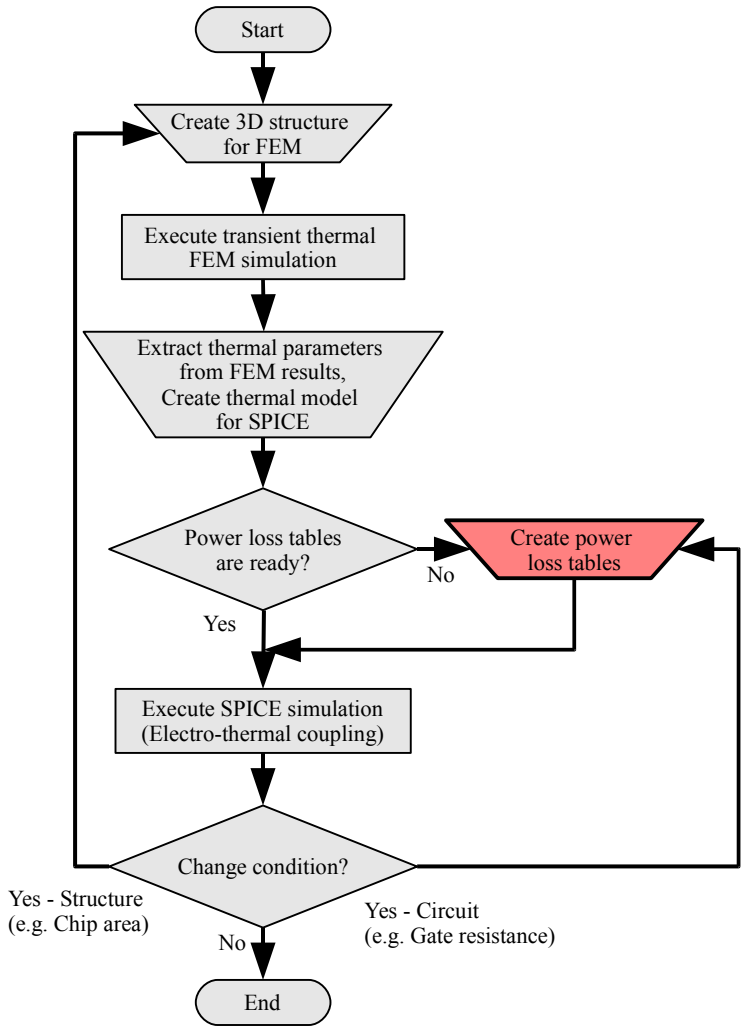


Figure 5-9. Electro-thermal coupling simulation circuit for SPICE3.

Two possible procedures for the electro-thermal coupling simulation of a real circuit including the “off-line operation” are shown in Fig. 5-10. The table look-up procedure requires a look-up table, which is time consuming to prepare (Fig. 5-10(a)). On the contrary, the HiSIM_HV simulation (Fig. 5-10(b)) does not require a look-up table. However, the power loss of the devices and the device temperatures are calculated simultaneously, so that iterative calculation is necessary for accurate simulation. Thus, computational stability is strongly required for the procedure.



(a) Conventional method (table look-up)

Figure 5-10. Procedures for the electro-thermal coupling simulation.

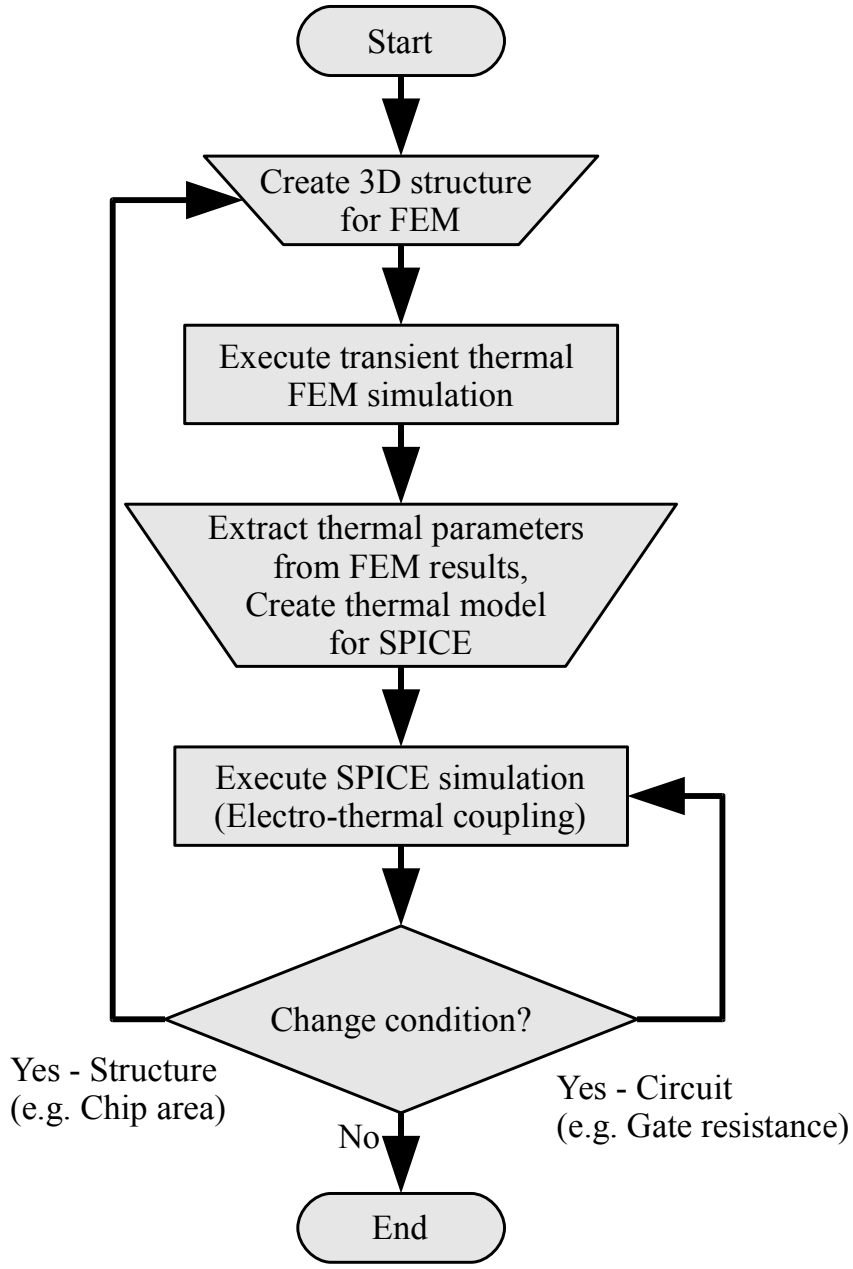


Figure 5-10. (b) Direct method using the HiSIM_HV LDMOS model.

5.4 Evaluation of Calculation Time

Evaluation of the HiSIM_HV model was performed on the following three aspects. Firstly, stability of the electro-thermal coupling simulation on SPICE3 was evaluates with long simulation time. Secondly, the calculation speeds between HiSIM_HV and MOS Level 3 on SPICE3 were compared. Finally, the calculation speeds between HiSIM_HV on SPICE3 and Power MOSFET model on SIMPLORER[10] were compared to evaluate the feasibility of the proposed method.

5.4.1 Stability evaluation in long time simulation

Figure 5-11 shows the complete circuit applied for the electro-thermal coupling simulation on SPICE3. This is a simple inductive load switching circuit, the same as

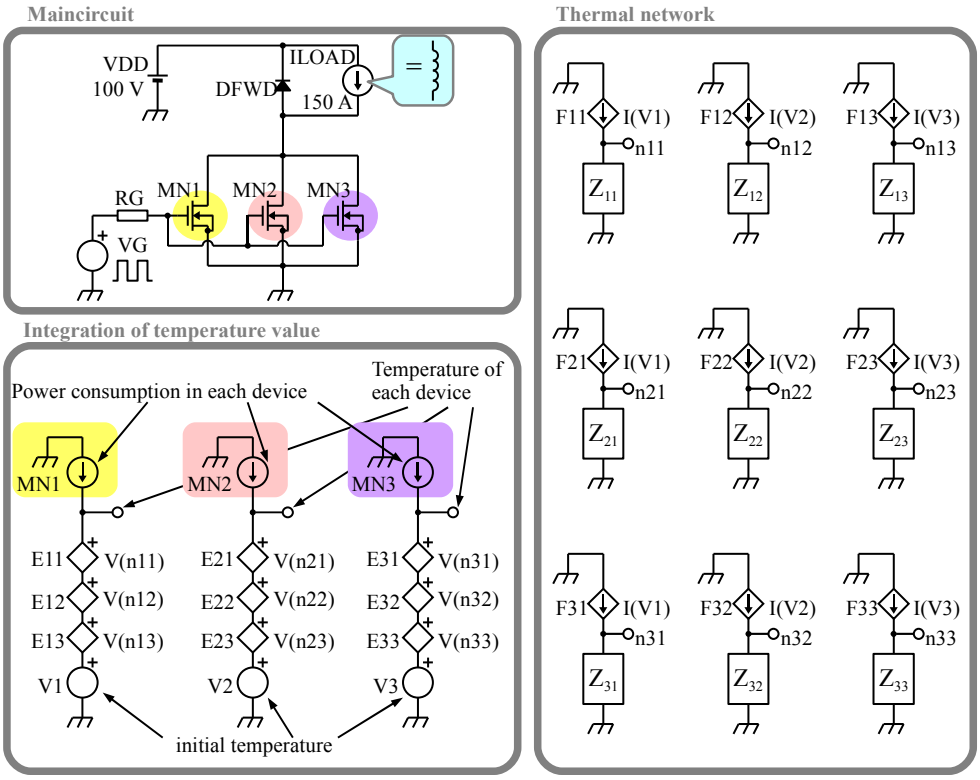


Figure 5-11. Complete circuit used to perform the electro-thermal coupling simulation on SPICE3.

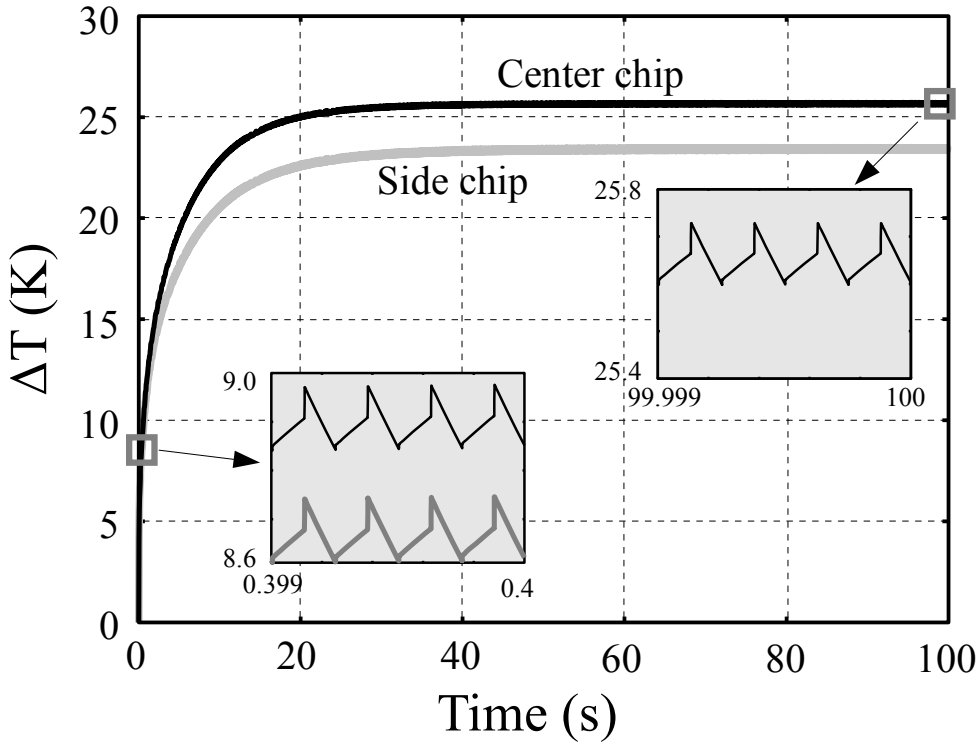
shown in Fig. 5-9, including three parallel-connected switching devices in which thermal interference occurs. In this circuit, the inductive load is replaced by a constant current source (ILOAD) for stable computation. The simulation conditions are listed in Table 5-I.

The simulation time (100 s) is determined by the thermal saturation time of the power module. Figure 5-12 shows the transient simulation results using HiSIM_HV. Figures 5-12(a) and 5-12(b) are plotted on linear and logarithmic time-scales, respectively. It takes six hours to complete the simulation using an Intel Xeon 5160 3 GHz (Core architecture). Considering the nanosecond simulation time step to perform the switching behavior of the power device, a six hour simulation time is a very short time to complete such a long time (100 s) simulation. Although small oscillations can be found in the temperature waveforms, discontinuity was not observed within the entire time range of Figs. 5-12(a) and (b). The observed waveforms reflect the enlarged power loss graphs in Fig. 5-12(a), because of switching operations of the power device. The enlarged graphs in Fig. 5-12(a) show the detailed temperature transitions of HiSIM_HV in the electro-thermal coupling simulation for four successive switching cycles. The temperature increases rapidly with both turn-on and turn-off of the current, and slowly increases during the “on” state and slowly decreases during the “off” state (see Fig. 5-13(a)).[2,24]) The switching behavior of this simulation is shown in Fig. 5-13. Figure 5-

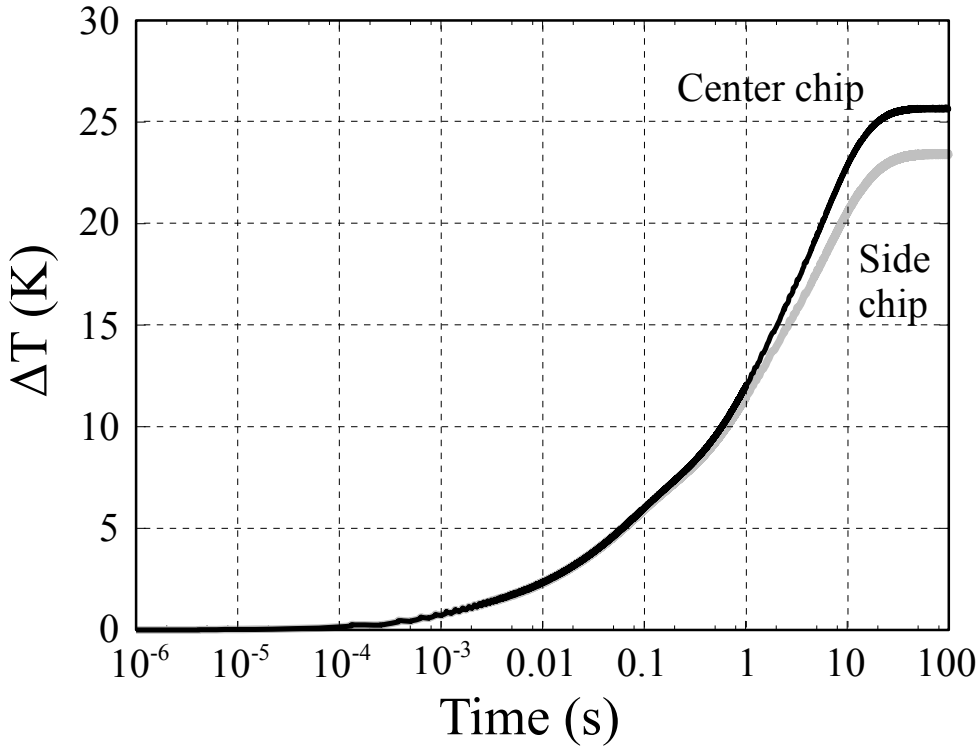
Table 5-I. Simulation conditions for stability evaluation in long time simulation.

Items	Conditions
Simulator	SPICE3F5 (HiSIM_HV is implemented)
CPU	Intel Xeon 5160 3 GHz (Core architecture)
Physical memory (GB)	2
Carrier frequency (kHz)	4
Final time (s) (TSTOP)	100
Suggested time step (ns) (TSTEP)	50
Simulator variables (.OPTIONS)	None

13(a) shows the results with HiSIM_HV, and Fig. 5-13(b) shows the results with MOS Level 3, in which the DC characteristics are described using different equations and are dynamically selected corresponding to the instantaneous voltage condition. MOS Level 3 includes no self-heating effect. Fluctuations are observed in the Id waveform for both the on-state and off-state with the MOS Level 3 model. On the other hand, stable switching waveforms are observed using the HiSIM-based model. These results demonstrate that electro-thermal simulation was successfully conducted using HiSIM_HV on SPICE3.

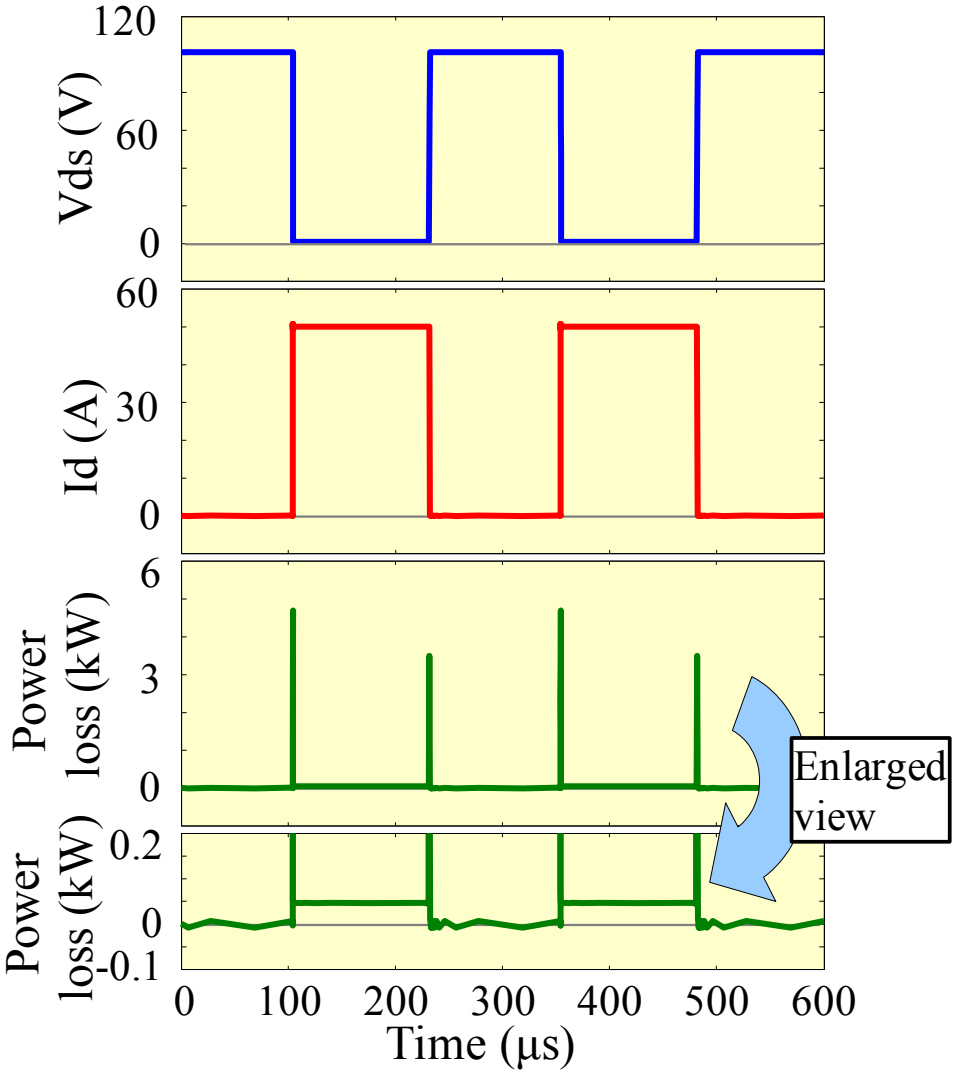


(a) Linear time-scale.



(b) Logarithmic time-scale.

Figure 5-12. Simulated temperature waveforms.



(a) HiSIM_HV LDMOS

Figure 5-13. Switching behavior of the MOSFET model. These waveforms were obtained from long time simulation results.

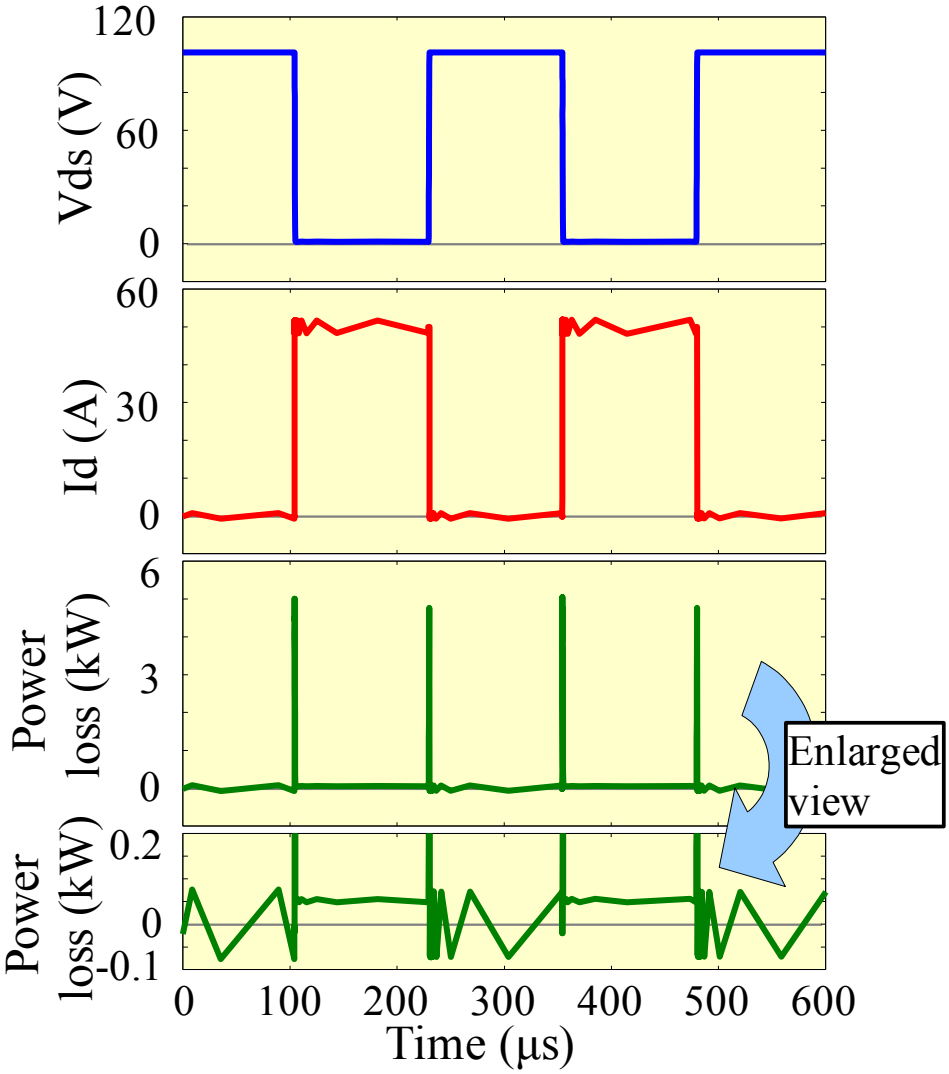


Figure 5-13. (b) MOS level 3.

5.4.2 Comparison of calculation speed between HiSIM_HV and MOS level 3

A simple inductive load switching circuit with a single switching device, shown in Fig. 5-14, was used for this evaluation. The three parallel-connected MOSFETs shown in Figs. 5-9 and 5-11 are reduced to a single MOSFET in order to shorten the calculation time for evaluation. The evaluation was performed under the conditions shown in Table 5-II. The simulation results executed on SPICE3 are presented in Fig. 5-15. It is clear that simulation results from HiSIM_HV are on average 42 % slower than those from the MOS Level 3 model. The reason can be attributed to the simplicity of the MOS Level 3 model. According to the investigation of the iteration steps, the number of iteration steps required for simulation with HiSIM_HV was 2.7 times less than that with MOS Level 3, which explains the high stability of HiSIM_HV for the circuit simulation. In addition, the difference in simulation time is reduced when extra circuits are added, which is illustrated as “with CTM” in Fig. 5-15. As a result, the calculation time with HiSIM_HV is expected to become relatively shorter for simulation of complicated circuits.

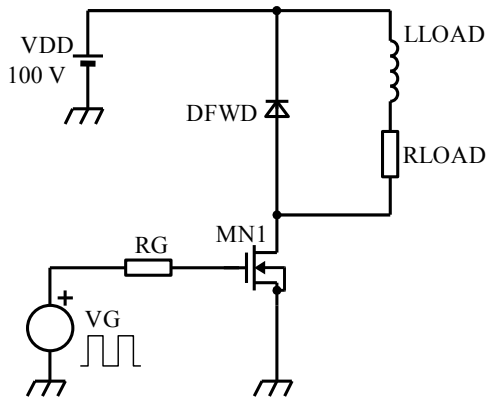


Figure 5-14. Main simulation circuit used for simulations described in subsections 5.4.2 and 5.4.3.

Table 5-II. Simulation conditions for comparison of calculation speed between HiSIM_HV and MOS level 3.

Items	Conditions
Simulator	SPICE3F5 (HiSIM_HV is implemented)
CPU	Intel Core2duo U7500 1.06 GHz
Physical memory (GB)	1.5
Switching period (μs)	20
Final time (ms)	100
Suggested time step (ns)	5
Simulator variables (.OPTIONS)	method=gear

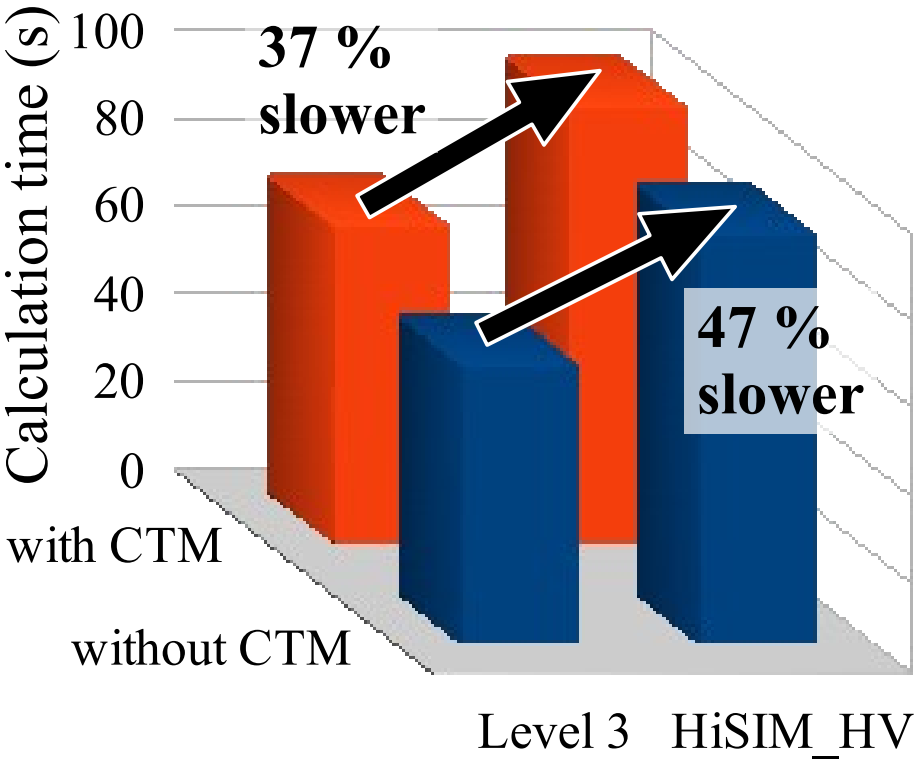


Figure 5-15. Comparison of calculation speed between HiSIM_HV and MOS level 3 on SPICE3.

5.4.3 Comparison of calculation speed between SPICE3 (HiSIM_HV) and SIMPLORER (Power MOS)

The calculation speeds between SPICE3 with HiSIM_HV and SIMPLORER with "Device Level" Power MOSFET model were compared on the same hardware. The core part of the Power MOSFET model in SIMPLORER is similar to the MOS Level 3 model; therefore, it is expected that the stability of the circuit simulation will decrease. The simulated circuit is the same as that used in subsection 5.4.2 (Fig. 5-14), and the simulation conditions are listed in Table 5-III. Figure 5-16 shows the results for calculation time under different conditions. In Fig. 5-16, "without CTM" indicates that the circuit does not include CTM, and "with CTM" indicates that the circuit includes CTM, but electro-thermal coupling is not performed. "Self-heating" indicates that the circuit includes CTM and electro-thermal coupling is performed. The calculation speed of HiSIM_HV on SPICE3 significantly exceeded that with the Power MOSFET model on SIMPLORER version 7. However, the quantitative ability of the two models is unclear from the results show in Fig. 5-16, because the result includes overheads (operating system, simulator, etc.). Although comparison of the absolute performance is quite difficult, it is clear that the degradation of speed by activation of the self-heating effect in HiSIM_HV is much smaller than that for Power MOSFET on SIMPLORER. The number of iteration steps of the two simulations resulted in similar values for calculation time. Thus, it can be concluded that a stable and fast electro-thermal coupling circuit simulation is possible using HiSIM_HV.

Table 5-III. Simulation conditions for comparison of calculation speed between SPICE3 (HiSIM_HV) and SIMPLORER (power MOS).

Items	Conditions
Simulator	(a) SPICE3F5 (HiSIM_HV is implemented) (b) SIMPLORER v.7 Student Version
CPU	Intel Core2duo U7500 1.06 GHz
Physical memory (GB)	1.5
Switching period (μs)	20
Final time (ms)	100
Time step (ns)	(a) Suggested time step: 5 (b) Minimum time step: 5
Simulator variables (Integration formula)	(a) method=gear (b) Euler

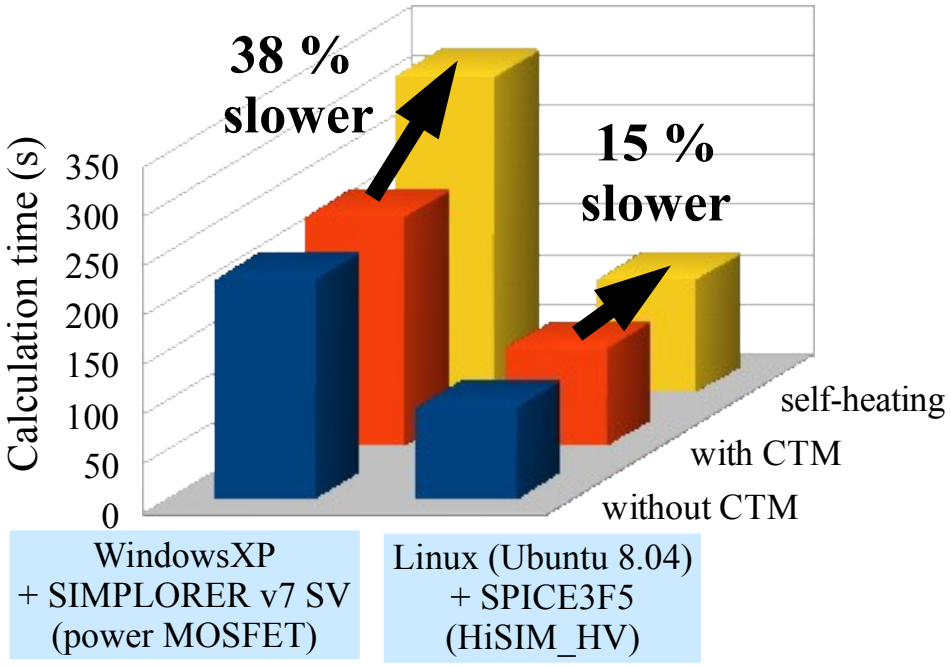


Figure 5-16. Comparison of calculation speed between HiSIM_HV on SPICE3 and power MOSFET model on SIMPLORER.

Chapter 6

Conclusion

A novel RC compact thermal model was proposed which has the capability of representing the thermal behavior of the multi chip power module for automotives accurately. This RC compact thermal model employs not only Foster network as the basic circuit configuration but also the thermal impedance matrix for representing the thermal interference among Si chips.

A novel electro-thermal coupling simulation technique using table look-up method was proposed. The technique mainly focused on a dynamic analysis of a HV inverter during real driving operations such as WOT. The electro-thermal coupling simulation with the RC compact thermal model offers reasonable accuracy for prediction of the Si chip temperature in HV inverter module. In addition, the electro-thermal coupling simulation technique enables long time scale calculation to finish at realistic time.

A methodology was developed that enables the consistent simulation of electro-thermal coupling using HiSIM_HV. The results have verified that the methodology provides fast and stable simulation for real automotive applications with power devices in which thermal interference occurs.

For above proposals, the electro-thermal simulation became more realistic than a design tool for automotive applications.

Chapter 7

Future Prospects and Problems

7.1 Future Prospects

Surface-potential-based models as represented by HiSIM_HV have prospects of power device model because of the good convergence and fast calculation. The applications of HiSIM_HV to power electronics circuit such as converter and inverter have been hardly reported. Evaluations of HiSIM_HV with more realistic circuit condition are needed. For example, detailed gate driver circuit model, stray inductance model, smoothing capacitor model and so on.

It is necessary to verify more complex circuit operation such as soft switching with HiSIM_HV model.

7.2 Problems

An off-line operation is required to build RC compact thermal models, because Foster network is not physics based, then transient heat 3D-FEM analysis is needed to define the RC parameters. A new thermal compact model where parameter extraction is not required is expected.

The difference of time scale between electrical behavior (nanosecond range), mechanical behavior (millisecond) and thermal behavior (second range) cause speed degradation for electro-thermal coupling simulation. Because simulation time steps are determined by smaller time range. If the calculation can be divided into a electric and a thermal solvers, and calculated simultaneously by optimum time step for each solver,

this problem can be solved.

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