Influence of bulk bias on negative bias temperature instability of *p*-channel metal-oxide-semiconductor field-effect transistors with ultrathin SiON gate dielectrics

Shiyang Zhu and Anri Nakajima[a)]
Research Center for Nanodevices and Systems, Hiroshima University, 1-4-2 Kagamiyama, Higashi-Hiroshima 739-8527, Japan

Takuo Ohashi and Hideharu Miyake
Elpida Memory, Inc., 7-10 Yoshikawa-kogyo-danchi, Higashi-Hiroshima 739-0198, Japan

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Bulk (well) bias effects (grounded, positively biased, and floating) on both static and dynamic negative bias temperature instability of *p*-channel metal-oxide-semiconductor field-effect transistors with ultrathin SiON gate dielectrics were systematically investigated. The device degradation under both static and dynamic negative bias temperature (NBT) stresses with relatively large gate voltage (V_g) is significantly enhanced by a positive bulk bias (V_b). Moreover, the device degradation under bipolar pulsed bias temperature (BT) stress is dramatically enhanced by floating the bulk electrode. Both phenomena can be attributed to an additional degradation related to hot hole injection. The holes are energized by an electrical field of the induced depletion region between channel and bulk provided by the positive V_b or, in the case of bipolar pulsed BT stress with the bulk electrode floating, by the transient depletion region below the channel induced by the *p-n* junction between source (drain) and bulk upon the gate voltage V_g being switched from positive to negative with a transition time less than about 0.2–100 ms. © *2006 American Institute of Physics*.
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I. INTRODUCTION

The negative bias temperature instability (NBTI) of *p*-channel metal-oxide-semiconductor field-effect transistors (*p*MOSFETs) has become an important reliability concern in modern complementary metal-oxide-semiconductor (CMOS) technology, especially when the gate-oxide thickness is scaled down to less than 2.0 nm and also nitrogen is introduced into the gate-SiO_2 film in order to suppress the boron penetration and to increase the dielectric constant.[1,2] Considerable efforts have been done for both static (Refs. 3–6) and dynamic (Refs. 7–10) NBTI, in which a constant or pulsed voltage is applied on the gate electrode (V_g) while the source, drain, and bulk (well) electrodes are grounded. Interface traps and/or positive fixed oxide charges being created under the negative bias temperature (NBT) stress are generally believed to be Si dangling bonds ($\equiv$Si•, P_b centers in the electron spin resonance studies[11]) originating from the dissociation of hydrogen passivated Si–H bonds at and/or near the SiO_2/Si interface.[3–10] The dissociation is widely accepted to be associated with holes in the inversion channel under the NBT stress,[3–5] but the exact role of the channel holes has not been fully understood yet. To clarify this problem, the bulk bias (V_b) effect on NBTI was intentionally studied in literature because V_b can modify the population of channel holes while keeping the other stress conditions constant.[12–16] However, the reported V_b effects are controversial. For example, Mitani *et al.*[13] and Hurad *et al.*[14] found that NBTI under an identical V_g stress is independent of the positive bulk bias up to 3 or 4 V, while Kimizuka *et al.* observed that the NBTI lifetime begins to reduce significantly at V_b larger than about 1.5 V.[12] Moreover, Mahapatra *et al.* reported that NBTI at high V_b ($\geqslant$4 V) shows identical degradation rate for short stress time while the degradation rate drastically increases at longer stress times.[15] The V_b induced degradation enhancement has been attributed to the substrate hot hole injection.[12,15] On the other hand, to the best of our knowledge, the V_b effect on the dynamic NBTI has not been reported.

In this paper, the V_b effects under both static and dynamic NBT stresses were studied systematically. We find that NBTI can be significantly enhanced by applying a positive bulk bias. The enhancement depends on both V_g and V_b. Moreover, we find a frequency-dependent degradation enhancement under bipolar pulsed BT stress with the bulk electrode floating. The enhancement is much more significant than that under the V_b grounded case.[9,10] A model based on the hot hole injection is proposed to explain the degradation enhancement in both stress configurations, i.e., static stress with positive V_b and bipolar stress with V_b floating.

II. DEVICES FABRICATION AND NBTI CHARACTERIZATION

The tested *p*MOSFETs were fabricated on the *n* well of *p*-Si (100) substrates using a standard CMOS process[17] with lightly doped source (drain) structure, p^+ polycrystalline-Si gate electrode, and plasma-nitrided SiON gate dielectric, which has a base SiO_2 thickness of about 2 nm and a peak

[a)]Author to whom correspondence should be addressed; FAX: 81-82-424-3499; electronic mail: nakajima@sxsys.hiroshima-u.ac.jp

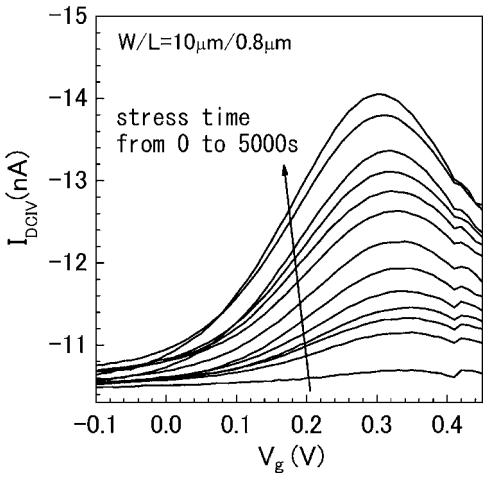

FIG. 1. Typical modified DCIV curves measured on a *p*MOSFET before and after static NBT stress at $V_g=-2.5$ V, $V_b=1$ V, and 125 °C for 3, 10, 20, 40, 100, 200, 400, 700, 1100, 2000, 3000, and 5000 s, respectively. The DCIV peak height is proportional to the interface trap density (N_{it}), while the peak position shift is related to the oxide charge generation (ΔN_{ot}).

nitrogen concentration of about 9% around the upper half oxide film toward the poly-Si/SiO_2 interface. The equivalent oxide thickness (EOT) is extracted to be about 2.22 nm from the high-frequency capacitance-voltage (*C-V*) measurement. The channel width (W) is 10 μm and the length (L) is between 0.32 to 1.12 μm. Unless specially noted, devices were stressed at 125 °C for 1000 s, by applying a constant or pulsed voltage on the gate electrode while the source (drain) electrode was grounded and the bulk (well) electrode was grounded, positively biased, or floating. The pulsed voltage has a square wave form with a duty factor of 50%, and a minimum rise and fall time of 4.5 ns. The impact of the possible voltage overshoot upon rapid V_g reversal in the dynamic stressing configuration, which may enhance the device degradation,[18] seems minor in our experiments because (1) no degradation enhancement is observed under the unipolar stress, as will be shown in this paper; (2) the square wave form keeps quite well even at 10^7 Hz with 4.5 ns transition time as monitored by an oscilloscope. Note that the actual stress time under the dynamic stress is half of the nominal stress time predicted in this paper by taking the 50% duty factor into account. Immediately after stress interruption, the device transfer characteristics (I_d-V_g curves at $V_d=-0.1$ V) and a modified direct-current-current-voltage (DCIV) curve[19] were recorded at the stressing temperature to extract the threshold voltage (V_{th}) and the interface trap density (N_{it}), respectively. Each stress was carried out on a fresh device whose initial N_{it} is between 1.5 and 3.0×10^9 cm^{-2}. One example of DCIV curves is shown in Fig. 1 for a pMOSFET before and after NBT stress from 3 to 5000 s. By increasing the stress time, the DCIV peak height increases and the peak position shifts to the negative direction, reflecting the interface trap generation and the fixed oxide charge buildup, respectively.[20]

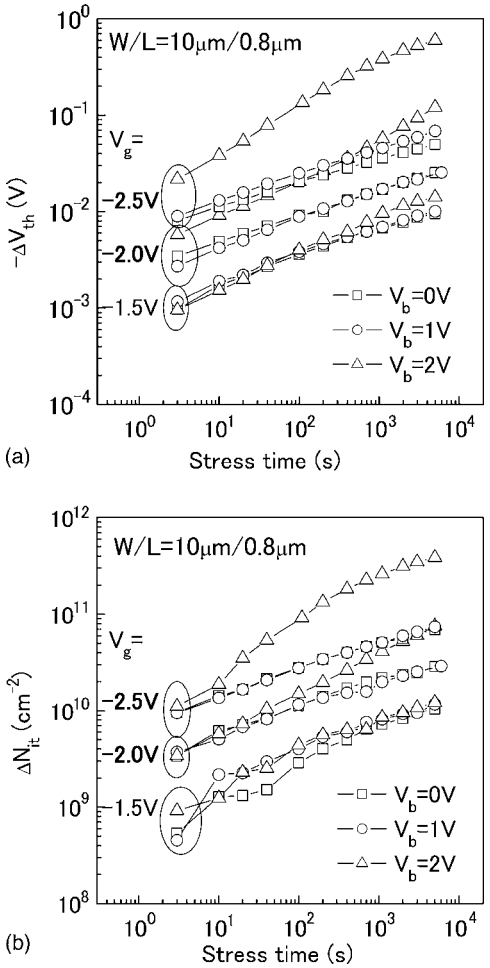

FIG. 2. (a) The threshold voltage shift (ΔV_{th}) extracted from the I_d-V_g curves, and (b) the corresponding interface trap generation (ΔN_{it}) deduced from the modified DCIV curves as a function of stress time under static stress with various V_g and V_b. *p*MOSFETs with $W/L=10$ μm/0.8 μm were stressed and measured at 125 °C.

III. RESULTS AND DISCUSSION

A. Positive bias of the bulk electrode

By applying a positive bulk bias V_b, the initial threshold voltage is modified due to the body effect. For example, a device with $W/L=10$ μm/0.32 μm has a V_{th} of −0.365 V, −0.597 V, and −0.726 V at $V_b=0$ V, 1 V, and 2 V, respectively. Therefore, the hole population in the inversion channel, which is proportional to $|V_g-V_{th}|$, decreases with increasing V_b at the identical stress voltage. The oxide electrical field (E_{ox}) was also kept the same because the inversion channel has the same potential as the grounded source (drain) electrode.

Figure 2 shows the threshold shift (ΔV_{th}) and corresponding interface trap generation (ΔN_{it}) as a function of stressing time under static NBT stress with various V_g and V_b. Both ΔV_{th} and ΔN_{it} exhibit similar V_b and V_g dependence. At low stress voltage ($|V_g|=1.5$ V), the device degradation (ΔV_{th} and ΔN_{it}) is almost independent of V_b (up to 2 V), in agreement with those reported by Mitani *et al.*[13] and Huard *et al.*[14] At high $|V_g|$ ($\geq$2.0 V), the degradation is significantly enhanced and has a large degradation rate. The enhancement magnitude depends on both V_g and V_b, i.e., the

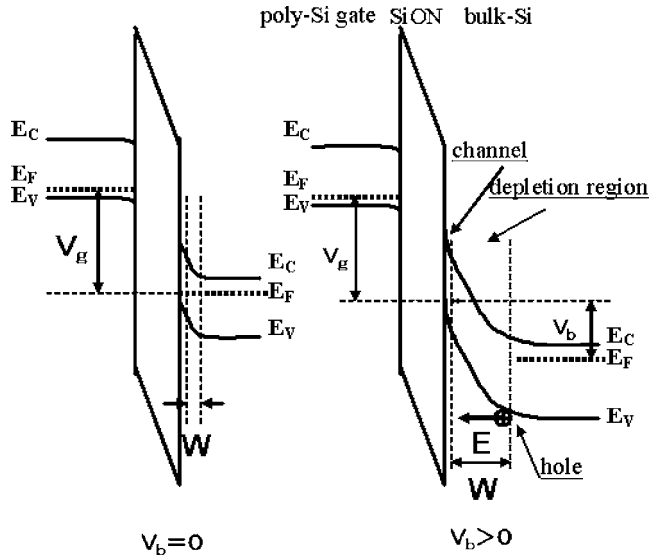

FIG. 3. Energy band diagrams for a p^+ poly-Si gate pMOSFET under NBT stress with the bulk electrode grounded ($V_b=0$) (left), and positively biased ($V_b>0$) (right). Both the depletion width (W) and the built-in electrical field (E) are below the channel layer increase with V_b increasing.

higher $|V_g|$, the lower V_b to trigger the enhancement is. It should be noted that the value of $|V_g|$ and V_b to trigger the degradation enhancement is much lower than that reported by Mahapatra *et al.*,[15] while is similar to those reported by Kimizuka *et al.*[12] and Varghese *et al.*[16] The V_b induced degradation enhancement can be explained by energetic (hot) hole injection from the substrate.[12,15,16] The energy band diagrams for a pMOSFET under NBT stress with $V_b=0$ and $V_b>0$ are schematically shown in Fig. 3. The width (W) of the induced space charge (depletion) region between the channel and the bulk, and the maximum electrical field (E_m) in this region, are both proportional to $V_b^{1/2}$ approximately.[21] Holes from the bulk to the channel can be accelerated by this electrical field to be hot. Thus, the number of hot holes in the channel as well as their kinetic energy increases with V_b increasing although the population of total inversion holes is reduced. It is reasonable to assume that only the holes which can tunnel through the interface layer of 1–2 Å to be captured by the Si–H bonds can give contribution to dissociate the Si–H bonds.[5] In this way, hot holes are more effective to induce degradation than the normal cold channel holes. With V_b increasing, the degradation induced by the normal cold holes decreases due to the decrease of the channel hole density, while an additional degradation induced by the hot hole injection increases. At low V_b, these two opposite effects make the device degradation appear almost independent of V_b. With V_b further increasing, the latter increases more quickly and prevails over the former, resulting in a significant degradation enhancement at high V_b. Moreover, the injected hot holes may break the Si-O bonds at or near the SiO_2/Si interface besides the Si–H bonds, as suggested by Varghese *et al.*[16] This effect makes the V_b induced degradation enhancement more significant.

The field-dependent tunneling coefficient of holes from the channel to the interface layer depends almost exponentially on the local electrical field at the interface. In other

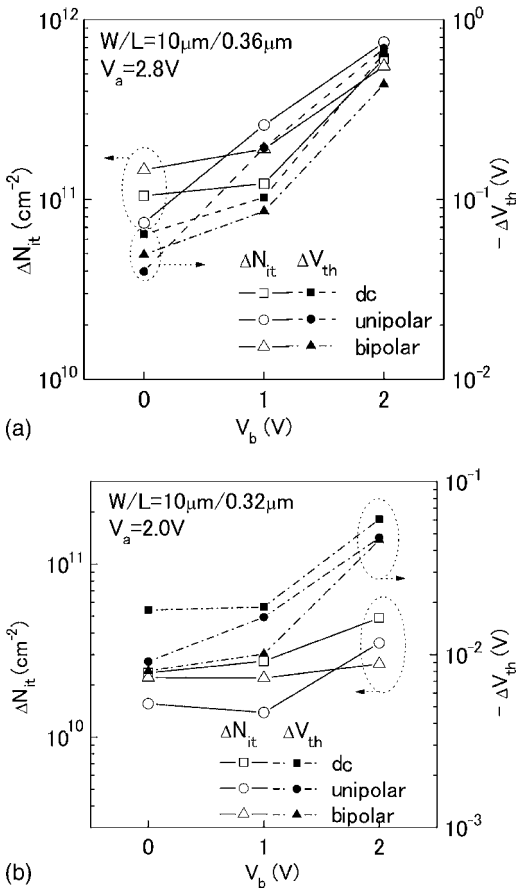

FIG. 4. The device degradation (ΔN_{it} and ΔV_{th}) as a function of the bulk bias V_b under static, unipolar, and bipolar pulsed BT stresses. The stress voltage magnitude (V_a) is (a) $V_a=2.8$ V, and (b) $V_a=2.0$ V. The dynamic stress has a square wave form of 1 MHz frequency, 50% duty factor, and 4.5 ns transition time. Devices were stressed at 125 °C for 1000 s.

words, the barrier height of the bond dissociation decreases with E_{ox} (i.e., V_g) increasing.[5] Therefore, the V_b effect is more significant at high $|V_g|$ than that at low $|V_g|$, and the minimum V_b to trigger the degradation enhancement decreases with increasing $|V_g|$.

Figure 4 shows ΔN_{it} and ΔV_{th} as a function of V_b under static and dynamic NBT stresses (with unipolar or bipolar square wave form) with different magnitudes of the stressing voltage, i.e., $V_a=2.8$ V in Fig. 4(a) and $V_a=2.0$ V in Fig. 4(b). The frequency of the dynamic stress is 1 MHz. Consistent with the static stress, a similar V_b effect also appears under the dynamic stress. It is worth noticing that the bipolar BT stress exhibits a relatively smaller enhancement as compared with other two stress configurations (static and unipolar) with identical V_a and V_b values. The reason is explained as follows.

In the normal V_b grounded case, it has been known that the device degradation under high-frequency bipolar BT stress is enhanced.[9] Such a frequency-dependent degradation enhancement (also see Fig. 6) has been ascribed to the trapped electrons at or near the Si/SiO_2 interface states upon the Si surface potential reversal from accumulation to inversion quickly.[10] The electrical field built by the trapped electrons or the recombination of the trapped electrons with the channel free holes can accelerate the dissociation of the Si–H

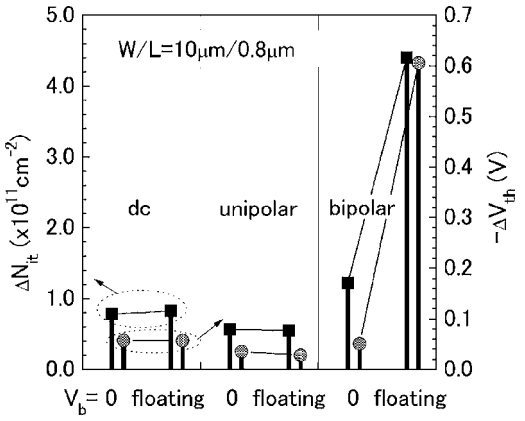

FIG. 5. The interface trap generation ΔN_{it} (left axis) and the threshold voltage shift ΔV_{th} (right axis) after static, unipolar, and bipolar pulsed BT stresses with V_b grounded or floating. Devices with $W/L=10\ \mu m/0.8\ \mu m$ were stressed at $V_a=2.8$ V, 125 °C for 1000 s. The degradation is dramatically enhanced under the bipolar stress with V_b floating.

bonds, resulting in an additional degradation at each pulse fall edge during the bipolar BT stress. Because the occupied interface states in the upper half of the band gap are negative while those in the lower half are neutral,[1] the additional degradation occurs only when the high level of the bipolar wave form (V_+, see inset of Fig. 8) is larger than the midgap voltage (V_{mg}) and increases rapidly with V_+ further increasing.[9] If the bulk electrode is applied by a positive V_b, the midgap voltage increases with V_b. Therefore, this additional degradation induced by V_g reversal quickly decreases with V_b increasing. Meanwhile, the V_b induced degradation enhancement (due to the bulk hot holes injection) in the "on" state (i.e., at the $V_g=V_-$ stage) of the bipolar stress keeps similar to that in the case of the static or unipolar BT stress. Thus, the increasing rate of overall degradation with V_b increasing under the bipolar BT stress is apparently smaller than that under other two stress configurations.

B. Floating of the bulk electrode

Figure 5 compares the device degradation under static and dynamic BT stresses with the bulk electrode floating or grounded. The degradation remains almost unchanged under the static and unipolar BT stresses, while it is dramatically enhanced under the bipolar stress with V_b floating. The ΔV_{th} enhancement is more significant than that of ΔN_{it}, indicating that more ΔN_{ot} than ΔN_{it} is created under the bipolar BT stress with V_b floating.

The frequency dependences of the degradation (ΔN_{it} and ΔV_{th}) under bipolar BT stresses with V_b grounded or floating are shown in Fig. 6. In the normal bipolar BT stress with V_b grounded, the degradation enhancement occurs at frequency larger than ~10 kHz. ΔN_{it} increases about two times with the frequency increasing from 10 kHz to 10 MHz at $V_a=2.8$ V, and with more large enhancement ratio at higher V_a (not shown here, see Ref. 9). On the other hand, with V_b floating, the degradation enhancement starts to occur at 1 Hz. ΔN_{it} increases about 7–10 times with frequency increasing from 1 Hz to 1 kHz and then almost saturates with further increasing of the stressing frequency. Moreover, under the same bipolar BT stress, the degradation with V_b floating is much larger than that with V_b grounded. The ΔV_{th} can reach about 0.4 V at a relatively small V_a stress (2.5 V).

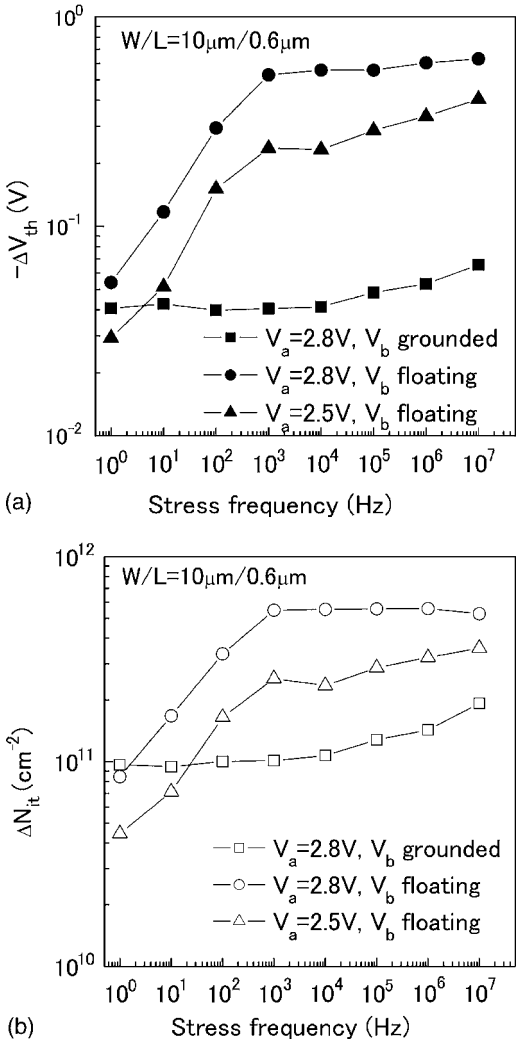

FIG. 6. (a) ΔV_{th} and (b) ΔN_{it} as a function of stressing frequency under bipolar BT stresses with V_b floating. Devices with $W/L=10\ \mu m/0.6\ \mu m$ were stressed at $V_a=2.8$ V or 2.5 V, and at 125 °C for 1000 s. The corresponding frequency dependences for devices stressed with V_b grounded and $V_a=2.8$ V are also shown for comparison.

Since the degradation almost saturates around 1 kHz, we fix the frequency at 1 kHz while changing one of the wave form parameters in the following experiments to further clarify the degradation behaviors under the bipolar BT stress with V_b floating.

First, the transition time (both the rise and the fall time) is modified from 4.5 ns to 10^5 ns. In the V_b grounded case, it has been known that the additional degradation under high-frequency bipolar BT stress decreases with increasing the transition time (t_T) of the pulse wave form because the portion of trapped electrons in the interface states which can follow the V_g variation through the emission process increases, and the degradation enhancement almost vanishes if t_T is larger than about 60 ns.[10] This critical time constant corresponds to the emission time constant of the trapped electrons in the interface states.[22] In the V_b floating case, Fig. 7 shows that the degradation is almost independent of t_T up

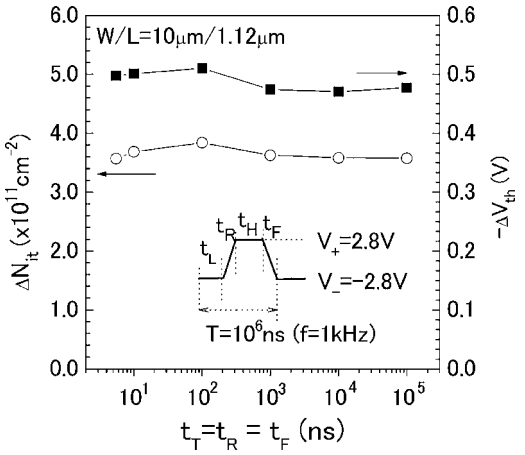

FIG. 7. The device degradation (ΔN_{it} and ΔV_{th}) as a function of the pulse transition time t_T under bipolar BT stresses with V_b floating. Devices with W/L=10 μm/1.12 μm were stressed at 125 °C for 1000 s by a stressing wave form of V_a=2.8 V and f=1 kHz. Inset is the schematic wave form depicting the rise time t_R and the fall time t_F.

to 10^5 ns. Thus, the corresponding time constant is at least larger than 10^5 ns and is probably around 1–1000 ms because the degradation enhancement starts to occur at 1 Hz and saturates at 1 kHz, as shown in Fig. 6.

Second, the low level voltage (V_-) of the pulse wave form (i.e., the stress voltage) is kept at −2.8 V while its high level voltage (V_+) is changed from 0 (as in the unipolar stress) to 2.8 V (as in the normal bipolar stress). Figure 8 shows that the degradation is independent of V_+ at the small V_+ region, and then it increases with V_+ quickly when V_+ is larger than about 1.5 V. The minimum V_+ to trigger the degradation enhancement is larger than that in the V_b grounded case.[9]

Third, the V_a dependence of the device degradation is shown in Fig. 9. Both ΔN_{it} and ΔV_{th} increases almost exponentially with V_a increasing. The increase rate of ΔN_{it} (and ΔV_{th}) with V_a becomes larger when V_a is larger than about 1.8 V, indicating more significant degradation enhancement at larger V_a, similar to that in the V_b grounded case.[10] The

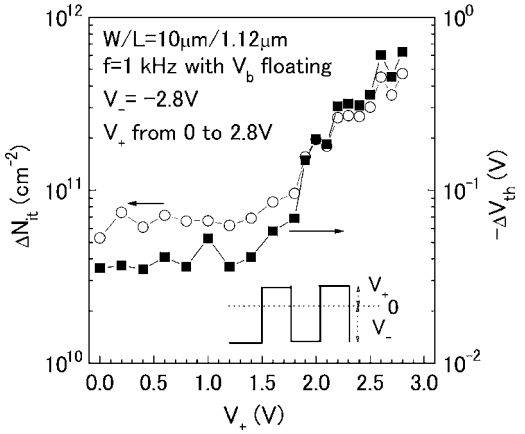

FIG. 8. The device degradation (ΔN_{it} and ΔV_{th}) as a function of V_+ under unsymmetrical bipolar BT stresses with V_b floating. Devices with W/L =10 μm/1.12 μm were stressed at 125 °C for 1000 s by a stressing wave form of V_-=−2.8 V, f=1 kHz, and t_T=4.5 ns. Inset is the schematic wave form depicting the high level voltage (V_+) and the low level voltage (V_-).

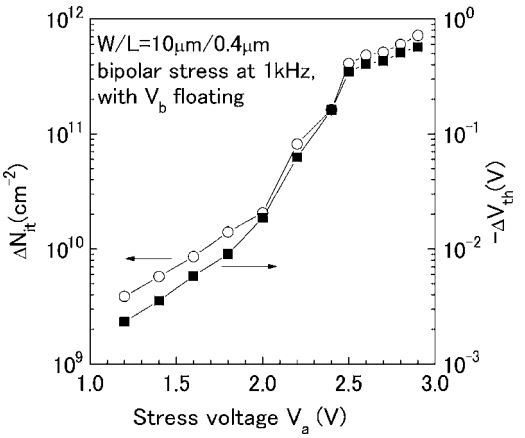

FIG. 9. The device degradation (ΔN_{it} and ΔV_{th}) as a function of the stress voltage magnitude (V_a) under 1 kHz bipolar BT stresses with V_b floating. Devices with W/L=10 μm/0.4 μm were stressed at 125 °C for 1000 s.

reduction of the increase rate at the even higher V_a region (V_a>2.5 V) can be attributed to the saturation effect, as will be explained below.

The time evolutions of ΔN_{it} and ΔV_{th} under bipolar BT stress with V_b floating are shown in Fig. 10. The stress voltage is V_a=2.6 V or 2.8 V. At the early stressing time of the

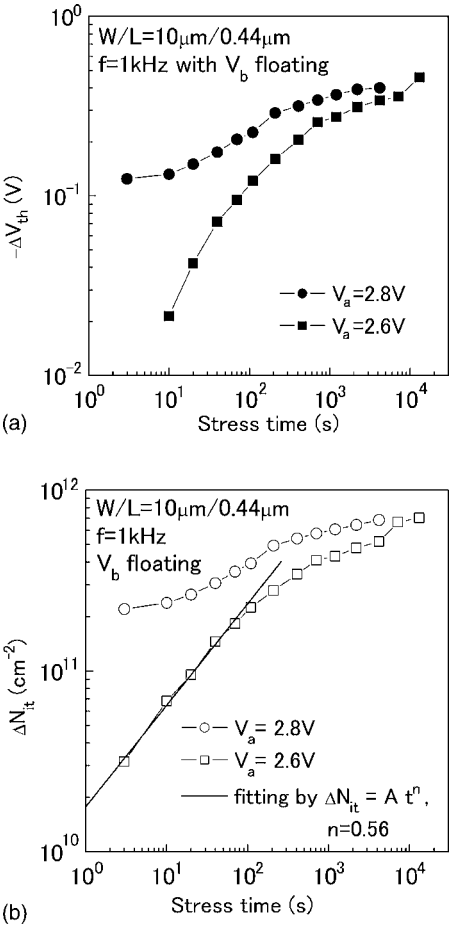

FIG. 10. The time evolutions of (a) ΔV_{th} and (b) ΔN_{it} under 1 kHz bipolar BT stress with V_b floating. Devices with W/L=10 μm/0.44 μm were stressed at 125 °C with V_a=2.6 or 2.8 V. At the early stage of the V_a =2.6 V stress, a fitting line based on the power-law dependence is drawn for ΔN_{it}.

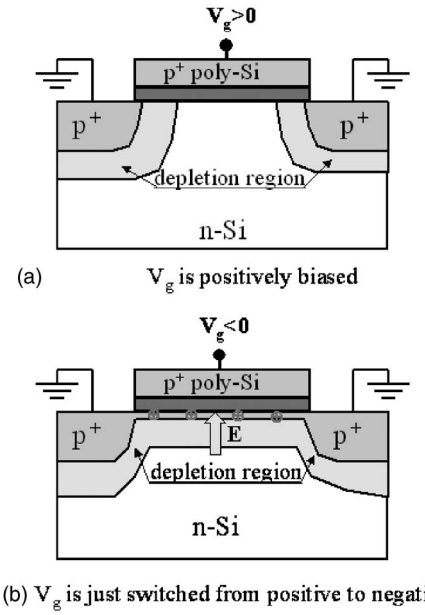

FIG. 11. Schematic cross-sectional view of a *p*MOSFET with the source (drain) grounded and the bulk floating at the stage of (a) V_g is positively biased: there exists a depletion region between the source (drain) and the bulk Si; and (b) V_g is just switched from positive to negative: the inversion channel is formed almost simultaneously due to the holes supported from the source (drain) electrode while the depletion region still exists due to the absence of electrons supported from the bulk electrode.

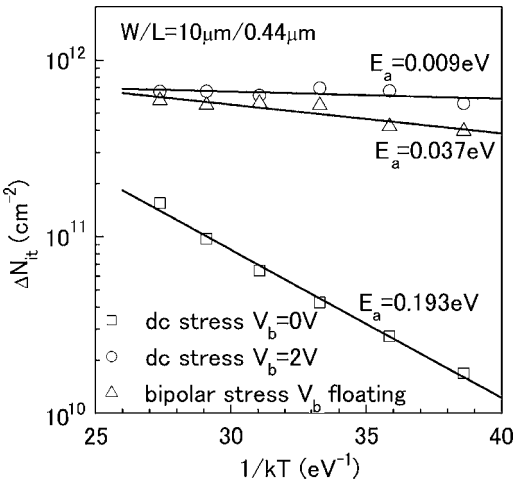

FIG. 12. Temperature dependence of ΔN_{it} under static NBT stress with $V_b=0$, static NBT stress with $V_b=2$ V, and bipolar BT stress with V_b floating. Devices with $W/L=10$ μm/0.44 μm were stressed at $V_a=2.6$ V, 125 °C for 1000 s. The frequency of the bipolar stress is 1 kHz. The activation energy E_a was extracted from the linear fitting of these Arrhenius plots.

$V_a=2.6$ V stress, ΔN_{it} follows approximately a power-law dependence of time with an exponent n of 0.56 approximately, which is much larger than the typical value (around 0.25) expected from the conventional reaction-diffusion model for NBTI.[4] With increasing the stressing time, the ΔN_{it} generation rate decreases continuously, showing a saturation trend at the longer stressing time. ΔV_{th} has an approximately similar trend to that of ΔN_{it} but with a slight different slope, indicating the fact that the created oxide charge is not one-to-one related with the interface trap.[20] At the $V_a=2.8$ V stress, the saturation effect appears at the very earlier stress times due to the large ΔN_{it}. The degradation saturation effect can be explained by the limited Si–H bond number in the SiO_2/Si interface.[14] If the Si–H bonds have been substantially broken to be the P_b centers, the generation rate decreases. The saturation trend at frequency larger than 1 kHz in Fig. 6 and at V_a larger than about 2.5 V in Fig. 9 can be attributed to the same reason.

C. Hot hole injection under bipolar BT stress with V_b floating

We propose that the degradation enhancement under the bipolar stress with V_b floating can also be attributed to the hot hole injection upon V_g is switched from positive to negative quickly. When the gate electrode is positively biased ($V_g=+V_a$), the potential of the bulk Si also increases due to V_b floating, forming a reversely biased *p-n* junction between the grounded source (drain) and the bulk Si, as shown in Fig. 11(a) schematically. The depletion width and the maximum electrical field in this region increase with $+V_a$ increasing. When V_g is switched to negative ($V_g=-V_a$), an inversion layer is formed almost immediately at the Si surface with holes supported from the source (drain) electrode. Meanwhile, the depletion region below the source (drain) [and the channel, because the source (drain) and the channel are electrically connected together to have the same potential by the inversion holes at $V_g=-V_a$] will be vanished by electrons filling in. If V_b is grounded, the electrons can be supported from the bulk electrode almost simultaneously (the time constant is about 10^{-4} ns).[21] If V_b is floating, the electrons are provided by the electron-hole generation-recombination (G-R) process in the depletion region. The corresponding time constant is quite large. From the low-frequency C-V measurement of a MOS capacitance, the time constant for electrons responding to the V_g variation through the G-R process is around 0.2–100 ms.[21] Therefore, if the transition time of V_g from $+V_a$ to $-V_a$ is shorter than the above time constant, there exists a transient stage that V_g has already been $-V_a$ while the depletion region below the inversion layer still exists, as shown in Fig. 11(b) schematically. This remaining transient depletion region can provide hot hole injection from the bulk to the channel, as in the case of V_b positively biased, thus enhances the device degradation. This model explains qualitatively the frequency dependence in Fig. 6 and the absence of the transition time dependence up to 0.1 ms in Fig. 7. The V_+ dependence in Fig. 8 can be explained by the fact that the transient depletion region should be larger than a critical value to trigger the degradation enhancement, as in the case of positively biased V_b. The degradation enhancement increases with V_+ further increasing, resulting in a larger V_a accelerating factor at the higher V_a region, as shown in Fig. 9. The tunneling electrons from gate to substrate at the $V_g=-V_a$ stage may not play an important role because these electrons can recombine with the inversion holes in the channel quickly.

Since the hot holes in the above model are energized by the electrical field, and also taking into account the fact that the tunneling coefficient depends on temperature weakly, the hot hole injection induced degradation is expected to be dependent on temperature weakly. Figure 12 compares ΔN_{it} as

a function of the reciprocal of the stress temperature under normal NBT stress (static and V_b grounded), static NBT stress with V_b=2 V, and bipolar BT stress with V_b floating with the identical stress voltage of V_a=2.6 V. ΔN_{it} under the latter two stress configurations is much larger than that under the first one, indicating that the device degradation is dominated by the hot hole injection. From the linear fitting of these Arrhenius plots, the activation energy E_a was extracted to be 0.197, 0.009, and 0.037 eV, respectively. The E_a value of the normal NBT stress is in consistent with that reported in literature.[9,14,20] On the other hand, the hot hole injection induced degradation has a very small E_a value, both for the V_b positive bias in the static stress and the V_b floating in the bipolar stress, in agreement with our model.

IV. CONCLUSION

The V_b (grounded, positively biased, or floating) effects on both static and dynamic NBT stress are studied. Significant degradation enhancement is observed by applying a positive bulk bias in both static and dynamic NBT stresses or by V_b floating in the bipolar BT stress. The degradation enhancement in both cases is attributed to an additional degradation related with the hot hole injection. The holes are energized by the electrical field provided by the positive bulk bias V_b or, in the case of bipolar BT stress with V_b floating, by the transient depletion region below the channel induced by the *p-n* junction between the source (drain) and the bulk upon V_g being switched from positive to negative so quickly that electrons cannot respond to the V_g variation through the R-G process.

From the viewpoint of device application, our finding indicates that, in some cases, the bulk electrode is floating, e.g., for silicon-on-insulator (SOI) devices without body contact, a dramatic degradation may occur if a bipolar gate voltage is applied. On the other hand, very large V_{th} shift (e.g., $>$1 V) can be obtained at a relatively small gate voltage by applying a bipolar V_g with V_b floating.

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