Periodic Coulomb oscillations in Si single-electron transistor based on multiple islands

Kensaku Ohkura, Tetsuya Kitade, and Anri Nakajima[a)]
Research Center for Nanodevices and Systems, Hiroshima University, 1-4-2 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8527, Japan

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We fabricated highly doped Si single-electron transistors (SETs) with a series of geometrically defined islands. The conduction mechanism was systematically investigated in the temperature range from 4.2 K to 100 K. Despite their island size variation, some of the SETs showed clear periodic and quasiperiodic Coulomb oscillations. This is in contrast to the conventional idea that only geometrically uniform islands show periodic Coulomb oscillations. We showed theoretically that periodic Coulomb oscillation appears under the small deviation of gate capacitances with the period determined by the average of the capacitances. We also found that the formed charge soliton that was conducted through the islands was spread over the whole array. This may also contribute to the periodicity of the Coulomb oscillation. The SET with multiple islands was applied to an Exclusive-OR circuit and achieved a room temperature operation. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2143116]

I. INTRODUCTION

Single-electron devices utilizing the Coulomb blockade effect are promising candidates for use as basic elements of future low-power and high-density integrated circuits.[1–12] To develop these devices into commercial products, the use of Si for their construction is important because of Si's compatibility with conventional fabrication techniques for large-scale integrated devices.

Recently, room-temperature operation of Si single-electron transistors (SETs) with a single island has been reported by several groups.[4,10,12] For room-temperature operation, the island size should be reduced to under 10 nm. In addition, the junction should be thinned so that electrons can tunnel into and out of the island. The junction size also should be reduced in order to reduce the total capacitance and raise the operating temperature. Therefore, for practical application, an island of 10 nm size, thin junctions, and a control gate formed near the island must be fabricated uniformly and reproducibly for stable electrical characteristics among devices. However, it seems difficult to fabricate such uniform SETs reproducibly by using currently available fabrication techniques, even though many groups have proposed various SET structures.

One way to overcome the difficulty is to utilize serially connected islands instead of a single island. In such a multiple-island system, the effective total capacitance decreases compared with that in a single-island system when the stray capacitances are small because the junction capacitances are connected in series.[13,14] This leads to an increase in the charging energy of the islands and to an increase in the operation temperature. In other words, to enable room-temperature operation, a multiple-island system can use a larger island compared with a single-island system. Moreover, SETs with serially connected islands should be able to suppress cotunneling, which increases the valley current of Coulomb oscillation and prevents higher temperature operation.[14–16]

Recently, SETs have been applied to logic circuits operating at high temperatures.[12,17,18] In particular, a small number of SETs with multiple gates were found to have an advantage in implementation of logic functions.[19] Therefore, we applied an SET with two gates and multiple islands connected in series to an exclusive-not-OR[17] and exclusive-OR (XOR) circuit.[18] The circuit achieved room temperature operation.

Periodic Coulomb oscillation is also important for application because it makes it easy to design a logic circuit. However, a serially connected multiple-island system usually has complicated electrical characteristics when an island size fluctuation exists.[20] In our case, fabricated islands would have varied in size to some extent because it is very difficult to form a pattern with a completely uniform size even by using lithography.[21]

In this study, we investigated the conduction mechanism of SETs with serially connected islands. We obtained periodic characteristics of Coulomb oscillations for some of these SETs even though the island size fluctuated to some extent. We discuss this point by considering the periodicity of free energy of the system under the small deviation of gate capacitances. We also described the system from the viewpoint of solitons.[22,23] In a one-dimensional array system, a charge soliton is the basic element of electrical conduction. Section II describes the fabrication process of our SETs. Section III gives the results of the electrical characteristics and discussions, and presents the application of the SET to a logic circuit operating at room temperature. Section IV is a brief summary of this work.

[a)]Author to whom correspondence should be addressed; electronic mail: nakajima@sxsys.hiroshima-u.ac.jp

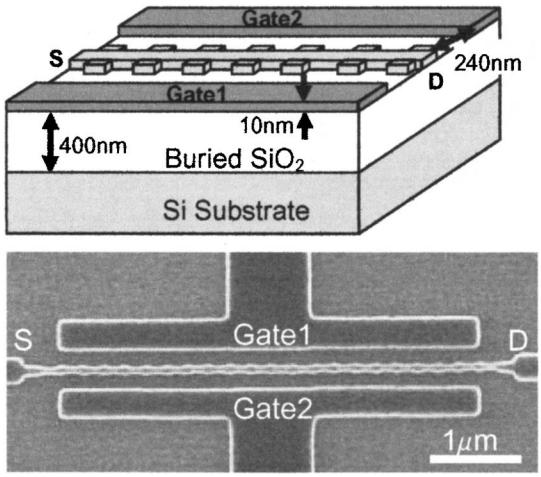

FIG. 1. (a) Schematic diagram and (b) plan view scanning electron microscopy (SEM) micrograph of the fabricated SET's resist pattern. Only one of the two gates was used in the electrical measurements. *S* and *D* stand for source and drain. In (b), there are 22 geometrically defined Si islands.

II. EXPERIMENT

Figure 1 shows a schematic diagram (a) and resist pattern (b) of the SET we produced with geometrically defined nanoscale islands. We fabricated a one-dimensional regular array of nanoscale islands using electron-beam (EB) direct writing to an SOI layer. The top Si layer and the buried oxide on the SOI wafers were 50 and 400 nm thick, respectively. Doping of the top Si layer was done by $POCl_3$ diffusion for 10 min. We measured the sheet resistance with a four-point probe method at room temperature to determine the doping level. The doping levels of 2×10^{19} and 1×10^{20} cm^{-3} were obtained depending on the temperature during $POCl_3$ diffusion. Due to the high doping level, characteristics peculiar to the metallic system are expected.[8] The fabrication process included EB lithography using a negative resist (SAL601 SR2) and dry etching using an electron cyclotron resonance etcher with the resist pattern as a mask. Subsequent isotropic wet etching in an $NH_4OH/H_2O_2/H_2O$ solution at 70 °C reduced the dimensions of the device and the damage introduced during the dry etching process.[21] The final thickness of the top Si layer was about 10 nm. Each island was about 20 nm wide, and the distance between the centers of adjacent islands was 250 nm; the width of the narrowest region between adjacent islands was about 10 nm. The distance between the channel wire and the side gates was 240 nm. After the interlayer dielectrics were deposited, the device fabrication was completed with the formation of Ohmic contacts. We measured the current-voltage characteristics with an HP 4156B semiconductor parameter analyzer and a cryogenic manipulated probe system (HYTT-01). Except for the circuit application of our SET presented in Sec. III F, the measurement used only one of the two gates shown in Fig. 1.

III. RESULTS AND DISCUSSION

A. Number of islands and junctions

We measured a lot of devices with various numbers of islands. Among these, some devices showed periodic Coulomb oscillations and some showed aperiodic oscillations. In this study, we focused on the periodic oscillations as mentioned in the introduction.

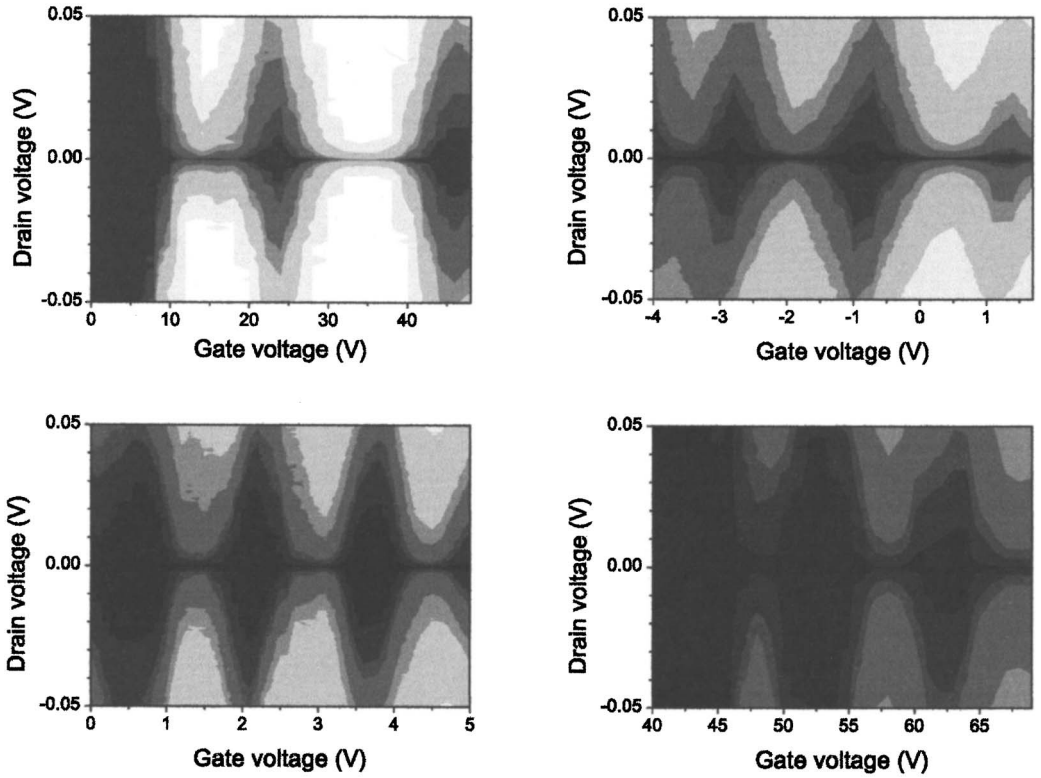

FIG. 2. Contour plot of drain current as a function of drain voltage and gate voltage at 4.2 K for SETs with (a) a single, (b) 11, (c) 22, and (d) 60 islands. Coulomb diamonds are clearly observed.

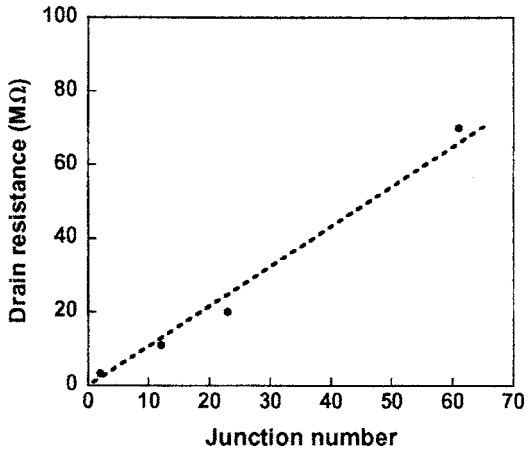

FIG. 3. Drain resistance as a function of junction number in SETs at 4.2 K (drain voltage is 0.1 V). The drain resistance is nearly proportional to the junction number. The dotted line is to guide the reader's eye.

Figures 2(a)–2(d), respectively, show the drain current I_d as a function of drain voltage V_d and gate voltage V_g at 4.2 K for SETs with 1, 11, 22, and 60 islands. Coulomb diamonds were observed for all SETs. I_d decreased as the number of islands increased.

To confirm whether the fabricated SETs indeed have the intended number of islands and junctions, the drain resistance of the SETs was plotted as a function of the junction number at 4.2 K (Fig. 3). Here, drain resistance is defined as $(\partial I_d/\partial V_d)^{-1}$, which was measured at the V_g of the peak of Coulomb oscillation (V_d=0.1 V). As can be seen in the figure, the drain resistance is almost proportional to the junction number. The resistance per junction is calculated to be 1 MΩ, which is much larger than the quantum resistance (25.8 kΩ). Therefore, the junctions were formed as designed and had enough large resistance to confine electrons in the islands between junctions. Since the conductive region between junctions acts as a Coulomb island, the number of Coulomb islands was also considered to be as designed.

B. Coulomb oscillation

Figure 4(a) shows the drain conductance, V_g characteristics of the SET with 22 islands at 4.2 K. A very periodic conductance oscillation was observed in the V_g region from 0 to 8.5 V. The observed period ΔV_g was about 1.55±0.10 V. Above 8.5 V, irregular peak height characteristics appeared. These may be due to another conduction path of electrons and/or the additional tunnel junctions and islands caused by the V_g difference.

Figure 4(b) shows the drain conductance, V_g characteristics of the SET with 11 islands at 4.2 K. A quasiperiodic conductance oscillation was observed in the V_g region from −5.0 to 5.0 V. The observed period ΔV_g was 1.90±0.30 V. Assuming a one-dimensional array of islands with the same size, the capacitance C_g between an island and gate is given by $\Delta V_g = e/C_g$ as shown in Sec. III D. For ΔV_g of 1.9 V, C_g is estimated to be 0.1 aF. The intervals between the fourth and fifth conductance peaks (2.6 V) and between the fifth and sixth peaks (2.7 V) are much larger than other intervals mentioned above. These may also be due to the presence of another conduction path caused by the V_g difference. On the other hand, the capacitance C_{sub} between an island and substrate was 0.1 aF from the peak intervals of the drain conductance as a function of the substrate voltage.

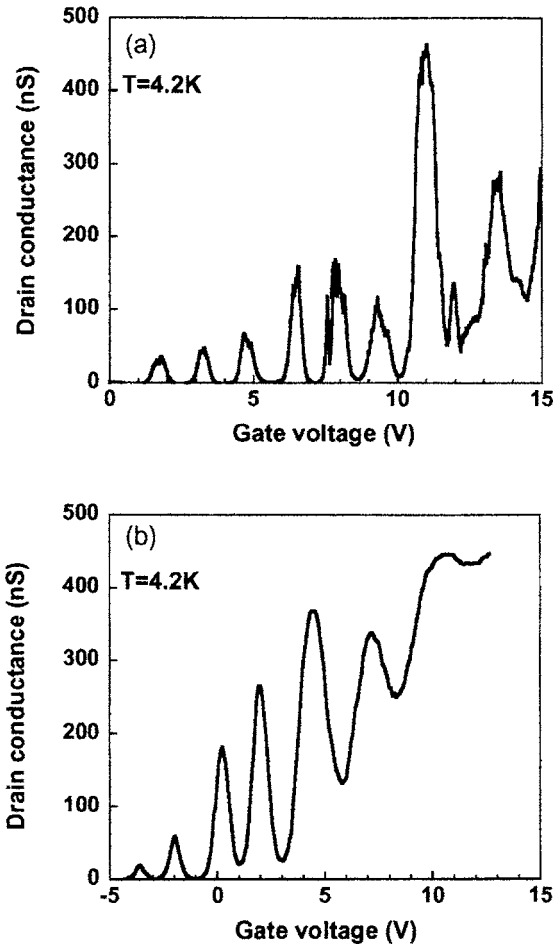

FIG. 4. Drain conductance as a function of gate voltage at 4.2 K for SETs with (a) 22 and (b) 11 islands. Clear Coulomb oscillations are observed. The periods of the oscillations are (a) 1.55±0.10 V and (b) 1.90±0.30 V, respectively.

C. Temperature dependence of Coulomb oscillation

Figure 5 shows the temperature dependence of the Coulomb oscillation of the SET with 11 islands as a function of V_g. The peak position hardly changed, and the peak number did not change in the temperature range from 4.2 K to 100 K. In a multiple-island system with different island sizes, the peak number and intervals of the Coulomb oscillation peaks usually change with temperature. Ruzin *et al.*[24] theoretically demonstrated that the number of Coulomb oscillation peaks increases with temperature due to thermal broadening of the energy levels in two islands connected in series when the difference in the gate capacitances of the islands is large. Indeed, the number of peaks was shown to increase with temperature in a poly-Si wire system, which was considered as a multiple-island system with a relatively large island-size variation.[20] On the other hand, in a homogeneous one-dimensional array system, i.e., a one-dimensional array comprised of islands with the same size, periodic Coulomb oscillations with a period of e/C_g appear

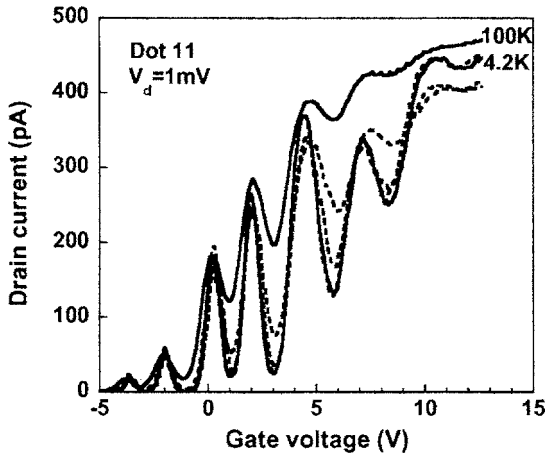

FIG. 5. Temperature dependence of I_d-V_g [Fig. 3(a)] of the SET with 11 islands; T=4.2, 20, 40, 60, and 100 K. The Coulomb oscillation period hardly changes and the peak number does not change in the temperature region from 4.2 K to 100 K. The bottom and top thick lines, respectively, show Coulomb oscillations at 4.2 and 100 K.

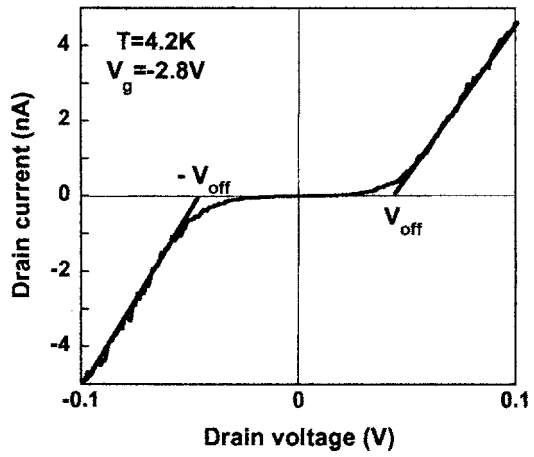

FIG. 6. Drain current as a function of drain voltage V_d at a V_g of a valley of the Coulomb oscillation (−2.8 V). The offset voltage was measured to be 0.047 V. The thin solid line illustrates the determination of the linearly extrapolated offset voltage, V_{off}.

and the peak number does not change with temperature. In our case, fabricated islands would have varied in size to some extent. However, the periodic characteristics of the Coulomb oscillations still appeared and the peak number did not change with temperature.

D. Free energy analysis

The observed periodic Coulomb oscillation in spite of the existence of size fluctuation of the island can be understood by the free energy analysis. Consider a one-dimensional array of $N-1$ islands with junction capacitances only between adjacent islands and gate capacitance C_{gi} between an island and the gate electrode. Here, the gate voltage V_g is biased, and the source and drain voltages V_s and V_d are set to zero. As shown in the Appendix assuming that there is no background charge, the free energy F of the system is written in the form

$$F = \tfrac{1}{2}[-en_1 + C_{g1}V_g \cdots - en_{N-1} + C_{gN-1}V_g]A^{-1} \times \begin{bmatrix} -en_1 + C_{g1}V_g \\ \vdots \\ -en_{N-1} + C_{gN-1}V_g \end{bmatrix}, \quad (1)$$

where n_i is the electron number of the ith island, and A^{-1} is the inverse of the matrix A given by Eq. (A3). The periodicity of the free energy of the system is investigated to know the periodicity of Coulomb oscillation.

First, consider the case of uniform gate capacitances, where $C_{g1}=C_{g2}=\cdots=C_g$. Then the free energy given by Eq. (1) is the periodic function of V_g with the period of e/C_g accompanied by increasing the numbers of electrons in each island by one. Hence the Coulomb oscillation is also the periodic function of V_g with the period of e/C_g. Note that the periodicity is independent of the variation of junction capacitances. Due to this, we neglect that in the following discussion. The variation of junction capacitances generally spoils the alignment of the energy levels in each island, which is necessary for sharp peaks of Coulomb oscillation.

Now, we take into account small variation of gate capacitances. Here, we assume that the numbers of electrons in each island are the same and increased one by one as V_g is increased. Then, F is invariant under interchanging any pairs of junction capacitance (C_{gi} and C_{gj}), which results in $\partial F/\partial C_{gi}=\partial F/\partial C_{gj}$ at $C_{gi}=C_{gj}$. By using this relation, $F(C_{g1}, C_{g2}, \ldots)$ is calculated to equal $F(\langle C_g\rangle, \langle C_g\rangle, \ldots)$ up to the order of $(\delta C_g/\langle C_g\rangle)^2$, where $\langle C_g\rangle$ denotes the average of gate capacitances and δC_g is a deviation of a gate capacitance from the $\langle C_g\rangle$. This is because the first order term of $\delta C_g/\langle C_g\rangle$ is proportional to the summation of deviation of gate capacitances from the average value $\langle C_g\rangle$ over all islands, which vanishes by definition. Thus for small deviation of gate capacitances, F is almost periodic function of V_g with the period of $e/\langle C_g\rangle$ accompanied by increasing the numbers of electrons in each island by one. Therefore, periodic Coulomb oscillation with the period of $e/\langle C_g\rangle$ would appear even in the nonuniform array as long as the deviation of C_g is small.

E. Charge soliton

In a one-dimensional array system, a charge soliton rather than a single electron is the basic element of electrical conduction since the presence of one electron on an island induces a polarization of neighboring islands. In view of the soliton, we present the physical picture of the conduction mechanism. Consider a simple system, a homogeneous one-dimensional array of tunnel junctions. If an electron is placed on an island of an infinitely long array of multiple junctions, the effective total capacitance is given by

$$C_{\text{eff}} = (C_0^2 + 4CC_0)^{1/2}, \quad (2)$$

where C and C_0 are the junction and stray capacitances, respectively.[22,23,25] The main contribution to C_0 is considered to be C_g and C_{sub}. Taking the double gate structure into account, C_0 is given by $2C_g+C_{\text{sub}}$. From this relation, C_0 is about 0.3 aF since C_g and C_{sub} are 0.1 aF as mentioned in Sec. III B. Figure 6 shows I_d as a function of V_d at the V_g of a valley of the Coulomb oscillation (−2.8 V) for the SET

with 11 islands. We obtained an almost symmetric curve with respect to the origin. From the figure, the offset voltage is 0.047 V. Here, the offset voltage is defined as the extrapolated intercept of the linear portion of the I_d curve with the V_d axis. On the other hand, C and C_{eff} can be obtained from the offset voltage equation,

$$V_{\mathrm{off}} = (N - (C/C_0)^{1/2})e/(2C), \tag{3}$$

where N is the number of junctions.[26] Here, N equals 12, since the SET has 11 islands. A C of 10 aF is obtained by substituting V_{off}(0.047 V), C_0(0.3 aF), and N(12) into Eq. (3). Once C is obtained, C_{eff} is evaluated as 3.6 aF from Eq. (2). Using this value of C_{eff}, we can know the information about a solution. By using the expression

$$1/M = \ln[(C_{\mathrm{eff}} + C_0)/(C_{\mathrm{eff}} - C_0)], \tag{4}$$

the soliton length $2M$ is estimated to be about 12. Thus, the soliton length almost equals the array length; i.e., the soliton spreads over the whole array.

Let us regard the region where a soliton spreads as an island of a SET. Then, the formed single charge soliton conducts through all the islands in our system as if an electron conducts through a single island because the soliton length equals the array length. In this case, averaged gate capacitance over the region where the soliton spreads takes a single value in spite of the existence of the island size fluctuation. This may also contribute to the periodic aspects of Coulomb oscillation in our system. If an array length was longer than the soliton length, then the average gate capacitance could vary depending on the position of the soliton when the size fluctuation of island exists. This spoils the periodicity of Coulomb oscillation. Further study is necessary for the relation between the soliton length and the periodicity of Coulomb oscillation.

F. Application

To clarify the advantage from the viewpoint of operating temperature, we consider a SET with a single island and the same C and C_0 as in the 11-island case. The total capacitance of an SET with a single island is given by $2C+C_0$, (about 20 aF in this case). Since the effective total capacitance C_{eff}(3.6 aF) of the multiple island system is about one-sixth this value, the operation temperature becomes six times higher by multiplexing islands.

Owing to the lower C_{eff} of the multiple-island system, we believed that SET circuits employing it would be capable of high-temperature operation. We applied SETs with two gates to an exclusive-not-OR (operating at 77 K)[17] and XOR circuit (operating at room temperature).[18] Figure 7 shows the I_d switching characteristics of the XOR circuit using the SET with 22 islands as a function of V_{g1} and V_{g2} at room temperature. Here, V_{g1} and V_{g2} are the input voltages applied to Gate 1 and Gate 2 shown in Fig. 1. V_{g1} and V_{g2} were switched between 15 V(L) and 19.3 V(H). The operation of the XOR circuit is that the output current is low when V_{g1} and V_{g2} are both H or both L, whereas the output current is high when the one of the input voltages is H and the other is L. An ideal output current I_d for an XOR circuit is shown as the dotted line in the lower part of Fig. 7. The observed I_d is shown as the solid line in the lower part of Fig. 7. If we define the $H(L)$ output state to be when the I_d is larger than 0.6 pA (smaller than 0.3 pA), we can confirm the XOR operation at room temperature.

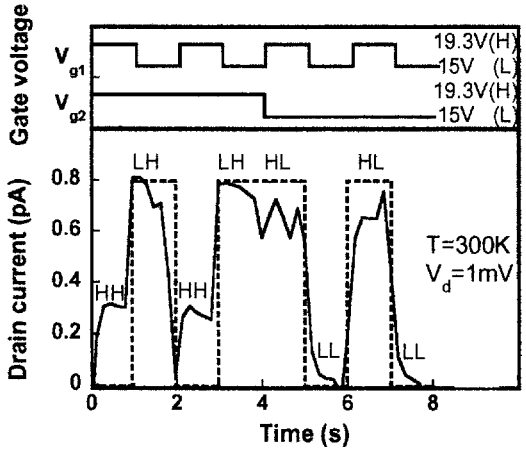

FIG. 7. Measured I_d switching characteristics when the input gate voltages (V_{g1} and V_{g2} shown in the upper part) were switched at room temperature. The input gate voltages (V_{g1} and V_{g2}) were switched between a low voltage level (15 V) and a high voltage level (19.3 V). The dotted line shows the ideal output current for an XOR circuit.

IV. SUMMARY

We fabricated highly doped Si SETs with a series of geometrically defined islands. Some of the SETs showed periodic and quasiperiodic Coulomb oscillations though some small size variation exists among islands. There was no temperature dependence in either the peak position or the peak number from 4.2 K to 100 K. The drain resistance was almost proportional to the junction number and was much larger than the quantum resistance (25.8 kΩ). Therefore, the number of the Coulomb islands and the number of junctions were fabricated as designed. We showed theoretically that periodic Coulomb oscillation appeared under the small deviation of gate capacitances. The soliton length was also estimated to be almost equal to the array length; i.e, the soliton spreads over the whole array. This may also contribute to the periodic aspects of Coulomb oscillation. Taking account of the advantage for high temperature operation that the effective total capacitance in the multiple-island system was reduced in comparison with the one-island case, we applied the SET to an exclusive-OR circuit and achieved a room temperature circuit operation.

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APPENDIX

The free energy F of the system is written in the form

$$F = \frac{1}{2}\sum_{i=1}^{N} C_{i-1,i}(\varphi_i - \varphi_{i-1})^2 + \frac{1}{2}\sum_{i=1}^{N-1} C_{gi}(\varphi_i - V_g)^2 + \sum_{i=1}^{N-1} C_{gi}(\varphi_i - V_g)V_g, \tag{A1}$$

where $C_{i-1,i}$ is the junction capacitance between the $(i-1)$th and ith islands, and C_{gi} is the gate capacitance between the ith island and the gate electrode, φ_i is a potential of the ith island.

We can rewrite the free energy as

$$F = \tfrac{1}{2}\varphi^T A \varphi, \tag{A2}$$

by using $(N-1)$-by-$(N-1)$ matrix A given by the band matrix

$$A = \begin{bmatrix} C_{g1}+C_{01}+C_{12} & -C_{12} & & & \\ -C_{12} & C_{g2}+C_{12}+C_{23} & 0 & & \\ & \ddots & & & \\ & 0 & C_{gN-2}+C_{N-3,N-2}+C_{N-2,N-1} & -C_{N-2,N-1} & \\ & & -C_{N-2,N-1} & C_{gN-1}+C_{N-2,N-1}+C_{N-1,N} \end{bmatrix}, \tag{A3}$$

and $(N-1)$ column vector φ given by

$$\varphi = \begin{bmatrix} \varphi_1 \\ \vdots \\ \varphi_{N-1} \end{bmatrix}. \tag{A4}$$

On the one hand, from the charge conservation law we get the following equation:

$$C_{i,i+1}(\varphi_i - \varphi_{i+1}) + C_{i-1,i}(\varphi_i - \varphi_{i-1}) + C_{gi}(\varphi_i - V_g) = -en_i. \tag{A5}$$

Here, we neglected the background charge so that an island has integral number of electrons. Using the matrix A defined in Eq. (A3) and φ defined in Eq. (A4), Eq. (A5) leads to

$$A\varphi = \begin{bmatrix} -en_1 + C_{g1}V_g \\ \vdots \\ -en_{N-1} + C_{gN-1}V_g \end{bmatrix}. \tag{A6}$$

Substituting the Eq. (A6) into Eq. (A2), we obtain the following expression:

$$F = \frac{1}{2}[-en_1 + C_{g1}V_g \ \cdots \ -en_{N-1} + C_{gN-1}V_g]A^{-1} \times \begin{bmatrix} -en_1 + C_{g1}V_g \\ \vdots \\ -en_{N-1} + C_{gN-1}V_g \end{bmatrix}. \tag{A7}$$

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