Interface trap and oxide charge generation under negative bias temperature instability of *p*-channel metal-oxide-semiconductor field-effect transistors with ultrathin plasma-nitrided SiON gate dielectrics

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(Received 3 August 2005; accepted 26 October 2005; published online 9 December 2005)

The interface trap generation (ΔN_{it}) and fixed oxide charge buildup (ΔN_{ot}) under negative bias temperature instability (NBTI) of *p*-channel metal-oxide-semiconductor field-effect transistors (*p*MOSFETs) with ultrathin (2 nm) plasma-nitrided SiON gate dielectrics were studied using a modified direct-current–current-voltage method and a conventional subthreshold characteristic measurement. Different stress time dependences were shown for ΔN_{it} and ΔN_{ot}. At the earlier stress times, ΔN_{it} dominates the threshold voltage shift (ΔV_{th}) and ΔN_{ot} is negligible. With increasing stress time, the rate of increase of ΔN_{it} decreases continuously, showing a saturating trend for longer stress times, while ΔN_{ot} still has a power-law dependence on stress time so that the relative contribution of ΔN_{ot} increases. The thermal activation energy of ΔN_{it} and the NBTI lifetime of *p*MOSFETs, compared at a given stress voltage, are independent of the peak nitrogen concentration of the SiON film. This indicates that plasma nitridation is a more reliable method for incorporating nitrogen in the gate oxide. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2138372]

I. INTRODUCTION

The negative bias temperature instability (NBTI) of *p*-channel metal-oxide-semiconductor field-effect transistors (*p*MOSFETs) is a critical reliability issue for state-of-the-art ultralarge-scale integration circuits, and it is becoming even more critical as the gate dielectric thickness is further scaled down and nitrogen is incorporated in the gate oxide.[1] The degradation of device parameters (e.g., threshold voltage, transconductance, saturation current, and leakage current) is widely accepted to be caused by interface trap (including fast-state interface trap $Si_3 \equiv Si\bullet$ and slow-state interface trap $O_3 \equiv Si\bullet$) generation (ΔN_{it}) and/or fixed oxide charge buildup (ΔN_{ot}) due to the dissociation of Si–H bonds at or near the SiO_2/Si interface and to the diffusion of broken H-related species (X):[2–4]

$$Si_3 \equiv Si\text{–}H + h^+ \leftrightarrow Si_3 \equiv Si\bullet + X_{interface}, \tag{1}$$

$$O_3 \equiv Si\text{–}H + h^+ \leftrightarrow O_3 \equiv Si\bullet + X_{interface}, \tag{2}$$

$$X_{interface} \leftarrow (\text{diffusion}) \rightarrow X_{bulk}{}^+. \tag{3}$$

The species X diffuses into the gate dielectric and a positive charge is generated. According to this model, ΔN_{it} generated during the negative bias temperature (NBT) stress is equal to ΔN_{ot}. This prediction is confirmed by some reports in the literature, e.g., Blat *et al.* for 56 nm SiO_2 gate dielectrics[3] and, recently, Tan *et al.* for ultrathin SiO_2 and SiON gate dielectrics.[4] However, contrary observations are also reported,[5–8] e.g., absence of a correlation between ΔN_{ot} and ΔN_{it} (Refs. 5 and 6) or negligible ΔN_{ot} as compared to ΔN_{it} for ultrathin gate dielectrics.[7,8] To clarify the problem, N_{it} and N_{ot} must be measured accurately and independently. Conventionally, ΔN_{ot} is monitored using a midgap voltage (V_{mg}) shift to be extracted from a *I-V* (Ref. 4) or *C-V* (Ref. 5) measurement. However, as described below, obtaining an accurate ΔV_{mg} value is difficult, especially for an ultrathin gate dielectric. Recently, a direct-current–current-voltage (DCIV) method was developed to measure ΔN_{it} from the DCIV peak height and ΔN_{ot} from the peak position shift.[9,10] The method can be used for an ultrathin gate dielectric at arbitrary temperatures after a simple modification to reduce the gate tunneling effect.[11]

On the other hand, an oxynitride (SiON) layer has been widely adopted as a gate dielectric in state-of-the-art devices to suppress boron penetration and to increase the dielectric constant. However, as has been pointed out, incorporating nitrogen in the gate oxide can reduce the NBTI activation energy[12] and/or provide more reaction sites,[4] which can be translated to a reduction in the NBTI lifetime. NBT-stress-induced ΔN_{it} and ΔN_{ot} were reported to increase significantly with increasing nitrogen concentration for NO-annealed nitrided devices.[13] Recently, plasma-nitridation was recognized to reduce the nitrogen-induced NBTI enhancement due to the removal of the nitrogen peak position from the SiO_2/Si interface.[14] However, the quantitative impact of nitrogen concentration on NBTI for plasma-nitrided dielectrics has not been reported yet.

In our research, NBT-stress-induced ΔN_{it} and ΔN_{ot} were studied using the modified DCIV method and were compared

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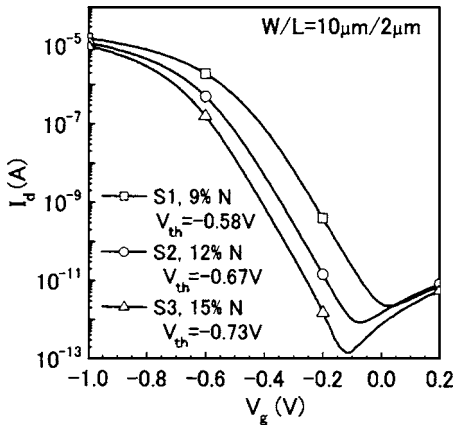

FIG. 1. Room-temperature drain-current–gate-voltage (I_d-V_g) curves for *p*MOSFETs with plasma-nitrided SiON gate dielectrics having peak nitrogen concentration of 9% (S1), 12% (S2), and 15% (S3).

with the data extracted from the conventional *I-V* method. The nitrogen concentration dependence of plasma-nitrided devices on NBTI was also studied.

II. EXPERIMENTAL DETAILS

p-channel MOSFETs with lightly doped source/drain structures and p^+-polycrystalline Si gate electrode were fabricated on *n* wells of *p*-Si(100) substrates using a standard complementary metal-oxide-semiconductor (CMOS) process.[15] Approximately 2 nm base gate-SiO_2 was formed by rapid thermal oxidization, followed by a plasma-nitridation procedure to introduce nitrogen into the oxide. The nitrogen peak is around the upper half of the SiO_2 layer toward the poly-Si/SiO_2 interface, and the concentrations are 9%, 12%, and 15% for samples 1, 2, and 3, as estimated using secondary-ion-mass-spectroscopy (SIMS) analysis.[16] The corresponding equivalent oxide thicknesses (EOT) are 2.22, 2.17, and 2.12 nm, as extracted from a 100 kHz *C-V* measurement. Devices with gate lengths of 2 μm and widths of 10 μm were tested. The I_d-V_g curves for these three samples measured at V_d=−0.1 V are shown in Fig. 1, in which the threshold voltages (V_{th}) are read to be −0.58, −0.67, and −0.73 V. The difference in V_{th} is mainly due to the boron penetration because higher nitrogen concentration can more effectively suppress the boron penetration.

During the NBT stress, the gate electrode was biased at a constant voltage, while the source, drain, and *n*-well (bulk) electrodes were grounded. The devices were kept at a temperature ranging from room temperature to 150 °C, with a stability of ±1 °C. The stress was interrupted at predetermined moments to sequentially measure the I_d-V_g and DCIV at the stress temperature.

III. RESULTS AND DISCUSSION

A. Interface trap density versus subthreshold swing

The DCIV measurements were performed by measuring the bulk current (I_b) at a forward bias of the source (drain)-well junction ($V_e=V_s=V_d>0, V_b=0$) and subsequently at zero bias ($V_e=0$) as a function of V_g, as depicted in Fig. 2(a). The modified DCIV current (I_{DCIV}) is obtained using I_{DCIV}

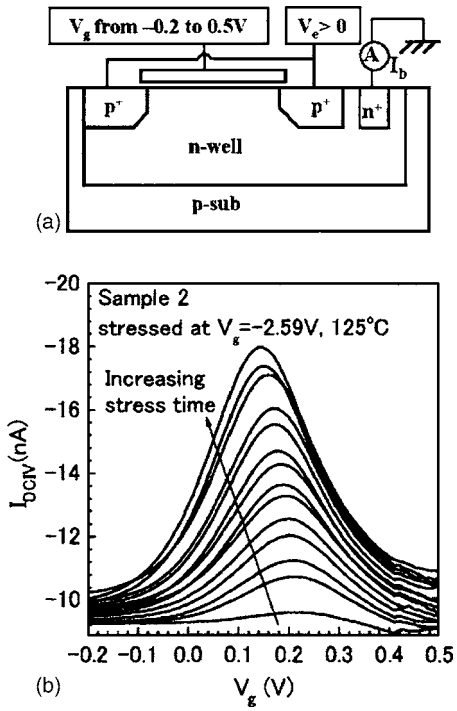

FIG. 2. (a) Configuration for DCIV measurement. (b) Modified DCIV curves of sample 2 before (fresh) and after NBT stress at V_g=−2.59 V for 10, 30, 100, 200, 400, 700, 1200, 2200, 4200, 7200, 13200, 21200, and 31200 s, stressed and measured at 125 °C.

$=I_b(V_e>0)-I_b(V_e=0)$ to reduce the direct-tunneling-current effect of the ultrathin gate dielectric.[11] Figure 2(b) shows the modified DCIV curves of sample 2 before and after NBT stress from 10 to 31 200 s, with a clear peak at a certain V_g (denoted as V_{peak}). The DCIV peak height above the base line (ΔI_{DCIV}) is approximately proportional to the effective interface trap density (N_{it}):[9,11]

$$\Delta I_{\text{DCIV}} = \frac{qN_{\text{it}}WLn_i\sigma v_{\text{th}}}{2}[\exp(qV_e/nkT) - 1], \tag{4}$$

where $\sigma=\sqrt{\sigma_n\sigma_p}$, σ_n, and σ_p are the electron and hole capture cross sections, q is the electronic charge, n_i is the intrinsic carrier concentration, v_{th} is the thermal velocity, k is Boltzmann's constant, T is the temperature in Kelvin, and n is a factor around 1.7–1.8. It has been confirmed that N_{it} extracted from the above formula is independent of the measurement temperature.[11] The NBT-stress-induced interface trap generation is calculated as

$$\Delta N_{\text{it}} = N_{\text{it}}(\text{stress}) - N_{\text{it}}(\text{fresh}). \tag{5}$$

On the other hand, the stress-induced ΔN_{it} is related to the change of the subthreshold swing (ΔS) by the following formula:[17]

$$\frac{\Delta S}{S_0} = \frac{S(\text{stressed}) - S(\text{fresh})}{S(\text{fresh})} = \frac{q\Delta N_{\text{it}}/\Delta E_{\text{it}}}{C_{\text{ox}} + C_D}, \tag{6}$$

where $S_0=S(\text{fresh})$ is the subthreshold swing before stress, C_{ox} is the gate oxide capacitance, C_D is the depletion capacitance, and ΔE_{it} is the energy width of the interface trap distribution. The corresponding I_d-V_g curves of sample 2 before and after NBT stress from 10 to 31 200 s are shown in Fig. 3.

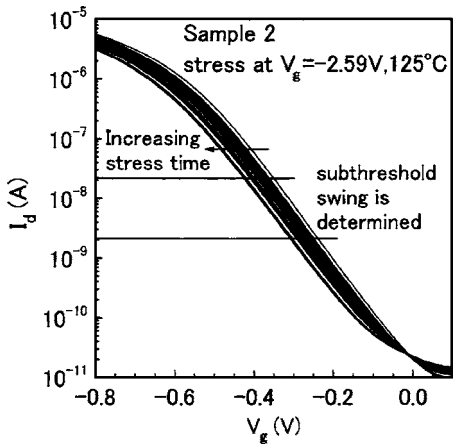

FIG. 3. I_d-V_g curves of sample 2 before (fresh) and after NBT stress (as in Fig. 2). Subthreshold swings are extracted from linear fitting in 2×10^{-9}–2×10^{-8} A region.

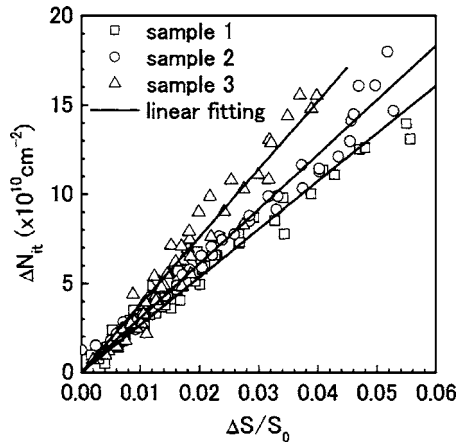

FIG. 5. Correlation between $\Delta S/S_0$ and ΔN_{it} extracted using the DCIV method for different samples stressed at 125 °C at different voltages.

The S values are extracted by linearly fitting the curves at a range of I_d between approximately 2×10^{-9} and 2×10^{-8} A. The correlation between ΔN_{it} and $\Delta S/S_0$ is almost linear, independent of the stress voltage, as shown in Fig. 4. The correlations for different samples are compared in Fig. 5. The data for each sample are dropped around a line through zero. From the slope of these lines, EOT can be estimated from C_{ox} according to Eq. (6). Here we simply assume that $\Delta E_{it}=E_g/2$ (where E_g is the Si energy gap) and C_D is independent of stress. The values are approximately 3.0, 2.6, and 2.1 nm for samples 1, 2, and 3, in rough agreement with those extracted from the C-V measurement, indicating that the ΔN_{it} value extracted from the modified DCIV measurement has a relatively high degree of accuracy.

B. DCIV peak position versus midgap voltage

Interface traps are commonly believed to be acceptorlike in the upper half of the band gap and donorlike in the lower half, so all interface traps are neutral when the Si surface Fermi level E_{Fs} is at the middle energy E_i,[1] namely, at $V_g=V_{mg}$. Therefore, the V_{mg} shift (ΔV_{mg}) is only due to the stress-induced oxide charges (ΔN_{ot}) as $\Delta N_{ot}=C_{ox}\Delta V_{mg}/q$.

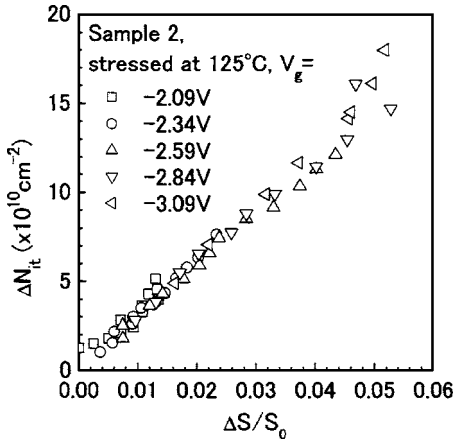

FIG. 4. Correlation between subthreshold swing change ($\Delta S/S_0$) and ΔN_{it} extracted using the DCIV method for sample 2 stressed at 125 °C and at voltages between −2.09 and −3.09 V.

Conventionally, V_{mg} can be measured from C-V (Ref. 5) or I_d-V_g curves.[4,18] Using the C-V measurement requires a relatively large area and is adversely affected by large gate leakage current of the ultrathin gate dielectric, resulting in a large experimental error for our samples. In the I_d-V_g method, the midgap current (I_{mg}) is calculated by substituting the surface potential $\Psi_s=(kT/q)\ln(N_D/n_i)$ into the subthreshold current equation:[17,18]

$$I_{mg}=\mu_{eff}\left(\frac{W}{L}\right)\frac{aC_{ox}}{2(q/kT)^2}\left(\frac{n_i}{N_D}\right)\left(1-e^{-V_Dq/kT}\right)\left(\ln\frac{N_D}{n_i}\right)^{-1/2}, \tag{7}$$

where μ_{eff} is the effective hole mobility, a is a parameter, and N_D is the channel doping concentration. When I_{mg} is calculated, the V_{mg} value can be read from the extrapolation of the linear fitting of the $\log(I_d)$ vs V_g curves (Fig. 3).[18] The difficulty of the method is to estimate the μ_{eff} value because it depends on the interface trap density N_{it}. In this paper, an ideal μ value (approximately 400 cm^2/V s) is used without taking the N_{it} effect into account for simplicity; thus systematic error is expected for the estimated V_{mg} value.

In the DCIV measurement, the electron-hole recombination at the SiON/Si interface reaches a maximum at which $\sigma_nN_s\approx\sigma_pN_p$, where N_s and P_s are the surface concentrations of the electrons and holes.[10,19] Because $\sigma_n\approx\sigma_p$, V_{peak} corresponds to the case where $N_s\approx P_s$, namely, E_{Fs} is close to E_i at V_{peak}. Therefore, the shift of ΔV_{peak} is mainly due to the oxide charges. Note that V_{peak}, which is dependent on V_e, is different from V_{mg}, which corresponds to the case where $V_e=(=V_s=V_d)=0$ because the channel potential is modified by the source/drain bias V_e during the DCIV measurement.

The relationship between ΔV_{peak} and ΔV_{mg} is shown in Fig. 6. All data are dropped roughly around the line of $\Delta V_{peak}=\Delta V_{mg}$. The relatively large deviation arises from the uncertainty of I_{mg} as mentioned above and from the broad DCIV peak as shown in Fig. 2 due to the interface trap spatial and energy-level distributions.[10] Nevertheless, ΔV_{peak} can be used as a rough, simple, and direct indicator of the stress-induced oxide charges.

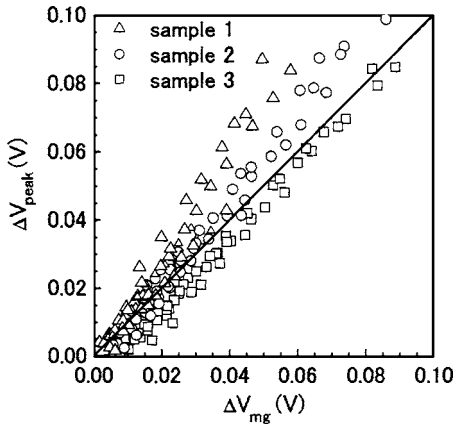

FIG. 6. Correlation between midgap voltage shift (ΔV_{mg}) extracted from I_d-V_g curves and DCIV peak position shift (ΔV_{peak}) for different samples stressed at 125 °C at different voltages.

C. Time evolutions of ΔV_{th}, ΔN_{it}, and ΔV_{peak}

The evolution of ΔV_{th} over time for sample 2 stressed at different voltages is shown in Fig. 7. V_{th} is read from the I_d-V_g curves (Fig. 3) with a criterion of I_d=0.5 μA. Consistent with other reports, ΔV_{th} has a power-law dependence on stress time,[2]

$$\Delta V_{th} = Ct^n, \tag{8}$$

where C and n are fitting parameters. By linearly fitting the experimental data, the exponent n under low V_g stresses is found to be around 0.24. At a stress of −3.1 V, n is slightly large (0.26) at the earlier stress times, and then the slope decreases, showing a saturation effect after longer stress times.

The corresponding ΔN_{it} time evolutions for sample 2 are shown in Fig. 8. They follow the power-law dependence at stress times less than approximately 1000 s, with n around 0.29. The slope continues to decrease with increasing stress time. With increasing $|V_g|$, the deviation from the power-law dependence starts at earlier stress times. This saturation trend at the longer stress times can be explained by the finite Si–H bond number at the SiO_2/Si interface and the distribution of Si–H bond energies. Based on this assumption, the interface trap generation can be approximately expressed as[20]

$$\Delta N_{it} = N_{it\text{-}max}\left(1 - \frac{1}{1 + (t/\tau)^{\alpha}}\right), \tag{9}$$

where $N_{it\text{-}max}$, τ, and α are fitting parameters, and all depend on V_g (or the oxide field E_{ox}). The experimental data can be perfectly fitted in the whole stress region using Eq. (9), as shown in Fig. 8.

The DCIV peak shift ΔV_{peak} as a function of stress time and the fitting lines based on Eq. (8) are shown in Fig. 9. The exponent n is around 0.27. At the earlier stress times under low V_g stresses, ΔV_{peak} is much smaller than that predicted by the power-law dependence. With increasing stress time, it follows the power-law dependence, and the saturation effect occurs at the longer stress times of the −3.1 V stress. The same is true for ΔV_{th}.

The other two samples show similar ΔV_{th}, ΔN_{it}, and ΔV_{peak} time evolution behaviors. Based on the above findings, the NBTI scenario can be briefly described as follows. In the earlier stress stages, ΔN_{it} follows the power-law dependence while ΔN_{ot} is negligible, and not all the released species X seem to form positive charges during reactions (1) and (2). With increasing stress time, the generation rate of

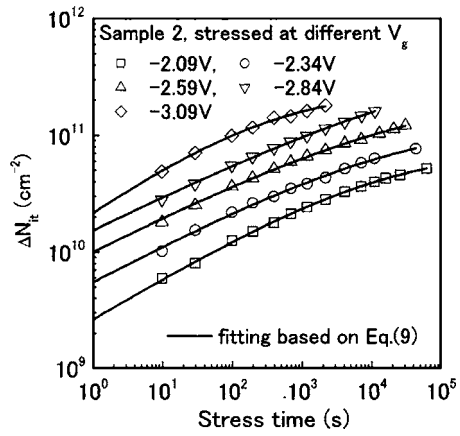

FIG. 8. Stress time evolution of interface trap generation (ΔN_{it}) for sample 2 stressed at 125 °C at different voltages. Fitting lines are based on Eq. (9).

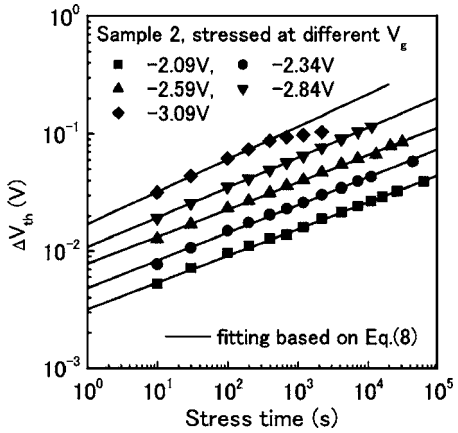

FIG. 7. Stress time evolution of threshold voltage shift (ΔV_{th}) for sample 2 stressed at 125 °C at different voltages and linear fitting based on assumption of the power-law dependence [Eq. (8)].

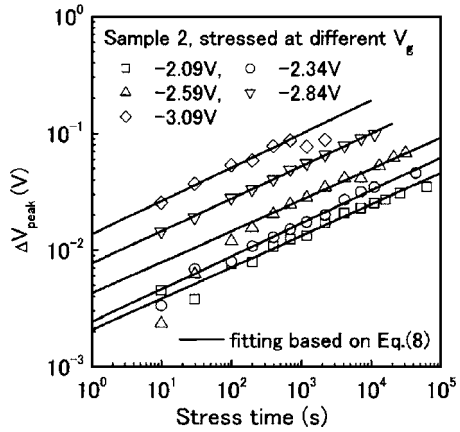

FIG. 9. Stress time evolution of DCIV peak position shift (ΔV_{peak}) for sample 2 stressed at 125 °C at different voltages and linear fitting based on Eq. (8).

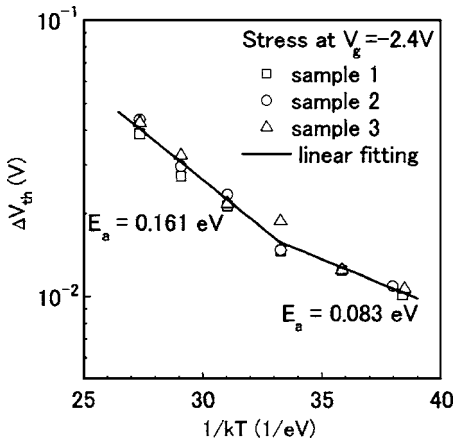

FIG. 10. Stress temperature dependence of ΔV_{th} for *p*MOSFETs with different nitrogen concentrations stressed at V_g=−2.4 V for 1000 s. Activation energy E_a is extracted from linear fitting at two ranges.

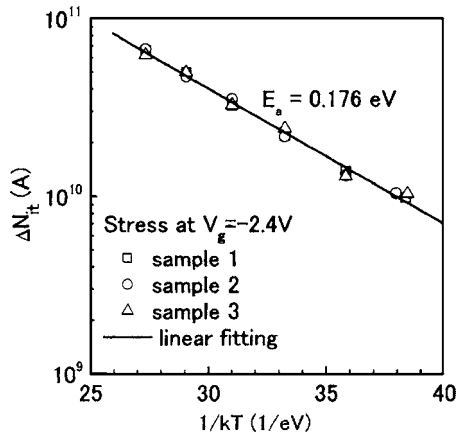

FIG. 11. Stress temperature dependence of ΔN_{it} for *p*MOSFETs with different nitrogen concentrations stressed at V_g=−2.4 V for 1000 s. E_a is extracted from linear fitting.

ΔN_{it} declines continuously, showing a saturation trend at the longer stress times, while ΔN_{ot} still follows the power-law dependence, so the relative contribution of ΔN_{ot} to ΔV_{th} increases. The ΔN_{it} saturation effect can be explained by the limited number of Si–H bonds at the SiO_2/Si interface and the distribution of the Si–H activation energy,[20] and may also be ascribed to the gradual decrease of electrical field at the oxide/Si interface due to a positive charge buildup in the oxide and to the gradual increase in favorability of the reverse reaction (1) due to increasing N_{it}.[21] Increasing $|V_g|$ can increase the consumption rate of the Si–H bonds so that the ΔN_{it} saturation appears at an earlier stress time. The delay of the ΔN_{ot} saturation as compared to that of ΔN_{it} may be attributed to the continuous dissociation of $O_3{\equiv}Si$–H bonds in the oxide far from the interface even after the interfacial Si–H bonds have been substantially consumed. Because these $O_3{\equiv}Si\bullet$ defects can be positively charged by capturing holes or H^+ and the trapped charges cannot communicate with Si surface carriers by tunneling, the defects behave as fixed oxide charges, not as slow-state interface traps. When the $O_3{\equiv}Si$–H bonds in the SiO_2 layer are mostly consumed, ΔN_{ot} becomes saturated.

D. Nitrogen concentration dependence

The temperature dependence of ΔV_{th} for devices with various peak nitrogen concentration and their corresponding ΔN_{it} temperature dependences are shown in Figs. 10 and 11. The devices were stressed at V_g=−2.4 V for 1000 s. For ΔN_{it}, the Arrhenius plots show good linearity, and the thermal activation energy (E_a) can be extracted as 0.176 eV. On the other hand, the linearity of ΔV_{th} is quite poor. There seems to exist two E_a's: approximately 0.083 eV at low temperatures and approximately 0.161 eV at high temperatures. The latter and E_a of ΔN_{it} are similar to those reported in literature.[4,12] The different E_a values were also observed by Huard *et al.* They reported that E_a of ΔV_{th} is 0.063 eV and that of ΔN_{it} is 0.156 eV.[20] Our E_a result implies that the interface trap generation dominates in the high-temperature range, while the positive charge creation due to hole trapping and/or X^+ species diffusion into the dielectric dominates in the low-temperature range because it has lower activation energy.

The lifetime of devices as a function of the stress voltage V_g is shown in Fig. 12. The lifetime is defined using a criterion of ΔV_{th}=50 mV. Contrary to our expectation, the lifetime at a given V_g and the above E_a values seem to be independent of the nitrogen concentration or, at least, the NBTI enhancement due to the increase of the peak nitrogen concentration from 9% to 15% is under the measurement limit. As has been pointed out, the NBTI enhancement is mainly induced by interfacial nitrogen, rather than by nitrogen in the bulk dielectric.[4,12] The absence of nitrogen dependence for our plasma-nitrided samples may arise from the fact that the peak nitrogen concentration is around the upper half of the dielectric, so the difference in the interfacial nitrogen concentration at the SiON/Si interface is quite small for these three samples, as observed in the SIMS analysis.[16] Therefore, the nitrogen concentration in the plasma-nitrided SiON layer can be further increased without sacrificing the NBTI lifetime.

IV. CONCLUSION

The modified DCIV method is used to monitor and separate the time evaluation of NBT-stress-induced interface

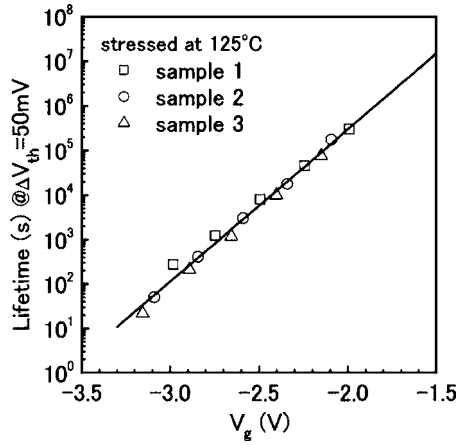

FIG. 12. Lifetime of *p*MOSFETs with different nitrogen concentrations as function of stress voltage V_g. Lifetime is defined as stress time when ΔV_{th} reaches 50 mV.

traps and oxide charges of *p*-MOSFETs with ultrathin gate dielectrics. During the NBT stress, ΔN_{ot} is not linearly related to ΔN_{it}. At the earlier stress times, ΔN_{it} dominates, and at the longer stress times, it deviates from the power-law dependence in time, showing a saturation effect. Increasing the nitrogen concentration of the plasma-nitrided SiON gate dielectric from 9% to 15% has not detectably enhanced the NBTI, while the suppression of boron penetration and the EOT reduction have been significantly improved, indicating that plasma nitridation is a superior method to fabricate the SiON gate dielectric in the viewpoint of NBTI reliability.

ACKNOWLEDGMENT

This study was supported in part by the 21st Century COE program "Nanoelectronics for Tera-Bit Information Processing" of the Ministry of Education, Culture, Sports, Science and Technology.

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