Abnormal enhancement of interface trap generation under dynamic oxide field stress at MHz region

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By stressing metal-oxide-semiconductor field-effect transistors with ultrathin silicon dioxide or oxynitride gate dielectrics under square wave form voltage at the MHz region, an abnormal enhancement of interface trap generation in the midchannel region has been observed at some special frequencies. A hypothesis, including self-accelerating interface trap generation originated from the positive feedback of a charge pumping current to be contributed by the stress-induced near-interface oxide traps and a resonant tunneling via the near interface oxide trap states at those frequencies, is proposed to explain the observed phenomenon. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1857083]

Devices under ac stresses may display different degradation behaviors as compared to those under dc stresses.[1–6] It has been found that the trap generation and trapping rates in thin gate oxide films is reduced[1] and the time to breakdown (t_{BD}) is enhanced significantly under bipolar stress.[2,3] On the other hand, the interface trap generation (ΔN_{it}) under dynamic stresses has been observed to be frequency dependent.[3–6] However, the frequency dependences reported in literature are controversial. For example, Rosenbaum *et al.*[4] observed that ΔN_{it} under bipolar stress increases first and then decreases with stress frequency with a maximum at around 2 kHz, while Chen *et al.*[5] reported that ΔN_{it} is essentially independent of frequency at frequencies less than 30 kHz and increases with frequency at frequencies larger than 30 kHz. We also found similar frequency enhancement at high frequencies, but the enhancement of ΔN_{it} saturates or decreases at the MHz region (10^6–10^7 Hz).[6] The above disagreements may be attributed to the differences in the geometry of tested devices (e.g., the gate oxide thickness, the channel width/length ratio, etc.), the stress setup,[7] the wave form of stress voltage (e.g., the rise and fall times) etc. Furthermore, the step of stress frequency in previous studies is usually quite large (normally one order of magnitude). Therefore, information near the "turn-around" frequency may be lost. In this letter, a fine frequency dependence at the MHz region was studied with a step of 1 MHz. An abnormal enhancement of interface trap generation occurs at some special frequencies, resulting in a dramatic decrease of t_{BD} at those frequencies.

Polycrystalline silicon gate *n*-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) with a lightly doped-drain structure fabricated by a standard process were tested in our studies. Gate dielectrics are pure or plasma-nitrided SiO_2 films with a base SiO_2 thickness of 2.34 nm or 3.48 nm. The devices were stressed by applying a square wave form voltage with a duty factor of 50% and the rise and fall time of less than 8 ns on the gate electrode while the substrate, drain, and source were grounded. The substrate current (I_{bulk}) was monitored during stress. Before and after stress, the interface trap density (N_{it}) in the midchannel region was measured using a recently developed direct-current current-voltage (DCIV) method.[8,9] which requires smaller measurement voltage and is easier for N_{it} extraction than the conventional charge pumping method. A close correlation between the DCIV peak, the threshold voltage shift, and the transconductance degradation has been observed.[6]

Figure 1 shows the frequency dependence of interface trap generation ($\Delta N_{it} = N_{it}(\text{stressed}) - N_{it}(\text{fresh})$) after bipolar and unipolar (positive and negative) stresses between 1 and 20 MHz for two typical samples with [Fig. 1(a)] 2.34 nm pure SiO_2 and [Fig. 1(b)] 3.48 nm oxynitride with nitrogen concentration of 12%. Three peaks of ΔN_{it} can be identified at the frequencies of 5, 9, and 15 MHz on almost frequency-independent baseline ΔN_{it}, with higher peak at higher frequencies. All other devices with different nitrogen concentrations, equivalent oxide thickness (EOT), and channel width/length ratio show similar abnormal ΔN_{it} enhancement at the same frequency positions. The peak position is independent of the device geometry as well as the amplitude (V_a) and polarity of the stress voltage. The ΔN_{it} peak increases sharply as V_a increases, resulting in an abnormal reduction of t_{BD} at those frequencies (not shown). For the sample of Fig. 1(b), t_{BD} is about 71 s at 15 MHz bipolar stress, and is much shorter than those stressed at other frequencies. Here, the breakdown is identified as the suddenly increasing of I_{bulk} during stress, and no DCIV peak can be detected after breakdown due to the overwhelming source (drain) junction current.

Figure 2 compared the stress time evolution of ΔN_{it} under dynamic stresses at 15 MHz and under dc stresses. All of them obey a power law with a quite close exponent, i.e., ~0.40 for negative polarity (unipolar and dc), ~0.34 for positive polarity, and a value between them (~0.38) for the bipolar stress, implying that the dynamics of ΔN_{it} generation at 15 MHz dynamic stresses may be similar to that at dc stresses. The larger than 0.25 exponent suggests that the in-

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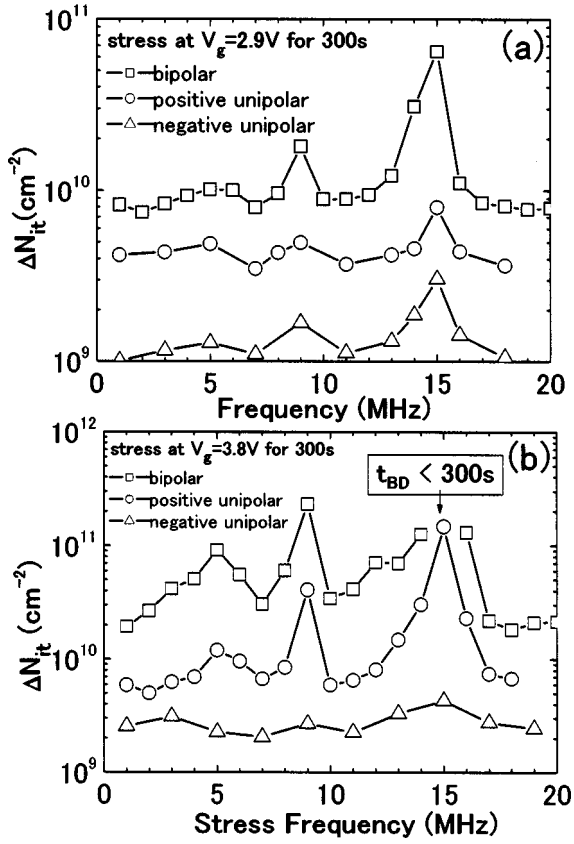

FIG. 1. Frequency dependence of interface trap generation under MHz dynamic stress of two types of *n*-MOSFETs; (a) Pure SiO_2 with EOT of 2.34 nm, channel width/length $(W/L)=10\ \mu m/10\ \mu m$, and $V_a=2.9$ V, and (b) plasma-nitrided SiO_2 with EOT of 2.94 nm, $W/L=10\ \mu m/10\ \mu m$, and $V_a=3.8$ V. The duty factor of the stress wave form is 50% and the stress time is 300 s.

terface trap generation is reaction limited according to the reaction-diffusion model.[10] The larger exponent of negative polarity indicates that the negative voltage stress may generate interface traps more effectively.[5]

The enhancement of ΔN_{it} under bipolar stress at high frequencies has been attributed to a contribution of recombination of trapped electrons with holes from the substrate, which is identified as a charge pumping current (I_{CP}).[6] Figure 3 shows average I_{bulk} at the first 10 s of stress as a function of

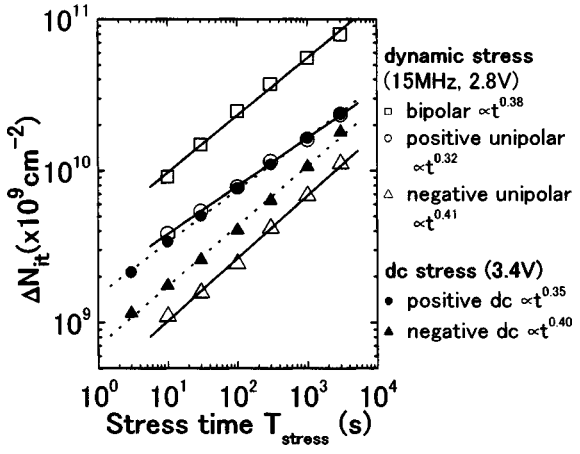

FIG. 2. Stress time (T_{stress}) evolution of interface trap density induced by dynamic stresses at 15 MHz (bipolar, positive, and negative unipolar) and dc stresses. They obey a power law with an exponent between 0.32 and 0.41.

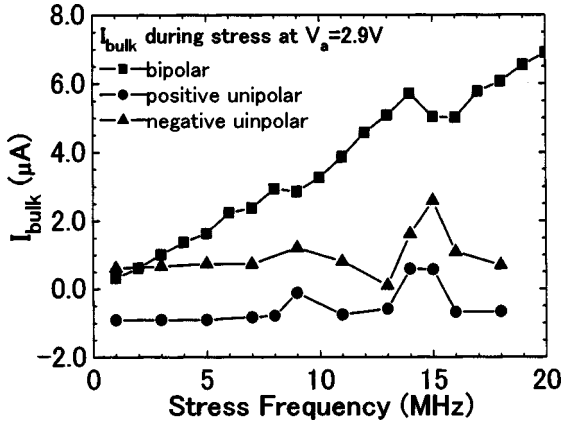

FIG. 3. Bulk current (I_{bulk}) during stress as a function of frequency. I_{bulk} is averaged from the values measured at first 10 s during stress.

frequency. I_{bulk} includes the average dc tunneling currents and I_{CP} [$\propto \Delta F(f)\cdot f$, where f is a stress frequency and $\Delta F(f)$ is a filling factor] to be contributed by both interface states (fast states, $I_{CP\text{-}FS}$) and near-interface states (slow states, $I_{CP\text{-}SS}$).[11] Except at frequencies around 9 and 15 MHz, I_{bulk} of bipolar stress is almost linearly proportional to the frequency, while that of unipolar stresses is almost independent of frequency. Notice that at the frequency range used here, $I_{CP\text{-}FS}$ still depends on frequency linearly, while $I_{CP\text{-}SS}$ becomes almost frequency independent[11] because the filling factor of slow states decreases at a much lower frequency ($\sim$1 MHz) than that of fast states. It reflects that $I_{CP\text{-}FS}$ is the dominant component of I_{bulk} at the bipolar stress, while $I_{CP}(=I_{CP\text{-}FS}+I_{CP\text{-}SS})$ is negligible at the unipolar stress because the voltage swing (V_{SW}) is not large enough for I_{CP} in the unipolar stress cases. However, the baseline of ΔN_{it} for bipolar stress in Fig. 1 (except the abnormal ΔN_{it} enhancement around 5, 9, and 15 MHz) does not display frequency dependence. It suggests that the ΔN_{it} enhancement is mainly induced by $I_{CP\text{-}SS}$, rather than $I_{CP\text{-}FS}$ (Ref. 6) even though $I_{CP\text{-}SS}$ is much smaller than $I_{CP\text{-}FS}$. We suspect that the abnormal increase of ΔN_{it} in Fig. 1 and the fluctuations of I_{bulk} around 9 and 15 MHz in Fig. 3 are both closely correlated and may also be attributed to $I_{CP\text{-}SS}$. Similar oscillations of the dJ_{Sub}/df versus f curves have also been observed in Fig. 7 of Ref. 12 at the 10^6–10^7 Hz range, but the authors just ignored this phenomenon. The absence of I_{bulk} peak at 5 MHz may be simply due to the fact that $I_{CP\text{-}SS}$ at 5 MHz is too small to be distinguished as the ΔN_{it} peak at 5 MHz is also much smaller than that at 9 and 15 MHz.

Figure 4 shows I_{bulk} during bipolar stresses at 13, 15, and 17 MHz, respectively. At the beginning of stress, I_{bulk} at 15 MHz is between those of 13 and 17 MHz, as shown in Fig. 3. However, I_{bulk} at 15 MHz increases with stress time much faster than that at the nearby frequencies. I_{bulk} displays a peak at 15 MHz after a sufficient stress period. It reflects a strong self-accelerating mechanism of ΔN_{it} at 15 MHz, namely, the higher stress-induced-interface traps results in a higher I_{CP}, and the larger I_{CP} creates more interface traps. Such a strong positive feedback process results in the abnormal increase of ΔN_{it} and the dramatic decrease of t_{BD} at those special frequencies.

The onset of the strong self-acceleration of ΔN_{it} and $I_{CP\text{-}SS}$ at 5, 9, and 15 MHz is not as easily understood. It is suspected to be correlated to resonant tunneling via near-

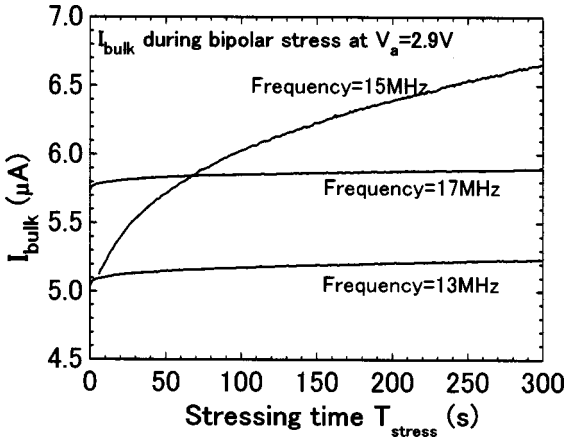

FIG. 4. Stress time (T_{stress}) evolution of I_{bulk} during bipolar stress at 13, 15, and 17 MHz.

interface states.[13,14] As is well known, at the dynamic stress with a square voltage wave form, inversion electrons from the source/drain are able to tunnel into the near-interface oxide states during the time interval of positive V_a (inversion phase of the Si surface) and the trapped electrons are able to tunnel back and to recombine with substrate holes during the time interval of negative V_a (accumulation phase of the Si surface), resulting in $I_{\text{CP-SS}}$.[11,12,15] These trap states are assumed to be strongly localized, namely, enclosed by high barrier surroundings, hence they behave as eigenstates of their energy wells.[13] Electron tunneling through an energy barrier between the Si surface and the trap states has its owner eigenfrequencies, which is mainly determined by the barrier height, the distance from Si surface, and the eigenstate of the well. A resonant tunneling may occur if the frequency of the applied stress is in consonance with the eigenfrequency of tunneling. Therefore, the onset of resonant tunneling is independent of the oxide thickness, the nitrogen concentration, the device geometry, and the applied V_a, while it is sensitive to the applied wave form. It is expected that the variation of the rise (t_r) and/or fall time (t_f) of the stress wave form will alter the resonant behavior. We actually observed that the enhancement of ΔN_{it} is reduced as t_r and/or t_f of the square wave form increased, and no abnormal ΔN_{it} enhancement exists under a sinusoidal wave form stress at the MHz region due to the reduction and absence of the interval time $[(T-t_r-t_f)/2]$; here, T is the stress period.

In summary, interface trap generation in the midchannel region of standard MOSFETs is enhanced under the dynamic stress of high frequencies, attributed to the charge pumping current to be contributed by near-interface states. At some special frequencies in the MHz region, an abnormal enhancement of ΔN_{it} occurs due to resonant tunneling between the Si surface and the near-interface states. Special caution is necessary to ensure sufficient device reliability in practical use at MHz frequencies.

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