Atomic-layer-deposited silicon-nitride/SiO_2 stacked gate dielectrics for highly reliable *p*-metal–oxide–semiconductor field-effect transistors

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An extremely thin (~0.4 nm) silicon-nitride layer has been deposited on thermally grown SiO_2 by an atomic-layer-deposition (ALD) technique. The boron penetration through the stacked gate dielectrics has dramatically been suppressed, and the reliability has been significantly improved, as confirmed by capacitance–voltage, gate-current–gate-voltage, and time-dependent dielectric-breakdown characteristics. The ALD technique allows us to fabricate an extremely thin, very uniform silicon-nitride layer with atomic-scale control. © *2000 American Institute of Physics.* [S0003-6951(00)00544-1]

One of the important challenges for deep submicron complementary metal–oxide–semiconductor (CMOS) technology is the suppression of boron penetration through thin gate oxides in *p*-metal–oxide–semiconductor field-effect transistors (MOSFETs). Oxynitride is thought to be a promising candidate for the gate insulator of the deep submicron *p*-MOSFETs. However, typical high-thermal budget in oxynitridation processes results in nitrogen incorporation at the SiO_2/Si interface, leading to degradation of device performance, i.e., reduction of the channel mobility.[1] Also, oxynitride cannot eliminate the boron penetration into the insulator layer, which leads to the reliability degradation.[2,3] Therefore, it is desirable to introduce the nitride layer only at the polycrystalline-Si/insulator interface. Only a few methods have been proposed for such a precise N-atom-profile control up to now.[4–7] Recently, we have developed a technique for N-atom-profile engineering by employing self-limiting atomic-layer deposition (ALD) of silicon nitride.[8–10] In this study, we have fabricated metal–oxide–semiconductor (MOS) diodes with a very thin ALD silicon-nitride layer on the top of gate SiO_2 and reliability enhancement has been demonstrated.

The MOS capacitors have been fabricated using *n*-type Si(001) wafers (10 Ω cm). After the growth of 2.0–3.0-nm-thick gate oxides, the silicon-nitride layer was deposited by alternately supplying $SiCl_4$ and NH_3 gases. The $SiCl_4$ exposure at 375 °C followed by NH_3 exposure at 550 °C was cyclically repeated five times, leading to a silicon-nitride physical thickness of ~0.4 nm (~2 ML), as estimated from ellipsometry and the accumulation capacitance of the MOS diodes. The gas pressure of $SiCl_4$ and NH_3 during the deposition was 170 and 300 Torr, respectively. The substrate temperature was changed by a computer synchronized with the gas-supply sequence. After the ALD silicon-nitride deposition, a 200-nm-thick polycrystalline-Si gate was formed by 20 keV BF_2^+-ion implantation at a dose of $5\times10^{15}\,cm^{-2}$. Subsequently, the activation annealing was performed at 1000 °C for 10 or 40 s in a N_2 ambient.

Figure 1 shows the angle-resolved x-ray photoelectron spectroscopy (XPS) spectra of the N_{1s} core level for the ALD silicon-nitride/SiO_2 stacked gate dielectrics. The ''take-off angle'' is the angle between the wafer plane and the analyzer axis and was taken as 5°, 10°, and 30°. In each spectrum, the intensity of N_{1s} was normalized using the O_{1s} peak intensity. It is seen that the intensity of the N_{1s} peak increases with decreasing the take-off angle. Since the smaller take-off angle enhances the surface sensitivity more, this result suggests that the nitrogen bonds are not located uniformly in the gate-oxide layer or closer to the SiO_2–Si substrate interface, but rather on top of the surface of the dielectrics.

The surface microroughnesses measured using atomic-force microscopy (AFM) are shown in Fig. 2 for the samples before and after the ALD of silicon nitride on the gate oxide. For comparison, we also measured the surface of silicon nitride deposited on the gate oxide using conventional low-pressure chemical-vapor deposition (LPCVD) at 750 °C. Here, the thickness of the LPCVD silicon nitride (0.3 nm from ellipsometry) is almost the same as that of the ALD silicon nitride (~0.4 nm). As shown in Fig. 2 the surface microroughness of the ALD silicon nitride was almost the same as that of the underlying gate oxide. The average surface roughness (R_a) is 0.030 and 0.031 nm for the samples before and after the ALD, respectively. In contrast, the surface microroughness of the sample of the LPCVD silicon nitride ($R_a=0.043$ nm) is much larger than the former two. This increased surface microroughness of the LPCVD silicon nitride is probably ascribed to three-dimensional nucleation growth. This indicates that the ALD silicon nitride has an advantage concerning surface microroughness control, especially when a few monolayers of silicon nitride are deposited on ultrathin SiO_2 surfaces.

Figure 3 shows capacitance–gate voltage (C–V) characteristics of p^+-polycryatalline-Si gate capacitors. Measurements were carried out at 1 kHz [except for the closed diamonds in Fig. 3(b)]. The SiO_2 thickness is 2.0 nm for the no-ALD samples. The equivalent oxide thickness (T_{eff}) of the ALD samples is 2.2 nm. As seen in Fig. 3(a), the C–V

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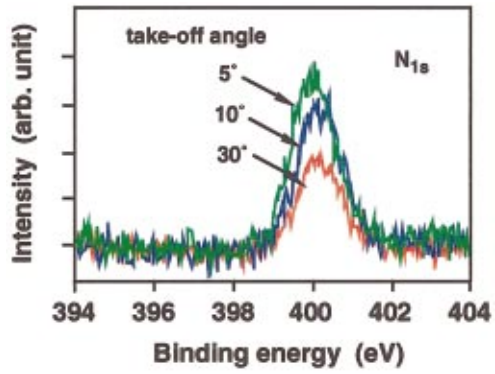

FIG. 1. (Color) Angle-resolved x-ray photoelectron spectroscopy (XPS) spectra of the N_{1s} core-level signal relative to the O_{1s} spectrum for the ALD silicon nitride on top of a 3.0-nm-thick gate oxide.

curve for the no-ALD sample annealed at 1000 °C for 10 s shows a small shift to a positive voltage side by approximately 0.05 V with respect to the capacitor with ALD silicon nitride on SiO_2. Compared with the calculated C–V curve as determined from the substrate and gate electrode doping levels, there is a small deviation of the C–V curve for the ALD sample annealed at 1000 °C for 10 s. This is probably due to the interface traps. The positive shift of the no-ALD sample is ascribed to the boron penetration to the substrate.[11] In Fig. 3(b), a significant flatband voltage shift (0.70 V) is observed for the no-ALD sample annealed at 1000 °C for a longer time (40 s) compared with the ALD sample (flatband voltage shift of 0.25 V) of the same annealing condition (at 1000 °C for 40 s), which clearly indicates the suppression of boron diffusion in the ALD sample. For the no-ALD sample annealed at 1000 °C for 40 s, the measurement at 100 kHz was also carried out. From the frequency dependence, the tail of the curve at 1 kHz in the low-gate-voltage region (0.5–1.7 V) is ascribed to the interface traps.

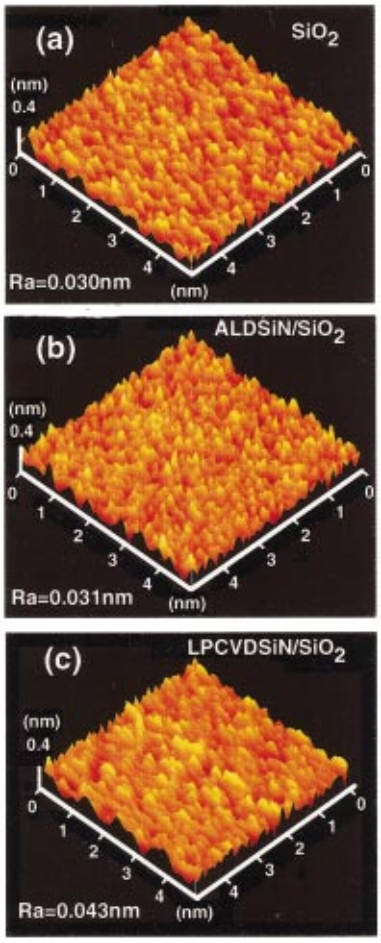

FIG. 2. (Color) Atomic-force microscopy (AFM) image for (a) the SiO_2 surface (average surface roughness $R_a=0.030$ nm), (b) ALD silicon nitride ($R_a=0.031$ nm), and (c) LPCVD silicon nitride ($R_a=0.043$ nm). The thickness of the ALD layer is ~0.4 nm from ellipsometry and the accumulation capacitance of the MOS capacitors. The thickness of the LPCVD silicon nitride is 0.3 nm from ellipsometry.

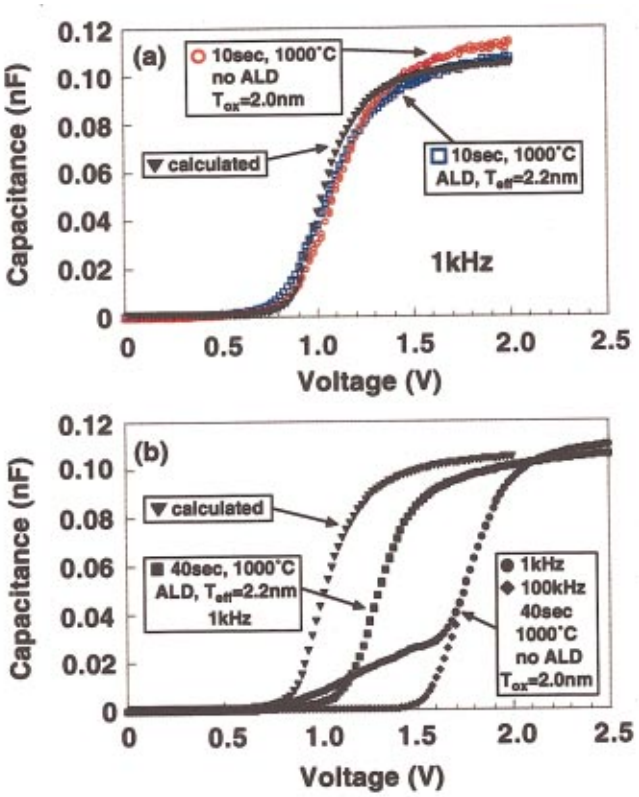

FIG. 3. (Color) Capacitance–voltage (C–V) characteristics at 1 kHz for p^+-poly-Si gate MOS capacitors annealed at 1000 °C for 10 s (a) and 40 s (b) in a N_2 ambient. The SiO_2 thickness is 2.0 nm (form ellipsometry) for both no-ALD samples. The equivalent oxide thickness (T_{eff}) of the ALD silicon-nitride/SiO_2 stacks is 2.2 nm. Calculated C–V curves are also shown assuming no boron penetration in the gate insulator. For the no-ALD sample annealed at 1000 °C for 40 s (b), the 100 kHz C–V curve is also shown.

Figure 4 shows the tunnel current measured as a function of electric field through the gate stack dielectrics of MOS capacitors annealed at 1000 °C for 40 s. The SiO_2 thickness is 2.0 nm from ellipsometry for the no-ALD sample. The T_{eff} of the ALD sample is 2.2 nm. In the ALD sample, the tunnel current is suppressed compared with that of the no-ALD sample at the same electric field, indicating a significant decrease in the gate leakage current for the ALD sample. The extent of current suppression for the ALD sample is larger than that expected for the SiO_2 layer with the same equivalent oxide thickness, owing to the larger physical thickness of the ALD sample. For instance, the tunnel current for the ALD sample with $T_{eff}=2.2$ nm is 2×10^{-3} A/cm^2 at an effective oxide field of 5 MV/cm in Fig. 4 and is almost the same as that through the gate oxide with $T_{ox}=2.4$ nm.[12] Also, it is seen that the electric-field strength where the dielectric breakdown occurs is larger for the ALD sample than

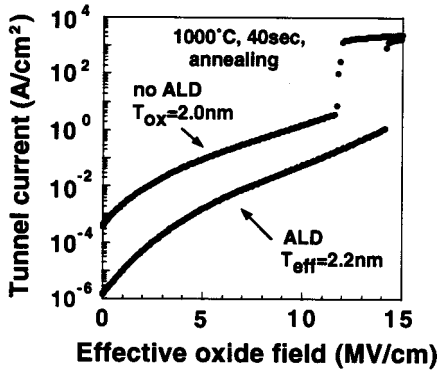

FIG. 4. Tunnel current measured as a function of electric field through the gate dielectrics of MOS capacitors annealed at 1000 °C for 40 s in a N_2 ambient. The samples are the same as shown in Fig. 3. The SiO_2 thickness is 2.0 nm for the no-ALD sample. The equivalent oxide thickness (T_{eff}) of the ALD sample is 2.2 nm.

that for the no-ALD sample, indicating the improved reliability for the ALD sample.

Figure 5 shows the time-dependent dielectric-breakdown characteristics of the MOS capacitors annealed at 1000 °C for 40 s, under constant electric field. The electric field is 12 MV/cm for the ALD sample with $T_{eff}=2.2$ nm, and the no-ALD sample with $T_{ox}=2.0$ nm. It is 14 MV/cm for the ALD sample and for the no-ALD sample with $T_{eff}=3.0$ nm. Here, the underlying SiO_2 thickness (2.8 nm) of the ALD sample with $T_{eff}=3.0$ nm is slightly smaller than that of the no-ALD sample with $T_{ox}=3.0$ nm. It is seen that the ALD samples show better reliability compared with the no-ALD samples. Particularly, the reliability for the ALD silicoin-nitride/2.0-nm-thick SiO_2 stack (closed circles) is significantly improved compared to the corresponding no-ALD sample (open circles).

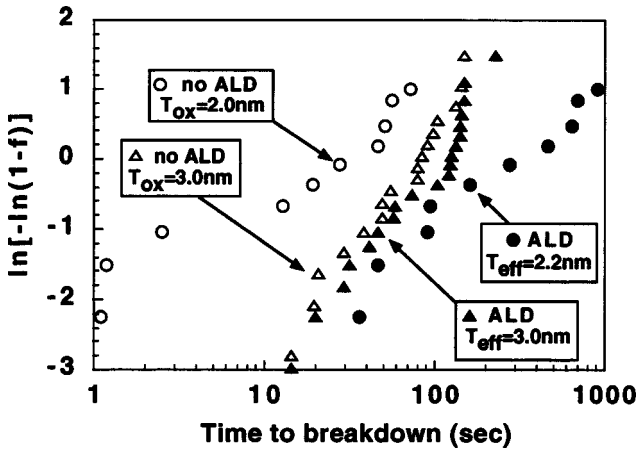

FIG. 5. Time-dependent dielectric-breakdown characteristics of p^+-polycrystalline-Si gate MOS capacitors annealed at 1000 °C for 40 s in a N_2 ambient, under constant electrical field, at 12 MV/cm for the ALD sample with $T_{eff}=2.2$ nm and for the no-ALD sample with $T_{ox}=2.0$ nm, and at 14 MV/cm for the ALD and for no-ALD samples with $T_{eff}=3.0$ nm.

In summary, it is demonstrated that extremely thin (~2 ML) ALD silicon-nitride/SiO_2 stacked gate dielectrics can efficiently reduce boron diffusion from the p^+-polycrystalline-Si gate without modifying the SiO_2/Si interface structure. This leads to significant improvement in the reliability of ultrathin stacked gate dielectrics. Because of the extremely uniform thickness control capability, the ALD silicon nitride on a thin gate oxide will fulfill the severe requirements for ultrathin stacked gate dielectrics for deep submicron CMOS transistors. The low-thermal-budget ALD process (<550 °C) can offer the tailored gate stack not only for ultrathin gate oxides but also for high-k gate dielectrics.

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