Growth and electrical properties of atomic-layer deposited ZrO_2/Si-nitride stack gate dielectrics

Hiroyuki Ishii, Anri Nakajima,[a] and Shin Yokoyama
Research Center for Nanodevices and Systems, Hiroshima University, 1-4-2 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8527, Japan

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We deposited ZrO_2 thin films by atomic-layer deposition (ALD) using zirconium tertiary–butoxide [$Zr(t\text{-}OC_4H_9)_4$, (ZTB)] and H_2O source gases on Si substrates at low temperatures. We grew ZrO_2 films layer by layer in a temperature range of 175–250 °C to minimize surface roughness. The deposited ZrO_2 film thickness had self-limiting properties with the exposure time of ZTB and vapor pressures of ZTB and H_2O. The deposition rate per cycle was independent of the vapor pressure of ZTB from 0.01 kPa to 0.04 kPa. Transmission electron microscopy revealed that the formation of an SiO_x interfacial layer could be suppressed by using an ALD ZrO_2/ALD Si-nitride (~0.5 nm) stack structure. We found the fixed charge, interface trap density, and leakage current density in the ALD ZrO_2/ALD Si-nitride stack dielectrics to be less than those in ALD ZrO_2 dielectrics. In spite of the same equivalent oxide thickness of 1.6 nm, the relative dielectric constant ε_r (11.5) of the ALD ZrO_2/ALD Si-nitride stack capacitor was higher than that (10.5) of the ALD ZrO_2 capacitor due to the suppression of formation of the interfacial SiO_x layer (1.0–1.5 nm) by an ultrathin ALD Si nitride (~0.5 nm). The current conduction mechanism is identified as direct tunneling of electron except at very low dielectric fields. Comparing structural and electrical properties, ALD ZrO_2/ALD Si-nitride stack dielectrics are promising candidates for sub-0.1-μm metal–oxide–semiconductor field-effect transistors. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1629773]

I. INTRODUCTION

The aggressive scaling down of conventional SiO_2 films in sub-0.1-μm metal-oxide-semiconductor (MOS) field-effect-transistors is reaching its limit from the viewpoint of gate leakage current. Various high-k (relative dielectric constant) gate dielectrics (HfO_2, ZrO_2, Al_2O_3, La_2O_3 etc.) have been investigated over the last several years as a possible replacement for SiO_2 to suppress the leakage current.[1–13] The matter is still being debated and consensus has not yet been reached. One of the most promising candidates to replace SiO_2 is ZrO_2, due to its high relative dielectric constant ($\varepsilon_r = 20-25$),[4] thermodynamic stability in contact with Si,[5] large energy band gap (5.2 eV),[6] and small lattice mismatch of 2.1% with Si (100).[4]

Various methods have been proposed to form ZrO_2 gate dielectrics, such as sputtering[7,8] and chemical vapor deposition.[6,9] Recently, the use of self-limiting atomic-layer deposition (ALD) has been accelerating because it offers significant benefits in the fabrication of various gate dielectrics in terms of film uniformity, thickness control in the thin region, and low thermal budget.[14–18] To date, in the ALD of ZrO_2 gate dielectrics, alternating exposures of $ZrCl_4$ and H_2O gases have mainly been applied.[10,19] However, in ALD using these source gases, ZrO_2 exhibits islandlike growth when deposited directly on Si.[10] There is also a risk of Cl contamination and particle adhesion to the substrate surface because $ZrCl_4$ is in a solid state at room temperature.

Zirconium tertiary-butoxide [$Zr(t\text{-}OC_4H_9)_4$, (ZTB)] is an alternative Zr precursor with the highest vapor pressure, allowing evaporation at low temperature. However, only a few reports[20] have been published regarding the ALD of ZrO_2 using ZTB as a gas source. In particular, the growth in the ultrathin region has not yet been examined. Recently, we have preliminarily reported[21] the formation of an ultrathin ZrO_2 layer by ALD using ZTB and H_2O as source gases. Also, we have formed an ultrathin Si nitride layer by ALD between ZrO_2 and a Si substrate and found that it acts as an effective barrier against oxygen indiffusion from transmission electron microscopy (TEM) measurement. Without the barrier layer, an interfacial SiO_x layer, which has a smaller dielectric constant than that of $HfO_2(ZrO_2)$, is formed between ZrO_2 and the Si substrate during film deposition in an oxygen ambient or oxygen-containing precursor ambient due to the oxygen indiffusion.[9,10] This reduces the overall dielectric constant, and increases the equivalent oxide thickness (EOT). It has already been reported that a stack structure with a thin barrier layer of SiON (Refs. 11 and 12) and Al_2O_3 (Ref. 13) between $HfO_2(ZrO_2)$ and a Si substrate is advantageous for the suppression of this interfacial layer.

In this study, we investigate the growth of ultrathin ZrO_2 by the alternate supply of ZTB and H_2O in detail to find the process window of ALD. We added the examination of the dependence of the growth properties on substrate temperature and on ZTB pressure and discuss the growth mechanism. Also, we compared the electrical properties of ALD ZrO_2 with those of a stack structure of ALD ZrO_2 with ALD Si-nitride barrier layer, clarifying the advantages of the stack structure.

[a]Author to whom correspondence should be addressed: electronic mail: nakajima@sxsys.hiroshima-u.ac.jp

II. EXPERIMENT

ALD ZrO_2 films were deposited by alternately supplying ZTB and H_2O gases on *p*-type Si(100) wafers (8–12 Ω cm). Before the deposition of ZrO_2, the wafers were cleaned with an $NH_4OH:H_2O_2:H_2O=0.15:3:7$ solution at 80 °C for 10 min and treated with 0.5% HF to eliminate native oxide and terminated with hydrogen. The ALD was carried out using a cold-wall-type deposition chamber where Si wafers were heated with a halogen lamp. The introduction of source gases and exposure time were controlled by a computer. ZTB exposure followed by H_2O exposure was cyclically repeated 2–15 times at various substrate temperatures (T_{sub}). The exposure time for ZTB was 10–180 s and 60 s for H_2O. The vapor pressure of ZTB during deposition was controlled to 0.01–0.04 kPa and H_2O pressure was controlled to 0.13–1.05 kPa. T_{sub} was between 75–400 °C. Just after the ALD of ZrO_2, *in situ* N_2 annealing was done for 5 min at 400 °C. To form the ALD ZrO_2/ALD Si-nitride stack structure, an ultrathin Si-nitride barrier layer was deposited using the ALD process, alternately supplying $SiCl_4$ and NH_3 gases.[14,15] The physical thickness (T_{phy}) of the barrier ALD Si nitride was about 0.5 nm after two deposition cycles. When the diode structures were formed for electrical measurements, the exposure times of ZTB and H_2O were both 60 s at 0.04 kPa (ZTB) and 0.7 kPa (H_2O) vapor pressures. Here, 15 deposition cycles were used. The Al electrode was then deposited by sputtering using a hard mask with several circular openings 2 mm in diameter (area of 3.1×10^{-2} cm^2).

Microstructure and film thickness were measured with TEM (Hitachi HF-2100 field emission TEM operating at 200 keV). Film thickness was also measured by ellipsometry. Surface roughness was evaluated by atomic force microscopy (AFM), and the electrical properties were characterized with an HP 4284 inductance–capacitance–resistance meter and an HP 4156B semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Figure 1 shows the self-limiting properties of ZrO_2 film growth with ZTB exposure time (10–180 s) for various ZTB vapor pressures. The vapor pressure of H_2O was fixed to 0.7 kPa over five deposition cycles. The thickness of each of the deposited ZrO_2 films tends to saturate at ZTB exposure times longer than 60 s. At ZTB vapor pressures from 0.01 kPa to 0.04 kPa, ZrO_2 film growth exhibited similar properties, also suggesting the self-limiting properties of ZrO_2 film growth with ZTB vapor pressure. The film thickness was measured by ellipsometry, assuming the ZrO_2 refractive index was 2.05.[4]

Figure 2(a) is a plot of the deposited ZrO_2 film thickness as a function of ZTB vapor pressure. A saturated film thickness of 2.5–2.8 nm is achieved with five deposition cycles. We can also see the self-limiting properties of film growth with H_2O vapor pressure in Fig. 2(b). This indicates that there are rather large process windows for ALD in terms of the gas pressure.

Figure 3 shows the dependence of ZrO_2 film thickness deposited on Si and ALD Si-nitride/Si on the number of deposition cycles for different ZTB vapor pressures. The film thickness of ZrO_2 on a Si substrate is in a single linear relation with the number of deposition cycles even in different ZTB vapor pressures ranging from 0.01 kPa to 0.04 kPa. In the ZTB vapor pressure range, the film growth rates obtained from the slope of linear lines, using a least-squares program for each vapor pressure, are almost the same and are estimated to be 0.22 ± 0.02 nm/cycle. One monolayer of amorphous ZrO_2 film thickness is considered to be about 0.2–0.3 nm since the Zr—O bond distance obtained from the ionic radius is 0.22 nm.[22,23] This value is consistent with the ZrO_2 growth rate obtained in our experiments, which indicates that layer-by-layer growth of ZrO_2 takes place in our experiments. Also, there is almost the same offset thickness of about 1.5 nm for different ZTB pressures without a Si-nitride barrier structure, which is considered to be due to the presence of an interfacial SiO_x layer between ZrO_2 and the Si substrate. An interfacial layer with almost the same film thickness (about 1.2 nm) was previously reported by TEM measurements.[21] On the other hand, the film thickness of the ZrO_2 deposited on the ALD Si nitride also shows a linear relation with the number of deposition cycles. An almost identical deposition rate of 0.23 nm/cycle to that for the ZrO_2 deposited on a Si substrate is obtained from the slope of the linear line, using a least-squares program. The offset thickness of 0.6 nm is obtained from the linear line, which coincides well with the film thickness of the deposited ALD Si nitride measured by TEM. This suggests that the growth of the interfacial SiO_x layer was suppressed in this stack structure.

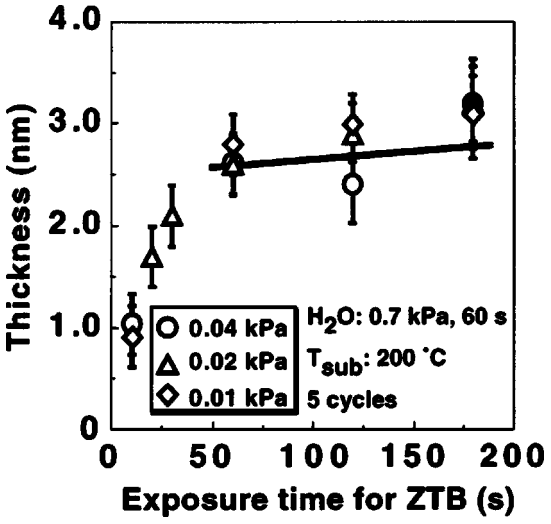

FIG. 1. Dependence of ALD ZrO_2 film thickness on ZTB exposure time after five deposition cycles for different vapor pressures of ZTB. Vapor pressure of H_2O was 0.7 kPa and exposure time for each gas was 60 s.

Figure 4 shows the dependence of deposited ZrO_2 film thickness and the surface roughness (R_a) on T_{sub} in a temperature range from 75 to 400 °C. There are at least three different growth modes as indicated by the three regions (I–III). From 175 to 250 °C, the deposited film thickness is almost the same with an average value of 3.0 nm. Within this temperature range, the self-limiting properties indicate that ZrO_2 grows layer by layer. However, ZrO_2 film thickness

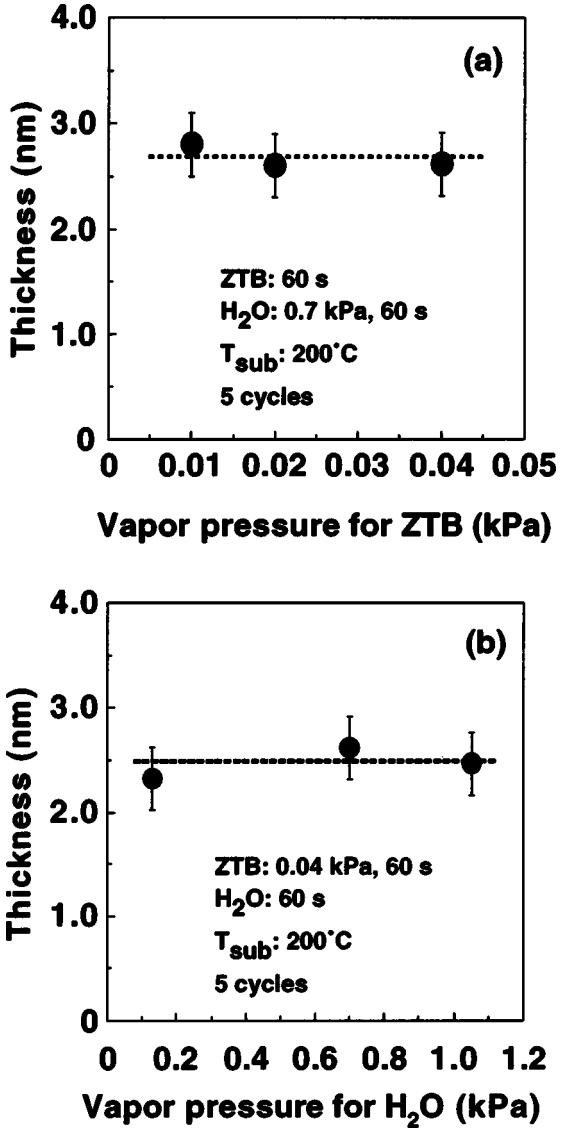

FIG. 2. (a) Dependence of ALD ZrO_2 film thickness on ZTB vapor pressure for exposure time of 60 s. (b) Dependence of ALD ZrO_2 film thickness on H_2O vapor pressure for exposure time of 60 s.

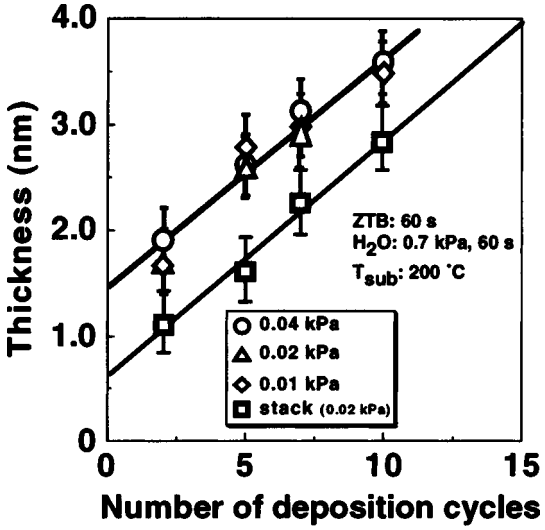

FIG. 3. Dependence of ALD ZrO_2 film thickness on number of deposition cycles for different vapor pressures of ZTB. The vapor pressure of H_2O was 0.7 kPa and the exposure time for each gas was 60 s. A growth rate of 0.22 nm/cycle, 0.24 nm/cycle, and 0.21 nm/cycle were extracted on a Si substrate at ZTB vapor pressures of 0.01 kPa, 0.02 kPa, and 0.04 kPa. A growth rate of 0.23 nm/cycle was extracted on the ALD Si nitride at ZTB vapor pressure of 0.02 kPa.

increases rapidly with decreasing temperature below 100 °C, which is considered to be due to the excess gas adhesion of ZTB. The thickness also increases rapidly with increasing temperature above 350 °C, which is considered to be due to the excess thermal decomposition of ZTB. Discussion of the surface roughness will be given later.

One of the possible mechanisms of self-limiting properties is as follows. When the OH terminated surface is exposed to ZTB ambient, the following reaction occurs:[20,24]

$$\mathrm{Zr(OH)}^{*} + \mathrm{Zr[OC(CH_3)_3]_4} \rightarrow \mathrm{Zr{-}O{-}Zr[OC(CH_3)_3]_3}^{*} + \mathrm{(CH_3)_3COH}. \quad (1)$$

Here,* means the top surface condition. This reaction automatically stops when all the OH groups on the surface react with ZTB, leading to a self-limiting property (Fig. 1). On the other hand, during the subsequent H_2O exposure, the following reaction occurs:

$$\mathrm{Zr{-}O{-}Zr[OC(CH_3)_3]_3}^{*} + 3\mathrm{H_2O} \rightarrow \mathrm{Zr{-}O{-}Zr(OH)_3}^{*} + 3[\mathrm{C(CH_3)_3}]\mathrm{OH}. \quad (2)$$

This reaction also automatically stops when all the $OC(CH_3)_3$ groups on the surface react with H_2O, again leading to a self-limiting property (Fig. 2). However, further investigations are necessary to clarify the details of the self-limiting mechanisms including the effect of surface migration of the precursors or of the steric hindrance.

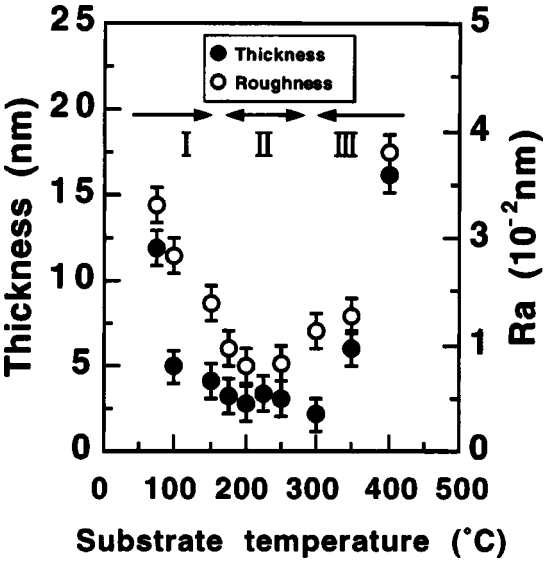

FIG. 4. Dependence of ZrO_2 film thickness and average surface roughness (R_a) on substrate temperature after five deposition cycles. Vapor pressure of ZTB was 0.01–0.02 kPa and that of H_2O was 0.7 kPa with equal exposure time of 60 s. It is obvious that ALD properties are achieved in the temperature range 175 °C–250 °C.

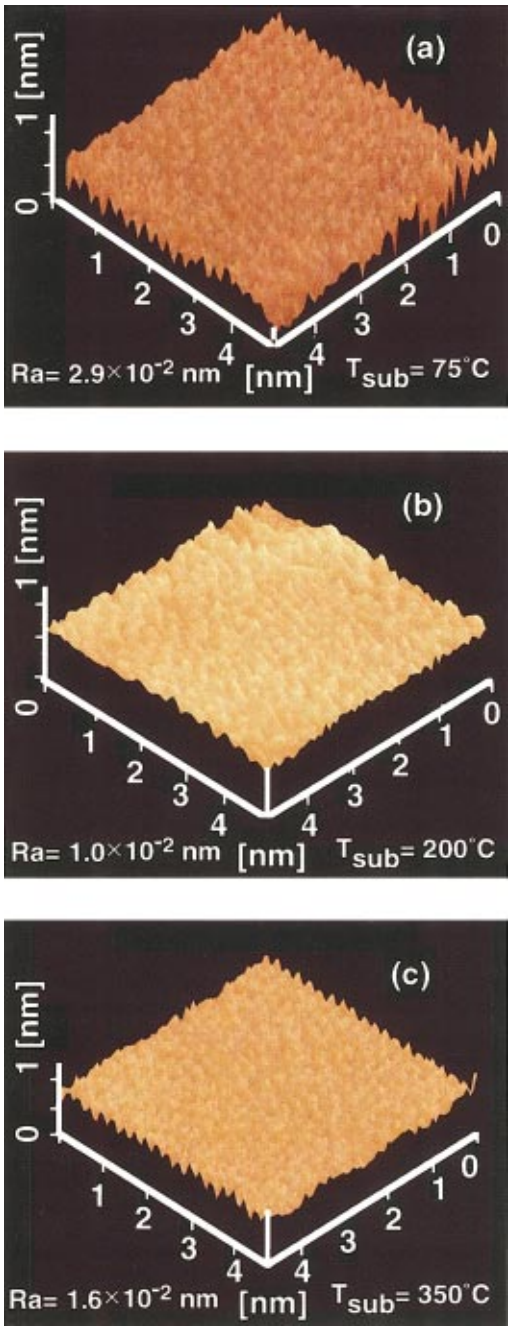

FIG. 5. (Color) AFM images in three different modes [substrate temperature range (T_{sub})] shown in Fig. 4. (a) at T_{sub} of 75 °C, (b) at T_{sub} of 200 °C, and (c) at T_{sub} of 350 °C. Average surface roughness (R_a) was 2.9×10^{-2} nm in (a), 1.0×10^{-2} nm in (b), and 1.6×10^{-2} nm in (c).

Figure 5 shows typical AFM images at T_{sub} of 75 °C, 200 °C, and 350 °C which are the representative T_{sub} for the three different growth modes in Fig. 4. R_a at a T_{sub} of 200 °C is the smallest.

The dependence of R_a on T_{sub} is summarized in Fig. 4. The surface roughness around 200 °C is minimized in the measured temperature region. The surface roughness increases rapidly with decreasing temperature below 150 °C. The R_a value also increases rapidly above 350 °C. The overall temperature dependence of R_a is qualitatively similar to that of the film thickness as seen in Fig. 4. The difference in R_a with temperature may be due to the following reasons. As

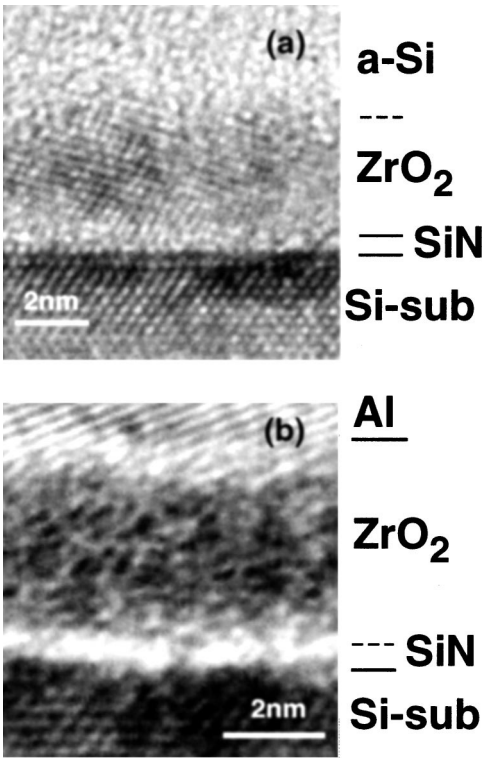

FIG. 6. High-resolution cross-sectional TEM micrograph of ALD ZrO_2/ALD Si-nitride stack films (a) with five ZrO_2 deposition cycles and (b) with fifteen deposition cycles. Vapor pressure of ZTB was 0.04 kPa and that of H_2O was 0.7 kPa with same exposure time of 60 s. There were two deposition cycles for underlying ALD Si nitride ($T_{phy}=\sim0.5$ nm). (a) Three minutes of 850 °C annealing followed annealing at 400 °C for 5 min after ALD ZrO_2 was deposited. (b) 400 °C annealing was only added for 5 min after ALD ZrO_2 was deposited.

described previously, we consider that the deposition below 150 °C is related to the excess gas adhesion of ZTB. Since the extent of surface migration of precursors is speculated to be small at these low temperatures, the R_a values become large below 150 °C because of inhomogeneous gas adhesion on the special adsorption site on the surface. On the other hand, the roughness above 350 °C is thought to be due to the excess thermal decomposition of ZTB.

Figure 6(a) is a high-resolution cross-sectional TEM micrograph of the ALD ZrO_2/ALD Si-nitride stack structure. ZrO_2 was deposited over five cycles by ALD. This sample was annealed at 850 °C for 3 min in an N_2 ambient after annealing at 400 °C for 5 min. We observed crystallized ZrO_2 in the 850 °C annealed sample and this roughens the surface of the ZrO_2. The thickness of the amorphous layer between ALD ZrO_2 and the Si substrate is about 0.5 nm, which is identical to the thickness derived from the intercept of Fig. 3 and is consistent with the film thickness of the deposited ALD Si nitride obtained from the deposition rate.[17] This suggests that the amorphous layer between ALD ZrO_2 and the Si substrate is presumably ALD Si nitride and the growth of the interfacial SiO_x layer could be suppressed. The smooth interface observed between ALD ZrO_2 and the Si nitride layer is also noteworthy. Figure 6(b) is a cross-sectional TEM micrograph of the Al/ALD ZrO_2/ALD Si-nitride stack capacitor used for the electrical measurements.

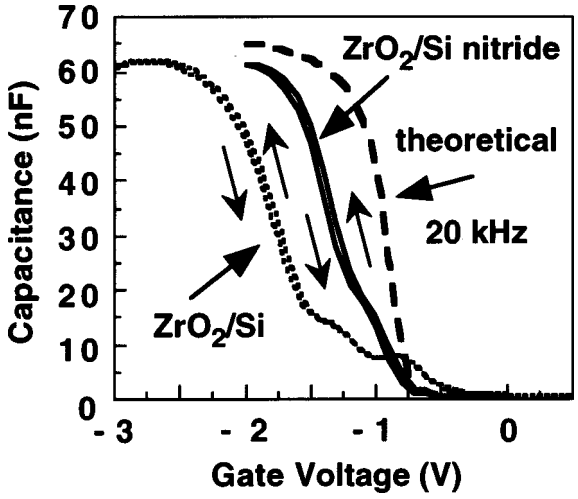

FIG. 7. $C-V_g$ characteristics at 20 kHz for ALD ZrO_2 (dotted line) and ALD ZrO_2/ALD Si-nitride capacitor (solid line). Fifteen deposition cycles for ZrO_2 and two for Si nitride. Vapor pressure of ZTB was 0.04 kPa and that for H_2O was 0.7 kPa with the same exposure time of 60 s. $C-V_g$ curve (broken line) calculated using a doping level of the Si substrate and a work function of Al is also shown.

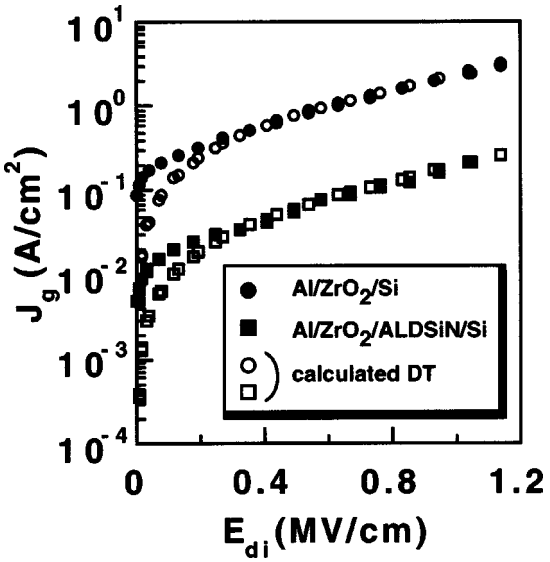

FIG. 8. Experimentally obtained J_g-E_{di} characteristics for ALD ZrO_2 (solid circles) and ALD ZrO_2/ALD Si-nitride capacitors (solid squares). Same devices were used to measure $C-V_g$ characteristics in Fig. 7. Calculated results of direct tunneling current for electron using a WKB approximation are also shown (open circles and squares).

The total T_{phy} value of the stack dielectrics is 4.7 nm. In the conventional complementary metal-oxide-semiconductor (CMOS) process, high thermal budgets are required after the formation of gate dielectrics for activation annealing of the polycrystalline Si gate and the source/drain region. Therefore, thermal stability of ALD Si nitride has been examined for ALD Si-nitride/SiO_2 stack dielectrics.[15] They were proven to be stable at 800 °C for 30 min in a vacuum. Also, *p*-channel MOS capacitors with the stack dielectrics with 1000 °C activation annealing has suppressed boron penetration into the dielectrics, which is due to the existence of the ALD Si nitride on the SiO_2.[14,15] In addition, *n*-channel MOS capacitors with ALD Si nitride with 900 °C activation annealing showed excellent reliability.[18] From these results, we consider that the ALD Si nitride in this study also has a good thermal stability.

Figure 7 shows the capacitance–gate voltage ($C-V_g$) curves of ALD ZrO_2 and ALD ZrO_2/ALD Si-nitride capacitors measured at 20 kHz. The ALD ZrO_2 was deposited at 15 cycles and the ALD Si nitride was deposited at two cycles. The small hysteresis ($\Delta V_{FB}=50$ mV) observed in the $C-V_g$ curves is considered to be due to charge trapping in ZrO_2 and/or near the ZrO_2/Si-nitride interface. In addition, the damage induced during Al sputtering for the electrode formation might be a possible reason as postmetallization annealing was not carried out after sputtering. The EOT is estimated to be 1.6 nm for both types of capacitors from the accumulation capacitance. The T_{phy} value of ALD ZrO_2 including the interfacial SiO_x in an ALD ZrO_2 capacitor was 4.3 nm observed by TEM. Taking this T_{phy} value into account, the ε_r value is 10.5. Compared against the theoretical $C-V_g$ curve (broken curve), the interface trap density D_{it} is estimated to be about $10-4\times10^{12}$ $cm^{-2}\,eV^{-1}$ between 0.2 and 0.45 eV above the valence-band edge. Also, the density of positive fixed charge is estimated to be 1.3×10^{13} cm^{-2} from a flat-band voltage shift (−0.9 V) with respect to the theoretical curve. However, for the ALD ZrO_2/ALD Si-nitride capacitor, the T_{phy} of ALD ZrO_2/ALD Si-nitride was 4.7 nm observed by TEM as previously mentioned and the overall ε_r of the film is estimated to be 11.5. From the same analysis above, D_{it} is estimated to be about $5-4\times10^{12}$ $cm^{-2}\,eV^{-1}$ between 0.1 and 0.3 eV above the valence-band edge. Also, the density of positive fixed charge is estimated to be 5×10^{12} cm^{-2} from a flat-band voltage shift (−0.4 V) with respect to the theoretical curve. Thus, it is evident that the incorporation of an extremely thin ($T_{phy}=0.5$ nm) ALD Si-nitride barrier layer has greatly reduced the fixed charge and interface trap densities while causing an increase in the dielectric constant.

We investigated the current transport mechanism in both dielectrics (Fig. 8) by plotting the current density as a function of dielectric field (J_g versus E_{di}). The dielectric field was obtained by dividing the dielectric voltage (V_{di}) by the physical thickness ($E_{di}=V_{di}/T_{phy}$). The value of V_{di} was derived from the space charge in Si (Q_{sc}) and C_{di}. Here, C_{di} stands for dielectric capacitance. The space charge was calculated as a function of surface potential (ψ_s) and V_{di} was obtained from the expression, $V_{di}=V_g-V_{FB}-\psi_s$, where V_{FB} is the flat-band voltage. Figure 8 shows the J_g-E_{di} characteristics of ALD ZrO_2 and ALD ZrO_2/ALD Si-nitride capacitors whose $C-V_g$ curves are in Fig. 7. We found that the leakage current density of ALD ZrO_2 with an ALD Si-nitride barrier layer is smaller than that of ALD ZrO_2 without an ALD Si-nitride barrier layer by about one order of magnitude. It is obvious that the leakage current is suppressed by the ALD Si-nitride barrier layer.

An electron is thought to be the main carrier in the dielectrics due to the following reason. For the samples shown in Fig. 8, electrons are injected from the Al gate electrode and holes from the Si substrate since negative bias voltage is applied to the gate. The barrier height for electrons between

the Al electrode and ZrO_2 is estimated to be about 1.4 eV since the metal work function of Al was reported to be 4.2 eV (Ref. 25) and the electron affinity of ZrO_2 was reported to be 2.8 eV (Ref. 26) from photoemission study. On the other hand, the barrier height for the holes between ZrO_2 and the Si substrate was reported to be 3.35 eV from photoemission study.[26] Consequently, electron injection from the Al gate dominates the current due to the smaller barrier height.

Direct tunnel currents for electrons calculated using the Wentzel–Kramers–Brillouin (WKB) approximation[27] are shown in Fig. 8 (open circles and squares). An effective mass used in the calculation is 0.12 times the free electron mass (m_0). For ALD ZrO_2 without an ALD Si-nitride barrier layer, the J_g-E_{di} characteristics (open circles) fit well to the experimental one (solid circles in Fig. 8) assuming the barrier height of 1.4 eV described previously. In the calculation, we used the physical thickness of 4.3 nm, which was obtained by the TEM measurement. The effective electron mass used is consistent with the reported value of 0.1 m_0 for high-k dielectrics.[28]

On the other hand, for ALD ZrO_2 with an ALD Si-nitride barrier layer, the J_g-E_{di} (open squares) characteristics fit well to the experimental one (solid squares in Fig. 8) assuming the barrier height of 1.55 eV. Here, the effective electron mass was assumed to be the same as that of ALD ZrO_2 without the barrier layer and the physical thickness of 4.7 nm from the TEM result was used. In order to simplify the calculation, we assumed that electrons tunnel through a single dielectric although the actual barrier structure is a stack dielectric. The slightly larger barrier height is considered to be due to the larger barrier height at the Si-nitride/Si interface than that at the ZrO_2/Si interface.[18]

From the above analyses, it is concluded that the main conduction mechanism is electron direct tunneling. However, the experimentally obtained current density is larger than that calculated result in the low E_{di} region (<0.2 MV/cm) for both dielectrics. This may be an effect of the interface or bulk traps, which may cause a trap-assisted tunneling,[29] because at the low E_{di} electrons directly tunnel to the states in the Si band gap. It is reasonable that the main conduction mechanism is direct tunneling for both dielectrics. And the current suppression in ALD ZrO_2 with the ALD Si-nitride barrier layer, is due to an increase in T_{phy}, maintaining the same EOT value compared to ALD ZrO_2 without the barrier layer.

IV. CONCLUSION

We characterized the growth and electrical features of an ALD ZrO_2/ALD Si-nitride stack structure by comparing them with those of the ALD ZrO_2 dielectrics. MOS capacitors with these dielectrics were fabricated under optimal process conditions with an EOT of $\sim$1.6 nm. TEM observation revealed that the inclusion of an ALD Si-nitride barrier layer suppressed the formation of an SiO_x interfacial layer which is prominent in ALD ZrO_2 dielectrics. $C-V$ characteristics exhibited a remarkable reduction in fixed charge and interface trap density in ALD ZrO_2/ALD Si-nitride stack dielectrics compared to ALD ZrO_2 dielectrics. In the stack dielectrics, J_g-E_{di} characteristics indicated reduced leakage current by about one order of magnitude. The current conduction mechanism is identified as direct tunneling of electrons except at a very low E_{di} (<0.2 MV/cm). In the low E_{di} region, the interface and bulk traps may affect the conduction mechanism. The ALD ZrO_2/ALD Si-nitride stack structure has a great deal of potential in the ultrathin gate dielectrics of sub-0.1-μm CMOS devices, because it completely suppresses the interfacial SiO_x layer, controls thickness extremely uniformly in the ultrathin region, and has low leakage characteristics.

ACKNOWLEDGMENTS

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