Conduction mechanism of Si single-electron transistor having a one-dimensional regular array of multiple tunnel junctions

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Uniformly doped Si single-electron transistors consisting of a one-dimensional regular array of multiple tunnel junctions (MTJs) and islands have been fabricated. The Coulomb blockade effect is found to play an important role in carrier conduction in the MTJ system at low temperatures (6 K). The conduction mechanism can be interpreted well by considering soliton. The soliton extends less than three islands in our MTJs, and the energy of a single soliton is found to be 0.024 eV from an analysis of low-temperature current–voltage characteristics. For high-temperature operation, it is effective to reduce the parasitic capacitance of each island, which leads to an increase in soliton length. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1492318]

Single-electron devices utilizing the Coulomb blockade effect are promising candidates for the basic elements of future low power, high density integrated circuits.[1–6] To develop these devices into commercial products, a Si construct is important because of the compatibility with conventional fabrication techniques of large-scale integrated devices. Another requirement to develop these devices into commercial products is room temperature operation.

One way to raise the operation temperature of the device is to utilize the multiple tunnel junctions (MTJs). In a MTJ system, the effective junction capacitance decreases because the capacitances are connected in series. This leads to a decrease in total capacitance of the island inside the MTJ system, to an increase in the charging energy of the island and to an increase in the operation temperature. To utilize such MTJ systems in a single-electron transistor (SET) for practical purposes, it is important to investigate the conduction mechanism in detail.

Detailed descriptions of the fabrication procedure and measurement for SETs having one- and two-dimensional regular arrays of MTJs with metallic islands can be found in Refs. 7–9. In such arrays, the presence (or absence) of one electron on an island induces a polarization of neighboring islands described as a charge soliton (or antisoliton). For a Si SET with a MTJ system, most of the investigated arrays were naturally formed ones where the junction size and position fluctuate and are not evaluated precisely.[10–13] Since the number of the junction is not known either, the details of the conduction mechanism and the effect of soliton have not been examined. Though SETs having double islands with a regular array of junctions connected in series have been fabricated using electron beam (EB) lithography,[14] the conduction mechanism for the regular array of MTJs having more islands, in which the concept of soliton becomes important, has not been investigated. In this study, we fabricated a Si SET with a one-dimensional regular array of MTJs with 11 islands for high-temperature operation, and investigated the conduction mechanism from the viewpoint of soliton.

Figure 1 shows the equivalent circuit and structure of the SET with MTJs in this study. A one-dimensional regular array of MTJs consisting of 11 islands is fabricated using EB direct writing in a silicon-on-insulator (SOI) layer. The tunnel barriers are formed in constrictions of silicon in between the islands due to the quantum-size effect. The thicknesses of the top silicon layer and buried oxide on SOI wafers are 50 and 400 nm, respectively. Doping of the top silicon layer was carried out by $POCl_3$ diffusion at 850 °C for 10 min. The doping level was about 2×10^{20} cm^{-3}. The fabrication process includes EB lithography and the dry etching using an electron-cyclotron resonance etcher with the resist pattern as a mask. Subsequent isotropic wet etching in a

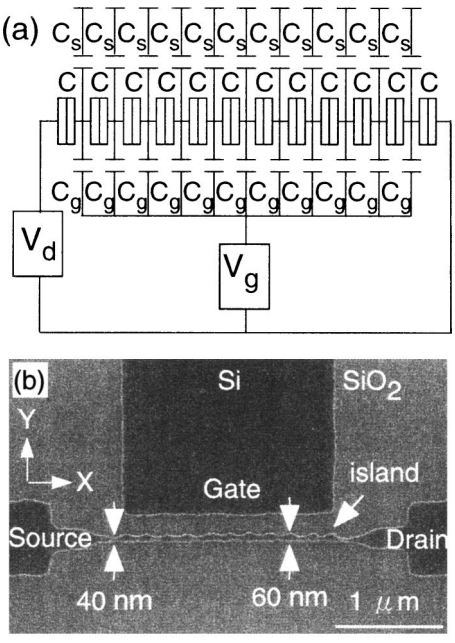

FIG. 1. (a) Equivalent circuit of a fabricated SET with MTJs consisting of 11 islands. C_s, C_g, and C represent the substrate capacitance, gate capacitance, and tunnel junction capacitance of a Coulomb island, respectively. Parasitic capacitance C_0 of the island consists of C_s and C_g. (b) Plan-view scanning electron microscopy micrograph of the SET.

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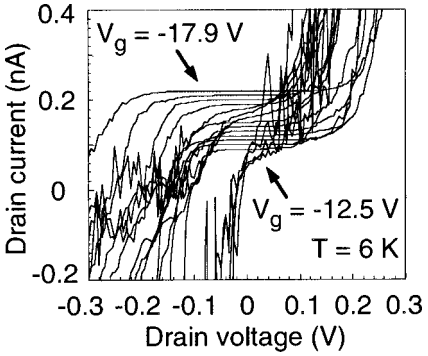

FIG. 2. Drain current vs drain voltage (I_d–V_d) characteristics as a function of gate voltage (V_g) at 6 K. V_g from −17.9 to −12.5 V in V_g steps of 0.3 V. The curve for V_g of −13.7 V is not shown due to measurement failure. Each curve is offset by 10 pA per 0.3 V of V_g to provide clarity.

$NH_4OH/H_2O_2/H_2O$ solution at 70 °C reduces the dimensions of the device and damage introduced during the dry etching process.[15] Final thickness of the top Si layer is about 20 nm. The widths of the barrier and island region are seen to be about 40 and 60 nm, respectively, in Fig. 1(b). The width of an island fluctuates between 30 nm and 70 nm among the devices. After the deposition of interlayer dielectrics, the device fabrication was accomplished by forming ohmic contacts. Low-temperature current–voltage (I–V) measurements were performed with a HP 4156B semiconductor parameter analyzer and a cryogenic manipulated probe system (HYTT-01).

Figure 2 shows the drain current (I_d) versus drain voltage (V_d) characteristics as a function of gate voltage (V_g) at 6 K. A zero-current Coulomb gap region and the modulation of the gap by V_g are clearly observed. It is seen that the gap is maximum at V_g of −14.6 V in the diamond-like pattern of characteristics in the V_g region between −16.4 and −12.5 V.

Figure 3 shows I_d versus V_g characteristics at V_d of 0.001 V. It shows a peak and a valley at $V_g = -16.4$ V and at $V_g = -15.8 \sim -14.2$ V, where the Coulomb gap disappears and appears in Fig. 2, respectively. In Fig. 3, I_d at V_gs around the valley is the background level (0.04 pA).

Figure 4 shows I_d versus V_d characteristics at V_g of −14.6 V. From the figure, we can estimate the maximum Coulomb gap precisely. We quantify the gap in terms of the threshold voltage V_t, where the I_d exceeds the background

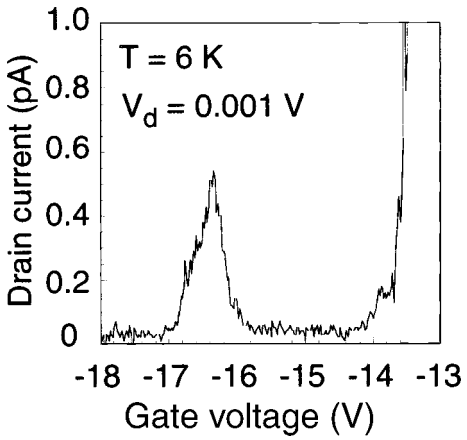

FIG. 3. Drain current vs gate voltage characteristics at 6 K (drain voltage V_d of 0.001 V).

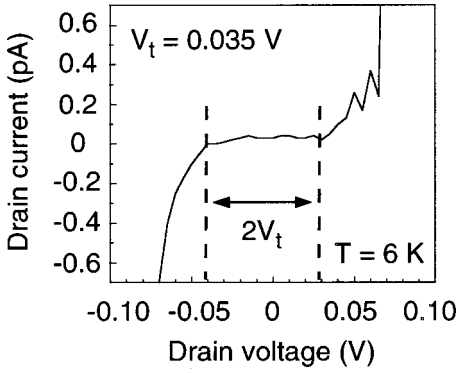

FIG. 4. Drain current vs drain voltage characteristics at 6 K (the gate voltage V_g of −14.6 V).

level (0.04 pA) and the steep onset of current appears. This voltage V_t is thought to be a measure of an edge barrier to a single soliton injection. The observed V_t value is 0.035 V from Fig. 4.

Tunneling in one-dimensional arrays of multiple junctions has been treated theoretically.[16,17] From the theory,

$$V_t = e[1 + \exp(-1/M)]/(2C_{\text{eff}}) \tag{1}$$

$$= e/(C_{\text{eff}} + C_0), \tag{2}$$

where M is the soliton length and e is the electron charge. C_{eff} and C_0 are the effective total and parasitic capacitances of a Coulomb island, respectively. The main contribution to C_0 is considered to be the gate capacitance C_g between the island and the side gate, and the substrate capacitance C_s between the island to the substrate. Taking the experimental result into account,

$$e/(C_{\text{eff}} + C_0) = 0.035 \text{ V}. \tag{3}$$

If a single electron is placed on an island of an infinitely long array of MTJs,

$$C_{\text{eff}} = (C_0^2 + 4CC_0)^{1/2}, \tag{4}$$

where C is the junction capacitance. Here, we neglect the capacitance coupling between the next-nearest-neighbor islands and higher order terms.[16] On the other hand, C can be obtained from the usual offset voltage for high drain voltages:[16]

$$V_{\text{off}} = Ne/(2C), \tag{5}$$

where N is the number of junction in the MTJ system. In this study, V_{off} was measured to be 0.45 V (not shown) since N is 12 in our SET. From the result, C is obtained to be 2.1 aF. Then, C_{eff} and C_0 become 3.4 and 1.2 aF, respectively, using Eqs. (3) and (4).

When we assume the diameter of the Coulomb island to be 12 nm, C_g is calculated to be about 0.4 aF from the parallel-plate capacitance approximation, considering the ratio of the solid angle for the island toward the side gate. Also, C_s is calculated to be 0.8 aF from the approximation, considering the ratio of the solid angle for the island toward the substrate. Thus, the C_0 ($= C_g + C_s$) becomes 1.2 aF for a diameter of 12 nm, which coincides with that experimentally obtained. Considering the size fluctuation and the potential distribution in the geometrically defined island, the Coulomb island with diameter of 12 nm is plausible.

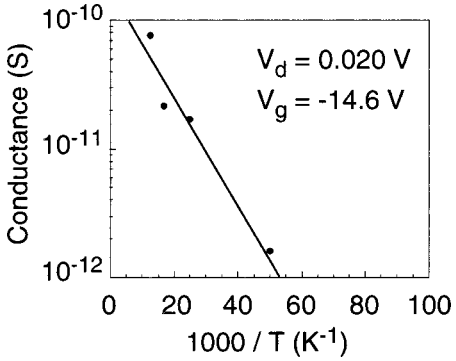

FIG. 5. Arrhenius plot of the conductance at drain voltage V_d of 0.020 V. The gate voltage V_g is -14.6 V.

On the other hand, the upper limit of C is calculated to be 2.7 aF. The capacitance of the Coulomb island is calculated to be 2.6 aF under the assumption that the two circular conductive plates with diameters of 12 nm (thickness≪diameter) were placed in Si with 190 nm distance between the centers [Fig. 1(b)]. The contribution of the island thickness to C is estimated to be 0.1 aF using the parallel-plate approximation, assuming that intervening dielectric is Si. In our sample, the value of C should be smaller than 2.7 aF because the Coulomb island with a 12 nm diameter is embedded in a geometrically defined Si island with a finite diameter (60 nm) and is also sandwiched with the interlayer dielectrics (SiO_2) and buried oxide on the SOI wafer. Furthermore, the adjacent two Si islands are connected in a narrow Si wire region. The lower limit of C is calculated to be 1.0 aF in the same manner, assuming that the two plates were in SiO_2. Here, for the influence of the plate thickness, the intervening dielectric is assumed to be Si, and it is again 0.1 aF. The experimentally obtained C value of 2.1 aF is indeed between these upper and lower limits.

From Eqs. (1) and (2), M can be expressed as

$$M^{-1}=\ln[(C_{\mathrm{eff}}+C_0)/(C_{\mathrm{eff}}-C_0)]. \tag{6}$$

Substituting the experimentally obtained values for the C_{eff} and C_0 in Eq. (6), M becomes 1.4 ($2M=2.8$). Since the soliton extends over approximately $2M$ junctions, the soliton in our SET extends less than three islands. As can be understood from Eq. (6), such small soliton length is due to the relatively large C_0 value in our SET. On the other hand, the energy on a single soliton E_S is expressed as[16]

$$E_S=e^2/(2C_{\mathrm{eff}}). \tag{7}$$

Here, E_S is the work required to enter a single soliton to the MTJ system. From Eq. (7), E_S is obtained to be 0.024 eV using the obtained C_{eff} value.

Figure 5 shows an Arrhenius plot of the conductance as a function of inverse temperature. The conductance was measured inside the Coulomb gap (at V_d of 0.020 V). The Arrhenius plot can be approximated well by a linear line and the activation energy Δ is obtained to be 0.01 eV from the slope. This Δ value is about half of the E_S value. On the other hand, the current within the Coulomb gap is considered to arise from the dissociation of thermally activated soliton–antisoliton pairs, which can move in response to an imposed electric field.[9] Since the thermal excitation creates a pair of charge carriers (a soliton and an antisoliton), the measured activation energy will be half of E_S.[9] Consequently, the measured activation energy closely matches our experimentally obtained E_S. Therefore, the soliton model explains the obtained experimental results well.

Finally, as can be understood from Eqs. (4) and (7), to get a higher device operation temperature, it is effective to reduce the parasitic capacitance C_0 of an island, which also increases the soliton length [from Eq. (6)].

In summary, we fabricated a Si SET with one-dimensional regular array of MTJs and investigated the conduction mechanism. The conduction mechanism can be explained well by considering soliton. The soliton extends less than three islands in the array and the energy of a single soliton E_S is 0.024 eV. For higher temperature operation, it is effective to reduce the parasitic capacitance C_0 of an island, which increases the soliton length.

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