Reliable extraction of the energy distribution of Si/SiO_2 interface traps in ultrathin metal–oxide–semiconductor structures

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A simple and effective method for the extraction of interface trap distribution in ultrathin metal–oxide–semiconductor (MOS) structures is presented. By a critical analysis of bipolar-pulse-induced currents through MOS capacitors, a technique is developed to determine the energy distribution of the interface traps without requiring the knowledge of surface potential and doping profile in the semiconductor. The proposed technique can be efficiently used to probe electrical stress, hot-carrier, and radiation-induced interfacial degradations in ultrathin MOS structures. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1481194]

The generation of interface traps at the semiconductor/oxide interface of metal–oxide–semiconductor (MOS) structures has long been demonstrated as one of the prime factors behind the degradation of MOS device characteristics. Characterization of the interface traps thus simultaneously has been an important job for accurate estimation of device lifetime and reliability. Several techniques have been proposed for the determination of the density of these traps and their energy distribution in the forbidden energy gap of the semiconductor materials.[1–5] Capacitance–voltage $(C-V)$[4–6] and charge pumping techniques[7,8] are widely employed for the characterization of the interface traps in large-area MOS capacitors and small-area transistors, respectively. Although the charge pumping technique is an efficient approach to the determination of the interface traps in small-area transistors, it cannot be effectively applied on large-area capacitors. On the other hand, the accuracy of estimated interface trap density using the $C-V$ technique is dependent on the accuracy of capacitance measurements. Terman[3] showed that interface trap capacitance could be determined from frequency dispersion of MOS capacitance. This is essentially a difficult and indirect method as the interface trap capacitance is extracted from a measured capacitance that consists of oxide capacitance, depletion capacitance, and the interface trap capacitance. A modified method to determine interface trap distribution from a measured conductance was proposed for its direct relationship with the interface traps.[1] Again, this method is not quite convincing as the value of the required conductance G_p is extracted from the maximum value of G_p/ω as a function of $\omega\tau$, where ω is the angular frequency and τ is interface trap lifetime. Berglund[4] described a method for determining the energy distribution of interface traps by using low-frequency capacitance measurements on MOS structures, while Koukab *et al.*[6] demonstrated a high-frequency $C-V$ method for the analysis of interface traps. However, various approximations and assumptions are usually made for the study of interface properties using the $C-V$ measurements, which are not always well justified. For instance, both the low- and high-frequency capacitance methods use a theoretical curve of semiconductor capacitance as a function of surface potential, which itself is dependent on approximated doping profile and other assumed parameters. Moreover, accurate measurements of $C-V$ characteristics are very difficult in MOS structures with ultrathin oxides due to large intrinsic tunneling leakage. So, the standard $C-V$ method cannot be applied for reliable extraction of the interface trap distribution in ultrathin oxides and hence cannot be used to investigate stress induced interfacial damages as well. Nevertheless, these methods have long been used to characterize interface traps despite low quantitative reliability. Therefore, an easy and more reliable method is highly desired for accurate characterization of interface traps in ultrathin oxide MOS capacitors. In this letter, we present a simple and reliable method for extracting the energy distribution of interface traps using bipolar pulse induced current measurements directly on the MOS capacitors.

Conventional MOS capacitors with SiO_2 dielectrics are used in this study. The capacitors are fabricated using *p*-type Si (001) wafers ($\sim$10 Ω cm). Gate oxide ($\sim$3.0 nm) is grown at 850 °C in dry oxygen ambient. After the growth of the gate SiO_2, a 200 nm thick polycrystalline silicon (poly-Si) gate is formed using $POCl_3$ diffusion at 900 °C for doping and activation annealing. The capacitors thus fabricated are subjected to bipolar-voltage-pulse-induced current measurements with a view to extract energy distribution of interface traps at the Si/SiO_2 interface.

An experimental setup is illustrated in Fig. 1. A bipolar pulse train of fixed amplitude and frequency ($\pm$3 V, 10 kHz) is applied to the gate of the MOS capacitor from a pulse generator (*HP* 8112A). The pulse fall/rise time (t_F/t_R) is gradually varied (keeping the rise/fall time constant) and the corresponding change in substrate current is monitored using a semiconductor parameter analyzer (*HP* 4156B). All experimental measurements are automated using a desktop personal computer. Under the proposed measurement conditions, the MOS device is switched between inversion and accumulation by the bipolar gate pulse. Electrons fill the

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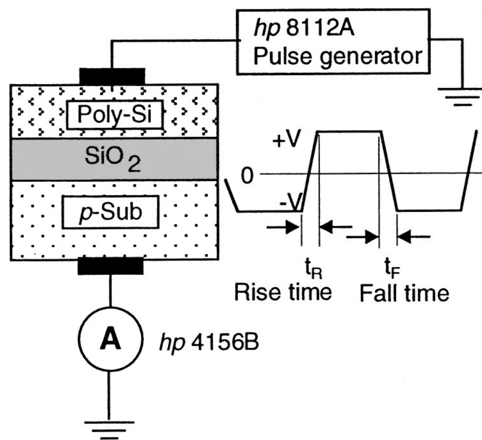

FIG. 1. Schematic illustration of experimental setup for measuring bipolar pulse induced current in MOS capacitors. Pulse fall/rise time is gradually changed during measurements in order to scan the energy levels of interface traps in the upper/lower half of the band gap.

traps at the Si/SiO_2 interface during inversion. Oxide traps existing within a few angstroms from the Si/SiO_2 interface may also be filled due to a tunneling mechanism.[7,9] As the gate bias is reversed, bringing the device into accumulation through depletion, some of the traps lose electrons by emission. Only those traps holding the captured electrons until the device is moved into complete accumulation may give rise to a net flow of charge into the substrate through a recombination with the accumulated majority carriers. This is the so-called charge pumping effect. In the case of MOS transistors, the substrate current thus measured is known as charge pumping current and is reliably used for characterizing the Si/SiO_2 interface traps. However, in the case of MOS capacitors, the measured substrate current is not exactly the charge pumping current, rather it is a net tunneling current through the capacitor. Therefore, unlike MOS transistors, the interface trap density cannot be estimated directly from the measured substrate current. Here, we introduce the concept of using bipolar pulse induced currents for probing interface traps in MOS capacitors. Figure 2 exhibits the substrate current as a function of the pulse fall time measured using the experimental setup shown in Fig. 1. Only the trapped interface electrons that can follow the change in pulse fall time can bring about a change in the measured current. Hence, the difference between two values measured under two different pulse fall times is essentially caused by the interface traps, which are responding to the change of emission time constant due to a change in the pulse fall time. Thus the interface

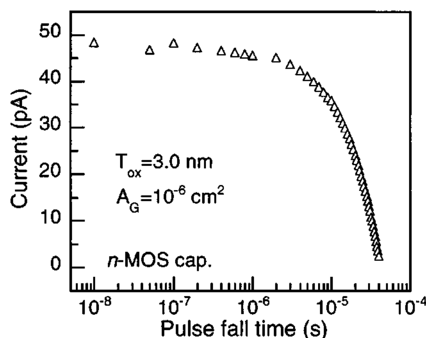

FIG. 2. Measured current as a function of pulse fall time.

trap charge probed between two measurements can be obtained as

$$Q_{\mathrm{it}}=(I_{S0}-I_S)(t_F-t_{F0}), \tag{1}$$

where I_{S0} is the measured current corresponding to the minimum pulse fall time, t_{F0} is permitted by the pulse generator, and I_S is the measured current for any fall time t_F. In fact, the application of a bipolar pulse with variable fall time scans the trap levels in the upper half of the band gap (acceptor-like traps) when the surface is changed from inversion to accumulation.[7,8] So, the trapped charges that are being probed between two measurements can also be expressed as

$$Q_{\mathrm{it}}=qA_G\int D_{\mathrm{it}}(E)dE, \tag{2}$$

where q is the electronic charge, A_G is the gate area, and $D_{\mathrm{it}}(E)$ is the interface trap density at an energy E. The limits of integration in Eq. (2) should be selected as the energies corresponding to the pulse fall times. From the simple theory of emission,[7,10] an expression for the energy E can be obtained as

$$E-E_c=kT\ln\left[\nu_{\mathrm{th}}\sigma_n n_i\frac{|V_{\mathrm{IA}}|}{|V_{\mathrm{PH}}|}t_F\right], \tag{3}$$

where E_c, ν_{th}, σ_n, and n_i, are the silicon conduction band energy, thermal velocity, electron capture cross section, and intrinsic carrier density, respectively. V_{IA} is the pulse voltage drop from inversion to the onset of accumulation and V_{PH} is the pulse height. It is obvious in Eq. (3) that the interface traps at different energies can be probed by varying the pulse fall time t_F. Now, the derivative of Q_{it} with respect to pulse fall time t_F is given by

$$\frac{dQ_{\mathrm{it}}}{dt_F}=qA_G D_{\mathrm{it}}(E)\frac{dE}{dt_F}, \tag{4}$$

and using the above equations, an expression for the interface traps in the upper half of the band gap can be obtained as

$$D_{\mathrm{it}}(E)=\frac{t_F}{qA_G kT}\frac{dQ_{\mathrm{it}}}{dt_F}. \tag{5}$$

Likewise, the energy distribution of the interface traps in the lower half of the band gap can be obtained by deriving a similar set of equations and measuring the pulse rise time dependence of the capacitor currents.

Energy distribution of interface traps thus obtained using the proposed method is presented in Fig. 3 (solid lines). A standard value of 6.6×10^{-15} cm^2 for electron and hole capture cross section[9] has been used to calculate the energy distribution. The triangles in Fig. 3 represent the interface traps obtained by using the conductance method[1] on the same samples, while the circles represent the interface traps estimated from the charge pumping currents measured on n-MOS transistors fabricated with identical oxide thickness (2.8 nm) and process flow. These results demonstrate that the proposed method has estimated the interface trap distribution in the forbidden energy gap of silicon. Note that the increasing feature of the interface trap density toward the band's edges and the magnitudes are in good agreement with the

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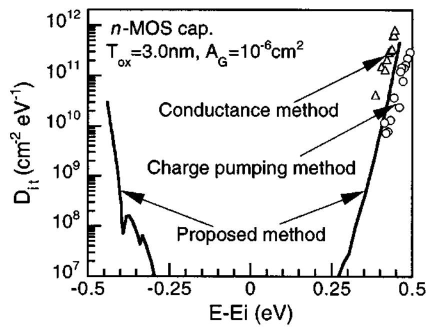

FIG. 3. Energy distribution of interface trap density as obtained using the proposed method. Triangles represent the interface traps obtained by the conductance method using the same *n*-MOS capacitors, while circles represent the interface traps obtained by the charge pumping method using *n*-MOS transistors with identical oxide thickness (2.8 nm).

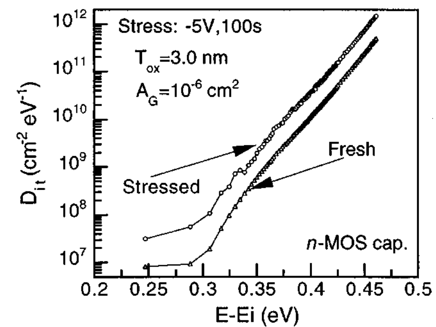

FIG. 4. Interface trap distribution in fresh and stressed (@−5 V for 100 s) samples.

reports of energy distribution of interface traps in MOS structures.[1,7,9] The validity and reliability of the proposed method is further examined by evaluating electrical stress induced interface trap generation. The interface trap densities measured before and after a constant voltage stressing at −5 V for 100 s are presented in Fig. 4. It reveals that the interfacial damage caused by high voltage stressing has been well measured. The nonsaturating feature of the distribution, as it approaches the band's edges (Figs. 3 and 4) can be explained as the result of carrier emission from bulk traps existing near the interface.

In summary, a simple and effective method of obtaining trap distribution at the Si/SiO_2 interface of MOS structures has been demonstrated. Bipolar pulse induced current through MOS capacitors and its dependence on the pulse fall/rise time is exploited to characterize the interface traps. The developed method does not require the knowledge of surface potential and doping profile curves and is free from any approximations and assumptions that are usually made in $C-V$ methods. Further, the method has been used to evaluate electrical stress induced interface trap generation in ultrathin MOS structures and hence can as well be used to probe hot-carrier and radiation induced interfacial damages. It is worth mentioning that the proposed method is a more accurate and reliable tool for quantitative characterization of the interface traps than the capacitance or the conductance methods that are often considered as qualitative.

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