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NH_3-annealed atomic-layer-deposited silicon nitride as a high-*k* gate dielectric with high reliability

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Extremely thin (equivalent oxide thickness, $T_{eq}=1.2$ nm) silicon-nitride high-k ($\epsilon_r=7.2$) gate dielectrics have been formed at low temperatures (≤550 °C) by an atomic-layer-deposition (ALD) technique with subsequent NH_3 annealing at 550 °C. A remarkable reduction in leakage current, especially in the low dielectric voltage region, which will be the operating voltage for future technologies, has made it a highly potential gate dielectric for future ultralarge-scale integrated devices. Suppressed soft breakdown events are observed in ramped voltage stressing. This suppression is thought to be due to a strengthened structure of Si–N bonds and the smoothness and uniformity at the poly-Si/ALD-silicon-nitride interface. © *2002 American Institute of Physics.*
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Scaling the dimension of metal-oxide-semiconductor field-effect transistors (MOSFETs) down to below 0.1 μm demands the thin ($T_{ox}<2.0$ nm) gate insulating (SiO_2) layers. This leads to large leakage current due to a tunnel current. One efficient way to reduce the leakage current is to use a gate dielectric with high dielectric constant, so-called high-*k* material, which provides a physically thicker film for the same electrically equivalent SiO_2 thickness (T_{eq}). Silicon nitride is an attractive candidate for this purpose due to its high relative dielectric constant ϵ_r (=7.5).[1] Besides this, the silicon nitride has the effect of suppression of boron penetration through thin gate oxides in *p*-MOSFETs. Another requirement for future gate dielectrics is the low thermal budget in the formation process to keep the precise doping profile in the ultrasmall devices. Besides, typical high thermal budget for fabricating oxynitride gate dielectrics[2–5] results in nitrogen incorporation at the SiO_2/Si interface, leading to reduction of the channel mobility.[6] Therefore, lower growth temperature of thin silicon nitride for a gate dielectric is a key for the fabrication of future ultralarge-scale integrated circuits (ULSIs).

Only a few methods have been proposed for such a low temperature growth of silicon nitride up to now.[7–10] Recently, we have developed a low temperature technique by employing self-limiting atomic-layer deposition (ALD) of silicon nitride.[11–14] We have also reported the preliminary results of the conduction mechanism of the leakage current through *p*-MOS capacitors with thin silicon-nitride gate dielectrics formed by ALD and their applicability to the future ULSIs.[15] In the previous study,[15] however, the dielectric constant ($\epsilon_r=5.7$) was obviously a little lower than the reported value.[1] Owing to this, the tunnel current remains only the same level as that of the SiO_2 gate dielectrics with the same T_{eq}.[15] In this study, we report the fabrication of ALD silicon-nitride high-*k* gate dielectrics with a substantially improved quality by employing a NH_3 annealing just after the deposition of silicon nitride. The annealing temperature is the same as the maximum temperature of the ALD, keeping the low thermal budget. The value of ϵ_r was improved to 7.2. This leads to the significant reduction of tunneling current compared with the SiO_2 gate dielectrics with the identical T_{eq}. In addition, the ALD silicon nitride shows the important aspect of suppression of the soft breakdown (SBD) phenomena.

The *n*-MOS capacitors have been fabricated using *p*-type Si (001) wafers (~10 Ω cm). The wafers were cleaned with a $NH_4OH:H_2O_2:H_2O=0.15:3:7$ solution at 80 °C for 10 min and terminated with hydrogen in a 0.5% HF solution to suppress the native oxidation. The silicon-nitride gate dielectrics were deposited by alternately supplying $SiCl_4$ and NH_3 gases. The $SiCl_4$ exposure at 340–375 °C followed by NH_3 exposure at 550 °C was cyclically repeated 20 times. The gas pressure of $SiCl_4$ and NH_3 during the deposition was 170 and 300 Torr, respectively. Just after the ALD, NH_3 annealing was carried out for 90 min at 550 °C. Then, a 200-nm-thick polycrystalline-Si (poly-Si) gate was deposited. $POCl_3$ diffusion at 900 °C was employed for gate doping and activation annealing. The T_{eq} value of the ALD silicon-nitride is determined to be 1.2 ± 0.2 nm from the ratio of the accumulation capacitances of the silicon nitride and the SiO_2 samples. Here, the capacitances were measured using the two frequency method and T_{ox} of the SiO_2 samples was estimated from the gate tunnel current versus gate voltage (I_g-V_g) characteristics. Transmission electron microscopy (TEM) observation was carried out using an Hitachi HF-2100 field emission TEM at 200 keV.

The surface microroughness measured using atomic force microscopy (AFM) is shown in Fig. 1 after the ALD of silicon nitride on a Si substrate. For comparison, we also measured the surface of conventional SiO_2 gate dielectrics formed by dry oxidation with subsequent wet etching using diluted HF solution. Here, the thickness of the ALD silicon nitride and SiO_2 was 2.2 and 2.3 nm from ellipsometry, respectively. The average surface microroughness (*Ra*) of the ALD silicon nitride was 0.010 nm [Fig. 1(a)]. The *Ra* of the

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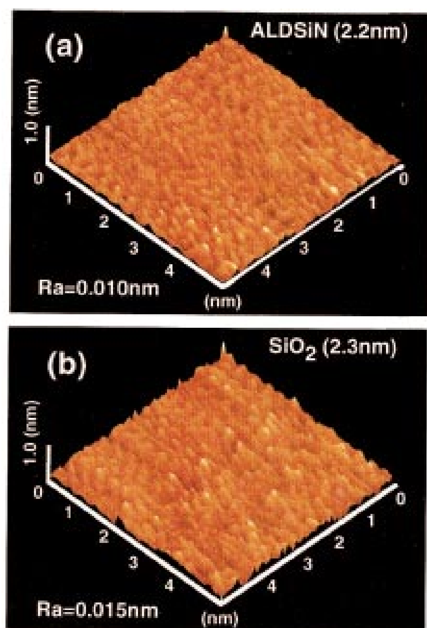

FIG. 1. (Color) Atomic force microscopy (AFM) image for (a) the surface of the fabricated ALD silicon nitride with NH_3 annealing (T_{phy}=2.2 nm from ellipsometry) on a Si substrate (average surface roughness *Ra* =0.010 nm), (b) conventional SiO_2 gate dielectrics with T_{ox}=2.3 nm (*Ra* =0.015 nm).

SiO_2 sample was 0.015 nm [Fig. 1(b)] and was slightly larger than that of the ALD silicon-nitride sample. This suggests the possibility of superior smoothness and uniformity of the poly-Si/ALD-silicon-nitride interface compared with the corresponding poly-Si/SiO_2 interface in SiO_2 samples. It should be noted that more rough surface is obtained for the silicon-nitride layer formed by the conventional low-pressure chemical vapor deposition.[15]

Figure 2 shows a high-resolution cross-sectional TEM micrograph of the ALD silicon-nitride gate dielectric. It is shown that the structure of the silicon nitride is amorphous. Also, extremely uniform thickness of the ALD silicon nitride and good smoothness was observed at the poly-Si/ALD-silicon-nitride interface. The physical thickness (T_{phy}) of the ALD silicon nitride was measured to be about 2.2 nm. As mentioned before, T_{eq} of the ALD silicon-nitride sample was 1.2 nm. Taking the T_{phy} value obtained from the TEM measurement into account, the ϵ_r value of the ALD silicon nitride is obtained to be 7.2. Compared with the ϵ_r value (5.7) of the ALD silicon nitride formed without NH_3 annealing previously reported,[15] the ϵ_r value increased significantly with the NH_3 annealing. We think that the stoichiometry of the dielectric was improved with NH_3 annealing resulting in

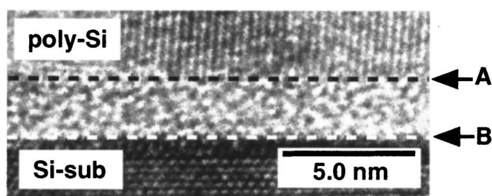

FIG. 2. High-resolution cross-sectional TEM micrograph of the fabricated ALD silicon-nitride gate dielectric with NH_3 annealing. Broken lines indicate the poly-Si/dielectric (marked as A) and the dielectric/Si-substrate (marked as B) interfaces.

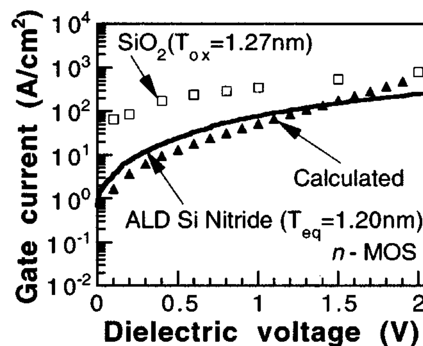

FIG. 3. Gate leakage current as a function of dielectric voltage (V_{di}) of the fabricated *n*-MOS capacitor having the ALD silicon-nitride gate dielectric with NH_3 annealing (solid line). The open squares represent the reported data for the gate SiO_2 of the same T_{eq}=1.27 nm (see Ref. 17). Calculated results using direct tunnel current model (see Ref. 17) are presented by closed triangles.

higher ϵ_r. The low ϵ_r value of the as-grown ALD silicon nitride is speculated to be due to the existence of dangling bonds accompanied with microvoids and/or hydrogen contamination. Oxygen contamination does not seem to be the reason for the low ϵ_r since Si–O bonds do not change to Si–N bonds by the low temperature annealing (550 °C) in NH_3 from the viewpoint of bonding energy.[16]

Figure 3 shows the gate leakage current as a function of dielectric voltage (V_{di}) across the ALD silicon nitride. Here, $V_{di}=V_g-\phi_s-V_{fb}$ where ϕ_s and V_{fb} are the surface potential of silicon and flatband voltage, respectively. For comparison, we also showed the leakage current for the MOS capacitor with the gate SiO_2 of T_{ox}=1.27 nm.[17] Significant reduction of the current level was observed for the ALD silicon-nitride sample compared with that for the SiO_2 dielectric with even thicker T_{ox}, especially at the low dielectric voltage region (<1 V). Previously, it was reported that the conduction mechanism through the ALD silicon nitride is probably the direct tunneling.[15] Accordingly, we calculated the direct tunnel currents through the silicon nitride using the same barrier height of silicon nitride (~2.0 eV) and electron effective mass (0.3 times the free electron mass) as those in the previous report.[15] The result (closed triangles) for T_{phy} =2.2 nm shows reasonable agreement with the experimental data. The remarkable reduction in leakage currents especially in the low dielectric voltage region is due to the thicker T_{phy} of silicon nitride. Since the low dielectric voltage region (≤1 V) will be the operating region for future technologies, ALD silicon nitride has a high potential to be used as a high-*k* gate dielectric for future ULSI devices.

Figures 4 and 5 show the typical stress-induced leakage and breakdown characteristics of *n*-MOS capacitors with the ALD silicon-nitride gate dielectric and with the conventional SiO_2 dielectric, respectively. The dielectric quality is investigated by ramped-voltage stress-induced electrical-breakdown measurements wherein the maximum gate voltage is slightly increased in successive measurement cycles. The ALD silicon-nitride dielectric shows excellent stability against high voltage stressing and a small amount of stress-induced leakage current (SILC) flows through the gate before a sharp and sudden breakdown [hard breakdown (HBD)] (Fig. 4). An exciting feature is the disappearance of the SBD phenomenon. It is to be noted that the suppression of the

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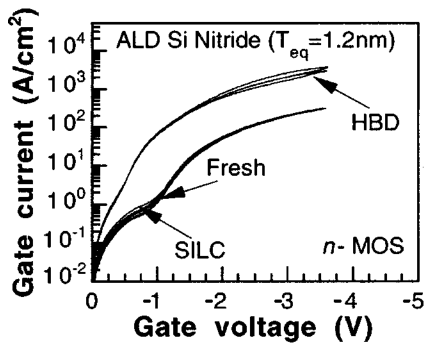

FIG. 4. Ramped-voltage stress induced gate-current density as a function of gate voltage for the *n*-MOS capacitor having the ALD silicon-nitride gate dielectric with NH_3 annealing.

SBD phenomena is also observed for the samples of ALD silicon-nitride gate dielectrics without NH_3 annealing (not shown). The *p*-MOS capacitors with ALD silicon-nitride dielectrics also show the disappearance of the SBD phenomenon (not shown). On the other hand, all known stress-induced features (SILC, SBD, HBD) are present in the conventional *n*-MOS (Fig. 5) and *p*-MOS (not shown) capacitors with SiO_2 gate dielectrics. Similar results for SiO_2 gate dielectrics were also observed in other reports.[18]

For SiO_2 gate dielectrics, it is reported that the conductive filaments near the SiO_2/Si-substrate interface are formed.[19,20] The localized conductive filaments near the poly-Si/SiO_2 interface may be formed in addition to the SiO_2/Si-substrate interface. The conductive filament is caused by the injected carriers during high voltage stressing and a week stability originated from the strained Si–O bonds.[21] Poor roughness characteristics, which will cause the concentration of the dielectric field, can be another reason for the formation of the conductive filaments near the poly-Si/SiO_2 interfaces.[22,23] These conductive filaments from both the interfaces trigger the SBD through a reduction of effective oxide thickness, leading to the eventual HBD. To the contrary, formation of the conductive filaments at the poly-Si/ALD-silicon-nitride and ALD-silicon-nitride/Si-substrate interface is suppressed due to a strengthened structure of Si–N bonds,[24] leading to the SBD suppression. Another possible reason is that the superior smoothness and uniformity at the poly-Si/ALD-silicon-nitride interface compared with those at the corresponding poly-Si/SiO_2 interface (Fig. 1) suppress the concentration of the dielectric field, leading to the SBD suppression. It should be noted that the SILC observed in the ALD silicon-nitride sample (Fig. 4) is considered to be caused by the trap in bulk silicon nitride.

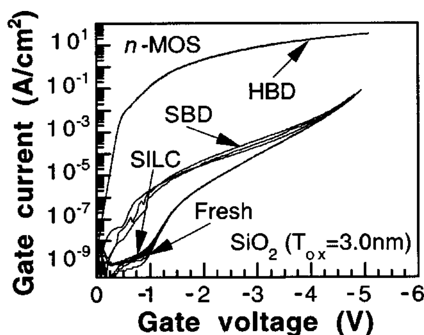

FIG. 5. Ramped-voltage stress induced gate-current density as a function of gate voltage for the *n*-MOS capacitor with the conventional SiO_2 dielectric (T_{ox}=3.0 nm). Only the first two of SBD events are presented. Several such SBD events are observed before the HBD in each device (not shown in the figure).

In summary, we reported thin (T_{eq}=1.2 nm) ALD silicon-nitride high-*k* gate dielectrics with NH_3 annealing. Extremely good flatness at the poly-Si/ALD-silicon-nitride interface was confirmed by AFM and TEM measurements of the ALD silicon nitride. A remarkable reduction in leakage currents, especially in the low dielectric voltage region has made it a highly potential gate dielectric for future ULSI devices. An exciting feature of no soft breakdown (SBD) events is observed in ramped voltage stressing. This disappearance is probably due to a strengthened structure of Si–N bonds and the superior smoothness and uniformity at the poly-Si/ALD-silicon-nitride interface. Because of extremely uniform thickness control capability in the thin thickness region and the low thermal budget of the ALD process ($\leq$550 °C), the ALD silicon nitride is promising candidate for the ultrathin gate dielectrics for deep submicron complementary MOS transistors taking into account the good barrier characteristics for the boron penetration.

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