Low-temperature formation of silicon nitride gate dielectrics by atomic-layer deposition

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Thin (equivalent oxide thickness T_{eq} of 2.4 nm) silicon nitride layers were deposited on Si substrates by an atomic-layer-deposition (ALD) technique at low temperatures (<550 °C). The interface state density at the ALD silicon nitride/Si-substrate interface was almost the same as that of the gate SiO_2. No hysteresis was observed in the gate capacitance–gate voltage characteristics. The gate leakage current was the level comparable with that through SiO_2 of the same T_{eq}. The conduction mechanism of the leakage current was investigated and was found to be the direct tunneling. The ALD technique allows us to fabricate an extremely thin, very uniform silicon nitride layer with atomic-scale control for the near-future gate dielectrics. © *2001 American Institute of Physics.*
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As the dimension of semiconductor devices is scaled down, the conventional processing temperature over 900 °C, such as the typical high thermal budget in the formation process of oxynitride gate insulators, will be incompatible with the desired device structures.[1,2] Besides this, suppression of boron penetration through thin gate oxides in *p*-channel metal–oxide–semiconductor field-effect transistors and the reduction of the gate leakage current are important challenges for the deep submicron complementary metal–oxide–semiconductor (CMOS) technology. Silicon nitride is known to have an effect of suppression of boron penetration.[3] On the other hand, one efficient way to reduce the leakage current is to use a gate insulator with high dielectric constant which provides a physically thicker film for the same electrically equivalent SiO_2 thickness (T_{eq}). Again, silicon nitride is an attractive candidate for this purpose due to its relatively high dielectric constant.[4] Therefore, the lower growth temperature of thin silicon nitride for a gate insulator is a key for the fabrication of future ultralarge-scale integrated circuits (ULSIs).

Only a few methods have been proposed for such a low temperature growth of silicon nitride up to now.[1–4] Hence, there have been only a few reports[4] of the conduction mechanism of the gate leakage current in such thin silicon nitride layers. Recently, we have developed a low temperature technique by employing a self-limiting atomic-layer deposition (ALD) of silicon nitride.[5–8] Also, we have fabricated the stacked gate dielectrics with extremely thin silicon nitride ($T_{eq}=0.2$ nm) on SiO_2(2.0 nm) using the ALD technique and showed the suppression of boron penetration.[5] In this study, we have applied the ALD technique to the fabrication of a thin gate insulator of silicon nitride and examined the conduction mechanism of the leakage current and applicability to the future ULSIs.

The MOS capacitors have been fabricated using *n*-type Si (001) wafers (~15 Ω cm). The wafers were cleaned with an $NH_4OH:H_2O_2:H_2O=0.15:3:7$ solution at 80 °C for 10 min and were terminated with hydrogen in a 0.5%HF solution to suppress the native oxidation. The silicon nitride gate insulator was deposited by alternately supplying $SiCl_4$ and NH_3 gases. The $SiCl_4$ exposure at 375 °C followed by NH_3 exposure at 550 °C was cyclically repeated 20 times, leading to a silicon nitride physical thickness of ~3.5 nm as estimated from transmission electron microscopy (TEM). The gas pressure of $SiCl_4$ and NH_3 during the deposition was 170 and 300 Torr, respectively. The substrate temperature was changed by a computer synchronized with the gas-supply sequence. After the ALD silicon nitride deposition, a 200-nm-thick polycrystalline-Si gate was deposited and implanted by 20 keV BF_2^+ at a dose of $5\times10^{15}\ cm^{-2}$. Subsequently, the activation annealing was performed at 850 °C for 10 min in a N_2 ambient. For comparison, p^+ polycrystalline-Si gate capacitors with a gate SiO_2 grown by dry oxidation at 850 °C were also fabricated. The SiO_2 thickness (T_{ox}) of the SiO_2 samples were estimated from the gate tunnel current versus gate voltage (I_g–V_g) characteristics. The equivalent thickness (T_{eq}) of the ALD silicon nitride sample is determined to be 2.4 nm from the ratio of the accumulation capacitance between the silicon nitride sample and the SiO_2 sample with $T_{ox}=2.1$ nm. Considering the physical thickness obtained from TEM measurement, the relative dielectric constant of the ALD silicon nitride is obtained to be ~5.7.

The surface microroughness measured using atomic force microscopy (AFM) are shown in Fig. 1 after the ALD of silicon nitride on a Si substrate. For comparison, we also measured the surface of silicon nitride deposited on a Si substrate using the conventional low pressure chemical vapor deposition (LPCVD) at 750 °C using SiH_2Cl_2 and NH_3. Here, the thickness of the ALD silicon nitride was 0.9 nm from ellipsometry. The average surface microroughness (R_a) of the ALD silicon nitride [0.023 nm, Fig. 1(a)] was almost the same as that of the underlying Si substrate ($R_a=0.021$ nm). In contrast, the surface microroughness of the thin (1.7 nm from ellipsometry) LPCVD silicon nitride ($R_a=0.042$ nm) is much larger than that of the ALD silicon nitride sample as shown in Fig. 1(b). Interestingly, for the thick LPCVD silicon nitride (7.3 nm from ellipsometry), the

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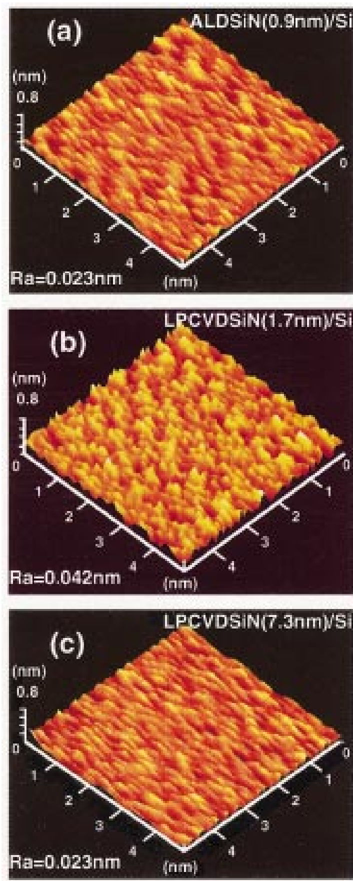

FIG. 1. (Color) AFM image for (a) the surface of the ALD silicon nitride on a Si substrate (average surface roughness $R_a = 0.023$ nm), (b) LPCVD silicon nitride with the thickness of 1.7 nm ($R_a = 0.042$ nm), and (c) LPCVD silicon nitride with the thickness of 7.3 nm ($R_a = 0.023$ nm).

surface microroughness decreases ($R_a = 0.023$ nm) [Fig. 1(c)]. The increased surface microroughness of the thin LPCVD silicon nitride on a Si substrate is probably ascribed to the three-dimensional nucleation growth. This result indicates that the ALD silicon nitride has a great advantage concerning the surface microroughness especially in thin thickness region compared with the silicon nitride formed by the conventional LPCVD method. It is noted that the three-dimensional nucleation also occurs in the early stages of thermal nitridation of silicon.[9,10] This also implies that the ALD is the important formation method of very thin silicon nitride in view of thickness uniformity.

Figure 2 shows the capacitance–gate voltage ($C-V_g$) characteristics of the p^+ polycrystalline-Si gate capacitors with the ALD silicon nitride ($T_{eq} = 2.4$ nm) and with the thermal $SiO_2(T_{ox} = 2.1$ nm). All the measurements were carried out at 1 kHz. The $C-V_g$ curve for the ALD silicon nitride sample shows a shift to a negative voltage side by approximately 0.1 V with respect to that for the SiO_2 sample: V_{fb} is 0.59 V for ALD silicon nitride sample and 0.70 V for the SiO_2 sample. Since the previous V_{fb} of the SiO_2 sample ($T_{ox} = 2.1$ nm) is the same as that ($V_{fb} = 0.70$ V) with thicker $SiO_2(T_{ox} = 3.0$ nm), the boron penetration to the substrate[11] was considered to be suppressed in the SiO_2 sample of $T_{ox} = 2.1$ nm at the employed anneal condition (850 °C, 10 min). Almost the same shape of the $C-V_g$ curves between the ALD silicon nitride and SiO_2 samples suggests the interface

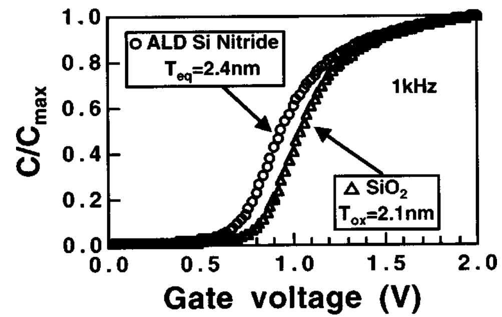

FIG. 2. Capacitance–gate voltage ($C-V_g$) characteristics at 1 kHz for p MOS capacitors annealed at 850 °C for 10 min. The SiO_2 thickness is 2.1 nm from the gate tunnel current vs dielectric voltage (I_g-V_{di}) characteristics for the sample with the gate SiO_2. The accumulation capacitance is 116 pF for the SiO_2 sample and 100 pF for the ALD silicon nitride sample at a V_{di} of 1.3 V. The equivalent oxide thickness (T_{eq}) of the ALD silicon nitride is 2.4 nm for the ALD sample. Capacitance was normalized using the maximum capacitance value (at $V_{di} = 1.3$ V) for each curve. Curves were shown for both the upward and downward gate voltage sweeps.

state density of the ALD silicon nitride sample is almost the same as that of the SiO_2 sample. Therefore, the negative V_{fb} shift of the ALD silicon nitride sample is considered to be due to the positive fixed charge in the film. The amount of the fixed charge was estimated to be 7.5×10^{11} cm^{-2}. Also, no hysteresis was observed (or less than 1 mV) in the $C-V_g$ curves for the ALD silicon nitride and SiO_2 samples. This indicates that the amount of the traps at the ALD silicon nitride/Si-substrate interface is extremely smaller than those reported,[12–14] suggesting the superiority of the ALD silicon nitride film. It is noted that Ma also reported no discernible hysteresis in the high-frequency $C-V_g$ curve in Ref. 4, indicating extremely low trap densities for the silicon nitride gate dielectrics formed by the jet vapor deposition.

Figure 3 shows the gate leakage current as a function of dielectric voltage (V_{di}) across the ALD silicon nitride. Here, $V_{di} = V_g - \phi_s - V_{fb}$ where ϕ_s and V_{fb} are surface potential of silicon and flatband voltage, respectively. For comparison, we also showed the leakage current for the MOS capacitor with gate SiO_2 of the same $T_{eq}(=2.4$ nm).[15] Comparable current level was observed for the ALD silicon nitride sample to that for the no-ALD sample with the same T_{eq} especially at the low dielectric voltage region (<1 V).

To investigate the conduction mechanism in the ALD

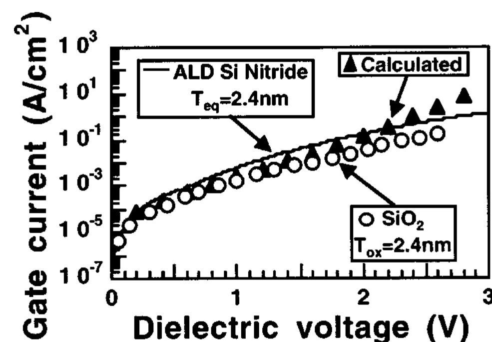

FIG. 3. Gate leakage current as a function of dielectric voltage (V_{di}) of the MOS capacitor with ALD silicon nitride gate dielectrics (solid line). For reference, the experimental data for the gate SiO_2 of the same $T_{eq} = 2.4$ nm (see Ref. 15) are also shown (open circles). Calculated direct tunnel currents through the silicon nitride are also plotted (closed triangles) using the barrier height of 2.0 eV and the physical thickness of 3.5 nm.

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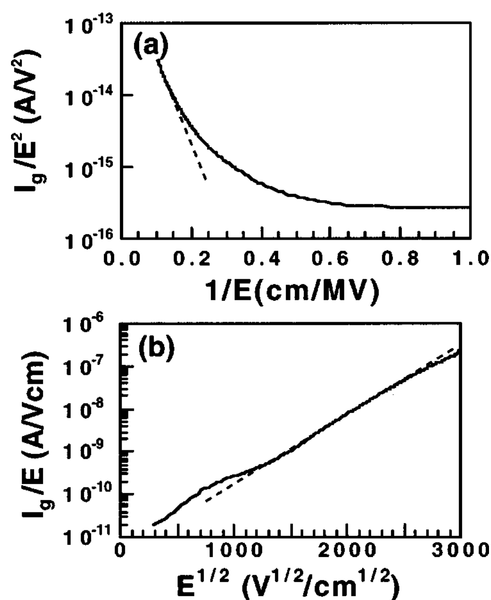

FIG. 4. F–N (a) and F–P (b) plots of leakage current characteristics of the MOS capacitor with ALD silicon nitride gate dielectrics in Fig. 3. Here, I_g and E represent the gate current density and dielectric field, respectively.

silicon nitride, we show the Fowler–Nordheim (F–N) and Frenkel–Poole (F–P) plots of the gate current–dielectric field ($I_g - E$) characteristics of the ALD silicon nitride sample in Fig. 4. In Fig. 4(a), $I_g - E$ characteristics clearly do not show a linear relation in the low dielectric field region ($1/E > 0.2$ cm/MV). Here, $E = V_{di}/T_{phy}$, where T_{phy} is the physical thickness of the silicon nitride. In high E region ($0.12 < 1/E < 0.2$ cm/MV), the barrier height obtained from the slope of the fitted broken linear line in Fig. 4(a) was 0.9 eV. This value is too small for the silicon nitride/Si barrier.[4] These results indicate that the conduction mechanism is not the F–N tunneling in the low dielectric field region studied in this letter. Similarly, the relative dielectric constant obtained from the slope of the broken linear line in Fig. 4(b) was 59, which is too large for silicon nitride. This suggests that the conduction mechanism is not the F–P conduction. In Fig. 3, calculated direct tunnel currents were shown using an effective mass of 0.3 times the free electron mass (closed triangles). When the barrier height is 2.0 eV, which is almost the same as that reported by Ma,[4] the calculated $I_g - V_{di}$ characteristics for the physical thickness of 3.5 nm fits well to the experimental one (solid line). Here, the thickness of 3.5 nm is consistent with the TEM results. Therefore, the conduction mechanism is probably the direct tunneling.

In summary, the thin ($T_{eq} = 2.4$ nm) ALD silicon nitride gate dielectrics have been applied to the gate insulator for future ULSIs. Almost the same shape of the $C - V_g$ curves between the ALD silicon nitride and SiO_2 sample suggests the interface state density of the ALD silicon nitride sample is almost the same as that of the SiO_2 sample. No hysteresis in the $C - V_g$ curve shows the extremely small amount of the traps at the ALD silicon nitride/Si-substrate interface. The gate leakage current is comparable to the level of the gate SiO_2 with the same T_{eq}. The conduction mechanism is considered to be the direct tunneling. Because of extremely uniform thickness control capability in the thin thickness region and the low thermal budget of ALD process (<550 °C), the ALD silicon nitride thin gate dielectrics combining with the other electrically high barrier insulator formed at low temperatures is a promising candidate for the ultrathin gate dielectrics for deep submicron CMOS transistors taking into account the good barrier characteristics for the boron penetration.

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