Low-temperature selective deposition of silicon on silicon nitride by time-modulated disilane flow and formation of silicon narrow wires

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The low-temperature (410 °C) selective deposition of Si on silicon nitride has been achieved by means of the time-modulated flow of disilane while a very small amount of Si is deposited on SiO_2. Very narrow (21 nm width and 28 nm thick) Si wires have been fabricated using the selective deposition. The resistivity of the Si wires fabricated by the selective deposition is much smaller ($\sim$1/5) than that fabricated by the conventional reactive ion etching followed by annealing. This technique will be applicable to the formation of a polycrystalline silicon gate with small resistivity for the high-performance ultrasmall metal–oxide–semiconductor transistors and quantum effect devices. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1387260]

The selective deposition technique has a big potential to fabricate structures with very narrow width which is not limited by the lithography resolution. We have been studying a selective atomic-layer deposition of silicon nitride on silicon and no deposition on SiO_2.[1,2] When the selective deposition of Si on silicon nitride and no deposition on SiO_2 is achieved, very narrow Si wires separated by the silicon nitride films can be integrated combined with this technique as shown in Fig. 1. In this case, the Si and silicon nitride films are alternately deposited on the sidewall of the SiO_2/silicon nitride/SiO_2 stacked structures.

Many studies concerning the selective deposition (including epitaxial growth) of Si have been reported.[3–7] In most cases, the selective deposition (or epitaxial growth) is carried out on the Si substrate partially covered with patterned SiO_2 or silicon nitride (Si_3N_4) film.[4–6] In a special case, the selective deposition (nucleation) on Si_3N_4 was achieved by Yonehara *et al.*[3] with a selectivity of 10^2-10^3 compared to a SiO_2 substrate at a relatively high growth temperature of 950 °C using SiH_2Cl_2. Yasuda *et al.*[7] also reported that a high density of Si nuclei is formed on Si_3N_4 substrate in the ultrahigh vacuum chemical vapor deposition (UHV-CVD) using Si_2H_6 at 580 °C.

In this letter, we report a method for the selective deposition of Si on Si_3N_4 at a lower temperature (410 °C) by the time-modulated flow of disilane (Si_2H_6). Very narrow (21 nm width) Si wires have been fabricated using the selective deposition and the electrical properties have been measured. The resistivity of the Si wires fabricated by the selective deposition is much smaller than that fabricated by the conventional reactive ion etching (RIE) followed by annealing.

The Si_2H_6 gas (He balance, 5%) is periodically admitted into the quartz chamber with an adequate interval time as shown in Fig. 2. The substrate was heated by a halogen lamp synchronized with the gas supply. The details of the experimental apparatus are in a previous paper.[8] There exists an incubation time before starting the Si film growth on SiO_2 in the UHV-CVD using Si_2H_6.[5] The incubation-time difference depending on the substrate material (Si or SiO_2) was utilized to the selective epitaxial growth.[5] However, in the continuous gas flow, the film thickness of the selective deposition is limited by the incubation time. The intermittent gas flow is expected to relieve the thickness limitation of the selective deposition, since the substrate surface condition may approach to the initial condition by the desorption of the adsorbed species during the vacuum evacuation. The chemistry of this selective deposition is completely different from that in the flow-modulated plasma enhanced selective chemical vapor deposition (CVD) using SiH_4 (Ref. 6) where hydrogen plasma etching during the interval between SiH_4 flow is essential.

The temperature dependence of the deposition rate of Si on thermal SiO_2 (grown at 1000 °C in O_2+H_2) and Si_3N_4 (deposited by a low-pressure CVD using SiH_2Cl_2 and NH_3 at 750 °C) is shown in Fig. 3. Both substrate surfaces were treated in the diluted HF followed by deionized water rinse for 1 min and spin dried. Therefore, the SiO_2 surface is O–H terminated,[9] while the bonded hydrogen does not exist on the Si_3N_4 surface[1] which was verified by the Fourier transform infrared attenuated total reflection spectroscopy. It is recognized that the Si film is selectively deposited on the Si_3N_4 surface with a small amount of Si deposition on SiO_2 in the two growth conditions. One is the high-temperature (>580 °C) and low-pressure (10^{-5} Torr) condition and the other is the low-temperature (<500 °C) and high-pressure (10^{-3} Torr) condition. The mechanism for the selective growth in the high-temperature and low-pressure region must be the reaction, $Si+SiO_2 \rightarrow 2SiO$ (with high vapor pressure),[10] resulting in a small amount of deposition on

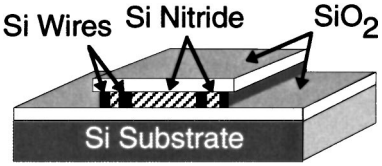

FIG. 1. Integration of Si nanowires by using the selective deposition of Si and silicon nitride is shown.

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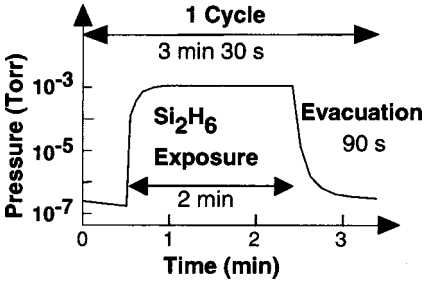

FIG. 2. Pressure versus time for the time-modulated flow method is shown. The substrate temperature was controlled synchronized with the gas supply. The lamp was off during the vacuum evacuation.

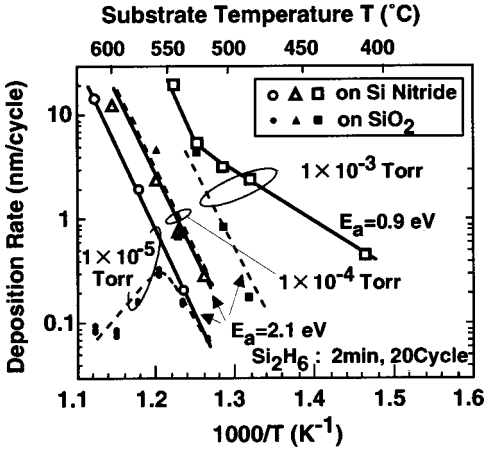

FIG. 3. Temperature dependence of the Si deposition rate on SiO_2 and on Si_3N_4 is shown. The deposition cycle is 20, and the deposited film thickness was measured by the ellipsometry.

SiO_2. The activation energy of 2.1 eV observed in Fig. 3 fits well to that of thermal dissociation of Si_2H_6.[11] On the other hand, at the low-temperature and high-pressure condition the growth rate on Si_3N_4 is remarkably enhanced and the activation energy of 0.9 eV is obtained. The enhancement of the growth rate may be partly due to the short incubation time on Si_3N_4 (Ref. 12) compared to that on SiO_2 and partly due to a kind of catalytic surface reaction on the Si_3N_4 surface. However, the detailed mechanism and the physical meaning of the activation energy of 0.9 eV remain unclear at present. It should be noticed that for the $Si_{1-x}Ge_x$ CVD using SiH_4 and GeH_4, the shorter incubation time on Si_3N_4 compared with that on SiO_2 is reported.[12]

The Si selective deposition was carried out on the $SiO_2/Si_3N_4/SiO_2$ sidewall formed by the RIE using CF_4+H_2 gas mixture. Figure 4 shows the cross sectional scanning electron microscope (SEM) images for different growth conditions. The Si wires of ~30 nm width are formed on the sidewall of the Si_3N_4 at the high-temperature, low-pressure condition [Fig. 4(a)] and at the low-temperature, high-pressure condition [Fig. 4(c)]. On the other hand, at the high-temperature, medium-pressure condition (600 °C and 10^{-4} Torr) [Fig. 4(b)], the Si film is conformably deposited on the whole surface.

The electrical properties of the Si wires were evaluated. Because of their smaller surface roughness than that grown at the high-temperature condition, the Si wires were fabricated under the low-temperature (410 °C) and high-pressure (10^{-3} Torr) condition. After the selective Si deposition, phosphorous doping using $POCl_3$ at 850 °C was carried out (see Table I). Then, a thin Si film grown on SiO_2 (a small amount of deposition occurs on SiO_2 even for the selective deposition) was removed by the chemical dry etching using remote microwave plasma of CF_4+O_2. The passivation layer formation (nondoped and phosphorous doped silicate glass, both 300 nm thick) by the atmospheric CVD at 400 °C, the contact hole formation by the wet etching, the Al sputter deposition and patterning by the wet etching were carried out. Finally, the sample was annealed at 450 °C for 30 min in a H_2+N_2 mixture to reduce the contact resistance. The size of the fabricated Si wires was 21 nm width×28 nm thick from the SEM observation.

Figure 5(a) shows the current–voltage ($I-V$) curves for the fabricated Si wires at room temperature (23 °C), which indicates the linear $I-V$ relationship. The length dependence of the resistance of the Si wires is plotted in Fig. 5(b), from which the resistivity of the Si wires is calculated. The result is summarized in Table I with the data for the Si wires fabricated by the RIE followed by annealing at 850 °C for 30 min. For the selective deposition sample, the resistivity is about 1/5 times that of the RIE sample, even though the phosphorous is more heavily doped. The large resistivity for the RIE sample is reported to be due to the plasma-induced damage at the etched sidewall of the Si wire during the RIE.[13] Actually, the resistivity increases by about one order of magnitude after the RIE as listed in Table I. Namely, the diffused phosphorous atoms are trapped and deactivated in the damaged region.[13] This effect becomes remarkable as the wire width is narrower. On the other hand, the Si wires fabricated by the selective deposition have no plasma damage, resulting in the high conductivity even though the size is smaller than the RIE sample.

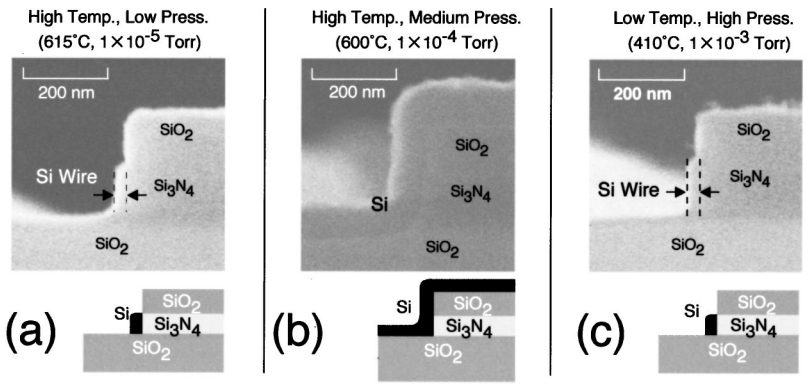

FIG. 4. Cross sectional SEM images for different growth conditions are shown. The deposition cycle is 60. The bottom parts indicate the schematic of the structures. The top SiO_2 layer was deposited by the atmospheric CVD at 400 °C, while the bottom SiO_2 layer was thermally grown at 1000 °C.

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TABLE I. Comparison between RIE (plasma etching) and selective deposition samples is shown. The resistivity of the Si wire was obtained from the $I-V$ characteristics, while that for the sample "before etching" was measured by the four-probe method. Detailed fabrication process of the RIE sample is in Ref. 13. W and T in the column of "Size" mean width and thickness of the Si wire, respectively.

Method	Plasma etching	Selective deposition
Size (nm)×(nm)	70(W)×220(T)	21(W)×28(T)
Resistivity (Ω cm)	2.6×10^{-2} (Before etching 2.1×10^{-3})	5.8×10^{-3}
$POCl_3$ doping	Flow 850 °C, 30 min Drive-in 850 °C, 10 min	Flow 850 °C, 10 min Drive-in 850 °C, 10 min
Postanneal	850 °C, 30 min	···

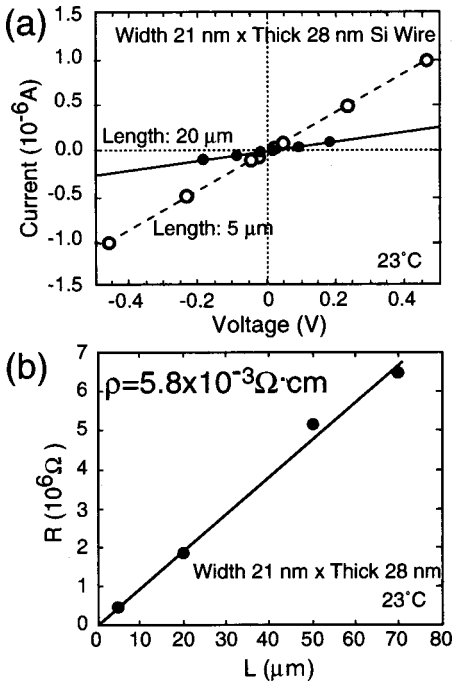

FIG. 5. (a) $I-V$ curves for the Si wires of 21 nm width×28 nm thick and (b) length dependence of the resistance of the Si wires are shown.

In conclusion, a low-temperature (410 °C) selective deposition method for Si, "time-modulated flow method," was developed. Owing to the low-growth temperature, the smooth surface is obtained. The Si wires with the size of 21 nm width×28 nm thick were fabricated by using the selective deposition. They have a larger conductance than that fabricated by the RIE. From the viewpoint of the good surface smoothness and low-temperature process with no damage, this technology can be used for the fabrication of the low resistivity polycrystalline silicon gate for the ultrasmall transistors and quantum effect devices.

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