

Characterization of Electronic Charged States of Si-Based Quantum Dots and Their Application to Floating Gate Memories

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Nanometer-size Si quantum dots (Si-QDs) with and without Ge core were prepared on thermally-grown SiO₂ in a self-assembling manner by controlling the early stages of low pressure chemical vapor deposition (LPCVD). The surface potential changes in individual dots caused by charging or discharging of one electron or a few as were measured by using a Kelvin probe technique in an atomic force microscope (AFM). For Si-QDs larger than 20nm in dot height, surface potential images with a characteristic potential profile with a dimple around the center of the charged dots are observable after electron or hole injection, indicating Coulomb repulsion among the charges retained in the dot. For Si-QDs with a Ge core, electrons are retained stably in Si clad while holes in Ge core, reflecting the energy band discontinuity at the interface between the Si clad and the Ge core. The influence of phosphorous doping to Si-QDs on their electron charging and discharging characteristics was also been studied. Electrical characteristics of metal-oxide-semiconductor (MOS) capacitors and n-channel MOS field-effect-transistors (nMOSFETs) with Si-QDs floating gates confirm multiple-step charging to and discharging from the Si-QDs floating gate at room temperature. From the temporal changes in the drain current with gate voltage switching, it is suggested that the change in the electron distribution in the Si-QDs floating gate play an important role to trigger the transition from a metastable charged state to the next charged state.

Introduction

The application of silicon-quantum-dots (Si-QDs) to a floating gate in MOSFETs has received increasing attention because of a few advantages to a conventional planer floating gate. The charge storage in individual Si-QDs can improve practically charge retention and endurance characteristics against the situation of dielectric wear-out, which enables us to decrease the tunneling oxide thickness for faster writing and erasing operations [1-2]. Another potential advantage is multi-valued memory capability reflecting discrete charged states in the Si-QDs floating gate [3-6]. Since both charging energy and quantization energy in each of Si-QDs are strongly size dependent, one of major concerns to achieve the multi-valued reliable operations at room temperature and above is the size uniformity of Si-QDs with an areal density comparable to the channel electron density. In that regard, the self-assembling process is thought to be adequate to control the formation of high density Si-QDs on SiO₂. So far, we have reported that, by controlling the early stages of low-pressure chemical-vapor deposition (LPCVD) using SiH₄ [7], Si-QDs are formed spontaneously with a fairly uniform size distribution and a high areal density ($>10^{11}\text{cm}^{-2}$) on thermally-grown SiO₂ and demonstrated multiple-step electron

charging in the Si-QDs floating gate [5, 6].

In this paper, from recent experimental results on electron charging and discharging characteristics of the Si-QDs floating gate, we discuss a role of Coulomb interaction among electrons in neighboring charged QDs and in channel into the characteristic progress of charge distribution in the Si-QDs floating gate.

Sample Preparation and Experimental Details

After conventional wet-chemical cleaning steps of Si(100) wafers, 2.4-4.1nm thick SiO₂ layers were grown by 1000°C oxidation in 2% O₂ diluted in N₂. Subsequently, hemispherical single-crystalline Si nanocrystals as quantum dots (QDs) were self-assembled on the ultrathin SiO₂ layers by controlling the early stages of LPCVD typically at 575°C using a SiH₄ gas [7]. For direct measurements of surface potential changes caused by electron injection to and emission from the Si dots using a Kelvin probe technique in atomic force microscopy (AFM), the dot surface was covered with 2nm-thick SiO₂ formed by 900°C in dry O₂. In the preparation of Si dots with a Ge core, we controlled CVD conditions for selective deposition of Ge on pre-grown hemispherical Si dots/SiO₂ at 400°C using 5% GeH₄ diluted with He and for subsequent Si capping with almost no new Si nucleation at a SiH₄ pressure as low as 0.02Torr at 540°C. The formation of Si dots with a Ge core was confirmed by high-resolution transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) [8].

For MOS capacitors and FETs with Si dots as a floating gate, a ~7.5nm-thick SiO₂ as a control oxide layer was formed conformally on Si-QDs by the following process flow. After the Si dot formation, the dot surface was first oxidized at 850°C in dry O₂ to form a ~1.0nm thick SiO₂ layer and subsequently dipped in a 0.1% HF solution to make uniform surface termination with OH bonds. And then, the surface was covered with a ~3.3nm-thick amorphous Si layer by LPCVD using 10% Si₂H₆ in He at 440°C, and followed by complete oxidation of the a-Si layer in dry O₂ at 1000°C. By repeating the Si dot formation and the surface oxidation, double-stacked structures of Si-QDs with an ~1.0nm thick SiO₂ interlayer were fabricated. The average dot height and the total dot density evaluated by AFM measurements were ~8.0nm and ~2.5x10¹¹cm⁻²/cycle for MOS capacitors, and ~7.2nm and ~6.0x10¹¹cm⁻² for n-MOSFETs with double-staked Si-QDs, respectively. Finally Al gates for MOS capacitors and n⁺-poly gates with 0.5~1.0μm in length and 10μm in width for n-MOSFETs were fabricated.

Results and Discussion

Evaluation of Electronic Charged States of Single Si Dot with and without a Ge Core by an AFM/Kelvin Probe Method

To examine charged states of individual dots by using an AFM/Kelvin probe method [9, 10], pure Si dots and dots with a Ge core were formed with an areal dot density as low as ~10⁸cm⁻² in consideration with a lateral resolution of the Kelvin probe method used in this study. Before and after scanning an electrically-biased Au- or Rh-coated AFM tip on the sample surface in a tapping mode, the topographic images and corresponding surface potential images were simultaneously taken in a non-contact Kelvin probe mode. A series of these experiments was made under clean room air at room temperature.

Figure 1 shows the surface potential change observed for individual Si-QD as a function of dot height with the simulated results. The surface potential change increases with decreasing dot size. At each dot size, the observed surface potential change on the charged dot is almost equal to the calculated value for the case that one

electron is retained in the dot. In the calculation, we assumed a simple equivalent circuit model as shown in the inset of Fig. 2. In the Kelvin probe mode, the extra bias, ΔV_s , corresponding to the surface potential is applied to the tip to cancel out the electric field between the tip and the sample surface. For simplicity, in the equivalent circuit, an inherent potential difference between the tip and the uncharged sample surface was ignored to discuss the change in the surface potential caused by electron injection. Thus, the surface potential change is given by $\Delta V_s = q/C_B$, where q and C_B are the electronic charge in the dot and the capacitance between the dot and the substrate, respectively. The C_B was crudely estimated from the thickness of bottom tunnel oxide and the equivalent oxide thickness of a half of the dot with a consideration of the spatial spread of electric line of force from the charged dot

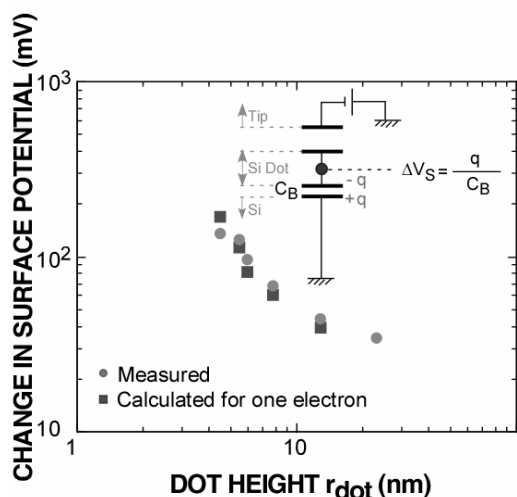


Fig. 1 The surface potential changes by electron injection to Si dots with different sizes. The calculated results using an equivalent circuit shown in the inset are also shown for the dots retaining one electron.

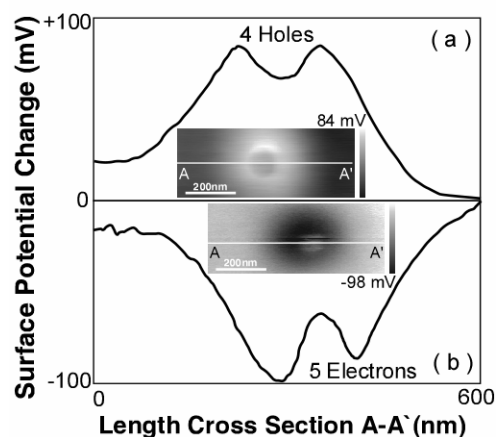


Fig. 2 The surface potential profiles across the dots after (a) electron emission at a tip bias of +3V and (b) electron injection at -3V in the tapping mode. In each case, the surface potential image is also shown as an inset. The dot heights for (a) and (b) are 21 and 25nm, respectively. The estimated retained charges are 4 holes for (a) and 5 electrons for (b).

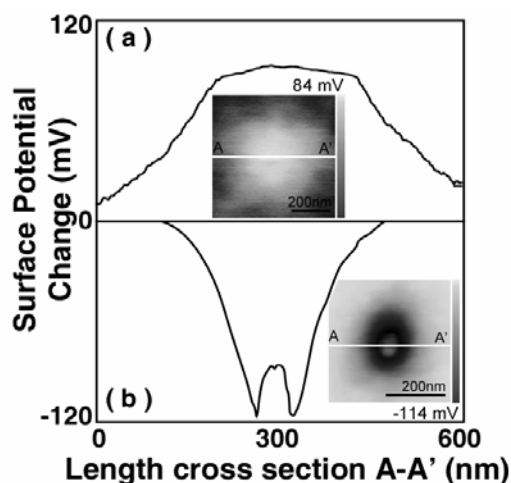


Fig. 3 The surface potential profiles across the Si dot with a Ge core after (a) electron emission at a tip bias of +3V and (b) electron injection at -3V in the tapping mode. In each case, the surface potential image is also shown as an inset. The dot heights for (a) and (b) are 16.2 and 20nm, respectively. The estimated retained charges are 2-3 holes for (a) and 3 electrons for (b).

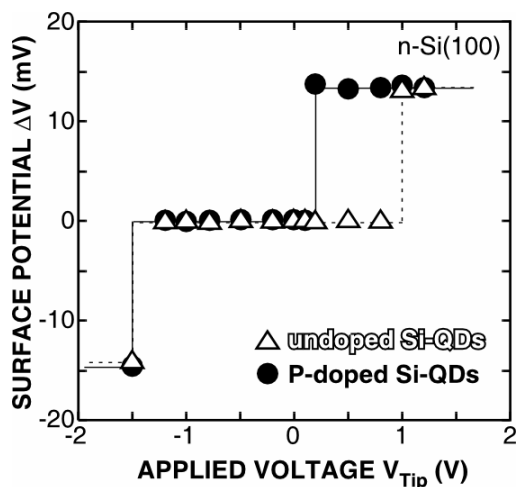


Fig. 4 The surface potential changes for Si dots with and without phosphorous doping as a function of tip bias.

toward the substrate. And the spread was also estimated from observed potential images. For Si dots larger than 20nm in dot height, where a few electrons (or holes) can be stored stably, the surface potential images after applying -3V for electron injection and +3V for hole injection show a characteristic potential profile with a dimple around the center of the charged dots as represented in Fig. 2. The result is interpreted in terms of Coulomb repulsion among the charges retained in the dot. In the case of a Si dot with Ge core with a total dot height of ~16nm, the surface potential image after electron injection shows a clear dimpled potential profile in the center of the dot, while, after hole injection, the maximum potential change appears in the center of the dot as seen in Fig. 3. These results imply that injected electrons and holes are located in the Si clad and the Ge core, respectively, as expected from the type II energy band discontinuity [11] between the Si clad and the Ge core. We have also studied the influence of phosphorous doping to Si-QDs on their electron charging and discharging characteristics. As shown in Fig. 4, the potential change corresponding to the extraction of one electron from each of P-doped Si dots was observed after applying a tip bias as low as +0.2V while for undoped Si dots with almost the same size as P-doped Si dots almost the same amount of the potential change was detectable only when a tip bias is increased to ~1V. The result indicates that, for P-doped Si dots, the electron extraction occurs from the conduction band and results in a positively-charged state with ionized P donor. There is no difference in the threshold voltage for electron injection between undoped and p-doped Si dots.

Characteristics of MOS Capacitors with Si-QDs as a Floating Gate

Electron Charging and discharging characteristics of a Si-QDs floating gate has been studied so far in dark at room temperature from unique hysteresis characteristics observed in high frequency capacitance-voltage (C-V) and displacement current-voltage (I-V) curves of Al-gate MOS capacitors with a Si-QDs floating gate on p-type and n-type Si(100) [12]. From the facts that the hysteresis characteristics are observed with a symmetrical pattern reflecting the Fermi energy of the substrate and both the capacitance and displacement current peaks appear around the flat-band condition, the contribution of traps to the measured hysteresis characteristics can be

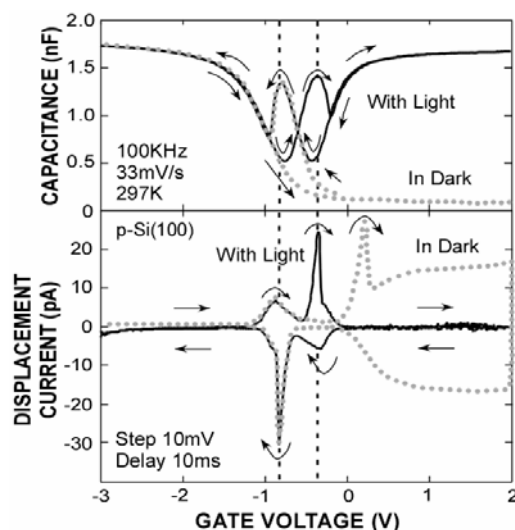


Fig. 5 100kHz capacitance-voltage and displacement current-voltage characteristics of an Al-gate MOS capacitor with a Si-QDs floating gate measured at room temperature in dark and under illumination of cold light in the wavelength region of 400-800nm.

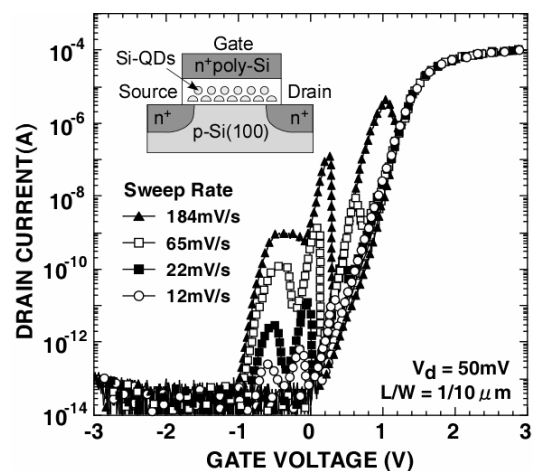


Fig. 6 Drain current - gate voltage (I_d - V_g) characteristics of a Si-QDs floating gate MOSFET, which were measured at room temperature after fully discharged at a gate bias of -4V. The drain voltage was 50mV. The voltage sweep rate was changed in the range from 12 to 184mV/s. A cross-sectional view of a Si-QDs floating gate MOSFET is illustrated in the inset.

ruled out.

When the high frequency C-V measurements were carried out under white light irradiation in the wavelength region of 400-800nm through a fiber-optics equipped with an infrared filter from a 100W halogen lamp, a distinct capacitance peak due to the charge injection to the Si-QDs floating gate in the inversion condition becomes observable (Fig. 5). This is because photo-generated carriers in the vicinity of the area masked with the Al gate flow into beneath the gate oxide and respond to the gate voltage modulation even at a high frequency. For nMOS on p-Si(100) seen in Fig.1, the observed capacitance peak in the inversion condition indicates that the injection of electrons to the electrically-neutral Si-QDs occurs in unison at a certain gate voltage as in the case of electron emission from the charged Si-QDs near the flat-band condition. Under a depletion condition at -0.3V, the transition from the C-V curve of dot neutral state to that of the charged state occurs due to the electron injection and correspondingly the displacement current peak due to the electron injection appears at the same voltage. Obviously, the voltage required for electron injection to the neutral state is markedly reduced under light illumination but in contrast, the voltages for electron emission from the charged state and neutral state and for the neutralization of the dots almost remain unchanged. In addition, the displacement current in the strong inversion condition is hardly observed under light illumination because the electron concentration of the Si surface can be changed within the delay time by the action of virtual source. In the depletion condition, because of little carrier flow from the peripheral region, the displacement current due to electron emission from the charged dots becomes observable.

Characteristics of Si-QDs Floating Gate n-MOSFETs

Based on the characteristics of MOS capacitors with the Si-QDs floating gate, we have designed and fabricated n-MOSFETs with a doubly-stacked Si-QDs floating gate [5]. The multi-step electron charging to the Si-QDs floating gate caused by the Coulomb blockade effect is confirmed from distinct bumps in drain current-gate voltage characteristics observed in ramping up the gate voltage after complete discharging (Fig. 6) and also from the temporal change in the drain current (I_D -t) at constant gate biases (Fig. 7). A decrease in the drain current with time arises from

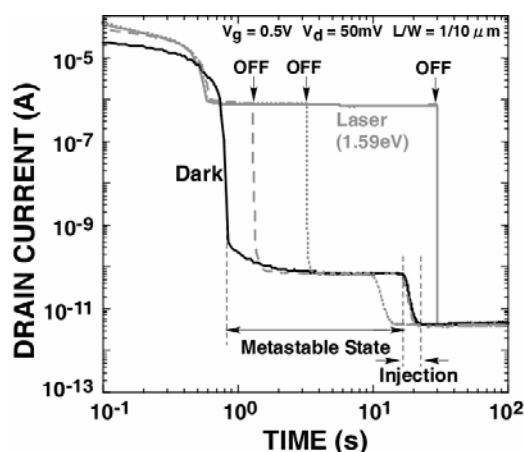


Fig.7 Temporal changes in the drain current measured at a gate voltage of 0.5V under irradiation of 780nm (1.59eV) light and in dark after complete discharging of the Si-QDs floating gate at a gate voltage of -4V.

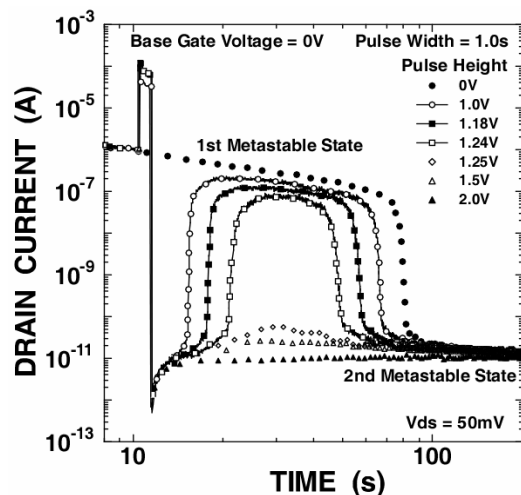


Fig. 8. Temporal changes in drain current at a gate voltage of 0V and a drain voltage of 50mV after applying different pulse gate biases. The pulse height was varied in the range of 1.0-2.0V at a constant pulse width of 1s. The result without an application of any pulsed bias is also shown as a reference.

the threshold voltage shift due to electron injection to the Si-QDs floating gate. There exists a metastable state with a fairly long incubation period to further electron injection. During the metastable state, although the total number of electrons injected to the Si-QDs floating gate is kept constant, injected electrons are likely to be redistributed in the Si-QDs floating gate by their Coulomb interaction to minimize the potential energy of the Si-QDs floating gate. Even under light irradiation, in which electron-hole pairs are generated in channel, the multi-step electron injection with the metastable state is still clearly observable although the current level is markedly increased [13]. Obviously light irradiation promotes electron injection to the Si-QDs presumably because of an increase in the electron concentration resulting in an increase in the electric field in the bottom tunnel oxide. Notice that when the light irradiation is turned off in the metastable state or in the stable state, the drain current drops immediately to the current level obtained in dark. The result indicates that a well-controlled number of electrons are injected in each of metastable and stable states. In other words, no excess electrons over a thermally equilibrium level in dark is not injected to the dots under this light irradiation, which implies sufficient energy separation between the charged state and the next. The temperature dependence of I_D - t characteristics show that the electron charging in dark proceeds with an activation energy corresponding to the 1st and 2nd energy states in neighboring dots.

The progress on charge distribution in Si-QDs was also examined from I_D - t characteristics after applying gate pulse biases with different pulse heights (Fig. 8) and widths (Fig. 9) [14]. For the cases with a pulse height of 1.24V and below (Fig. 8), the drain current rapidly increases to some current level and then decreases as seen in the electron injection without pulse except shorten time to the 2nd injected state. The increase in drain current means the emission of electrons stored in unstable charged state of Si-QDs floating gate. The emitted electrons were again injected in the Si-QDs floating gate through the metastable state. The metastable state in which the drain current slightly decreases with time is attributed to the redistribution of electrons remained in the Si-QDs floating gate. The period of the metastable state decreases with the pulse height. When the pulse height is increased only by 10mV from 1.24V to 1.25V, an increase in the drain current due to the electron emission with time becomes hardly observable, which indicates that injected electrons settle at a stable condition at $V_G=0V$. Similarly, as the pulse height is increased only by 50ms from 0.9s (Fig. 9), the electron

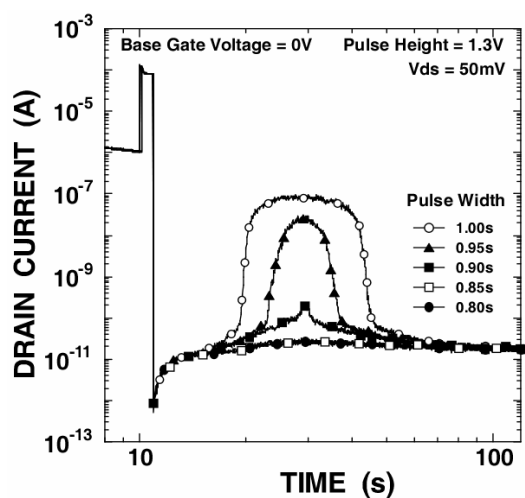


Fig. 9. Temporal changes in drain current at a gate voltage of 0V and a drain voltage of 50mV after applying different pulse gate biases. The pulse width was varied in the range of 0.8-1.0s at a pulse height of 1.3V.

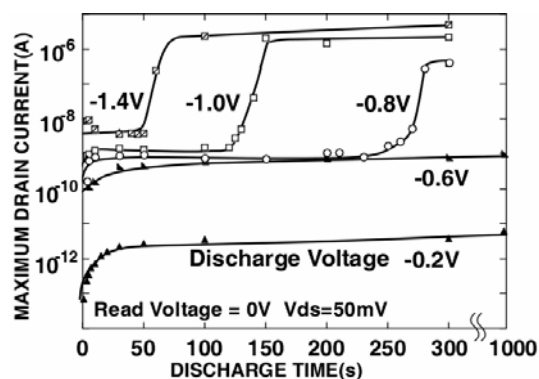


Fig. 10. The maximum drain current as a function of discharge time. The discharging voltage was varied from -0.2 to -1.4V. Before taking the data, the Si-QDs floating gate was precharged at a gate voltage of +3V for 1min.

emission no longer is observable. These results indicate that pulse height and width are crucial factors for the charge distribution in the metastable state even though the amount of injected charge is the same at each pulse height.

We have also investigated discharging characteristics of Si-QDs floating gate in the following method [15]. After being fully charged at +3V, the Si-QDs floating gate was discharged for a length of time at a certain negative V_G and then gate voltage was switched to 0V to monitor the progress in the discharging of the Si-QDs floating gate. As the gate voltage was switched to 0V, the drain current was increased immediately and then decreased due to the electron charging to the Si-QDs floating gate. The maximum drain current measured after switching to 0V was plotted as a function of discharging time at various discharging voltages as shown in Fig. 10. In the cases at discharging voltages ranging from -0.2 to -0.6V, the maximum drain current gradually increased with discharging time and is saturated at the current level between the 1st and 2nd charged state at $V_G=0V$. At the discharging voltages of -0.8V and over, the maximum drain current is increased stepwise so that the Si-QDs floating gate was fully discharged throughout an intermediate charged state. In the intermediate state, since the maximum drain current is almost constant with respect to discharging time, the amount of charge in the Si-QDs floating gate remains unchanged. This result suggests the change in electron distribution in the Si-QDs floating gate during the intermediate state as in the case of electron charging.

Summary

The electronic charged states of individual Si dot on ultrathin $SiO_2/Si(100)$ were evaluated successfully by surface potential measurements using an AFM/Kelvin probe technique. When a few electrons are injected to or extracted from Si-QDs larger than 20nm in dot height, surface potential images with a characteristic potential profile with a dimple around the center of the charged dots are observable. This results can be interpreted in terms of Coulomb repulsion among the charges retained in the dot. Si-QDs with a Ge core retain stably electrons in the Si clad and holes in the Ge core, which is attributable to the energy band discontinuity at the interface between the Si clad and the Ge core. Phosphorous doping into Si-QDs decreases the bias required for electron emission, namely generation of a positive charged state being indicative of ionized donors in the Si dots, in comparison with the electron emission from pure Si-QDs. From C-V and I-V measurements of MOS capacitors and nMOSFETs with Si-QDs floating gates, multiple-step charging and discharging characteristics of the Si-QDs floating gates are confirmed at room temperature. The temporal changes in the drain current caused by gate voltage switching suggest that the change in the electron distribution in the Si-QDs floating gate play an important role in such multiple-step charging and discharging.

Acknowledgments

This work was supported in part by Grant-in Aids for scientific research of priority area (A) and for the 21st Century COE Program "Nanoelectronics for Tera-bit Information Processing" from the Ministry of Education, Science, Sports and Culture of Japan. The author wishes to thank Dr. H. Murakami and Assoc. Prof. S. Higashi for their assistance and T. Nagai and T. Shibaguchi for their valuable contribution.

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