High-aspect-ratio structure formation techniques for three-dimensional metal-oxide-semiconductor transistors

Hideo Sunami, Koji Yoshikawa, and Kiyoshi Okuyama

Research Center for Nanodevices ans Systems, Hiroshima University, Kagamiyama, Higashi-Hiroshima 739-8527, Japan

Elsevier use only: *Received date here; revised date here; accepted date here*

Abstract

Besides further scaling of the metal-oxide-semiconductor transistor, which has continuously been achieved for these thirty-five years in large-scale integration, three-dimensional transistors having fin-type silicon substrate have been increasingly important for its promising potential to ultimately scaled ones. In this research, a beam-channel transistor featuring very-tall silicon beam has been proposed and its structure formation techniques are presented in this article. They are tall beam formation, conformal gate formation, uniform source/drain formation, and conformal metal contact.

Key words: Metal-oxide-semiconductor transistor; Three-dimension, Beam channel, High-aspect ratio, Plasma doping

1. Introduction

To overcome performance degradation in further-scaled MOS transistors, three-dimensional (3-D) structures such as double-gate [1] and FINFET [2] have been proposed. As a different approach, a beam-channel transistor, BCT [3] has been proposed by the authors featuring higher-drive current in small planar area. These device structures are shown in Fig. 1. Since the height of silicon beam of the BCT is designed to be 1 μm, almost 20-times larger drive current can be expected in same planar area as compared to that of FINFET of which height is around 50 nm.

Potential applications of the BCT are a pull-down power transistor, as shown in Fig. 2, which is connected in series to a circuit block providing ultra-low stand-by current and a monolithically integrated

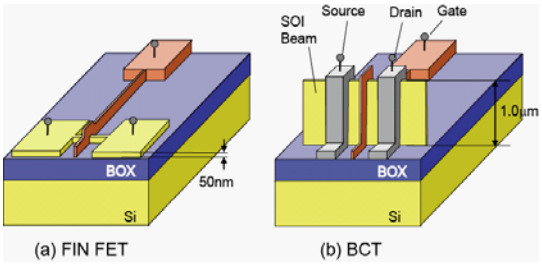


Fig. 1 Proposed 3-D MOS transistors such as FINFET (a) and beam-channel transistor, BCT (b).

RF power transistor, etc. To make the transistor as small as possible, a corrugated-channel transistor, CCT [3] which has multi-silicon beams has also been

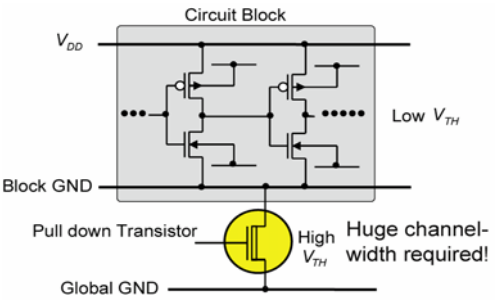


Fig. 2 A potential application of BCT for a pull-down transistor for a circuit block to control power consumption and stand-by ciurrent.

While, several three-dimensional, 3-D device structures, as shown in Fig. 3, such as sidewall channel MOS transistor (a), tri-gate MOS transistor (b), beam sidewall-channel MOS transistor (c), and vertical-channel CMOS transistor (d) together with trench-capacitor DRAM cell [5].

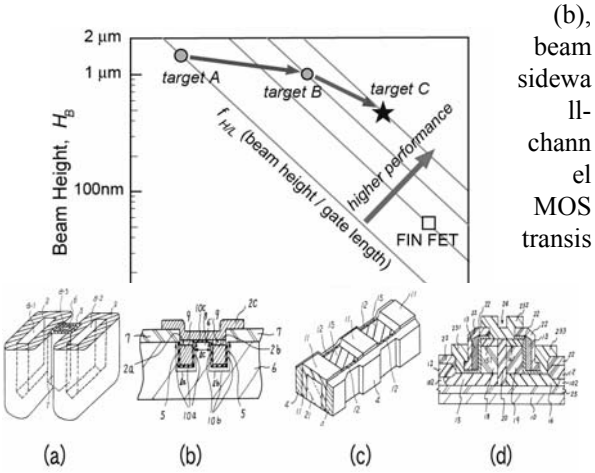


Fig. 3 Proposed three-dimensional device structures utilizing side-wall channel of silicon beam.

Fig. 4 Device targets of this study..

Targets of this research and development are shown in Fig. 4 aiming higher performance in terms of current drivability.

2. Experimental

Key techniques to realize BCT are (a) high-aspect ratio lithography and etching, (b) 3-D gate formation, (c) 3-D impurity doping, and (d) conformal source and drain, S/D electrode formation.

(a) High-aspect ratio lithography and etching

Direct electron beam exposure system is employed to delineate up to 2-μm thick photoresist. Orientation-dependent preferential etching with tetra-methyl-ammonium-hydroxide, TMAH is used to form silicon beams on (110) substrate [3]. Aspect ratios greater than 10 can easily be obtained in this preferential etching. Figure 5 indicates 31-multi channel silicon beams on (110) silicon substrate.

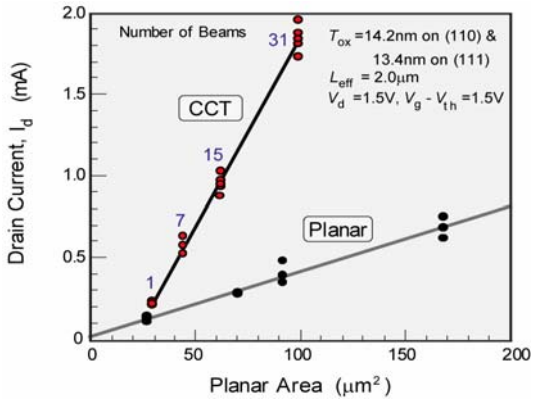


Fig. 5 Realized 31-multi-cannel silicon beams of which height and width are 900 nm and 82 nm, respectively.

Using this multi-channel beams, corrugated-channel transistor, CCT are realized. Obtained drain currents are shown in Fig. 6 clearly showing more than 5-fold increase in the current.

Fig. 6 Obtained drain currents of a CCT (target A) of which channels are already shown in Fig. 5. Both transistors are fabricated on a same wafer.

(b) 3-D gate formation

Conformal gate delineation on tall silicon beam is also a key to realize sub-μm gate length, however, there may be no choice but to utilize isotropic etching at present. A less-directional plasma etching technique can realize the gate length almost equal to the height of the silicon beam at present. Figure 7 shows an imagined failure of side-wall residue generation with anisotropic etching.

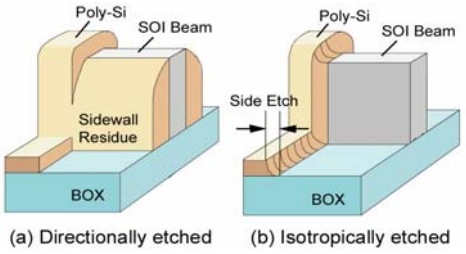


Fig. 7 Presumed hazardous residue generation along silicon beam at gate formation step.

For side-wall spacer formation for the gate shown in Fig. 7 (b), impurity-enhanced oxidation is applied [6]. With this technique the polysilicon gate is covered with its own oxide in self-aligned manner. Obtained structure is shown in Fig. 8

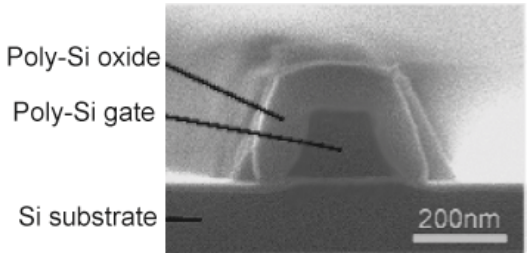


Fig. 8 Self-aligned side-wall oxide formation with impurity enhanced oxidation.

(c) 3-D impurity doping

Since strongly directional ion implantation may not be adequate to achieve uniform doping to tall comb-shaped silicon beams, plasma doping with AsH_3+Ar is utilized to form lightly-doped region along the beam surface. Figure 9 shows an example of the plasma dopin along a beam surface. An obtained typical sheet resistance value is about 500 Ω/sq.

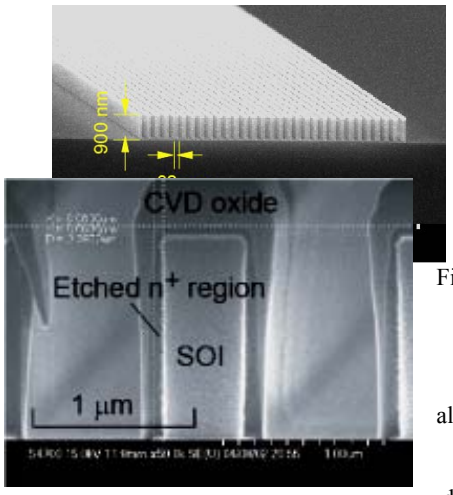


Fig. 9 Arsenic plasma doped layer along a beam surface delineated with preferential wet etching.

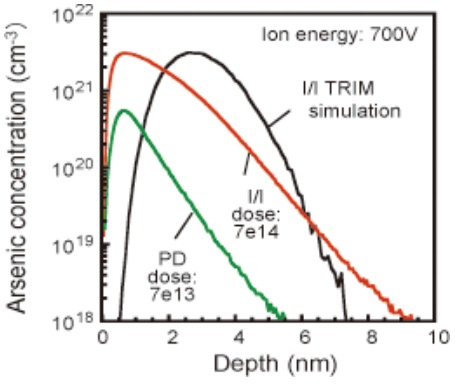


Fig. 10 SIMS profiles for ion implantation, I/I and plasma doping. PD. At most 1 % of arsenic atoms is electrically active. The rest of 99 % flow into substrate except the

wafer.

This plasma doping is adequate for formation of extension of source and drain in terms of resistivity. SIMS profiles are shown in Fig. 10. Resistivity and profile are adequate, however, induced plasma damages obviously degrade gate oxide integrity at present causing degraded transistor performance. Further investiga-tion is needed.

(d) Conformal S/D electrode formation

While, very low resistance of source and drain (S/D) regions are also inevitable not to sacrifice transistor drivability. Ni-silicided S/D beam, of which cross section is shown in Fig. 11, achieves a resistivity of 2.5×10^{-5} W-cm, while phosphorus-doped beam, 4.2×10^{-4} W-cm. To make electrode contact to tall S/D, TiN CVD method can be used. Conven-tional aluminum sputtering technique is not adequate due to its poor conformability.

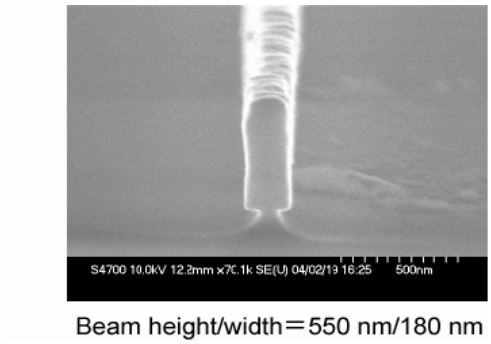
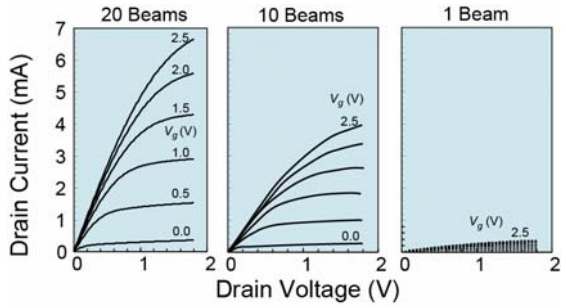


Fig. 11 Ni-silicided silicon beam to be used for low resistive source and drain regions.



A cross section and performance of the target B of CCT are shown in Figs. 12 and 13. Increased drain currents are realized in proportion to the number of the beams.

Fig. 11 An SEM cross section of the target B of CCT fabricated on (100) SOI wafer.

Fig. 12 Obtained drain currents of the target B of CCT fabricated on (100) SOI .

Conclusion

Key techniques to realize 3-D MOS transistor such as the CCT are addressed. They are successfully carried out, however, the channel length which is smaller than the beam height is still difficult to get with sufficient reproducibility caused by high-aspect-ration pattern formation. Furthermore plasma doping should be improved to some extent in terms of plasma damage generation.

Since BCT/CCT have achieved excellent device performance corresponding to their tall and multi-beam structure, they provide strong potential for applying themselves to area-conscious, i. e. cost-conscious LSI integrating on-chip power transistor. While, even if sub-half-μm gate length has already been obtained on 0.5-μm tall silicon beam, further scalability beyond sub-100 nm is not yet achieved.

Acknowledgements

The authors would like to thank to T. Furukawa, A. Katakami, and K. Kobayashi for their technical supports. This work was partly supported by Grant-in-Aids for Scientific Research (B#12555102, A(2)#13025232) from the Ministry of Education, Science, Sports, and Culture, Japanese Government and the 21st COE program "Nanoelectronics for Terabit Information Processing".

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