Enhancement of BTI Degradation in pMOSFETs Under High-Frequency Bipolar Gate Bias

Shiyang Zhu, *Member, IEEE*, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake

***Abstract*—Negative bias temperature (NBT) instability of p-MOSFETs with ultrathin SiON gate dielectric has been investigated under various gate bias configurations. The NBT-induced interface trap density ($\Delta N_{\rm it}$) under unipolar bias is essentially lower than that under static bias, and is almost independent of the stress frequency up to 10 MHz. On the contrary, $\Delta N_{\rm it}$ under bipolar pulsed bias of frequency larger than about 10 kHz is significantly enhanced and exhibits a strong frequency dependence, which has faster generation rate and smaller activation energy as compared to other stress configurations. The degradation enhancement is attributed to the energy to be contributed by the recombination of trapped electrons and free holes upon the silicon surface potential reversal from accumulation to inversion.**

***Index Terms*—Dynamic stress, negative bias temperature instability (NBTI), pMOSFETs, recombination, ultrathin gate oxide.**

I. Introduction

NEGATIVE bias temperature instability (NBTI) of p-channel MOSFETs, originated from generations of interface traps and fixed charges due to the dissociation of Si-H bonds at and near the SiO_2/Si interface, has become a severe limiting factor for continuous scaling down of ultra-large-scale integration (ULSI) devices [1]. Recent dynamic NBTI studies show that the NBTI degradation at ac operation is significantly reduced and the device lifetime can be prolonged as compared to dc ones [2]–[6]. The reason is believed that the interface traps generated during the on-state (gate voltage $V_g < 0$) can be partially recovered during the subsequent off-state ($V_g = 0$) due to the electrical passivation (EP) effect of the negative bias temperature (NBT)-induced Si dangling bonds. It is also known that positive BT (PBT) stress ($V_g > 0$) has much smaller degradation on pMOSFETs than NBT stress [7]. Furthermore, the positive gate bias annealing after NBT stress exhibits the same [8] or even larger [1], [2] EP effect than that of $V_g = 0$. It implies that the ac NBT stress with $V_g > 0$ at the off-state, namely bipolar pulsed BT (BBT) stress, may have the similar or even lower degradation than the unipolar NBT stress. However, as will be shown in this letter, the degradation under BBT stress depends strongly on frequency. This degradation enhances significantly under high-frequency BBT stresses, and its mechanism is studied in this letter.

Manuscript received February 17, 2005; revised March 17, 2005. This work was supported in part by the 21st Century COE Program "Nanoelectronics for Tera-Bit Information Processing" from the Ministry of Education, Culture, Sports, Science, and Technology. The review of this paper was arranged by Editor K. De Meyer.

S. Zhu and A. Nakajima are with the Research Center for Nanodevices and Systems, Hiroshima University, Hiroshima 739-8527, Japan (e-mail: nakajima@sxsys.hiroshima-u.ac.jp).

T. Ohashi and H. Miyake are with Elpida Memory, Incorporated, Kanagawa, 229-1198, Japan.

Digital Object Identifier 10.1109/LED.2005.848075

II. Devices and Interface Trap Measurement

PMOSFETs with P^+ poly-Si gate, nitrided gate oxide and lightly doped drain structure were fabricated on n-well of p-Si(100) substrates using a standard CMOS process [9]. Plasma-nitrided SiON gate dielectric has a base SiO_2 of 2.0 nm physical thickness and peak nitrogen concentration of 12% near the poly-Si/SiO_2 interface, as estimated from secondary ion mass spectroscopy. The channel width is 10 μm and the length is between 0.28–0.44 μm. BT stress was performed by applying a dc or pulsed voltage with square waveform of 50% duty factor and less than 8-ns rise and fall time on the gate electrode while other electrodes were grounded. The waveform keeps its normal square form up to 10 MHz as monitored by an oscilloscope. The stress temperature was set at 125 °C unless specifically noted. Immediately after stress interruption, the interface trap density ($N_{\rm it}$) was probed using a modified direct-current current-voltage (DCIV) method at the same temperature [10]. Each stress was carried out on a fresh device with initial $N_{\rm it}$ of $1.5 \sim 3.0 \times 10^9$ cm^{-2}.

III. Results and Discussion

Fig. 1(a) shows $\Delta N_{\rm it}$ after static and unipolar pulsed NBT stresses, i.e., V_g switched between $-V_a$ and 0, as a function of frequency at different V_a, here V_a is the amplitude of the stress voltage. The measurement error of $\Delta N_{\rm it}$ is estimated to be less than $\sim 10^{10}$ cm^{-2} [10]. To compare at the same real stress time, the nominal stress time for dynamic NBT (DNBT) is twice of that for static NBT (SNBT). In agreement with the previous reports [2]–[6], DNBT creates generally lower $\Delta N_{\rm it}$ than SNBT due to the partial recovery at the "off" state during the ac stress, and is almost independent of the stress frequency up to 10 MHz. Because the recovery occurs as soon as the stress is stopped [4], and there is an unavoidable waiting time ($\sim$30 s in our case) before $N_{\rm it}$ measurement, the measured $\Delta N_{\rm it}$ suffers an unintentional recovery. Fortunately, a qualitative comparison is still available because it is expected that this recovery has similar ratio for all $\Delta N_{\rm it}$. Fig. 1(b) shows that, under bipolar BT stresses, i.e., V_g switched between $-V_a$ and $+V_a$, $\Delta N_{\rm it}$ is almost independent of frequency at the low-frequency region, while it increases with frequency at frequencies larger than $\sim$10 kHz. This increase is more rapid at higher V_a. At 10 MHz, $\Delta N_{\rm it}$ at 2.9 V is close to that at 2.7 V, showing a $\Delta N_{\rm it}$ saturation, probably because all Si-H bonds (interface trap precursors) have

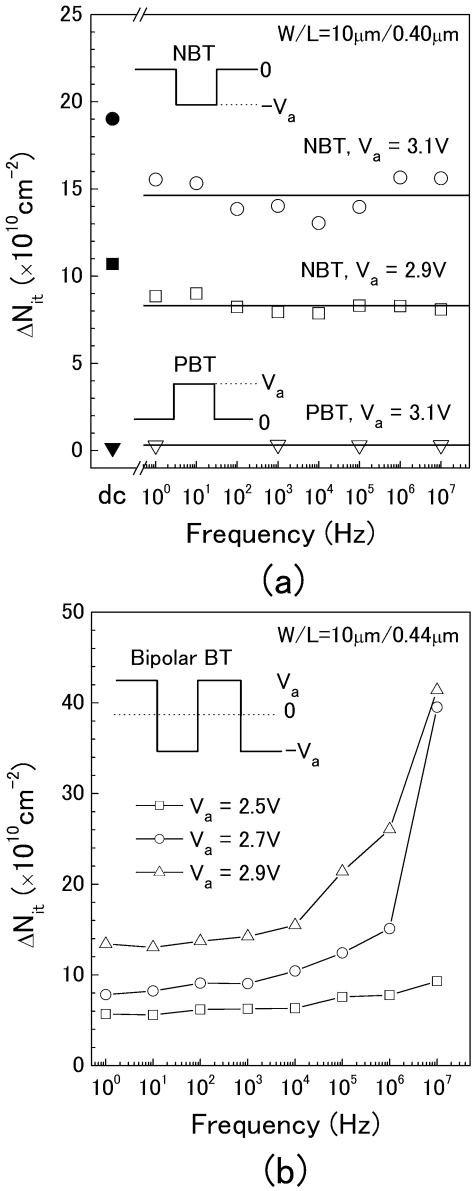

Fig. 1. Interface trap generation $\Delta N_{\rm it}$ as a function of stress frequency at different stress voltage $V_{\rm stress}$, under (a) unipolar pulsed stress (L $= 0.40\,\mu$m), (b) bipolar pulsed stress (L $= 0.44\ \mu$m). Stressed at 125 °C for 10^3 s. The data of dc stresses are also shown for comparison, whose nominal stress time is 500 s. Inset is a schematic waveform applied on the gate.

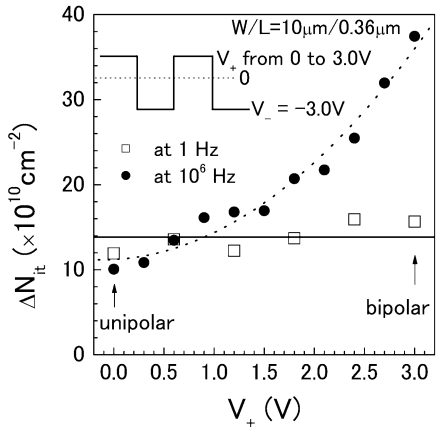

Fig. 2. Interface trap generation $\Delta N_{\rm it}$ under unsymmetrical bipolar BT stress as a function of V^+ at 1 and 10^6 Hz. V^- is fixed to -3.0 V. Devices with L $= 0.36\ \mu$m, stressed at 125 °C for 10^3 s. Inset is a schematic waveform applied on the gate.

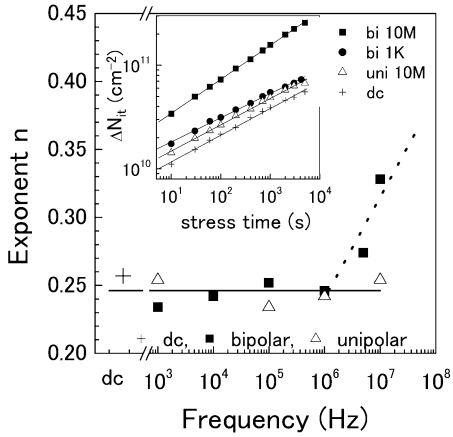

Fig. 3. Exponent n of the $\Delta N_{\rm it}$ time power function as a function of stress frequency at unipolar and bipolar pulsed stresses. The data of dc stress is also given for comparison. Inset is the time evolution of $\Delta N_{\rm it}$ for four typical stresses. The exponent n was extracted from the linear fitting of these plots.

been broken. The effect of positive voltage (V^+) in an unsymmetrical bipolar BT stress is shown in Fig. 2, where the negative voltage $(\mathrm{V\_})$ of the stress waveform was fixed to -3.0 V, while V^+ was changed from 0 (unipolar) to $+3.0$ V (bipolar) at 1 and 10^6 Hz. At the low frequency, $\Delta N_{\rm it}$ is almost independent of V^+, while at the high frequency, $\Delta N_{\rm it}$ increases with V^+ substantially. It has been known [7], and also confirmed in Fig. 1(a), that $\Delta N_{\rm it}$ under PBT stress (both as and dc) on fresh devices is very small. Moreover, positive bias on NBT-stressed devices exhibits the same [8] or even larger [1], [2] recovery than the zero bias. Therefore, above evidence strongly suggests that an additional $\Delta N_{\rm it}$ generation occurs under high-frequency bipolar BT stress. The amount of this additional $\Delta N_{\rm it}$ exceeds the recovery component at the off-state of the ac stress cycle, and depends strongly on both frequency and V^+.

The time evolution of $\Delta N_{\rm it}$ is shown in inset of Fig. 3 for four typical stress configurations, i.e., bipolar 10^7 and 10^3 Hz, unipolar 10^7 Hz and dc. They all obey a fractional power-law on time within the measurement duration: $\Delta N_{\rm it} = C \cdot t^{\rm n}$, where C and n are constants, and t is the iterated NBT stress time. Fig. 3 shows the exponent n, which was extracted by a linear fitting, as a function of stress frequency. Except at high-frequency bipolar BT stresses, exponents are close to a ubiquitous value 0.25, indicating that $\Delta N_{\rm it}$ generation under these BT stresses obeys a well-accepted diffusion-limited reaction-diffusion model [11]. On the contrary, $\Delta N_{\rm it}$ under high-frequency bipolar BT stress has a fast and frequency-dependent generation rate. Fig. 4 shows $\Delta N_{\rm it}$ under five typical NBT stress configurations as a function of the reciprocal of the stress temperature. From the linear fitting of these Arrhenius plots, the activation energy E_a was extracted to be 0.156, 0.164, 0.191, 0.184, and 0.193 eV for bipolar 10^7, 10^6 and 1 Hz, unipolar 10^6 Hz and dc stresses, respectively. E_a at high-frequency bipolar stress has a slightly, but distinguishable, smaller value than that at other stresses. The above E_a difference can not be simply explained by a measurement error of E_a, which is expected to be $\sim$0.01 eV in our case mainly due

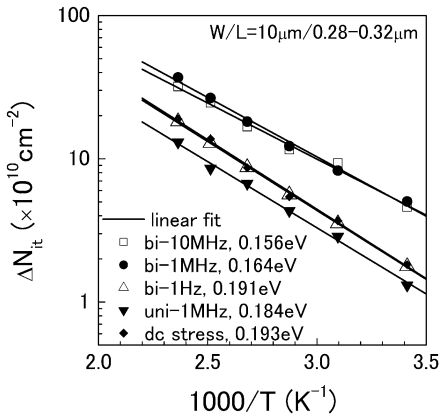

Fig. 4. Temperature dependence of $\Delta N_{\rm it}$ at five typical stress configurations. Devices with L = 0.28–0.32 μm, stressed for 10^3 s at $V_a = 2.9$ V except that $V_a = 2.6$ V for 10-MHz bipolar stress to avoid. $\Delta N_{\rm it}$ saturation. The activation energy E_a was extracted from the linear fitting of these Arrhenius plots.

to the difference in measurement temperatures [10], and also can not be explained by the device size effect because the E_a values at the unipolar 10^6 Hz stress extracted from two series samples with the channel length of 0.28 and 0.32 μm respectively exhibits a difference smaller than 0.01 eV. The large n and the small E_a of $\Delta N_{\rm it}$ (both are frequency-dependent) indicate that the additional $\Delta N_{\rm it}$ generation dominates under high-frequency bipolar BT stress and the device lifetime deceases significantly with increasing the frequency of the bipolar bias.

Similar frequency-dependent $\Delta N_{\rm it}$ enhancement was also observed in nMOSFETs performed by bipolar oxide field stresses (room temperature and high stress voltage) [12], [13], and the enhancement was attributed to the charge pumping current $(I_{\rm CP})$ [12]. We suppose that the similar mechanism also play a key role in the bipolar pulsed BT stress on pMOSFETs, i.e., the Si-H bond breaking can be accelerated by energy to be contributed by the recombination of trapped electrons at or near the Si–SiO_2 interface with the free holes upon the Si surface potential reversal from accumulation to inversion when V_g is switched from $+V_a$ to $-V_a$, which is similar to $I_{\rm CP}$ in the nMOSFET case. Unfortunately, such an $I_{\rm CP}$-like current can not be distinguished due to an overwhelming gate tunneling component through the ultrathin gate oxide [12]. However, a close correlation between this $I_{\rm CP}$-like current increase and the $\Delta N_{\rm it}$ enhancement can be expected as it is well known that $I_{\rm CP}$ depends on V^-, V^+ and is linearly proportional to frequency [14], and $I_{\rm CP}$ is negligible at unipolar stress or at low-frequency bipolar stress. Furthermore, the new generated interface traps also contribute to $I_{\rm CP}$, and larger $I_{\rm CP}$ generates more $\Delta N_{\rm it}$, therefore this is a positive feedback process. It qualitatively explains the steeper increase of $\Delta N_{\rm it}$ with frequency and V^+, as shown in Figs. 1(b) and 2, than that of conventional $I_{\rm CP}$ [14]. However, $I_{\rm CP}$ will saturate when V^+ is larger than the flatband voltage $(V_{\rm FB})$, while Fig. 2 shows that $\Delta N_{\rm it}$ still increases with V^+. A possible reason is that the carriers can obtain larger energy from the gate electric field when V^+ becomes larger. More detailed model about the $\Delta N_{\rm it}$ enhancement mechanism is being developed.

In conclusion, the device degradation is significantly enhanced under high-frequency bipolar pulsed BT stress on pMOSFETs. $\Delta N_{\rm it}$ under this stress has faster generation rate and smaller activation energy than that under other stress configurations. This additional $\Delta N_{\rm it}$ generation is related to the $I_{\rm CP}$-like current. Special attention should be taken if devices are operated at high-frequency bipolar gate bias.

REFERENCES

[1] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, no. 1, pp. 1–18, 2003.

[2] G. Chen, M. F. Li, C. H. Ang, J. Z. Zheng, and D. L. Kwong, "Dynamic NBTI of p-MOS transistors and its impact on MOSFET scaling," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 734–736, Dec. 2002.

[3] W. Abadeer and W. Ellis, "Behavior of NBTI under ac dynamic circuit conditions," in *Proc. 41st Ann. Int. Rel. Physics Symp.*, 2003, pp. 17–22.

[4] M. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, J. Babcock, R. Lindley, P. Clifton, M. Redford, and A. Shibkov, "Dynamic recovery of negative bias temperature instability in p-type metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 83, no. 8, pp. 1647–1649, 2003.

[5] H. Usui, M. Kanno, and T. Morikawa, "Time and voltage dependence of degradation and recovery under pulsed negative bias temperature stress," in *Proc. 41st Ann. Int. Rel. Physics Symp.*, 2003, pp. 610–611.

[6] S. S. Tan, T. P. Chen, C. H. Ang, and L. Chan, "A new waveform-dependent lifetime model for dynamic NBTI in pMOS transistor," in *Proc. 41st Ann. Int. Rel. Physics Symp.*, 2004, pp. 35–39.

[7] M. Denais, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, N. Revil, and A. Bravaix, "Interface trap generation and hole trapping under NBTI and PBTI in advanced CMOS technology with a 2-nm gate oxide," *IEEE Trans. Device Mater. Reliab.*, vol. 4, no. 4, pp. 715–722, Apr. 2004.

[8] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," in *IEDM Tech. Dig.*, 2003, pp. 341–344.

[9] K. Saino, Y. Kato, E. Kitamura, Y. Takaishi, M. Ando, T. Taguwa, T. Kanda, S. Yamada, and T. Sekiguchi, *IEDM Tech. Dig.*, 2003, pp. 415–3418.

[10] S. Y. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, "Modified direct-current current-voltage method for interface trap density extraction in metal-oxide-semiconductor field-effect-transistor with tunneling gate dielectrics at high temperature," *Jpn. J. Appl. Phys.*, vol. 44, no. 2, pp. L60–L62, 2005.

[11] S. Ogawa and N. Shiono, "Generalized diffusion-reaction model for the low-field charge-buildup instability at the Si-SiO_2 interface," *Phys. Rev. B*, vol. 51, no. 7, pp. 4218–4230, 1995.

[12] S. Y. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, "Interface trap generation induced by charge pumping current under dynamic oxide field stresses," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 216–218, Mar. 2005.

[13] T. P. Chen, S. Li, S. Fung, and K. F. Lo, "Interface trap generation by FN injection under dynamic oxide field stress," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1920–1926, Sep. 1998.

[14] R. E. Paulsen and M. H. White, "Theory and application of charge pumping for the characterization of Si-SiO_2 interface and near-interface oxide traps," *IEEE Trans. Electron Devices*, vol. 41, no. 7, pp. 1213–1216, Jul. 1994.