Atomic Layer-Deposited Si-Nitride/SiO_2 Stack Gate Dielectrics for Future High-Speed DRAM With Enhanced Reliability

Anri Nakajima, Takuo Ohashi, Shiyang Zhu, Shigeyuki Yokoyama, Shigetomi Michimata, and Hideharu Miyake

***Abstract*—Atomic layer-deposited (ALD) Si-nitride/SiO_2 stack gate dielectrics were applied to high-performance transistors for future scaled DRAMs. The stack gate dielectrics of the peripheral pMOS transistors excellently suppress boron penetration. ALD stack gate dielectrics exhibit only slightly worse negative-bias temperature instability (NBTI) characteristics than pure gate oxide. Enhanced reliability in NBTI was achieved compared with that of plasma-nitrided gate SiO_2. Memory-cell (MC) nMOS transistors with ALD stack gate dielectrics show slightly smaller junction leakage than those with plasma-nitrided gate SiO_2 in a high-drain-voltage region, and have identical junction leakage characteristics to transistors with pure gate oxide. MCs having transistors with ALD stack gate dielectrics and those with pure gate oxide have the identical retention-time distribution. Taking the identical hole mobility for the transistors with ALD stack gate dielectrics to that for the transistors with pure gate oxide both before and after hot carrier injection (previously reported) into account, the ALD stack dielectrics are a promising candidate for the gate dielectrics of future high-speed, reliable DRAMs.**

***Index Terms*—Atomic layer deposition (ALD), DRAM, MOSFET, Si nitride, stack gate dielectrics.**

I. Introduction

DEMANDS in the DRAM market are strongly shifting toward high-density, high-speed, and low-power products. To meet these demands, high-performance transistors are inevitable. Plasma-nitrided SiO_2 has been proposed as the gate dielectrics for next-generation DRAMs [1]. However, with scaling of oxide thickness, the low nitrogen concentration in the oxynitride may result in an insufficient suppression of boron penetration due to the heavy thermal budget peculiar to the DRAM fabrication process, which leads to an undesired $V_{\rm th}$ shift. On the other hand, high nitrogen concentration in the oxynitride may lead to a nitrogen incorporation at the SiO_2/Si-substarate interface and seriously degrade negative-bias temperature instability (NBTI) characteristics [2]. It is therefore desirable to introduce new gate dielectrics which suppress boron penetration more effectively and do not degrade NBTI characteristics too much. Atomic layer deposition (ALD) of Si nitride on SiO_2 has been found to have a high suppression ability of boron penetration [3]–[5]. It also produces excellent reliability characteristics such as soft breakdown (SBD)-free phenomena [3]–[6]. In this letter, to apply the ALD Si-nitride/SiO_2 stack gate dielectrics to future high-speed and high-reliability DRAM, we examined the suppression ability of boron penetration during the heavy thermal budget and NBTI degradation of peripheral pMOS transistors as well as the leakage and retention characteristics of memory cell (MC).

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II. Experimental

The chips tested were 2.5-V 512-Mbit double-data-rate (DDR) synchronous DRAMs (half pitch $F = 0.135$ μm). Chips having polymetal/N^+-gate MC transistors were prepared. Capacitor-over-bit-line(COB)-type cells with MIS Ta_2O_5 capacitors were fabricated. Gate doping for both nMOS and pMOS transistors was carried out by adding two I-line masking steps to the conventional (single work function) DRAM process. A perfect $8F^2$ cell was formed by using a self-align contact (SAC) process.

ALD Si-nitride/SiO_2 stack gate dielectrics were employed to suppress boron penetration from the p^+-gate. Plasma-nitrided SiO_2 gate dielectrics with a peak nitrogen concentration of 14% and pure gate oxide were also prepared for reference. Post-deposition annealing (PDA) for the ALD stack [6] and that for the plasma-nitrided SiO_2 were not carried out. For the peripheral transistors, equivalent oxide thickness (EOT) of the gate dielectrics is 3.3, 2.8, and 3.3 nm for the stack gate dielectrics, plasma-nitrided gate SiO_2, and pure gate oxide, respectively. The base oxide thickness is 2.0 and 3.5 nm for the ALD stack and plasma-nitrided gate SiO_2, respectively. For the MC nMOS transistors, EOT is 6.7, 6.8, and 6.9 nm for the stack dielectrics, plasma-nitrided gate SiO_2, and pure gate oxide, respectively. Base oxide thickness of the stack and plasma-nitrided gate SiO_2 is 3.6 and 7.0 nm, respectively. The highest temperature process after the formation of gate dielectrics was 1000 °C annealing for source/drain activation and a heavy thermal budget of 750 °C annealing for 60 min was carried out to fabricate DRAM capacitors.

III. Results and Discussion

Fig. 1 summarizes the $V_{\rm th}$ obtained from I_d-V_g characteristics of peripheral transistors. nMOS transistors with ALD stack gate dielectrics show almost the same $V_{\rm th}$ as those with pure gate

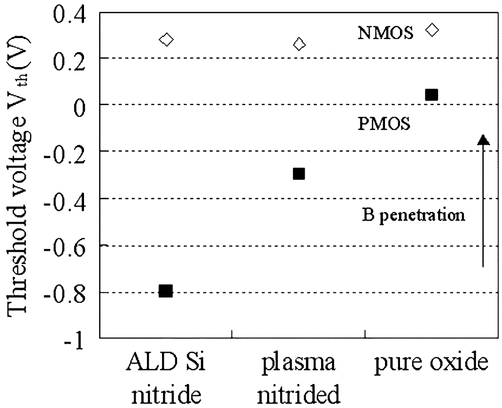

Fig. 1. $V_{\rm th}$ of peripheral nMOS and pMOS transistors. $L/W = 1\ \mu$m/10 μm.

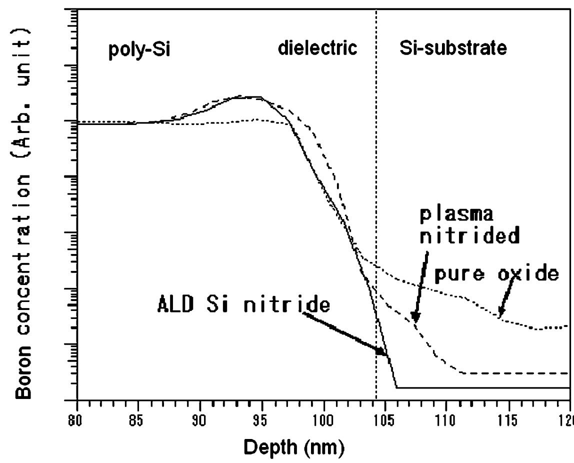

Fig. 2. Boron profile obtained from a backside SIMS measurement. The interface between poly-Si gate and gate dielectrics is not shown due to the large ambiguity.

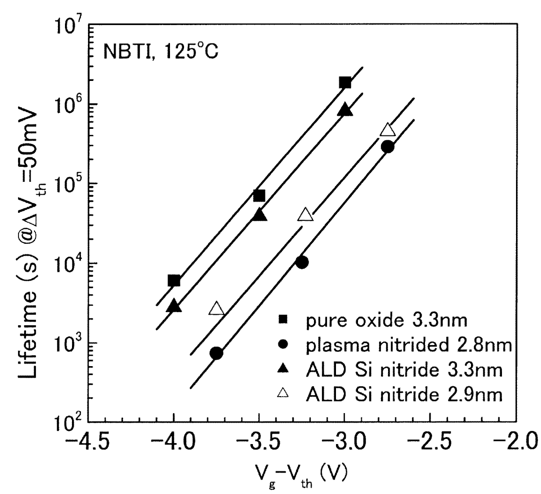

Fig. 3. Device lifetime as a function of $V_{\rm g}$-$V_{\rm th}$ at 125 °C for peripheral pMOS transistors with $L/W = 2\ \mu$m/10 μm.

oxide, which indicates that the amount of fixed charge is small in the ALD stack dielectrics. Consequently, significant positive $V_{\rm th}$ shifts seen in pMOS transistors for the pure gate oxide and the plasma-nitrided gate SiO_2 compared with that for the ALD stack gate dielectrics are mainly due to the boron penetration caused by the heavy thermal budget peculiar to the DRAM fabrication process. In addition, an increase in $|V_{\rm th}|$ with increasing the dose of channel implantation in the pMOS transistor with ALD stack dielectrics suggests that its high $|V_{\rm th}|$ is mainly due to the high channel doping.

Fig. 2 shows boron profiles obtained from backside SIMS measurements. An excellent suppression of boron penetration to the substrate is seen for the ALD stack gate dielectrics. On the other hand, the pure gate oxide suffers from very large extent of boron penetration. Even the plasma-nitrided SiO_2 shows large extent of boron penetration.

Fig. 3 shows NBTI characteristics of the peripheral pMOS transistors. The device lifetime defined by a $V_{\rm th}$ shift of 50 meV is plotted as a function of V_g-$V_{\rm th}$. To have a fair comparison, we added the data of the ALD stack gate dielectrics with an identical EOT to that of the plasma-nitrided SiO_2. It is well known that both the nitrogen incorporation at the SiO_2/Si-substrate interface and the boron penetration into the gate oxide can degrade NBTI [2]. The fact that the pure gate oxide shows better lifetime than that of the ALD stack dielectrics while it has the largest boron penetration (shown in Fig. 2) implies that the contribution of the boron penetration induced NBTI degradation is smaller than the nitrogen incorporation induced one. The ALD stack gate dielectrics show better reliability than the plasma-nitrided SiO_2. It can be attributed to an expectation that the extent of nitrogen incorporation at the SiO_2/Si-substrate interface is smaller for the ALD stack than that for the plasma-nitrided SiO_2. Unfortunately, we cannot obtain the nitrogen distribution from the SIMS analysis due to the limit of depth resolution. The other reason for the NBTI improvement for the ALD stack is its excellent boron penetration suppression. In other words, even if the extent of nitrogen at the interface is similar for the ALD stack and plasma-nitrided SiO_2, the ALD stack can show better NBTI than the plasma-nitrided SiO_2.

Fig. 4 shows the junction leakage characteristics and the data-retention characteristics of MCs. The junction leakage current [Fig. 4(a)] of transistors with the ALD stack gate dielectrics is slightly smaller in the high-drain-voltage region (>5 V) compared with that of the plasma-nitrided gate SiO_2. The current for the ALD stack is as small as that for the pure gate oxide. Because MC transistors are nMOS transistors with an n^+-gate and negligible dopant penetration occurs, pure gate oxide is considered to have small interface trap density similar to the ALD stack gate dielectrics.

Fig. 4(b) shows the data-retention characteristics of samples with MC transistors with stack gate dielectrics and pure gate oxide. Almost the same retention time $(T_{\rm ref})$ distribution was obtained for the ALD stack gate dielectrics as that for the pure gate oxide. This result is consistent with that regarding junction leakage current [Fig. 4(a)].

Large hole mobility of peripheral pMOS transistors is necessary for high-speed DRAM operation. Identical hole mobility was reported for the transistors with ALD stack gate dielectrics

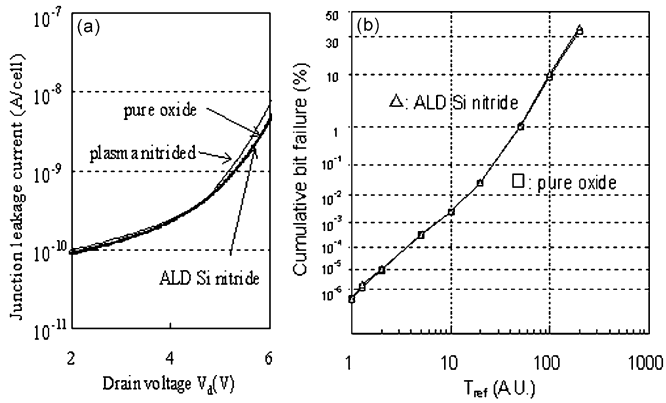

Fig. 4. Memory-cell characteristics. (a) Junction leakage current of the transistors with the three kinds of gate dielectrics. (b) Data-retention characteristics of samples with the transistors having ALD stack gate dielectrics and pure gate oxide.

and pure gate oxide [7]. Also, hot-carrier-induced mobility degradation of the transistors with ALD stack gate dielectrics was found to be identical to that of the transistors with the pure gate oxide [7]. Note that the thermal budget for fabricating the transistors reported in [7] is not as heavy as that for fabricating DRAMs. If the heavier thermal budget in the DRAM fabrication process is taken into account, ALD stack gate dielectrics are expected to have an advantage over pure gate oxide from the viewpoint of hole mobility. This advantage leads to high-speed DRAM operation due to the high drive current in the peripheral transistors.

It is noted that PDA for both ALD stack and plasma-nitrided SiO_2 gate dielectrics is expected to improve the dielectric property such as an increase in dielectric constant of ALD Si nitride [6]. Also, both the dielectrics are considered to suppress boron penetration more effectively with the PDA. However, the impact of the PDA to the other results described here, especially to NBTI degradation, is not clear and will be studied in the next step to make our study more useful.

IV. Conclusion

ALD stack gate dielectrics have a special advantage over plasma-nitrided gate SiO_2 and pure gate oxide as regards the suppression of boron penetration. ALD stack gate dielectrics exhibit enhanced reliability in NBTI compared with the plasma-nitrided gate SiO_2. For MC nMOS transistors, ALD stack gate dielectrics show identical junction leakage current to that of pure gate oxide and better characteristics than the plasma-nitrided gate SiO_2. Moreover, MCs having transistors with ALD stack gate dielectrics show identical T_{ref} distribution to those having transistors with pure gate oxide. If the reported hole-mobility characteristics are taken into account as well, ALD stack dielectrics can be considered to be a promising candidate for gate dielectrics of future high-speed and high-reliability DRAMs.

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