Mechanism of Dynamic Bias Temperature Instability in p- and nMOSFETs: The Effect of Pulse Waveform

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***Abstract*—The waveform effect on dynamic bias temperature instability (BTI) is systematically studied for both p- and nMOSFETs with ultrathin SiON gate dielectrics by using a modified direct-current current–voltage method to monitor the stress-induced interface trap density. Interface traps are generated at the inversion gate bias (negative for pMOSFETs and positive for nMOSFETs) and are partially recovered at the zero or accumulation gate bias. Devices under high-frequency bipolar stress exhibit a significant frequency-dependent degradation enhancement. Approximate analytical expressions of the interface trap generation for devices under the static, unipolar, or bipolar stress are derived in the framework of conventional reaction–diffusion (R–D) model and with an assumption that additional interface traps ($N_{\rm it}^{*}$) are generated in each cycle of the dynamic stress. The additional interface trap generation is proposed to originate from the transient trapped carriers in the states at and/or near the SiO_2/Si interface upon the gate voltage reversal from the accumulation bias to the inversion bias quickly, which may accelerate dissociation of Si–H bonds at the beginning of the stressing phase in each cycle. Hence, $N_{\rm it}^{*}$ depends on the interface-state density, the voltage at the relaxation (i.e., accumulation) bias, and the transition time of the stress waveform (the fall time for pMOSFETs and the rise time for nMOSFETs). The observed dynamic BTI behaviors can be perfectly explained by this modified R–D model.**

***Index Terms*—Bias temperature instability (BTI), direct-current current–voltage (DCIV), dynamic stress, interface states, interface trap generation, MOSFET, reaction–diffusion (R–D) model, reliability.**

I. Introduction

With the CMOS feature size scaling down continuously, the negative bias temperature instability (NBTI) of pMOSFET performances, e.g., threshold voltage shift, subthreshold swing degradation, drain current, and/or transconductance reduction, has become an important reliability issue [1]. The performance degradation has been attributed to interface trap generation ($\Delta N_{\rm it}$) and/or oxide charge buildup ($\Delta N_{\rm ot}$) in the gate-oxide film. Both defects are believed to be Si dangling bonds ($Si_3 \equiv Si\bullet$ at the interface and $O_3 \equiv Si^{+}$ in the gate oxide), originating from dissociation of Si–H bonds at or near the SiO_2/Si interface. The trap generation rate is limited by diffusion of the released H-related species away from the interface. Such a reaction–diffusion (R–D) model has been widely accepted for NBTI [1]–[4]. For MOSFETs with ultrathin SiON or high-κ gate dielectrics, the degradation can also arise from charging of the preexisting and/or newly generated traps in the dielectric during stress [5], [6]. If the stress is removed, the H-related species can diffuse back to the SiO_2/Si interface to repassivate the dissociated Si dangling bonds, or discharging the occupied traps, so that the stress-induced degradation can be partially recovered [5]–[15]. Moreover, for the H-related defects, it has been found that the positive bias after the negative bias temperature (NBT) stress can provide similar [8] or even larger recovery [7], [11] than the zero bias. Therefore, the degradation under an ac (dynamic) stress with either unipolar (V_g switching from $-V_a$ to 0, where V_g is the gate voltage and V_a is the voltage amplitude) or bipolar waveform (V_g switching from $-V_a$ to $+V_a$) is smaller than that under the corresponding dc (static) stress even taking the frequency and the duty cycle into account. This prediction has been experimentally confirmed: The device degradation under the ac stress is approximately 30%–40% smaller than that under the corresponding dc stress [7], [12], [14]. The degradation under the ac stress is frequency independent [7], [12] or slowly decreases with increasing frequency [10], [14]. We also found a reduced and frequency-independent degradation under the unipolar NBT stress [16]. However, an opposite behavior was observed in our bipolar bias temperature (BT) experiments compared with that reported in literature: The degradation of pMOSFETs under high-frequency bipolar stress is significantly enhanced, and the enhancement is strongly frequency dependent [16]. Moreover, the degradation enhancement is found to be closely related to the fall time (t_F) of the pulse waveform, namely the time for V_g switching from $+V_a$ to $-V_a$, whereas it is almost independent of the rise time (t_R). The enhancement almost disappears when t_F is larger than about 60 ns [17]. Therefore, the absence of the degradation enhancement in other group's bipolar BT experiments may be attributed to the relatively large transition time ($t_T = t_F = t_R$) used in their dynamic stress experiments. For example, in Tan *et al.*'s experiments [11], t_T was set to be 5% of period (hence, 50 ns at 10^6 Hz), and no degradation enhancement was observed under the bipolar BT stress up to 10^6 Hz.

For nMOSFETs, similar frequency-dependent degradation enhancement was also observed under room-temperature bipolar gate-oxide field stress with square waveform by Chen *et al.* [18] and by us [19]. Although BTI of nMOSFETs is not as serious as that of pMOSFET [1], the knowledge about dynamic BTI behaviors of nMOSFETs, as well as their possible transition time effect, may help us understand the microscopic

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mechanism beyond the frequency-dependent degradation enhancement under the high-frequency bipolar BT stress.

In this paper, the waveform effects for both p- and nMOSFETs under dynamic stress are systematically studied. Within the framework of conventional R–D model and with an assumption that an additional interface trap generation occurs at each cycle of the dynamic stress, an analytical expression is developed to explain the observed dynamic NBTI behaviors. Then, kinetic mechanisms are proposed to reveal the origin of this additional interface trap generation.

II. Device and Measurement Details

Both p- and nMOSFETs were fabricated using a standard CMOS process with dual poly-Si gate electrode (p^+-poly-Si for pMOSFETs and n^+-poly-Si for nMOSFETs) and lightly doped source/drain structure [20]. Approximately 2-nm-thick base gate-SiO_2 film was formed by rapid thermal oxidization, followed by plasma nitridation to introduce nitrogen into the SiO_2 film. The nitrogen distribution has a peak position in the upper half oxide film (toward the poly-Si/SiO_2 interface) and has a peak concentration of approximately 9%, 12%, and 15% for wafers 1, 2, and 3 (i.e., W-1, W-2, and W-3), respectively, as estimated from secondary ion mass spectroscopy analysis. The flat-band voltages ($V_{\rm fb}$) extracted from the high-frequency capacitance–voltage measurement for these three wafers are 1.10, 1.02, and 0.98 V for p-type gate and -1.02, -1.01, and -1.00 V for n-type gate, respectively. The difference in $V_{\rm fb}$ of the p-type gate samples arises from the boron penetration, as the SiON film with higher nitrogen content can suppress the boron penetration more effectively [21]. On the other hand, the similarity in $V_{\rm fb}$ of the n-type gate samples indicates that the nitridation-related positive trapped charge in the bulk oxide is minor or has similar density for our three wafers with different nitrogen contents.

A VAX-2000 semi-auto probe station was used for wafer testing whose needle is protected by a steel coaxial cover. The naked part of the needle (tip) is shorter than 0.5–1 cm. For dynamic stress, an ac pulse voltage provided by an HP8112A pulse generator was applied on the gate electrode using a probe needle. The parameters of the pulse waveform, e.g., period (T), high level voltage ($V_{\rm hi}$), low level voltage ($V_{\rm lo}$), rise time (t_R), fall time (t_F), duration at $V_{\rm hi}$(t_H), and duration at $V_{\rm lo}$(t_L), can be modified independently, as depicted schematically in Fig. 1(a). The minimum transition time ($t_T = t_R = t_F$) is 4.5 ns. To check the overshoot effect of the ac voltage, another probe needle (whose coaxial cover is electrically separated to that of the above needle) was pressed on the gate electrode to record the waveform using an Agilent 54642A oscilloscope. A large voltage overshoot at both the rising and falling edges was observed by the oscilloscope, as shown in Fig. 1(b), for a voltage waveform with frequency of 1 MHz, $V_{\rm hi} = |V_{\rm lo}| = 3.0$ V, and $t_R = t_F = 4.5$ ns. Fortunately, if we intentionally connected the steel coaxial covers of these two needles electrically together using a wire, the overshoot was almost removed, as shown in Fig. 1(c). Therefore, we regard that the apparent voltage overshoot is originated from coupling of the space electromagnetic noise due to the screening offset

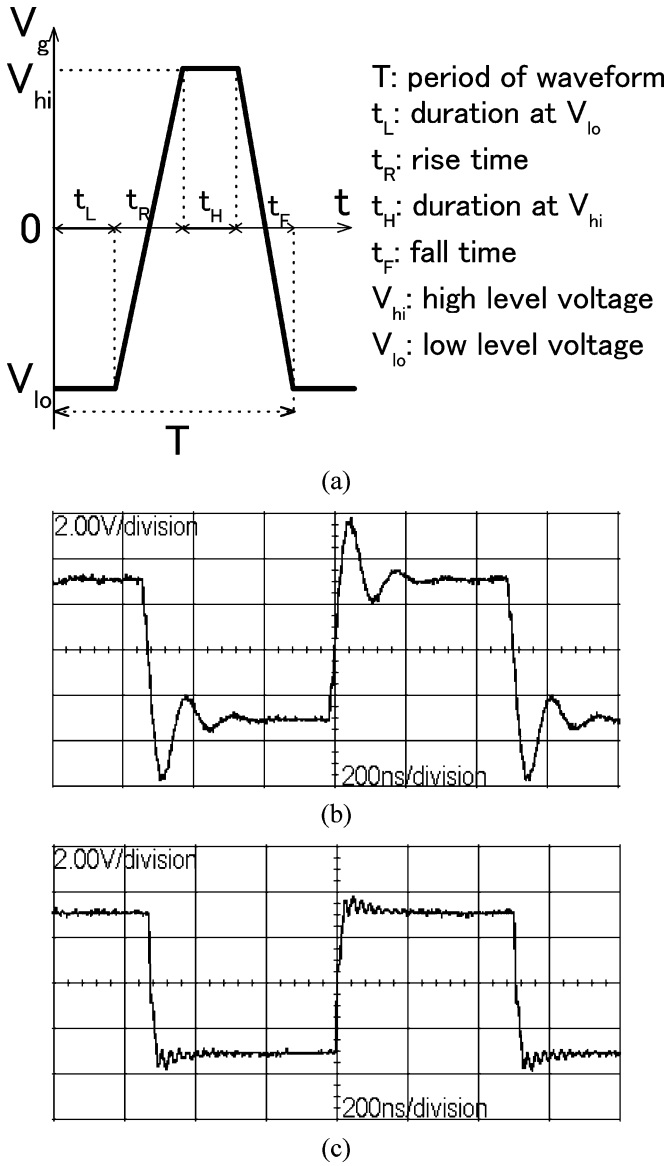

Fig. 1. (a) Schematic waveform of the dynamic stress voltage provided by an HP8112A pulse generator, where the parameters, i.e., T, t_L, t_R, t_H, t_F, $V_{\rm hi}$, and $V_{\rm lo}$, are defined and can be changed independently. (b) Waveform monitored from the gate electrode using a normal naked tip by an oscilloscope for an ac voltage of $T = 1000$ ns, $t_R = t_F = 4.5$ ns, and $V_{\rm hi} = |V_{\rm lo}| = 3.0$ V. (c) Waveform monitored after electrical screening the tips.

of these two needles, rather than from the coaxial cable and/or the wafer (e.g., the parasitic capacitance and inductance, and/or the surface reflection). In other words, the ac voltage applied on the gate electrode using the protected needle can keep its normal waveform even with the smallest transition time.

The tested MOSFETs have a drawn channel width (W) of 10 μm and a length (L) of 0.24–10 μm. Devices were stressed at a temperature ranging from 30 to 150 °C by applying a dc or ac voltage on the gate electrode while the other electrodes (source, drain, and bulk) were grounded. The stress was interrupted at a predetermined period to measure the interface trap density ($N_{\rm it}$) using a modified direct-current current–voltage (DCIV) method at the stress temperature [22], [23]. The temperature stability during whole stressing and sensing process is better than ± 1 °C. Each stress was carried out on a fresh

device. The data points in one figure were recorded from transistors with an identical W and L, one transistor for one point. However, at some "turnaround" points, more transistors were stressed identically to confirm the value.

The initial $N_{\rm it}$ of fresh devices is around $1.5-3.0\times 10^9$ cm^{-2} for pMOSFETs and around $4.4-8.0\times 10^9$ cm^{-2} for nMOSFETs, as calculated from the DCIV peak height by assuming the carrier capture rate coefficient of 10^{-8} cm^3/s for all devices [22]. It should be noted that the uncertainty of this coefficient may result in a systematic error for the calculated $N_{\rm it}$ value compared with that determined from other methods, but the relative value is true. The interface trap generation is calculated by $\Delta N_{\rm it} = N_{\rm it}$ (after stress) $- N_{\rm it}$ (before stress). However, due to an unavoidable waiting time between stressing and sensing, a partial $\Delta N_{\rm it}$ recovery may have already occurred before recording the DCIV curves. It makes the measured $\Delta N_{\rm it}$ somewhat smaller than the real $\Delta N_{\rm it}$. Fortunately, the recovery has been found to obey a power-law dependence on the waiting time approximately [12]. The waiting time is kept to be similar for all measurements in our experiments, so that the recovery portion during the waiting time can be expected to be roughly similar for all data points. Therefore, the apparent $\Delta N_{\rm it}$ data extracted in this paper can still be compared with each other.

III. Results and Discussion

A. Interface Trap Generation Under Dynamic Stresses With Various Waveforms

The time evolutions of interface trap generation under statically stressing, relaxing, and restressing sequence for p- and nMOSFETs are shown in Fig. 2(a) and (b), respectively. For pMOSFETs, interface traps are generated at the negative V_g bias and are partially recovered at the subsequent zero or positive V_g bias. The recovery is independent of the oxide field during relaxing. The time evolution of both interface trap generation and recovery approximately obeys a fractional power-law dependence, i.e., $\Delta N_{\rm it} \approx C \times t^n$ in the stressing phase and $\Delta N_{\rm it} \approx A - B \times t^n$ in the relaxing phase, where A, B, C, and n are fitting parameters. The exponent n is around 0.20–0.25, as determined from the fitting curves shown in Fig. 2(a). It implies that both processes follow the conventional R–D model, and the diffusing species are neutral [8], [12], [15].

For nMOSFETs, on the other hand, Fig. 2(b) shows that interface traps are generated at the positive V_g bias and are partially recovered by the subsequent zero or negative V_g bias. The time evolution of interface trap generation in the first stressing stage also obeys the power-law dependence, with the exponent n of approximately 0.38. In the subsequent relaxing phase, the negative V_g bias can provide more recovery than the zero bias. We suspect that the interface trap generation for nMOSFETs under the positive V_g stress also originates from dissociation of the Si–H bonds at or near the SiON/Si interface, whereas the dissociation may be associated by the channel inversion electrons and the diffusing species may be negatively charged [18]. Under the subsequent negative V_g bias, $\Delta N_{\rm it}$ reduces quickly at first, probably due to back diffusion of the negatively charged H-related species to repassivate the Si dangling bonds, and then $\Delta N_{\rm it}$ increases slowly probably due to new interface

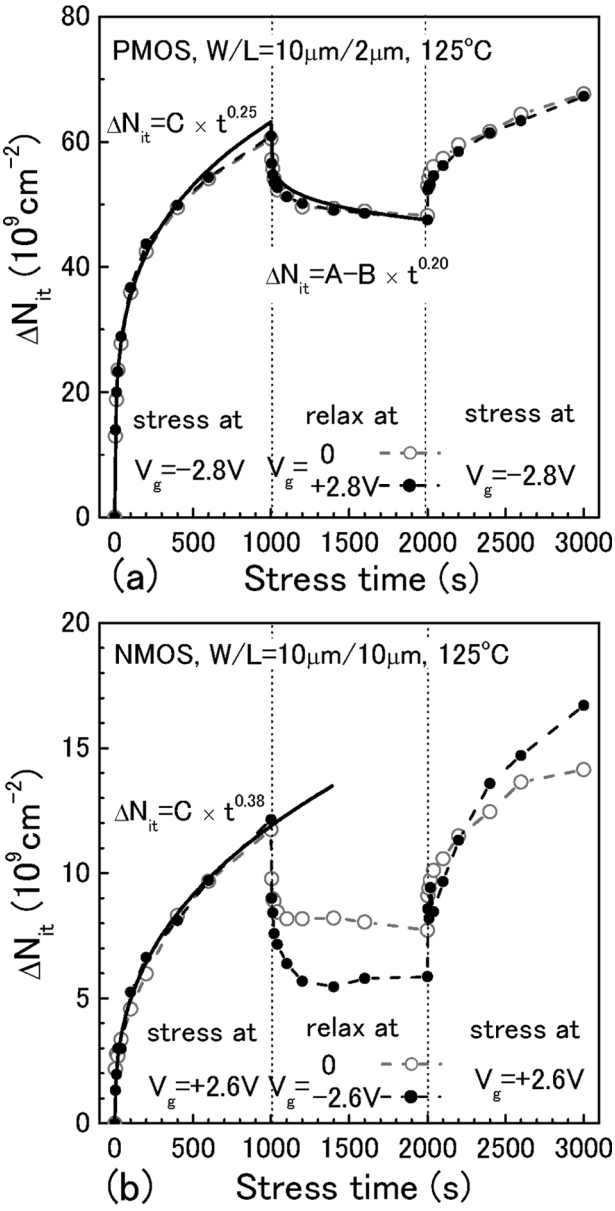

Fig. 2. Time evolution of interface trap generation and recovery at the dc stress, relaxation, and restress sequence at 125 °C. (a) pMOSFET with $W/L = 10\ \mu$m$/2\ \mu$m stressed at $V_g = -2.8$ V and relaxed at $V_g = 0$ or $+2.8$ V. (b) nMOSFET with $W/L = 10\ \mu$m$/10\ \mu$m stressed at $V_g = +2.6$ V and relaxed at $V_g = 0$ or -2.6 V. The solid curves are the fitting lines based on the power-law dependence. (Color version available online at http://ieeexplore.ieee.org.)

trap generation associated with the accumulation holes in the channel. Further detailed investigation is necessary to clarify the above scenario about nMOSFET degradation and relaxation under the positive and negative stresses; however, it is outside the scope of the present paper.

Nevertheless, the result of Fig. 2 indicates that, for both p- and nMOSFETs, if the sequence of stress–relaxation–stress–relaxation– . . . continues and the time of one stress–relaxation cycle decreases, namely in the dynamic stress with either bipolar or unipolar waveform, the final device degradation should be smaller than that under the continuous dc stress if no additional degradation occurs. The device degradation for p- and nMOSFETs under dynamic stress with bipolar (V_g from $-V_a$

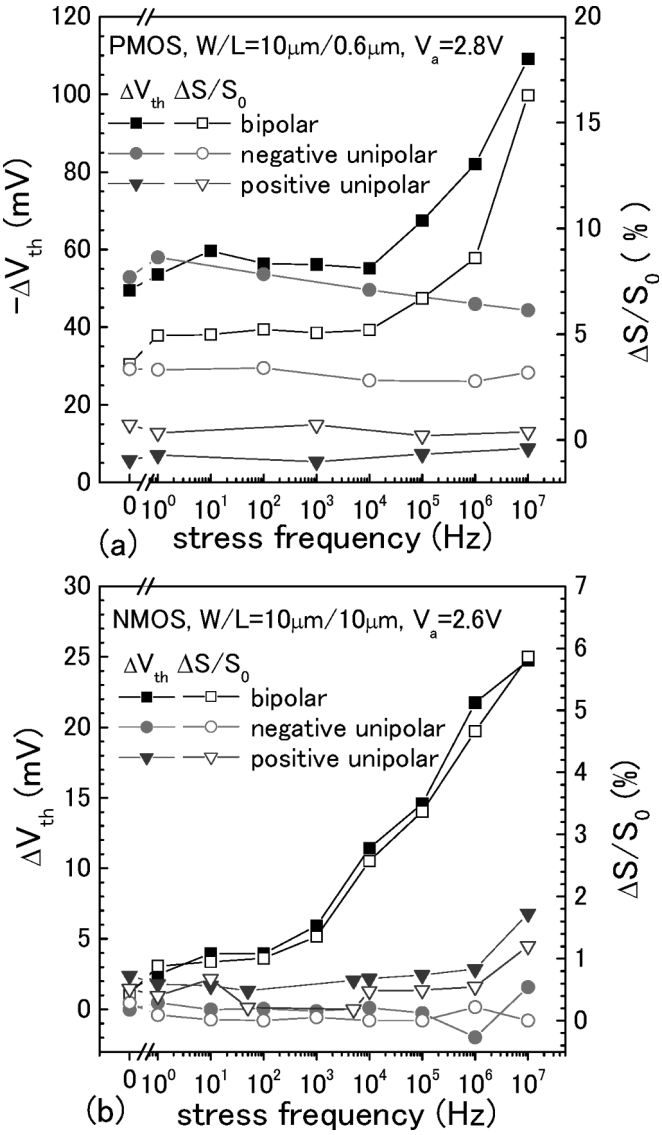

Fig. 3. Threshold voltage shift ($\Delta V_{\rm th}$, left axis) and the degradation of subthreshold swing ($\Delta S/S_0$, the right axis) as a function of frequency under bipolar (V_g from $-V_a$ to V_a), positive unipolar (V_g from 0 to $+V_a$), and negative unipolar (V_g from $-V_a$ to 0) stresses with a square waveform of $t_R = t_F = 4.5$ ns and duty factor = 50% at 125 °C. The nominal stress time is 10^3 s. (a) pMOSFETs with $W/L = 10\ \mu$m$/0.6\ \mu$m stressed at $V_a = 2.8$ V. (b) nMOSFETs with $W/L = 10\ \mu$m$/10\ \mu$m stressed at $V_a = 2.6$ V. (Color version available online at http://ieeexplore.ieee.org.)

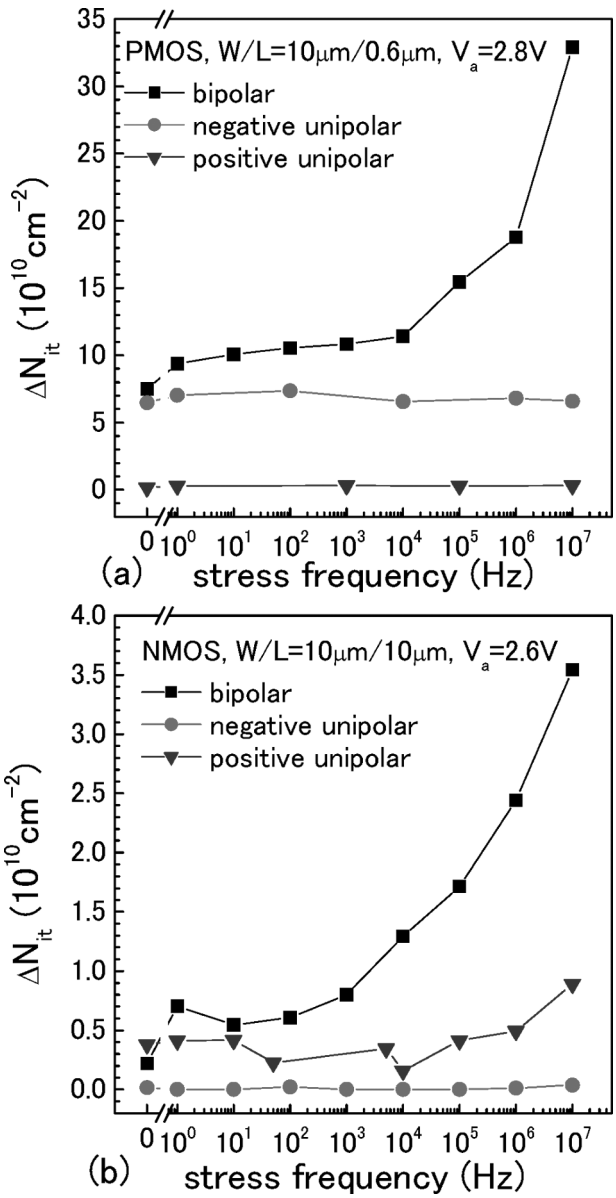

Fig. 4. Corresponding interface trap generation as a function of frequency under bipolar, positive unipolar, and negative unipolar stresses as those in Fig. 3. (a) pMOSFETs. (b) nMOSFETs. (Color version available online at http://ieeexplore.ieee.org.)

to $+V_a$), positive unipolar (V_g from 0 to $+V_a$), and negative unipolar (V_g from $-V_a$ to 0) square waveforms is shown in Fig. 3(a) and (b) as a function of frequency. The waveform has a minimum transition time ($t_R = t_F$) of 4.5 ns and a duty factor of 50%. The nominal stress time is retained at 1000 s. At "0 Hz," the device was statically stressed for 500 s followed by relaxation for another 500 s. The threshold voltage shift ($\Delta V_{\rm th}$) and the subthreshold swing degradation ($\Delta S/S_0$, where S_0 is the swing of the fresh device) are deduced from the $I_d - V_g$ characteristics recorded at $|V_{\rm ds}| = 0.1$ V [23]. The corresponding $\Delta N_{\rm it}$ data deduced from DCIV are shown in Fig. 4(a) and (b). $\Delta V_{\rm th}$, $\Delta S/S_0$, and $\Delta N_{\rm it}$ exhibit similar trends on the frequency dependence. Therefore, we only show the $\Delta N_{\rm it}$ data in the following part of this paper for simplification.

Both p- and nMOSFETs under dynamic stresses exhibit quite similar frequency dependence, i.e., 1) for pMOSFETs under the negative unipolar stress and nMOSFETs under the positive unipolar stress, $\Delta N_{\rm it}$ depends on frequency not at all or very weakly; 2) $\Delta N_{\rm it}$ for pMOSFETs under the positive unipolar stress and for nMOSFETs under the negative unipolar stress is negligible; and 3) for both p- and nMOSFETs, $\Delta N_{\rm it}$ under the bipolar stress increases with frequency rapidly when frequency is larger than approximately 10^4 Hz. $\Delta N_{\rm it}$ under the high-frequency bipolar stress can be much larger than that under the corresponding dc stress even for identical nominal stressing time. The possible influence of the stress setup on the enhanced dynamic BTI, as suggested by Bellens *et al.* [24], can be ruled out in our experiment because 1) the waveform keeps quite well even at $V_T = 4.5$ ns, $V_a = 3$ V, and $f = 10^6$ Hz,

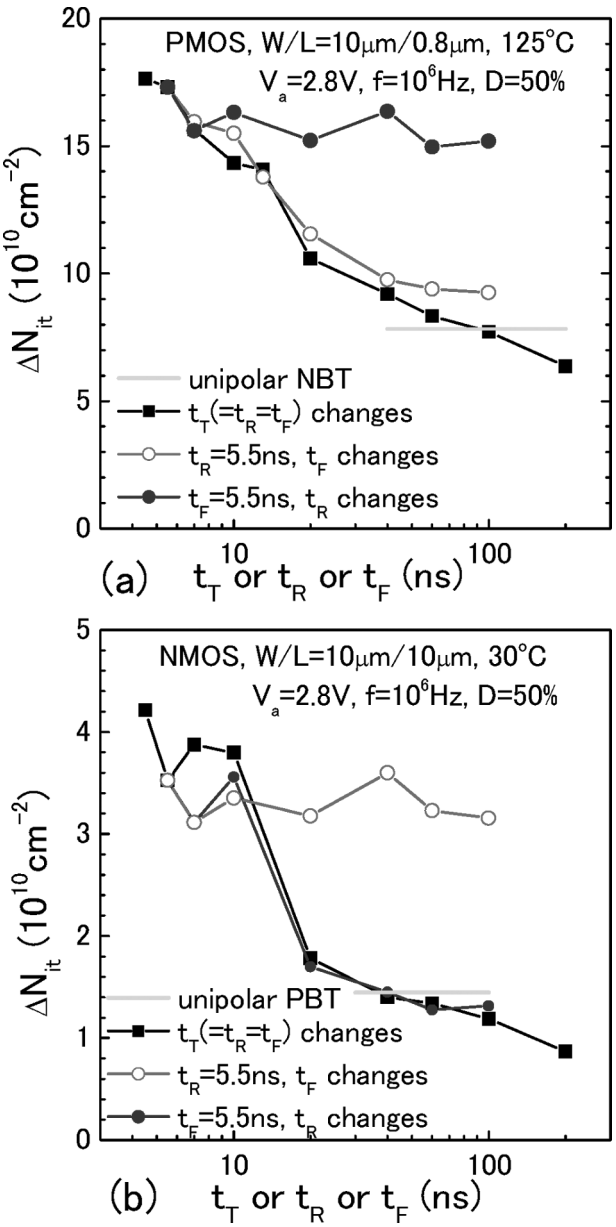

Fig. 5. Interface trap generation under high-frequency bipolar stress as a function of the transition time of the waveform: t_T, t_R, and t_F. The waveform has period $T = 1000$ ns, stress voltage $V_a = 2.8$ V, and duty factor $= 50\%$. The nominal stress time is 10^3 s. (a) pMOSFETs with $W/L = 10$ μm/0.8 μm at 125 °C. (b) nMOSFETs with $W/L = 10$ μm/10 μm at 30 °C. For comparison, $\Delta N_{\rm it}$ under corresponding unipolar stress ($t_T = 4.5$ ns) is also shown. (Color version available online at http://ieeexplore.ieee.org.)

as shown in Fig. 1(c); and 2) the $\Delta N_{\rm it}$ enhancement is not observed under the unipolar stress even at very high frequency (10^7 Hz). Therefore, a reasonable explanation for the $\Delta N_{\rm it}$ enhancement is that there exists additional interface trap generation or the degradation is remarkably enhanced under the high-frequency bipolar BT stress. For pMOSFETs, we have found that $\Delta N_{\rm it}$ under the high-frequency bipolar stress still obeys the power-law dependence on time but with the exponent n larger than 0.25 and the activation energy smaller than that under other stress configurations [16, Figs. 3 and 4]. We also found that the $\Delta N_{\rm it}$ enhancement decreases rapidly with the increasing fall time, and it is almost independent of the rise time [17, Fig. 3], as represented in Fig. 5(a). For nMOSFETs, we newly found that similar transition time effect also exists on the $\Delta N_{\rm it}$ enhancement under the high-frequency bipolar stress, as shown in Fig. 5(b). However, it is the rise time, not the fall time, that controls the $\Delta N_{\rm it}$ enhancement.

B. Empirical Model for Interface Trap Generation Under Various Stresses

1) Under Static Stress: Based on the aforementioned R–D model, the interface trap generation at the stress phase and its passivation at the relaxation phase for pMOSFETs are controlled by the following reactions [7], [8], [15]:

$$\mathrm{Si_3 \equiv Si{-}H + h^+ \rightleftharpoons Si_3 \equiv Si \bullet + X_{interface}} \tag{1}$$

$$\mathrm{X_{interface} \overset{(diffusion)}{\longleftrightarrow} X_{bulk}} \tag{2}$$

where X denotes hydrogen-related species. The time evolution of $\Delta N_{\rm it}$ can be expressed with the following equations [4], [13]:

$$\frac{dN_{\rm it}}{dt} = k_F \cdot P \cdot [N_0 - N_{\rm it}] - k_R \cdot N_H(x=0) \cdot N_{\rm it} \tag{3}$$

$$\frac{dN_H}{dt} = D \cdot \frac{d^2 N_H}{dx^2} \tag{4}$$

where $x = 0$ is chosen at the $\mathrm{Si/SiO_2}$ interface and $x > 0$ points toward bulk $\mathrm{SiO_2}$. N_0, P, and N_H are densities of the initial Si–H bonds, inversion holes in the channel, and released species (X), respectively; k_F and k_R are forward and reverse reaction rate constants; D ($\sim \exp(-E_a/kT)$ is the diffusivity of X. Here, E_a is the activation energy of the X diffusion process, k is the Boltzmann constant, and T is the absolute temperature. After stressing for several microseconds, the trap generation rate is limited by the X diffusion [4]. Assuming that the forward and reverse reactions of (1) are very fast compared with the net $N_{\rm it}$ generation, one can approximate $dN_{\rm it}/dt \approx 0$ in (3). Also, assuming $\Delta N_{\rm it}$ is far from saturation, namely $N_{\rm it} \ll N_0$, (3) and (4) can be approximately solved [4], i.e.,

$$N_{\rm it} = (P \cdot k_F \cdot N_0/k_R)^{0.5} \cdot (D \cdot t)^{0.25}. \tag{5}$$

The predicted $t^{0.25}$ relationship has been observed in many experiments including ours.

2) Under Unipolar NBT Stress: In the case of unipolar dynamic stress with duty cycle of 50%, if the time interval Δt is taken as one cycle period T, the traps created in a cycle between t_0 and $t_0 + T$ can be expressed as

$$\Delta N_{\rm it} = k_{\rm F} \cdot P \cdot [N_0 - N_{\rm it}] \cdot \frac{\Delta t}{2} - k_R \cdot N_H(x=0) \cdot N_{\rm it} \cdot \frac{\Delta t}{2}$$

(at the first half relaxing cycle, $t_0 < t < t_0 + \Delta t/2$) (6a)

$$\Delta N_{\rm it} = -k_R \cdot N_H(x=0) \cdot N_{\rm it} \cdot \frac{\Delta t}{2}$$

(at the second half relaxing cycle, $t_0 + \Delta t/2 < t < t_0 + \Delta t$) (6b)

where t_0 is the time at the end of previous cycle. It should be noted that the interface trap generation in the first half cycle and the trap recovery in the second half cycle are both limited by the X diffusion [13]. If Δt is sufficiently small, i.e., at higher frequency (e.g., >1 Hz), $\Delta N_{\rm it}$ in both half cycles is very small. Thus, the above two equations can be approximately averaged, giving

$$\frac{dN_{\rm it}}{dt} = 0.5 \cdot k_F \cdot P \cdot [N_0 - N_{\rm it}] - k_R \cdot N_H(x=0) \cdot N_{\rm it}. \tag{7}$$

The above equation is independent of frequency, in agreement with the numerical simulation result reported by Alam [13] that the distribution of X at the end of a certain stressing time under different frequency stresses has a similar profile in the oxide. In other words, the X distribution is essentially independent of the stress frequency after sufficient (several hundred) stress cycles. Using the same assumption as that in the static case, (4) and (7) can be approximately solved, and the interface trap generation under the unipolar NBT stress can be approximately expressed as

$$N_{\rm it} = (0.5 \cdot P \cdot k_F \cdot N_0/k_R)^{0.5} \cdot (D \cdot t)^{0.25} \tag{8}$$

where t is the real stress time. Equation (8) predicts that $\Delta N_{\rm it}$ under the unipolar NBT stress has similar time evolution and activation energy value as that under the static stress and is independent of stress frequency. $\Delta N_{\rm it}$ under the dynamic stress is approximately 30% smaller than that under the corresponding static stress. The above predication has been experimentally confirmed in our experiments [16] and in literatures [7], [12].

3) Under Bipolar BT Stress: Under bipolar stress, besides the trap generation and recovery as those under the unipolar stress, we assume that additional interface traps $(N_{\rm it}^*)$ are created for pMOSFETs at each falling edge of the stress cycle. At the first order, we simply assume that $N_{\rm it}^*$ is a constant (this is not accurate, as will be discussed below). $\Delta N_{\rm it}$ at the first several cycles of bipolar and unipolar stresses is schematically shown in Fig. 6. In the time interval of Δt, the cycle number is $(\Delta t \cdot f)$, and the number of additional traps is $(N_{\rm it}^* \cdot \Delta t \cdot f)$. Therefore, (6a) is modified to be

$$\Delta N_{\rm it} = (N_{\rm it}^* \cdot f) \cdot \Delta t + k_F \cdot P[N_0 - N_{\rm it}] \cdot \frac{\Delta t}{2} - k_R \cdot N_H(x=0) \cdot N_{\rm it} \cdot \frac{\Delta t}{2}$$

$$\text{at the first half stressing cycle}, t_0 < t < t_0 + \Delta t/2. \tag{6c}$$

If Δt is sufficiently small, by averaging of (6c) and (6b), one can obtain

$$\frac{dN_{\rm it}}{dt} = N_{\rm it}^* \cdot f + 0.5 \cdot k_F \cdot P \cdot [N_0 - N_{\rm it}] - k_R \cdot N_H(x=0) \cdot N_{\rm it}. \tag{9}$$

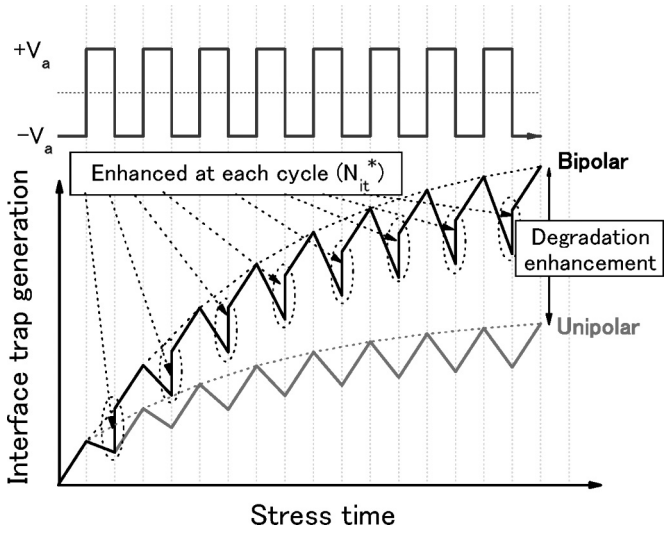

Fig. 6. Schematic diagram for interface trap generation under the first several cycles of bipolar and unipolar stresses. Assuming that additional interface traps $(N_{\rm it}^*)$ are generated in the falling edge of each cycle under bipolar stress. (Color version available online at http://ieeexplore.ieee.org.)

The above equation is implicitly assumed that the diffusion of X species is still the rate-limited process at the longer stress times. Using the same assumption as in the case of dc and unipolar stress, (4) and (9) can be approximately solved, i.e.,

$$N_{\rm it} = \left(\frac{N_{\rm it}^* \cdot f + 0.5 \cdot P \cdot k_F \cdot N_0}{k_R} \right)^{0.5} \cdot (D \cdot t)^{0.5}. \tag{10}$$

Equation (10) can qualitatively explain the observed frequency dependence under the bipolar stress. At low frequency, the first term in the bracket is negligible compared with the second term, so that $\Delta N_{\rm it}$ is similar to that under the corresponding unipolar stress and is independent of frequency. With the frequency increasing, the contribution of the first term continuously increases and may prevail over the second term contribution when the frequency is larger than approximately 10^4 Hz. With the frequency further increasing, the contribution of the second term dominates, and $\Delta N_{\rm it}$ follows an approximately 0.5 power-law dependence on frequency. To assess the value of $N_{\rm it}^*$, $\Delta N_{\rm it}$ under bipolar stresses is shown in Fig. 7 as a function of the stress frequency ranging from 0.5 to 5.0 MHz with a step of 0.5 MHz for three sets of devices with different nitrogen concentrations. Except for two abnormal peaks around 2.5 and 4.5 MHz, which will be discussed later in this paper, $\Delta N_{\rm it}$ increases monotonically with frequency. Fitting the experimental data based on (10) and assuming $D \approx 1.16 \times 10^{-9}$ cm^2/s (at 125 °C) [2] and $k_R \approx 10^{-18}$ cm^3/s [13], the value of $N_{\rm it}^*$ can be estimated to be on the order of 3.4, 4.2, and 6.2 cm^{-2} per cycle for devices of W-1, W-2, and W-3 under the bipolar stress with $V_a = 2.6$ V and $t_T = 4.5$ ns. The corresponding $(P \cdot k_F \cdot N_0)$ value is estimated to be on the order of 10^7 cm^{-2}/s. The $N_{\rm it}^*$ value is really small enough to be neglected at the low-frequency bipolar stress.

For nMOSFETs under the bipolar BT stress, the same assumption is proposed, i.e., an additional interface trap generation occurs at the rising edge of each stress cycle. Therefore,

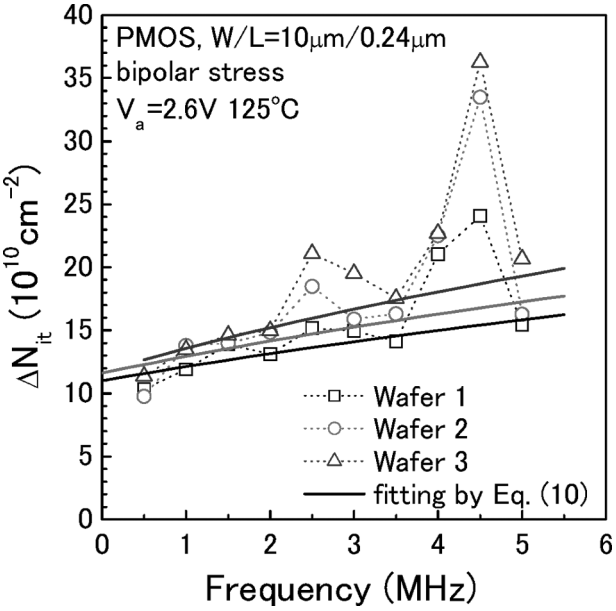

Fig. 7. Interface trap generation under bipolar stress as a function of stress frequency for three sets of pMOSFETs ($W/L = 10\ \mu$m/0.24 μm) with different nitrogen concentrations ($N\% = 9$, 12, and 15 for W-1, W-2, and W-3, respectively), ranging from 0.5 to 5 MHz with a step of 0.5 MHz. Devices stressed at 125 °C for 10^3 s with a square waveform of $t_T =$ 4.5 ns, $V_a = 2.6$ V, and 50% duty factor. (Color version available online at http://ieeexplore.ieee.org.)

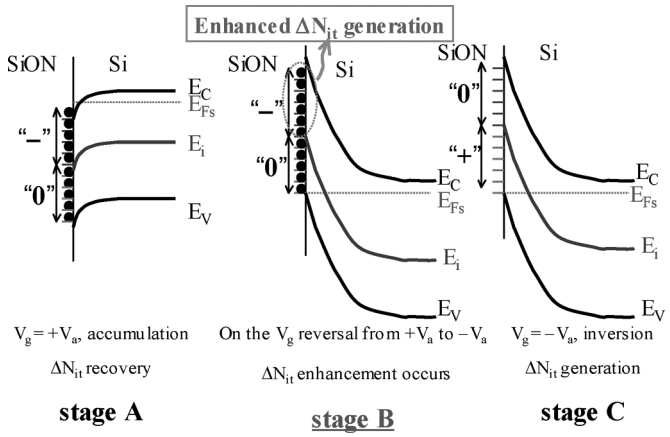

Fig. 8. Si band diagrams of a pMOSFET showing occupancy of interface states during bipolar stress. Stage A is at $V_g = +V_a$, whereas stage C is at $V_g = -V_a$. If V_g shifts from $+V_a$ to $-V_a$ quickly, there exists a transient stage B, where $E_{\rm Fs}$ has approached to E_v while interface states are still occupied by electrons. (Color version available online at http://ieeexplore.ieee.org.)

similar frequency dependence can be expected as that revealed in (10). However, because the X species in nMOSFETs are probably charged and their diffusion is electrical field dependent, the time evolutions of $\Delta N_{\rm it}$ for nMOSFETs under the dc, unipolar, and bipolar stresses differ from (5), (8), and (10), with the exponent n larger than 0.25 [25].

C. Mechanism of the Additional Interface Trap Generation Under Bipolar Stress

The energy band diagrams are illustrated in Fig. 8 for pMOSFETs (n-Si bulk) at the steady stages of $V_g = +V_a$ (stage A) and $-V_a$ (stage C) and at a transient stage B, wherein V_g is just switched from $+V_a$ to $-V_a$. At $V_g = +V_a$, the Fermi level at the Si surface ($E_{\rm Fs}$) approaches to the Si conduction band (E_c), so that the interface states in the upper half of the band gap are negatively charged (occupied by electrons). Moreover, the gate tunneling effect due to the ultrathin gate-oxide film (2 nm) results in the band bending more significantly, and the near interface traps or bulk oxide traps at a certain distance from the SiO_2/Si interface (i.e., the slow-state interface traps) are occupied by electrons, which are tunneling from the substrate. At $V_g = -V_a$, the Si channel is in inversion and $\rm E_{Fs}$ approaches to the valence band ($\rm E_v$), so that the interface states (including the slow-state interface traps) are unoccupied. It should be noted that the emission rate of trapped electrons from the interface states is finite, especially for electrons trapped in the slow-state interface traps. If V_g shifts from $+V_a$ to $-V_a$ so quickly that the emission of the trapped electrons cannot follow the V_g variation, there is a transient stage, denoted as stage B in Fig. 8, where V_g has already been switched to $-V_a$ while the interface states are still occupied by electrons. These trapped electrons can provide a built-in electric field. In the Si channel side, the direction of this field is the same as that provided by the gate bias of $-V_a$. Therefore, the electrical field in the Si channel side is strengthened, and the energy band is more significantly bent than that without the trapped electrons. Therefore, more holes can reach the SiO_2/Si interface to promote the reaction of (1) in stage B than that in stage C, resulting in the enhanced interface trap generation during stage B. An implicit assumption here is that not the total channel holes but those that can overcome the SiO_2/Si barrier (by thermal emission or tunneling) can play a role in breaking the Si–H bonds [26]. This assumption is supported by the observation that the population of the channel holes is not a rate-limiting factor for the NBTI degradation [27], and the observation that the positive bulk bias can enhance the NBTI degradation significantly [26].

Another possible mechanism for the degradation enhancement is that the recombination of the trapped electrons and free channel holes along the SiO_2/Si interface may contribute to give additional energy to break the Si–H bonds. The free hole current related to the recombination is defined as the charge pumping current and can be monitored from the bulk electrode in the case of nMOSFETs with relatively thick gate dielectric (low gate leakage current). A close correspondence between the $\Delta N_{\rm it}$ enhancement and the charge pumping current has been observed in our previous paper [19]. The abnormal $\Delta N_{\rm it}$ enhancement at some special frequencies (2.5 and 4.5 MHz) in Fig. 7 can be probably attributed to the resonant tunneling via near-interface states, as we have observed in nMOSFETs under high-frequency bipolar stresses at megahertz region [25].

For nMOSFETs, Figs. 2(b), 3(b), and 4(b) show that $V_g = +V_a$ is the stressing phase and $V_g = -V_a$ is the relaxing phase. The device degradation at $V_g = +V_a$ may associate with the channel inversion electrons, which can reach the SiO_2/Si interface [18]. Upon V_g quickly switching from $-V_a$ to $+V_a$, there is a transient stage when V_g has been $+V_a$ while the interface states are still occupied by holes due to the finite emission rate of the trapped holes. The degradation during this transient stage is thus enhanced due to the strengthened electrical field in the Si channel side provided by the positively charged interface states,

or due to the energy released from recombination of trapped holes and free channel electrons.

Now, we have proposed that the degradation is significantly enhanced by the charged interface states at the transient stage B. $\Delta N_{\rm it}$ in one bipolar stress cycle is the sum of the enhanced interface trap generation at stage B, normal trap generation at stage C, and normal trap recovery at stage A. Inasmuch as the duration of stage B (τ_B) is very short compared with the stress duration (t_L for pMOSFET and t_H for nMOSFETs), $\Delta N_{\rm it}$ in one cycle of the bipolar stress can be approximated to be $\Delta N_{\rm it}$ under the corresponding unipolar stress plus an additional interface trap generation. This is the assumption we used to develop (10). However, according to the above analysis of the $\Delta N_{\rm it}$ mechanism, $N_{\rm it}^*$ under an identical stress voltage V_a should depend on $N_{\rm it}(t)$, τ_B, and the relaxing voltage ($V_{\rm hi}$ for pMOSFETs and $V_{\rm lo}$ for nMOSFETs), namely $N_{\rm it}^* = N_{\rm it}^*(N_{\rm it}(t), V_{\rm hi}$ or $V_{\rm lo}, \tau_B)$. In the following sections, the dependences of $N_{\rm it}^*$ on these three parameters are discussed.

1) $N_{\rm it}$ Effect—Time and Frequency Evolution: Larger $N_{\rm it}$ can create more additional $N_{\rm it}^*$, and more $N_{\rm it}^*$ means larger $N_{\rm it}$. This is a positive feedback process. Therefore, the interface trap generation will increase with the stress time faster than that expected by (10). The effect becomes more significant at higher frequency. This explains our observation that the exponent n of the $\Delta N_{\rm it}$ time evolution under the high-frequency bipolar BT stress is lager than 0.25 and increases with frequency [16, Fig. 3]. Moreover, this effect makes $\Delta N_{\rm it}$ increase with frequency apparently faster than that predicted by (10). On the other hand, the interface trap generation rate will decrease and finally reach to a saturation level when N_0 (the density of initial Si-H bonds) has been substantially consumed [4], [27]. This trend is normally observed at the longer stress times. Under higher frequency, this saturation effect will appear earlier due to the faster $\Delta N_{\rm it}$ generation rate. In other words, after stressing for the same time, the saturation effect may begin to play a role at the higher frequency, whereas it has not yet at the lower frequency. Therefore, the increase of $\Delta N_{\rm it}$ with frequency (at the same t) is apparently smaller than that predicted by (10). The above two opposite effects make it quite complex to accurately express the frequency dependence of $\Delta N_{\rm it}$ under the bipolar stress.

2) $V_{\rm hi}$ Effect: It is well known that the trap states at the SiO_2/Si interface are acceptor-like in the upper half and donor-like in the lower half of the band gap [1]. Hence, the net interface states are negative at $V_g > V_{\rm mg}$ (the midgap voltage) and positive at $V_g < V_{\rm mg}$. According to our model, $V_{\rm hi}$ should be larger than $V_{\rm mg}$ to trigger the $\Delta N_{\rm it}$ enhancement for pMOSFETs under the dynamic stress. With $V_{\rm hi}$ further increasing, more electrons are being trapped in the SiO_2/Si interface and/or reaching near interface traps with larger energy level through the trap-assisted tunneling mechanism. Therefore, the degradation enhancement in stage B is more significant. This effect explains the absence of $\Delta N_{\rm it}$ enhancement under the unipolar NBT stress and the rapid increase of $\Delta N_{\rm it}$ with $V_{\rm hi}$ [16]. Fig. 9 compares the $V_{\rm hi}$ dependence for three sets of devices with different flat-band voltages (due to different nitrogen contents). The stress waveform has frequency of 1-MHz stress, $V_{\rm lo}$ of -3.0 V, and $V_{\rm hi}$ in the range from 0 (as the unipolar stress) to $+3.0$ V (as the bipolar stress). $\log(\Delta N_{\rm it})$ increases almost linearly with $V_{\rm hi}$ when $V_{\rm hi}$ is larger than a certain value around 0.2–0.6 V. The value is close to the $V_{\rm mg}$ value estimated from the DCIV peak position. Moreover, the critical voltage to trigger the degradation enhancement for these three sets of devices has a sequence of $V_{\rm hi}$(W-1) > $V_{\rm hi}$(W-2) > $V_{\rm hi}$(W-3), consistent with the sequence of the flat-band voltages. This finding confirms the above expectation that the degradation is triggered at $V_{\rm hi} > V_{\rm mg}$. For nMOSFETs, on the other hand, $V_{\rm lo} < V_{\rm mg}$ is needed to trigger the degradation enhancement.

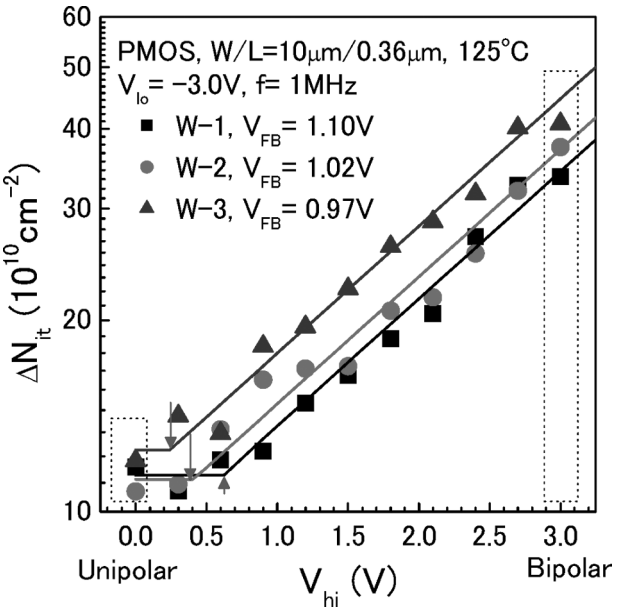

Fig. 9. Interface trap generation under unsymmetrical high-frequency BT stress as a function of $V_{\rm hi}$ for three sets of pMOSFETs ($W/L = 10\ \mu$m/0.36 μm) with different $V_{\rm fb}$ (due to different nitrogen concentrations: 9%, 12%, and 15% for W-1, W-2, and W-3, respectively). Devices are stressed by a square waveform of $f = 1$ MHz, $t_T = 4.5$ ns, $V_{\rm lo} = -3.0$ V, and duty factor = 50% at 125 °C for 10^3 s. $V_{\rm hi}$ ranges from 0 (the negative unipolar stress) to 3.0 V (the normal bipolar stress). The linear fitting of $\log(\Delta N_{\rm it})$ versus $V_{\rm hi}$ is also shown, and the minimum $V_{\rm hi}$ to trigger the $\Delta N_{\rm it}$ enhancement is indicated by the short arrows. (Color version available online at http://ieeexplore.ieee.org.)

3) t_F (or t_R) Effect: The trapped electrons can be eliminated by the emission process upon the V_g variation from $+V_a$ to $-V_a$. If the fall time is long enough, the emission of the trapped electrons can follow the V_g variation [28], so that τ_B approaches zero and the $\Delta N_{\rm it}$ enhancement vanishes. $\Delta N_{\rm it}$ as a function of t_F ranging from 5.5 to 99.9 ns is shown in Fig. 10(a) for pMOSFETs under 1-MHz bipolar stress with the fixed t_R of 5.5 ns and at temperatures ranging from 30 to 150 °C. The corresponding t_R effect for nMOSFETs at different temperatures is shown in Fig. 10(b). For both p- and nMOSFETs, $\Delta N_{\rm it}$ remains the same when the transition time (t_F for pMOSFETs and t_R for nMOSFETs) is less than approximately 10 ns. $\Delta N_{\rm it}$ decreases rapidly with the transition time increasing from 10 to 40 ns and then saturates to a value close to that under the corresponding unipolar stress at the transition time approaching to approximately 60 ns at any temperature. It indicates that the electron (or hole) emission process is negligible when t_F (or t_R) is smaller than approximately 10 ns,

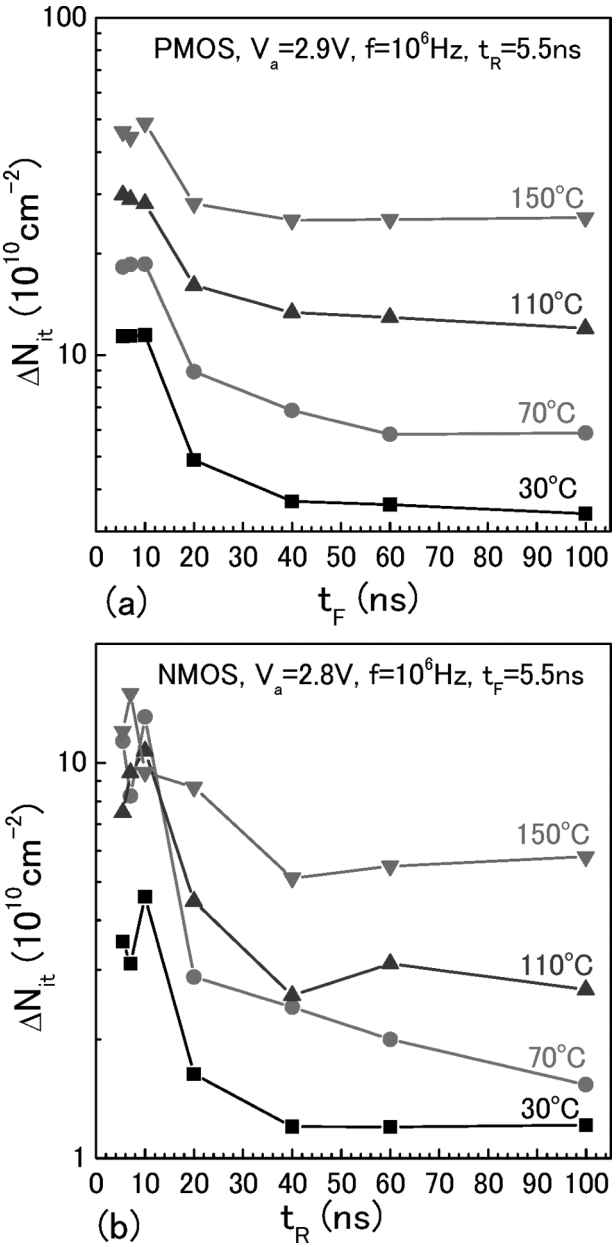

Fig. 10. Interface trap generation under 1-MHz bipolar stress as a function of the falling time or the rising time at temperatures ranging from 30 to 150 °C. The nominal stress time is 10^3 s, and the duty factor is 50%. (a) pMOSFETs of $W/L = 10\ \mu$m/0.4 μm stressed at $V_a = 2.9$ V, $t_R = 5.5$ ns, and t_F ranging from 5.5 to 99.9 ns. (b) nMOSFETs of $W/L = 10\ \mu$m/2 μm stressed at $V_a = 2.8$ V, $t_F = 5.5$ ns, and t_R ranging from 5.5 to 99.9 ns. (Color version available online at http://ieeexplore.ieee.org.)

whereas it prevails when t_F (or t_R) is larger than approximately 60 ns. The above time constants are roughly in agreement with those observed by Ghibaudo and Saks in their time-domain charge pumping current studies [28], [29].

The V_a effect for pMOSFETs under the bipolar BT stress (V_g from $-V_a$ to $+V_a$) with different transition times of 4.5, 20, and 100 ns is shown in Fig. 11, and that under the dc stress is also shown for comparison. We can see that $\log(\Delta N_{\rm it})$ versus V_a has an approximately linear relationship and the slopes for these four stress configurations are similar except at the higher V_a region of $t_T = 4.5$ ns, which exhibits a slightly larger slope. Compared with the dc stress, the ratio of $\Delta N_{\rm it}$ enhancement

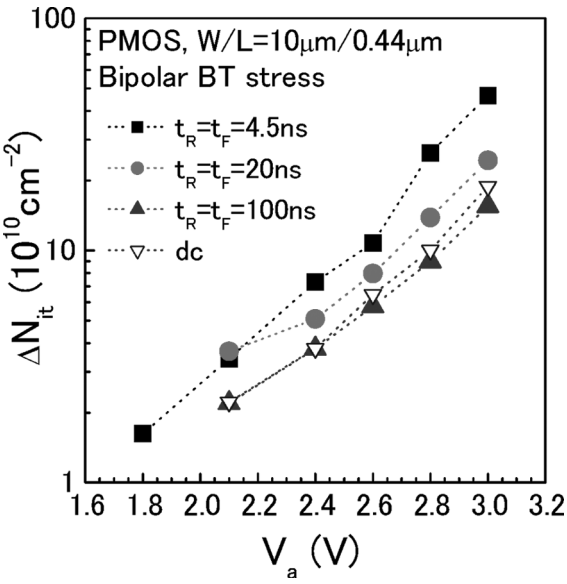

Fig. 11. Interface trap generation as a function of the stress voltage (V_a) for pMOSFETs with $W/L = 10\ \mu$m/0.44 μm under bipolar stress at 125 °C for 10^3 s with a square waveform of $f = 1$ MHz and duty factor = 50%. The transition time t_T is 4.5, 20, and 100 ns. The data of $\Delta N_{\rm it}$ under corresponding dc stress are also shown for comparison. (Color version available online at http://ieeexplore.ieee.org.)

under the bipolar stress decreases with t_T increasing from 4.5 to 20 ns and approaches to unity (no enhancement) when $t_T = 100$ ns. It indicates that the voltage acceleration factor of the additional interface trap generation at the transient stage B is similar to that of the conventional $\Delta N_{\rm it}$ generation at the steady stage C, in consistent with our assumption that the additional $\Delta N_{\rm it}$ generation in stage B also obeys the R–D model. In the case of $t_T = 4.5$ ns, the phenomenon that the $\Delta N_{\rm it}$ enhancement becomes more significant at the larger V_a region can be explained by the positive feedback process of the additional interface trap generation as discussed in Section III-C1.

IV. Conclusion

Interface trap generation is systematically studied for both p- and nMOSFETs under dynamic stresses with various waveforms. Interface traps are generated at the Si channel inversion phase and are partially recovered at the accumulation phase. Both mechanisms obey the conventional diffusion-limited R–D model. Upon switching the Si potential from accumulation to inversion, the transient carriers trapped in the interface states can enhance the interface trap generation; thus, additional interface traps are generated at each cycle during the dynamic stress. Although the amount of the additional interface traps ($N_{\rm it}^*$) is quite small, it becomes important at higher frequency. $N_{\rm it}^*$ depends on the interface trap density ($N_{\rm it}$), the fall time, and the high level voltage of the stress waveform for pMOSFETs and depends on $N_{\rm it}$, the rise time, and the low level voltage for nMOSFETs. Based on this modified R–D model, the observed phenomena about dynamic BTI can be consistently explained. For reliability improvement in high-frequency (such as VHF) CMOS logic operation, this waveform effect may need to be taken into account.

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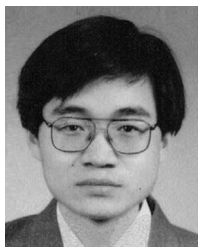

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Takuo Ohashi, photograph and biography not available at the time of publication.

Hideharu Miyake, photograph and biography not available at the time of publication.