Influence of bulk bias on negative bias temperature instability of p-channel metal-oxide-semiconductor field-effect transistors with ultrathin SiON gate dielectrics

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Bulk (well) bias effects (grounded, positively biased, and floating) on both static and dynamic negative bias temperature instability of p-channel metal-oxide-semiconductor field-effect transistors with ultrathin SiON gate dielectrics were systematically investigated. The device degradation under both static and dynamic negative bias temperature (NBT) stresses with relatively large gate voltage \( V_g \) is significantly enhanced by a positive bulk bias \( V_b \). Moreover, the device degradation under bipolar pulsed bias temperature (BT) stress is dramatically enhanced by floating the bulk electrode. Both phenomena can be attributed to an additional degradation related to hot hole injection. The holes are energized by an electrical field of the induced depletion region between channel and bulk provided by the positive \( V_b \) or, in the case of bipolar pulsed BT stress with the bulk electrode floating, by the transient depletion region below the channel induced by the \( p-n \) junction between source (drain) and bulk upon the gate voltage \( V_g \) being switched from positive to negative with a transition time less than about 0.2–100 ms. © 2006 American Institute of Physics.

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I. INTRODUCTION

The negative bias temperature instability (NBTI) of p-channel metal-oxide-semiconductor field-effect transistors (pMOSFETs) has become an important reliability concern in modern complementary metal-oxide-semiconductor (CMOS) technology, especially when the gate-oxide thickness is scaled down to less than 2.0 nm and also nitrogen is introduced into the gate-SiO2 film in order to suppress the boron penetration and to increase the dielectric constant.1,2 Considerable efforts have been done for both static (Refs. 3–6) and dynamic (Refs. 7–10) NBTI, in which a constant or pulsed voltage is applied on the gate electrode \( V_g \) while the source, drain, and bulk (well) electrodes are grounded. Interface traps and/or positive fixed oxide charges being created under the negative bias temperature (NBT) stress are generally believed to be Si dangling bonds \( \equiv \text{Si}, \text{Pb} \) centers in the electron spin resonance studies11 originating from the dissociation of hydrogen passivated \( \text{Si-H} \) bonds at and/or near the \( \text{SiO}_2/\text{Si} \) interface.3–10 The dissociation is widely accepted to be associated with holes in the inversion channel under the NBT stress,3–5 but the exact role of the channel holes has not been fully understood yet. To clarify this problem, the bulk bias \( V_b \) effect on NBTI was intentionally studied in literature because \( V_b \) can modify the population of channel holes while keeping the other stress conditions constant.12,16 However, the reported \( V_b \) effects are controversial. For example, Mitani et al.13 and Hurad et al.14 found that NBTI under an identical \( V_g \) stress is independent of the positive bulk bias up to 3 or 4 V, while Kimizuka et al. observed that the NBTI lifetime begins to reduce significantly at \( V_b \) larger than about 1.5 V.12 Moreover, Mahapatra et al. reported that NBTI at high \( V_b \) (≥4 V) shows identical degradation rate for short stress time while the degradation rate drastically increases at longer stress times.15 The \( V_b \) induced degradation enhancement has been attributed to the substrate hot hole injection.12,15 On the other hand, to the best of our knowledge, the \( V_b \) effect on the dynamic NBTI has not been reported.

In this paper, the \( V_b \) effects under both static and dynamic NBT stress were studied systematically. We find that NBTI can be significantly enhanced by applying a positive bulk bias. The enhancement depends on both \( V_g \) and \( V_b \). Moreover, we find a frequency-dependent degradation enhancement under bipolar pulsed BT stress with the bulk electrode floating. The enhancement is much more significant than that under the \( V_g \) grounded case.3,10 A model based on the hot hole injection is proposed to explain the degradation enhancement in both stress configurations, i.e., static stress with positive \( V_b \) and bipolar stress with \( V_b \) floating.

II. DEVICES FABRICATION AND NBTI CHARACTERIZATION

The tested pMOSFETs were fabricated on the \( n \) well of \( p-Si \) (100) substrates using a standard CMOS process17 with lightly doped source (drain) structure, \( p^+ \) polycrystalline-Si gate electrode, and plasma-nitried SiON gate dielectric, which has a base \( \text{SiO}_2 \) thickness of about 2 nm and a peak
nitrogen concentration of about 9% around the upper half oxide film toward the poly-Si/SiO₂ interface. The equivalent oxide thickness (EOT) is extracted to be about 2.22 nm from the high-frequency capacitance-voltage (C-V) measurement. The channel width ($W$) is 10 µm and the length ($L$) is between 0.32 to 1.12 µm. Unless specially noted, devices were stressed at 125 °C for 1000 s, by applying a constant or pulsed voltage on the gate electrode while the source (drain) electrode was grounded and the bulk (well) electrode was grounded, positively biased, or floating. The pulsed voltage has a square wave form with a duty factor of 50%, and a minimum rise and fall time of 4.5 ns. The impact of the possible voltage overshoot upon rapid $V_g$ reversal in the dynamic stressing configuration, which may enhance the device degradation,¹⁸ seems minor in our experiments because (1) no degradation enhancement is observed under the unipolar stress, as will be shown in this paper; (2) the square wave form keeps quite well even at 10⁷ Hz with 4.5 ns transition time as monitored by an oscilloscope. Note that the actual stress time under the dynamic stress is half of the nominal time as monitored by an oscilloscope. Immediately after stress interruption, the stress time predicted in this paper by taking the 50% duty stress time under the dynamic stress is half of the nominal time as monitored by an oscilloscope. \( \text{DCIV peak height is proportional to the interface trap density (} N_i \text{)} \), while the peak position shift is related to the oxide charge generation ($\Delta N_o$).

III. RESULTS AND DISCUSSION
A. Positive bias of the bulk electrode

By applying a positive bulk bias $V_b$, the initial threshold voltage is modified due to the body effect. For example, a device with $W/L=10 \mu m/0.32 \mu m$ has a $V_{th}$ of $-0.365 \, V$, $-0.597 \, V$, and $-0.726 \, V$ with $V_b=0 \, V$, 1 V, and 2 V, respectively. Therefore, the hole population in the inversion channel, which is proportional to $|V_g-V_{th}|$, decreases with increasing $V_b$ at the identical stress voltage. The oxide electrical field ($E_{ox}$) was also kept the same because the inversion channel has the same potential as the grounded source (drain) electrode.

Figure 2 shows the threshold shift ($\Delta V_{th}$) and corresponding interface trap generation ($\Delta N_i$) as a function of stressing time under static NBT stress with various $V_b$ and $V_g$. Both $\Delta V_{th}$ and $\Delta N_i$ exhibit similar $V_b$ and $V_g$ dependence. At low stress voltage ($|V_g|=1.5 \, V$), the device degradation ($\Delta V_{th}$ and $\Delta N_i$) is almost independent of $V_b$ (up to 2 V), in agreement with those reported by Mitani et al.¹³ and Huard et al.¹⁴ At high $|V_g|$ (≥2.0 V), the degradation is significantly enhanced and has a large degradation rate. The enhancement magnitude depends on both $V_g$ and $V_b$, i.e., the
higher \( |V_g| \), the lower \( V_b \) to trigger the enhancement is. It should be noted that the value of \( |V_g| \) and \( V_b \) to trigger the degradation enhancement is much lower than that reported by Mahapatra et al.,\textsuperscript{15} while is similar to those reported by Kimizuka et al.\textsuperscript{12} and Varghese et al.\textsuperscript{16} The \( V_b \) induced degradation enhancement can be explained by energetic (hot) hole injection from the substrate.\textsuperscript{12,15,16} The energy band diagrams for a pMOSFET under NBT stress with \( V_g=0 \) and \( V_b>0 \) are schematically shown in Fig. 3. The width \( (W) \) of the induced space charge (depletion) region between the channel and the bulk, and the maximum electrical field \( (E_{\text{max}}) \) in this region, are both proportional to \( V_b^{1/2} \) approximately.\textsuperscript{17} Holes from the bulk to the channel can be accelerated by this electrical field to be hot. Thus, the number of hot holes in the channel as well as their kinetic energy increases with \( V_b \) increasing although the population of total inversion holes is reduced. It is reasonable to assume that only the holes which can tunnel through the interface layer of 1–2 Å to be captured by the Si–H bonds can give contribution to dissociate the Si–H bonds.\textsuperscript{5} In this way, hot holes are more effective to induce degradation than the normal cold channel holes. With \( V_b \) increasing, the degradation induced by the normal cold holes decreases due to the decrease of the channel hole density, while an additional degradation induced by the hot hole injection increases. At low \( V_b \), these two opposite effects make the device degradation appear almost independent of \( V_b \). With \( V_b \) further increasing, the latter increases more quickly and prevails over the former, resulting in a significant degradation enhancement at high \( V_b \). Moreover, the injected hot holes may break the Si–O bonds at or near the SiO\(_2\)/Si interface besides the Si–H bonds, as suggested by Varghese et al.\textsuperscript{16} This effect makes the \( V_b \) induced degradation enhancement more significant.

The field-dependent tunneling coefficient of holes from the channel to the interface layer depends almost exponentially on the local electrical field at the interface. In other words, the barrier height of the bond dissociation decreases with \( E_{\text{ox}} \) (i.e., \( V_g \)) increasing.\textsuperscript{5} Therefore, the \( V_b \) effect is more significant at high \( |V_g| \) than that at low \( |V_g| \), and the minimum \( V_b \) to trigger the degradation enhancement decreases with increasing \( |V_g| \).

Figure 4 shows \( \Delta N_{th} \) and \( \Delta V_{th} \) as a function of \( V_b \) under static and dynamic NBT stresses (with unipolar or bipolar square wave form) with different magnitudes of the stressing voltage, i.e., \( V_g=2.8 \) V in Fig. 4(a) and \( V_g=2.0 \) V in Fig. 4(b). The frequency of the dynamic stress is 1 MHz. Consistent with the static stress, a similar \( V_b \) effect also appears under the dynamic stress. It is worth noticing that the bipolar BT stress exhibits a relatively smaller enhancement as compared with other two stress configurations (static and unipolar) with identical \( V_a \) and \( V_b \) values. The reason is explained as follows.

In the normal \( V_b \) grounded case, it has been known that the device degradation under high-frequency bipolar BT stress is enhanced.\textsuperscript{9} Such a frequency-dependent degradation enhancement (also see Fig. 6) has been ascribed to the trapped electrons at or near the Si/SiO\(_2\) interface states upon the Si surface potential reversal from accumulation to inversion quickly.\textsuperscript{10} The electrical field built by the trapped electrons or the recombination of the trapped electrons with the channel free holes can accelerate the dissociation of the Si–H bonds.
bonds, resulting in an additional degradation at each pulse fall edge during the bipolar BT stress. Because the occupied interface states in the upper half of the band gap are negative while those in the lower half are neutral, the additional degradation occurs only when the high level of the bipolar wave form ($V_{th}$, see inset of Fig. 8) is larger than the midgap voltage ($V_{mg}$) and increases rapidly with $V_{th}$ further increasing. If the bulk electrode is applied by a positive $V_{b}$, the midgap voltage increases with $V_{b}$. Therefore, this additional degradation induced by $V_{b}$ reversal quickly decreases with $V_{b}$ increasing. Meanwhile, the $V_{b}$ induced degradation enhancement (due to the bulk hot holes injection) in the “on” state (i.e., at the $V_{th}$ stage) of the bipolar stress keeps similar to that in the case of the static or unipolar BT stress. Thus, the increasing rate of overall degradation with $V_{b}$ increasing under the bipolar BT stress is apparently smaller than that under other two stress configurations.

**B. Floating of the bulk electrode**

Figure 5 compares the device degradation under static and dynamic BT stresses with the bulk electrode floating or grounded. The degradation remains almost unchanged under the static and unipolar BT stresses, while it is dramatically enhanced under the bipolar stress with $V_{b}$ floating. The $\Delta V_{th}$ enhancement is more significant than that of $\Delta N_{th}$, indicating that more $\Delta N_{th}$ than $\Delta N_{th}$ is created under the bipolar BT stress with $V_{b}$ floating.

The frequency dependences of the degradation ($\Delta N_{th}$ and $\Delta V_{th}$) under bipolar BT stresses with $V_{b}$ grounded or floating are shown in Fig. 6. In the normal bipolar BT stress with $V_{b}$ grounded, the degradation enhancement occurs at frequency larger than $\sim 10$ kHz. $\Delta N_{th}$ increases about two times with the frequency increasing from $10$ kHz to $10$ MHz at $V_{g}$ =2.8 V, and with more large enhancement ratio at higher $V_{g}$ (not shown here, see Ref. 9). On the other hand, with $V_{b}$ floating, the degradation enhancement starts to occur at 1 Hz. $\Delta N_{th}$ increases about 7–10 times with frequency increasing from 1 Hz to 1 kHz and then almost saturates with further increasing of the stressing frequency. Moreover, under the same bipolar BT stress, the degradation with $V_{b}$ floating is much larger than that with $V_{b}$ grounded. The $\Delta V_{th}$ can reach about 0.4 V at a relatively small $V_{g}$ stress (2.5 V).

Since the degradation almost saturates around 1 kHz, we fix the frequency at 1 kHz while changing one of the wave form parameters in the following experiments to further clarify the degradation behaviors under the bipolar BT stress with $V_{b}$ floating.

First, the transition time (both the rise and the fall time) is modified from 4.5 ns to $10^5$ ns. In the $V_{b}$ grounded case, it has been known that the additional degradation under high-frequency bipolar BT stress decreases with increasing the transition time ($t_T$) of the pulse wave form because the portion of trapped electrons in the interface states which can follow the $V_{th}$ variation through the emission process increases, and the degradation enhancement almost vanishes if $t_T$ is larger than about 60 ns. This critical time constant corresponds to the emission time constant of the trapped electrons in the interface states. In the $V_{b}$ floating case, Fig. 7 shows that the degradation is almost independent of $t_T$ up...
to $10^5$ ns. Thus, the corresponding time constant is at least larger than $10^5$ ns and is probably around 1–1000 ms because the degradation enhancement starts to occur at 1 Hz and saturates at 1 kHz, as shown in Fig. 6.

Second, the low level voltage ($V_-$) of the pulse wave form (i.e., the stress voltage) is kept at $-2.8$ V while its high level voltage ($V_+$) is changed from 0 (as in the unipolar stress) to 2.8 V (as in the normal bipolar stress). Figure 8 shows that the degradation is independent of $V_+$ at the small $V_+$ region, and then it increases with $V_+$ quickly when $V_+$ is larger than about 1.5 V. The minimum $V_+$ to trigger the degradation enhancement is larger than that in the $V_b$ grounded case.

Third, the $V_a$ dependence of the device degradation is shown in Fig. 9. Both $\Delta N_0$ and $\Delta V_{th}$ increase almost exponentially with $V_a$ increasing. The increase rate of $\Delta N_0$ (and $\Delta V_{th}$) with $V_a$ becomes larger when $V_a$ is larger than about 1.8 V, indicating more significant degradation enhancement at larger $V_a$, similar to that in the $V_b$ grounded case. The reduction of the increase rate at the even higher $V_a$ region ($V_a > 2.5$ V) can be attributed to the saturation effect, as will be explained below.

The time evolutions of $\Delta N_0$ and $\Delta V_{th}$ under bipolar BT stress with $V_b$ floating are shown in Fig. 10. The stress voltage is $V_a = 2.6$ V or 2.8 V. At the early stressing time of the
When one-to-one related with the interface trap. When the gate electrode is positively biased, there exists a depletion region between the source and the SiO2/Si interface. If the Si–H bonds have been sub-

decreases. The saturation trend at frequency larger than 2.5 V in Fig. 9 can be attributed to the same reason.

C. Hot hole injection under bipolar BT stress with $V_b$ floating

We propose that the degradation enhancement under the bipolar stress with $V_b$ floating can also be attributed to the hot hole injection upon $V_g$ is switched from positive to negative quickly. When the gate electrode is positively biased ($V_g=+V_a$), the potential of the bulk Si also increases due to $V_b$ floating, forming a reversed biased $p$-$n$ junction between the grounded source (drain) and the bulk Si, as shown in Fig. 11(a) schematically. The depletion width and the maximum electrical field in this region increase with $+V_a$ increasing. When $V_g$ is switched to negative ($V_g=-V_a$), an inversion layer is formed almost immediately at the Si surface with holes supported from the source (drain) electrode. Meanwhile, the depletion region below the source (drain) and the channel, because the source (drain) and the channel are electrically connected together to have the same potential by the inversion holes at $V_g=-V_a$ will be vanished by electrons filling in. If $V_g$ is grounded, the electrons can be supported from the bulk electrode almost simultaneously (the time constant is about $10^{-4}$ ns). If $V_g$ is floating, the electrons are provided by the electron-hole generation-recombination (G-R) process in the depletion region. The corresponding time constant is quite large. From the low-frequency C-V measurement of a MOS capacitance, the time constant for electrons responding to the $V_g$ variation through the G-R process is around 0.2–100 ms. Therefore, if the transition time of $V_g$ from $+V_a$ to $-V_a$ is shorter than the above time constant, there exists a transient stage that $V_g$ has already been $-V_a$ while the depletion region below the inversion layer still exists, as shown in Fig. 11(b) schematically. This remaining transient depletion region can provide hot hole injection from the bulk to the channel, as in the case of $V_b$ positively biased, thus enhances the device degradation. This model explains qualitatively the frequency dependence in Fig. 6 and the absence of the transition time dependence up to 0.1 ms in Fig. 7. The $V_a$ dependence in Fig. 8 can be explained by the fact that the transient depletion region should be larger than a critical value to trigger the degradation enhancement, as in the case of positively biased $V_a$. The degradation enhancement increases with $V_a$ further increasing, resulting in a larger $V_a$ accelerating factor at the higher $V_a$ region, as shown in Fig. 9. The tunneling electrons from gate to substrate at the $V_g=-V_a$ stage may not play an important role because these electrons can recombine with the inversion holes in the channel quickly.

Since the hot holes in the above model are energized by the electrical field, and also taking into account the fact that the tunneling coefficient depends on temperature weakly, the hot hole injection induced degradation is expected to be dependent on temperature weakly. Figure 12 compares $\Delta N_d$ as
a function of the reciprocal of the stress temperature under normal NBT stress (static and $V_b$ grounded), static NBT stress with $V_b = 2$ V, and bipolar BT stress with $V_b$ floating with the identical stress voltage of $V_g = 2.6$ V. $\Delta N_a$ under the latter two stress configurations is much larger than that under the first one, indicating that the device degradation is dominated by the hot hole injection. From the linear fitting of these Arrhenius plots, the activation energy $E_a$ was extracted to be 0.197, 0.009, and 0.037 eV, respectively. The $E_a$ value of the normal NBT stress is in consistent with that reported in literature. On the other hand, the hot hole injection induced degradation has a very small $E_a$ value, both for the $V_b$ positive bias in the static stress and the $V_b$ floating in the bipolar stress, in agreement with our model.

IV. CONCLUSION

The $V_b$ (grounded, positively biased, or floating) effects on both static and dynamic NBT stress are studied. Significant degradation enhancement is observed by applying a positive bulk bias in both static and dynamic NBT stresses or by $V_b$ floating in the bipolar BT stress. The degradation enhancement in both cases is attributed to an additional degradation related with the hot hole injection. The holes are energized by the electrical field provided by the positive bulk bias $V_b$ or, in the case of bipolar BT stress with $V_b$ floating, by the transient depletion region below the channel induced by the $p$-$n$ junction between the source (drain) and the bulk upon $V_g$ being switched from positive to negative so quickly that electrons cannot respond to the $V_g$ variation through the R-G process.

From the viewpoint of device application, our findings indicates that, in some cases, the bulk electrode is floating, e.g., for silicon-on-insulator (SOI) devices without body contact, a dramatic degradation may occur if a bipolar gate voltage is applied. On the other hand, very large $V_g$ shift (e.g., $>1$ V) can be obtained at a relatively small gate voltage by applying a bipolar $V_g$ with $V_b$ floating.

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