# Pulse Waveform Dependence on AC Bias Temperature Instability in pMOSFETs

Shiyang Zhu*, Member, IEEE*, Anri Nakajima, Takuo Ohashi, and Hideharu Miyake

*Abstract—***In this letter, the waveform effects on the degradation** enhancement of pMOSFETs under high-frequency ( $> 10^4$  Hz) **bipolar-pulsed bias-temperature (BT) stresses were systematically studied. The enhancement was found to be mainly governed by the** fall time  $(t_F)$  of the pulse waveform, namely, the transition time **of the silicon surface potential from strong accumulation to strong inversion, rather than the pulse rise time**  $(t_R)$  and the pulse duty **factor** (*D*). The enhancement decreases significantly with  $t_F$  in**creasing, and is almost eliminated when**  $t_F$  **is larger than**  $\sim 60$  **ns. This new finding is consistent with our newly proposed assumption that the recombination of free holes and trapped electrons at the SiO**<sup>2</sup> **Si interface and/or near-interface states can enhance the interface trap generation.**

*Index Terms—***Bias temperature instability (BTI), dynamic stress, interface trap generation, pMOSFET, pulse waveform.**

### I. INTRODUCTION

**T** HE negative bias temperature instability (NBTI) in pMOS-<br>FETs, which is originated from the interface trap gener-<br>extend (AM) and/or the oxide fixed shapes huildup (AM) ation  $(\Delta N_{\rm it})$  and/or the oxide fixed charge buildup  $(\Delta N_{\rm ot})$ , is one of the most crucial reliability concerns for the state-ofthe-art devices, and becomes even more severe as the gate oxide is further scaled down [\[1](#page-2-0)]. Recently, it was recognized that the degradation can be significantly reduced under ac NBT stresses where a repetitive unipolar (the gate voltage  $V_g$  between 0 and  $-V_a$ , where  $V_a$  is the voltage amplitude) or bipolar ( $V_g$  between  $+V_a$  and  $-V_a$ ) voltage was applied on the gate electrode as compared to the dc NBT stress where a constant voltage  $(-V_a)$  was applied [[2\]](#page-2-0)–[\[6](#page-2-0)]. The reduction has been ascribed to the fact that  $\Delta N_{\rm it}$  and/or  $\Delta N_{\rm ot}$  generated during the on-state (when  $V_g = -V_a$ ) of the dynamic stress can be partially recovered during its off-state (when  $V_q = 0$  or  $+V_a$ ) [\[2\]](#page-2-0)–[[6\]](#page-2-0). In the unipolar stress case, similar phenomena were also observed in our experiment [[7\]](#page-2-0). However, in the bipolar stress case, on the contrary to that observed by other groups [\[6](#page-2-0)], the degradation was found to be enhanced, rather than reduced, especially at the stress frequency larger than  $\sim 10^4$  Hz [\[7](#page-2-0)]. Similar degradation enhancement was also observed in nMOSFETs under dynamic oxide field stresses by Chen *et al.* [[8\]](#page-2-0) and by us [\[9](#page-2-0)]. A model

S. Zhu and A. Nakajima are with Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima 739-8527, Japan (e-mail: nakajima@sxsys.hiroshima-u.ac.jp).

T. Ohashi and H. Miyake are with Elpida Memory, Inc., Higashi-Hiroshima 739-0198, Japan.

Digital Object Identifier 10.1109/LED.2005.853645

related to the charge pumping current during the bipolar stress was proposed to explain the enhancement [[7\]](#page-2-0), [\[9](#page-2-0)]. In this letter, new results obtained from the waveform dependence are presented to understand the reason of the different observations in the bipolar BT experiments, e.g., between Tan *et al.* [[6\]](#page-2-0) and us, and to reveal the enhancement mechanism more clearly.

## II. EXPERIMENTAL

The tested pMOSFETs were fabricated on n-well of p-Si substrates using a standard CMOS process [\[10](#page-2-0)] with lightly doped drain/source structure,  $p^+$ -ploy-Si gate, and plasmanitrided gate oxide which has a physical thickness of  $\sim$ 2 nm and a peak nitrogen concentration of 15% near the poly-Si/oxide interface, as estimated by secondary ion mass spectroscopy. The channel width is 10  $\mu$ m and the channel length is between 0.44–2.0  $\mu$ m. The device was stressed at 125 °C for 1000 s, by applying a pulsed voltage from a pulse generator (HP8112A) on the gate electrode while all other electrodes were grounded.  $V_a$  was 2.8 V unless specially noted. Immediately after stress interruption (less than several seconds), an  $I_d - V_q$  and a modified direct-current current–voltage (DCIV) measurement [\[11](#page-2-0)], [[12\]](#page-2-0) were carried out at the stress temperature sequentially. The threshold voltage shift  $\Delta V_{\text{th}}$  and the transconductance degradation  $(\Delta g/g_0)$  are extracted form the  $I_d - V_g$  curves, while the  $N_{it}$  is extracted from the DCIV peak. Each stress was carried out on a fresh device with an initial  $N_{\text{it}}$ of  $1.5 \sim 3.0 \times 10^9$  cm<sup>-2</sup>. There is a close correlation among  $\Delta N_{\text{it}}$ ,  $\Delta V_{\text{th}}$  and  $\Delta G/G_0$  [[2\]](#page-2-0). Therefore, only the  $\Delta N_{\text{it}}$  data are shown follows.

## III. RESULTS AND DISCUSSION

Fig. 1 shows the frequency (*f*) dependence of  $\Delta N_{\text{it}}$  under both bipolar and unipolar NBT stresses. Both the rise  $(t_R)$  and fall time  $(t_F)$  of the waveform are set to the minimum value (4.5 ns) permitted by the pulse generator, and the duty factor is 50%. At "0" Hz,  $V_g$  keeps at  $-V_a$  for 500 s first, then at 0 V (for unipolar) or at  $+V_a$  (for bipolar) for the next 500 s. In consistence with our previous results,  $\Delta N_{\text{it}}$  under bipolar BT stress is enhanced as compared to that under unipolar stress or dc stresses (0 Hz), and the enhancement becomes significant at frequencies larger than  $\sim 10^4$  Hz [\[7](#page-2-0)]. The inset shows the time evolution of  $N_{it}$  under dc stress  $(-V_a)$ , relax (0 V or  $+V_a$ ) and re-stress  $(-V_a)$  sequence. The positive bias provides almost similar recovery of the stress-induced  $N_{it}$  as the zero bias [[4\]](#page-2-0). If only the dc effects, namely,  $N_{it}$  generation at  $V_g = -V_a$  and passivation at  $V_q = 0$  or  $+V_a$ , are involved, unipolar and bipolar BT stresses should result in similar  $\Delta N_{\text{it}}$ . Fig. 1 implies these

Manuscript received April 11, 2005; revised June 15, 2005. This work was supported in part by the Nanoelectronics for Tera-Bit Information Processing Program from the Ministry of Education, Culture, Sports, Science and Technology under the 21st Century COE program. The review of this letter was arranged by Editor M. Ostling.



Fig. 1. Interface trap generation  $\Delta N_{\rm{it}}$  as a function of stress frequency under unipolar and bipolar BT stresses with a square waveform of  $t_R = t_F$ 4.5 ns and duty factor of 50%. Devices have size of  $W/L = 10 \ \mu m/0.6 \ \mu m$ and are stressed at 125 °C for 10<sup>3</sup> s. Inset is the time evolution of  $N_{\rm it}$  under stress-relax-stress sequence.



Fig. 2. Interface trap generation  $\Delta N_{\rm{it}}$  as a function of duty factor under unipolar and bipolar stresses with a square waveform of  $t_R = t_F = 4.5$  ns and  $f = 10^6$  Hz. Devices have size of  $W/L = 10 \mu m/1.12 \mu m$  and are stressed at 125 °C for  $10^3$  s. The 100% duty factor represents the dc negative BT stress (SNBTI), and the 0% duty factor represents the dc positive BT stress (SPBTI).

exists a transient (ac) effect for  $N_{it}$  generation under the bipolar BT stress.

Fig. 2 shows the duty factor effect under bipolar and unipolar BT stresses with square waveform of  $f = 10^6$  Hz and  $t_R =$  $t_F = 4.5$  ns. Here, the duty factor is defined as  $D = (t_L +$  $(t_F)/T$ , where  $T = t_L + t_F + t_H + t_R$  is the pulse period (1000 ns at  $f = 10^6$  Hz),  $t_L$  and  $t_H$  are the duration at low  $(-V_a)$ and high  $( +V_a$  for bipolar, 0 for unipolar) voltage respectively. At the duty factor range of  $\sim$  5– $\sim$ 95%, the  $N_{it}$  generation under bipolar BT stress is much larger than that under unipolar NBT stress, and the enhancement is independent of the duty factor as we can see that  $\Delta N_{\rm{it}}$  increases almost linearly with the duty factor having a similar slope in both unipolar and bipolar cases. At 99% duty factor, the enhancement reduces because  $+V_a$  is not really reached, in other words,  $t_H$  approaches 0, as monitored by an oscilloscope. Similarly,  $t_L$  approaches 0 at the 1% duty factor, leading to the  $\Delta N_{\rm{it}}$  reduction.



Fig. 3. Interface trap generation  $\Delta N_{\rm it}$  as a function of  $t_R$  (or  $t_F$ ) under bipolar stresses at  $10^6$  Hz with a trapezoidal waveform. Inset shows a schematic waveform to define  $t_L$ ,  $t_R$ ,  $t_H$  and  $t_F$ . Devices have size of  $W/L = 10~\mu\text{m}/0.8~\mu\text{m}$  and are stressed at 125 °C for 10<sup>3</sup> s. For comparison,  $\Delta N_{\rm it}$  under unipolar stress with a square waveform  $(t_T = t_R = t_F = 4.5 \text{ ns})$ is also shown.

Under similar bipolar BT stress  $(10^6$  Hz, 50% duty factor,  $V_a = 2.8$  V) but with different transition time of the waveform  $t_T (= t_R = t_F)$ ,  $\Delta N_{\rm it}$  decreases nearly linearly with the increase of  $log(t_T)$ , as shown in Fig. 3. The  $\Delta N_{\rm it}$  vs  $log(t_T)$ curve has a larger slope at  $t_T < 20$  ns. Compared to  $\Delta N_{\text{it}}$ under unipolar NBT stress, the enhancement almost vanishes when  $t_T$  is larger than  $\sim 60$  ns. The continuous decreasing of  $\Delta N_{\text{it}}$  with further increasing of  $t_T$  can be simply ascribed to the stress period  $t_L (= T/2 - t_T)$  decreasing. Therefore, the reason for no  $\Delta N_{\text{it}}$  enhancement in Tan *et al.*'s high frequency bipolar BT experiment is due to the large  $t_T$  of the waveform,  $t_R = t_F = 500$  ns at  $10^5$  Hz as they mentioned.

To distinguish the effects of  $t_R$  and  $t_F$ , a trapezoidal stress waveform with different  $t_R$  and  $t_F$  is employed. In one case,  $t_R$  is fixed at 5.5 ns while changing  $t_F$  from 5.5 to 99.9 ns (the maximum of the pulse generator). In other case,  $t_F$  is fixed at 5.5 ns while changing  $t_R$  from 5.5 to 99.9 ns.  $t_L$  is kept constant of 500 ns in both cases. Fig. 3 shows that  $\Delta N_{\rm it}$  decreases very slightly with increasing  $t_R$ , while it decreases significantly with increasing  $t_F$  with a similar slope as that of  $t_T$ . The decrease almost saturates at  $t_F > \sim 60$  ns. Above results clearly indicates that the  $\Delta N_{\text{it}}$  enhancement under the bipolar BT stress is mainly originated from the rapid voltage transition from  $+V_a$ to  $-V_a$ , i.e., the  $dV_q/dt$  value. The  $\Delta N_{it}$  enhancement is eliminated when  $t_F$  is larger than  $\sim 60$  ns.

The  $V_a$  effect is shown in Fig. 4 under various BT stresses.  $\Delta N_{\rm it}$  increases with  $V_a$  in all stress configurations, and more rapidly under bipolar BT stress with  $t_T = 4.5$  ns. It also indicates that the  $\Delta N_{\text{it}}$  enhancement becomes more significant at larger  $V_a$ . One possible reason is that the  $dV_a/dt$  value increases with  $V_a$  increasing at the same  $t_T$ .

The  $\Delta N_{\rm it}$  enhancement under bipolar BT stress has been related to the recombination of trapped electrons at or near the  $Si/SiO<sub>2</sub>$  interface states with free holes upon the Si surface potential reversal from accumulation to inversion [\[7](#page-2-0)], [\[9](#page-2-0)]. Now we can describe the model more clearly. It is well known that the interface traps ( $Si_3 \equiv Si\bullet$ ), as well as the positive oxide charges

<span id="page-2-0"></span>

Fig. 4. Interface trap generation  $\Delta N_{\rm it}$  as a function of  $V_a$  under bipolar, unipolar and dc NBT stresses. Devices have size of W/L =  $10 \mu m/0.44 \mu m$ and are stressed at 125 °C for 10<sup>3</sup> s. The dynamic stress has a square waveform of  $f = 10^6$  Hz,  $D = 50\%$ , and  $t_T = 4.5$  ns or 20 ns.

 $(O_3 \equiv Si^+)$ , are generated from the dissociation of hydrogenterminated trivalent Si bonds (Si–H) associated with holes  $(h^+)$ as:  $Si_3 \equiv Si-H + h^+ \rightarrow Si_3 \equiv Si\bullet + H^+$  [1], [13]. In static NBT stress, holes come from the Si inversion layer. In bipolar BT stress, beside this contribution, there is another transient holes from the source/drain to recombine with the trapped electrons upon the gate voltage shifting from  $+V_a$  to  $-V_a$ , which is similar to the charge pumping current in the nMOSFET case. If  $t_F$ is small enough, the electrons trapped at the  $SiO<sub>2</sub>/Si$  interface or near-interface states still remain when the gate voltage  $V_q$ has been changed from  $+V_a$  to  $-V_a$ . The built-in electric field provided by the trapped electrons, which depends on  $V_a$ , can accelerate the free holes to be recombined. These "hot" holes can enhance the Si–H dissociation significantly. With increasing  $t_F$ , the trapped electrons can follow the  $V_q$  variation by the electron emission process, in other words, the recombination component decreases [14], hence the  $\Delta N_{\rm{it}}$  enhancement decreases. The emission time constant of the trapped electrons at 125  $\mathrm{^{\circ}C}$ is estimated to be several tens nanoseconds [15], in consistent with the critical  $t_F$  observed in this work ( $\sim 60$  ns). Another possible explanation may be related to the fact that the negative charged antibonding Si–H has much smaller activation energy for H detachment than the value for either the neutral or positive charge states [16]. Therefore, upon the channel surface shift from accumulation (in this stage, the antibonding Si–H may be negative charged) to inversion (in this stage, Si–H breaking occurs) quickly, those Si–H bonds are much easier to be broken.

In conclusion, it was clarified that the  $\Delta N_{\rm it}$  enhancement under bipolar BT stress is due to the quick switch of  $V_q$  from  $+V_a$  to  $-V_a$ . The enhancement decreases with increasing  $t_F$  quickly, and almost disappears at  $t_F \geq 60$  ns. This new finding supports our newly proposed assumption that the dissociation of Si–H bonds can be accelerated by free holes to be recombined with trapped electrons upon the quick shift of the channel surface potential from strong accumulation to strong inversion during the bipolar BT stress.

#### **REFERENCES**

- [1] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, no. 1, pp. 1–18, 2003.
- [2] G. Chen, M. F. Li, C. H. Ang, J. Z. Zheng, and D. L. Kwong, "Dynamic NBTI of pMOS transistors and its impact on MOSFET scaling," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 734–736, Dec. 2002.
- [3] M. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, J. Babcock, R. Lindley, P. Clifton, M. Redford, and A. Shibkov, "Dynamic recovery of negative bias temperature instability in p-type metal-oxidesemiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 83, no. 8, pp. 1647–1649, 2003.
- [4] S. Rangan, N. Mielke, and E. C. C. Yeh, "Universal recovery behavior of negative bias temperature instability," in *IEDM Tech. Dig.*, 2003, pp. 341–344.
- [5] M. A. Alam, "A critical examination of the mechanics of dynamic NBTI for PMOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 345–348.
- [6] S. S. Tan, T. P. Chen, C. H. Ang, and L. Chan, "A new waveform-dependent lifetime model for dynamic NBTI in pMOS transistor," in *Proc. 42nd Ann. Intern. Rel. Phys. Symp.*, 2004, pp. 35–39.
- [7] S. Y. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, "Enhancement of BTI degradation in pMOSFETs under high frequency bipolar gate bias," *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 387–389, Jun. 2005.
- [8] T. P. Chen, S. Li, S. Fung, and K. F. Lo, "Interface trap generation by FN injection under dynamic oxide field stress," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1920–1926, Sep. 1998.
- [9] S. Y. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, "Interface trap generation induced by charge pumping current under dynamic oxide field stresses," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 216–218, Mar. 2005.
- [10] K. Saino, Y. Kato, E. Kitamura, Y. Takaishi, M. Ando, T. Taguwa, T. Kanda, S. Yamada, and T. Sekiguchi, "A novel  $W/WN_x/du$ al  $-g$ ate CMOS technology for future high-speed DRAM having enhanced retention time and reliability," in *IEDM Tech. Dig.*, 2003, pp. 415–418.
- [11] A. Neugroschel, C. T. Sah, K. Michael Han, M. S. Carroll, T. Nishida, J. T. Kavalieros, and Y. Lu, "Direct-current measurement of oxide and interface traps on oxidized silicon," *IEEE Trans. Electron Devices*, vol. 42, no. 9, pp. 1657–1662, Sep. 1995.
- [12] S. Y. Zhu, A. Nakajima, T. Ohashi, and H. Miyake, "Modified directcurrent current-voltage method for interface trap density extraction in metal–oxide–semiconductor field-effect transistor with tunneling gate dielectrics at high temperature," *Jpn. J. Appl. Phys.*, vol. 44, no. 2, pp. L60–L62, 2005.
- [13] C. E. Blat, E. H. Nicollian, and E. H. Poindexter, "Mechanism of negative-bias-temperature instability," *J. Appl. Phys.*, vol. 69, no. 3, pp. 1712–1720, 1991.
- [14] G. Ghibaudo and N. S. Saks, "Investigation of the charge pumping current in metal-oxide-semiconductor structures," *J. Appl. Phys.*, vol. 65, no. 11, pp. 4311–4318, 1989.
- [15] S. M. Sze, *Physics of Semiconductor Device*, 2nd ed. New York: Wiley, 1981, ch. 7.
- [16] A. H. Edwards, "Interaction of H and  $H_2$  with the silicon dangling orbital at the  $\langle 111 \rangle$  Si $\langle$ SiO<sub>2</sub> interface," *Phys. Rev. B, Condens. Matter*, vol. 44, no. 4, pp. 1832-1838, 1991.